

## LP2980-ADJ Micropower 50 mA Ultra Low-Dropout Adjustable Voltage Regulator in SOT-23

Check for Samples: [LP2980-ADJ](#)

### FEATURES

- **Ultra Low Dropout Voltage**
- **Output Adjusts from 1.23V to 15V**
- **Specified 50 mA Output Current**
- **Uses Tiny SOT-23 Package**
- **Requires Few External Components**
- **<1  $\mu\text{A}$  Quiescent Current when Shutdown**
- **Low Ground Pin Current at All Loads**
- **High Peak Current Capability (150 mA Typical)**
- **Wide Supply Voltage Range (2.5V–16V)**
- **Overtemperature/overcurrent Protection**
- **–40°C to +125°C Junction Temperature Range**

### APPLICATIONS

- **Cellular Phone**
- **Palmtop/Laptop Computer**
- **Camcorder, Personal Stereo, Camera**

### DESCRIPTION

The LP2980-ADJ is a 50 mA adjustable voltage regulator designed to provide ultra low dropout in battery powered applications.

Using an optimized VIP (vertically Integrated PNP) process, the LP2980-ADJ delivers unequaled performance in all specifications critical to battery-powered designs:

**Adjustable Output:** output voltage can be set from 1.23V to 15V.

**Precision Reference:** 1.0% tolerance.

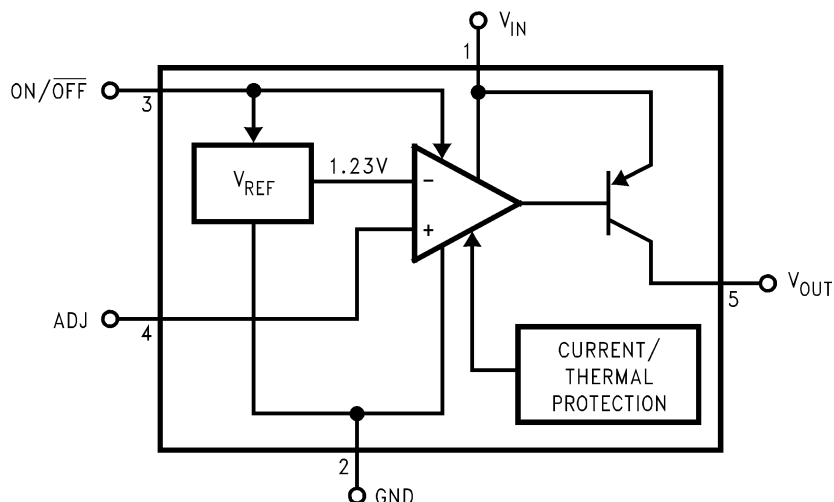
**Dropout Voltage:** typically 120 mV @ 50 mA load, and 7 mV @ 1 mA load.

**Ground Pin Current:** typically 320  $\mu\text{A}$  @ 50 mA load, and 80  $\mu\text{A}$  @ 1 mA load.

**Sleep Mode:** less than 1  $\mu\text{A}$  quiescent current when on/off pin is pulled low.

**Smallest Possible Size:** Package uses minimum board space.

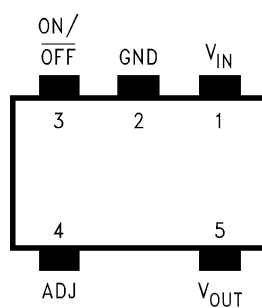
### Block Diagram



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## Connection Diagram



**Figure 1. 5-Lead Small Outline Package  
Top View  
See Package Number DBV0005A**

### PIN DESCRIPTIONS

| Name      | Pin Number | Function                         |
|-----------|------------|----------------------------------|
| $V_{IN}$  | 1          | Input Voltage                    |
| GND       | 2          | Common Ground (device substrate) |
| ON/OFF    | 3          | Logic high enable pin            |
| ADJ       | 4          | Output voltage feedback pin      |
| $V_{OUT}$ | 5          | Regulated output voltage         |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

|  |                         |
|--|-------------------------|
| Storage Temperature Range                      | -65 to +150°C           |
| Operating Junction Temperature Range           | -40 to +125°C           |
| Lead Temp. (Soldering, 5 seconds)              | 260°C                   |
| ESD Rating <sup>(3)</sup>                      | 2 kV                    |
| Power Dissipation <sup>(4)</sup>               | Internally Limited      |
| Input Supply Voltage (Survival)                | -0.3V to +16V           |
| Input Supply Voltage (Operating)               | 2.5V to +16V            |
| Shutdown Input Voltage (Survival)              | -0.3V to +16V           |
| Output Voltage (Survival) <sup>(5)</sup>       | -0.3V to 16V            |
| I <sub>OUT</sub> (Survival)                    | Short Circuit Protected |
| Input-Output Voltage (Survival) <sup>(6)</sup> | -0.3V to 16V            |

- (1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) The ESD rating of pins 3 and 4 is 1 kV.
- (4) The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance, θ<sub>J-A</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is calculated using: 
$$P (MAX) = \frac{T_J (MAX) - T_A}{\theta_{J-A}}$$
 The value of θ<sub>J-A</sub> for the SOT-23 package is 300°C/W. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
- (5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2980-ADJ output must be diode-clamped to ground.
- (6) The output PNP structure contains a diode between the V<sub>IN</sub> and V<sub>OUT</sub> terminals that is normally reverse-biased. Reversing the polarity from V<sub>IN</sub> to V<sub>OUT</sub> will turn on this diode (see [APPLICATION HINTS](#)).

## ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T<sub>J</sub> = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V<sub>IN</sub> = 4.3V, V<sub>OUT</sub> = 3.3V, I<sub>L</sub> = 1 mA, C<sub>IN</sub> = 1 μF, C<sub>OUT</sub> = 2.2 μF, V<sub>ON/OFF</sub> = 2V.

| Symbol                              | Parameter                         | Conditions  | Typ   | LP2980I-ADJ <sup>(1)</sup> |                       | Units |
|-------------------------------------|-----------------------------------|---|-------|----------------------------|-----------------------|-------|
|                                     |                                   |   |       | Min                        | Max                   |       |
| V <sub>REF</sub>                    | Reference Voltage                 |   | 1.225 | 1.213                      | 1.237                 | V     |
|                                     |                                   | 1 mA < I <sub>L</sub> < 50 mA<br>V <sub>OUT</sub> + 1 ≤ V <sub>IN</sub> ≤ 16V | 1.225 | 1.206<br><b>1.182</b>      | 1.243<br><b>1.268</b> |       |
| ΔV <sub>REF</sub> /ΔV <sub>IN</sub> | Reference Voltage Line Regulation | 2.5V ≤ V <sub>IN</sub> ≤ 16V  | 3     |                            | 6.0<br><b>15.0</b>    | mV    |
| V <sub>IN</sub> -V <sub>O</sub>     | Dropout Voltage <sup>(2)</sup>    | I <sub>L</sub> = 0  | 1     |                            | 3<br><b>5</b>         | mV    |
|                                     |                                   | I <sub>L</sub> = 1 mA   | 7     |                            | 10<br><b>15</b>       |       |
|                                     |                                   | I <sub>L</sub> = 10 mA  | 40    |                            | 60<br><b>90</b>       |       |
|                                     |                                   | I <sub>L</sub> = 50 mA  | 120   |                            | 150<br><b>225</b>     |       |

- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
- (2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential.

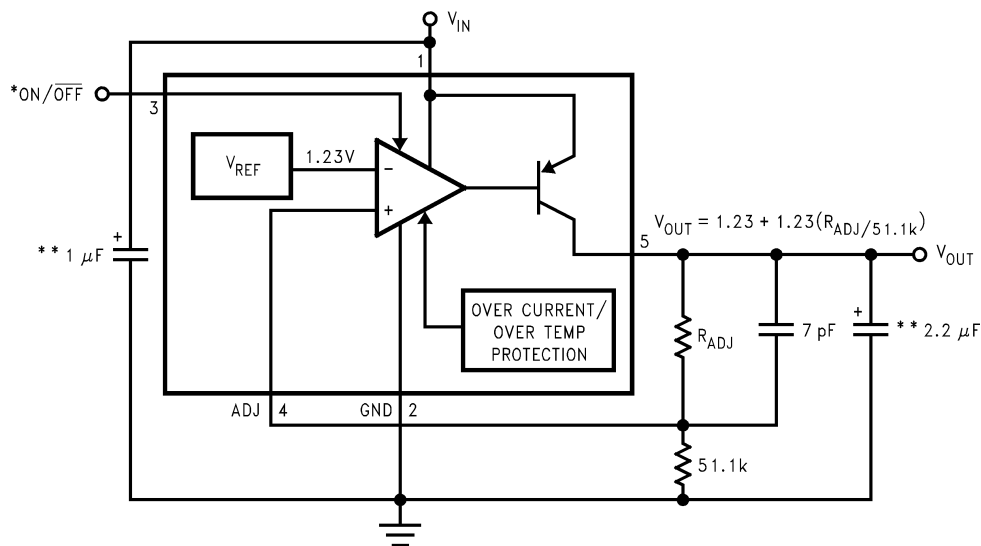
### ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ , and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified:  $V_{IN} = 4.3\text{V}$ ,  $V_{OUT} = 3.3\text{V}$ ,  $I_L = 1\text{ mA}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ ,  $V_{ON/OFF} = 2\text{V}$ .

| Symbol                         | Parameter                           | Conditions  | Typ  | LP2980I-ADJ <sup>(1)</sup> |                    | Units         |
|--------------------------------|-------------------------------------|---|------|----------------------------|--------------------|---------------|
|                                |                                     |   |      | Min                        | Max                |               |
| $I_{GND}$                      | Ground Pin Current                  | $I_L = 0$   | 60   |                            | 95<br><b>125</b>   | $\mu\text{A}$ |
|                                |                                     | $I_L = 1\text{ mA}$                                   | 80   |                            | 110<br><b>170</b>  |               |
|                                |                                     | $I_L = 10\text{ mA}$                                  | 120  |                            | 220<br><b>460</b>  |               |
|                                |                                     | $I_L = 50\text{ mA}$                                  | 320  |                            | 600<br><b>1200</b> |               |
|                                |                                     | $V_{ON/OFF} < 0.18\text{V}$                           | 0.01 |                            | <b>1</b>           |               |
| $I_{ADJ}$                      | ADJ Pin Bias Current                | $1\text{ mA} \leq I_L \leq 50\text{ mA}$              | 150  |                            | 350                | nA            |
| $V_{ON/OFF}$                   | ON/OFF Input Voltage <sup>(3)</sup> | High = O/P ON   | 1.4  | <b>1.6</b>                 |                    | V             |
|                                |                                     | Low = O/P OFF   | 0.55 |                            | <b>0.18</b>        |               |
| $I_{ON/OFF}$                   | ON/OFF Input Current                | $V_{ON/OFF} = 0$                                      | 0.01 |                            | <b>-1</b>          | $\mu\text{A}$ |
|                                |                                     | $V_{ON/OFF} = 5\text{V}$                              | 5    |                            | <b>15</b>          |               |
| $I_O(\text{PK})$               | Peak Output Current                 | $V_{OUT} \geq V_O(\text{NOM}) - 5\%$                  | 150  | 100                        |                    | mA            |
| $e_n$                          | Output Noise Voltage (RMS)          | BW = 300 Hz to 50 kHz,<br>$C_{OUT} = 10\ \mu\text{F}$ | 160  |                            |                    | $\mu\text{V}$ |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Ripple Rejection                    | f = 1 kHz<br>$C_{OUT} = 10\ \mu\text{F}$              | 68   |                            |                    | dB            |
| $I_O(\text{MAX})$              | Short Circuit Current               | $R_L = 0$ (Steady State) <sup>(4)</sup>               | 150  |                            |                    | mA            |

- (3) The ON/OFF input must be properly driven to prevent possible misoperation. For details, refer to [APPLICATION HINTS](#).
- (4) See [TYPICAL PERFORMANCE CHARACTERISTICS](#) curves.

### TYPICAL APPLICATION CIRCUIT



\*ON/OFF INPUT MUST BE ACTIVELY TERMINATED. TIE TO  $V_{IN}$  IF THIS FUNCTION IS NOT TO BE USED.  
 \*\*MINIMUM CAPACITANCE IS SHOWN TO ENSURE STABILITY OVER FULL LOAD CURRENT RANGE (SEE [APPLICATION HINTS](#)).

**TYPICAL PERFORMANCE CHARACTERISTICS**

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $I_L = 1\text{ mA}$ , ON/OFF pin tied to  $V_{IN}$ ,  $R_{ADJ} = 86.6\text{k}$ , and test circuit is as shown in Basic Application Circuit.

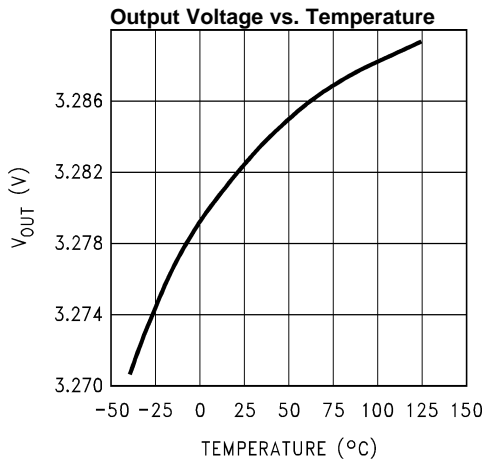


Figure 2.

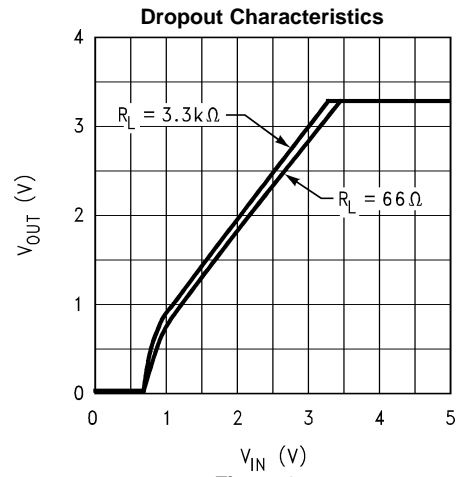


Figure 3.

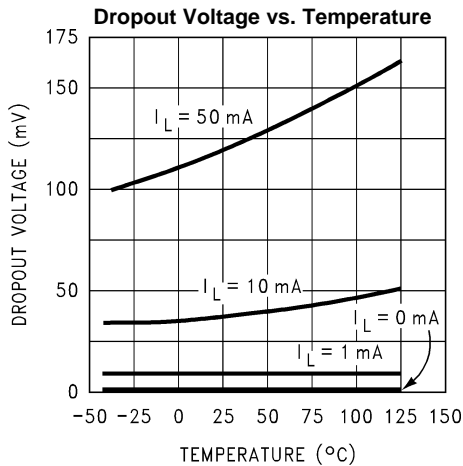


Figure 4.

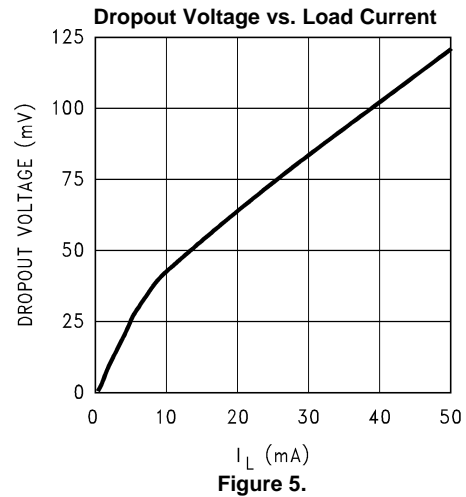


Figure 5.

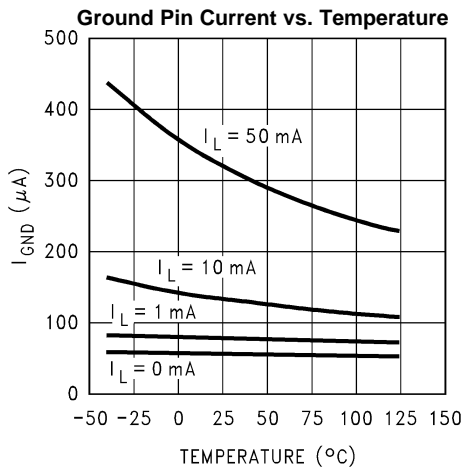


Figure 6.

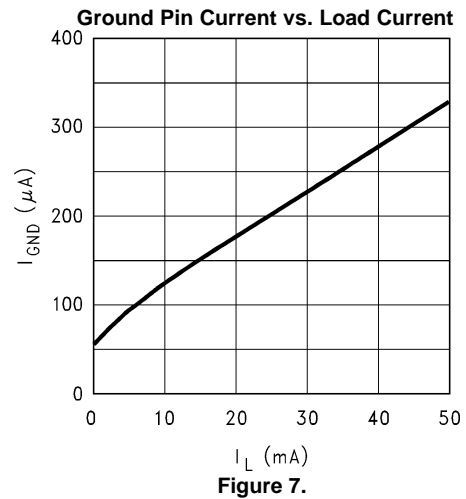


Figure 7.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{O(NOM)} + 1\text{V}$ ,  $I_L = 1\text{ mA}$ , ON/OFF pin tied to  $V_{IN}$ ,  $R_{ADJ} = 86.6\text{k}$ , and test circuit is as shown in Basic Application Circuit.

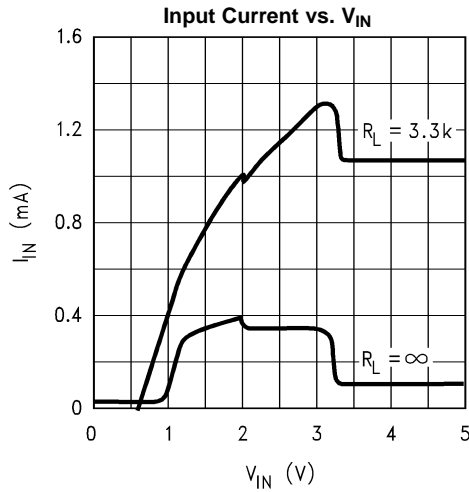


Figure 8.

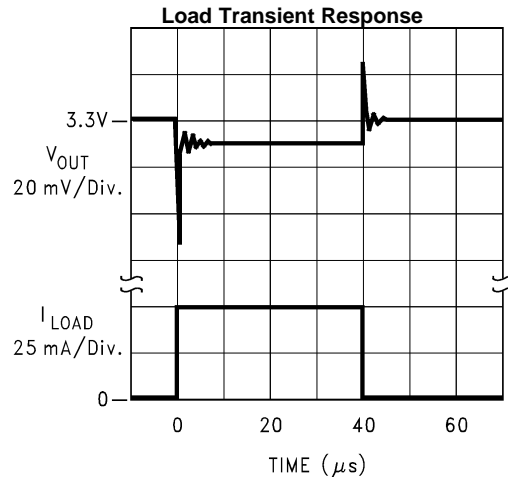


Figure 9.

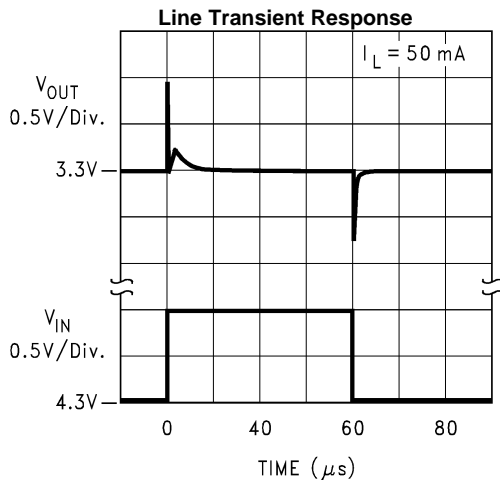


Figure 10.

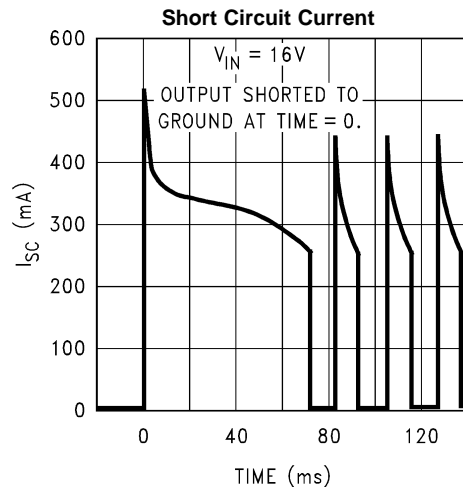


Figure 11.

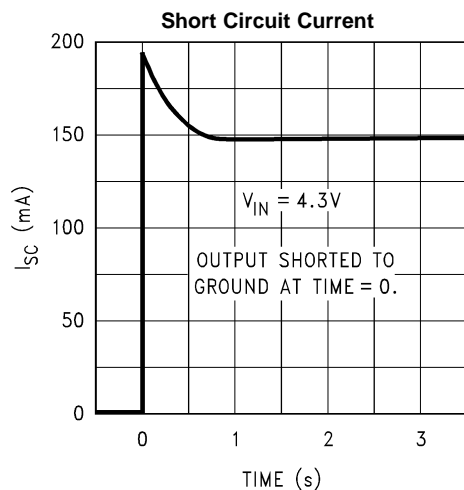


Figure 12.

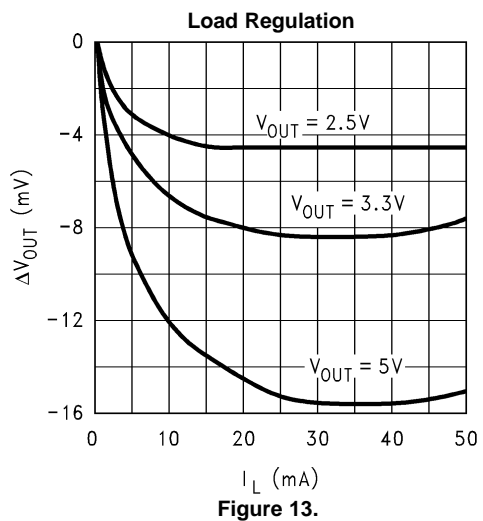


Figure 13.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{O(NOM)} + 1\text{V}$ ,  $I_L = 1\text{ mA}$ , ON/OFF pin tied to  $V_{IN}$ ,  $R_{ADJ} = 86.6\text{k}$ , and test circuit is as shown in Basic Application Circuit.

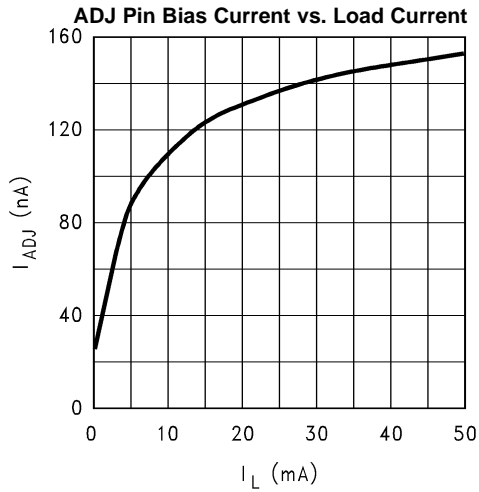


Figure 14.

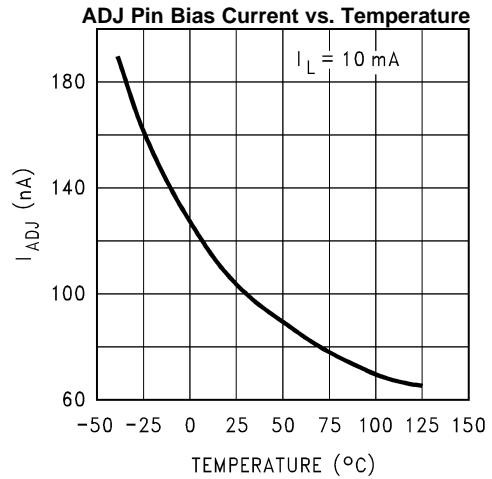


Figure 15.

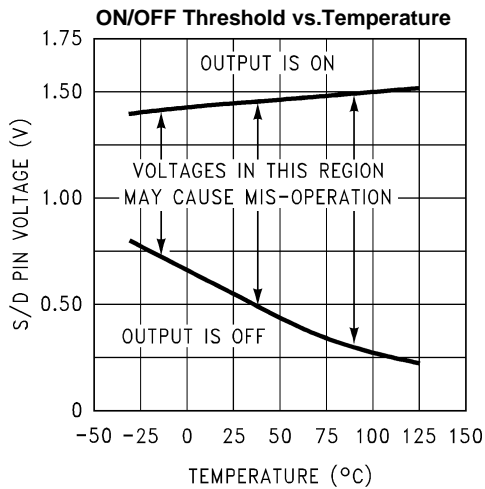


Figure 16.

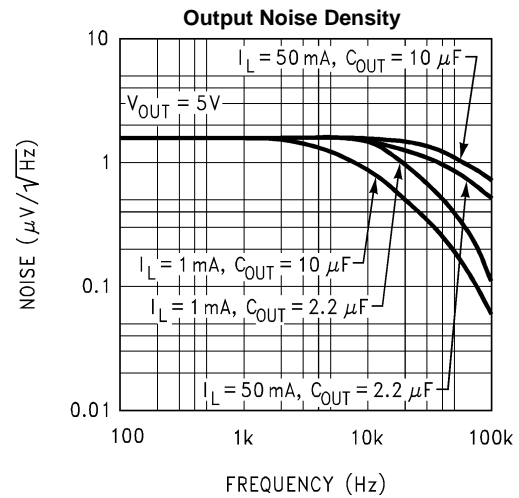


Figure 17.

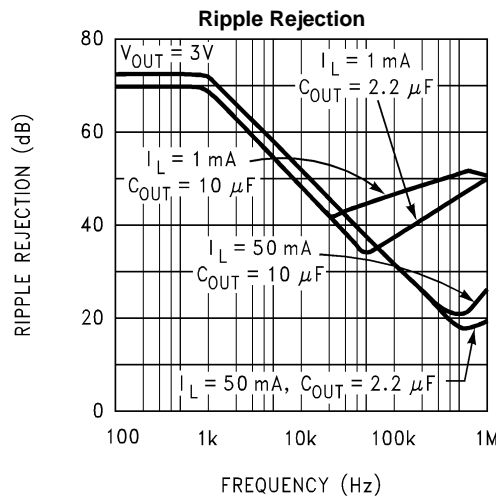


Figure 18.

## APPLICATION HINTS

### EXTERNAL CAPACITORS

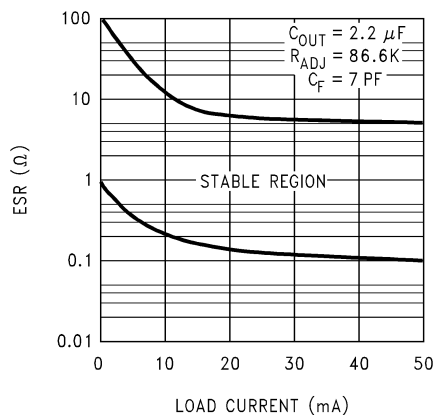
Like any low-dropout regulator, the external capacitors must be selected carefully to assure regulator loop stability.

**INPUT CAPACITOR:** An input capacitor whose value is  $\geq 1 \mu\text{F}$  is *required* (the amount of capacitance may be increased without limit).

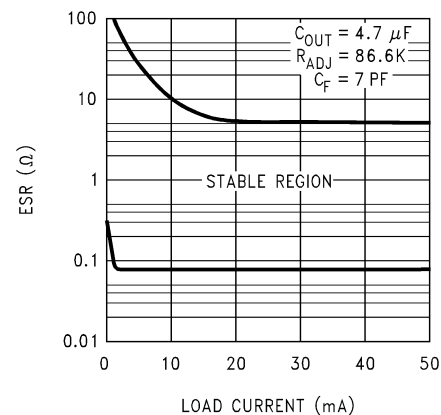
Any good quality Tantalum or Ceramic capacitor may be used here. The capacitor must be located not more than 0.5" from the input pin and returned to a clean analog ground.

**OUTPUT CAPACITOR:** The output capacitor must meet both the requirement for minimum amount of capacitance and E.S.R. (Equivalent Series Resistance) for stable operation.

Curves are provided below which show the allowable ESR of the output capacitor as a function of load current for both 2.2  $\mu\text{F}$  and 4.7  $\mu\text{F}$ . A solid Tantalum capacitor is the best choice for the output.



**Figure 19. 2.2  $\mu\text{F}$  ESR Curves**



**Figure 20. 4.7  $\mu\text{F}$  ESR Curves**

**IMPORTANT:** The output capacitor must maintain its ESR in the stable region *over the full operating temperature range* to assure stability. Also, capacitor tolerance and variation with temperature must be considered to assure the minimum amount of capacitance is provided at all times.

Note that this capacitor must be located not more than 0.5" from the output pin and returned to a clean analog ground.

**FEED-FORWARD CAPACITOR:** A 7 pF feed-forward capacitor is required (see [Basic Application Circuit](#)). The function of this capacitor is to provide the lead compensation necessary for loop stability.

A temperature-stable ceramic capacitor (type NPO or COG) should be used here.

### CAPACITOR CHARACTERISTICS

**TANTALUM:** The best capacitor choice for the LP2980-ADJ output is solid Tantalum. The ESR of a good quality Tantalum is almost perfectly centered in the middle of the "stable" range of the ESR curve (about 0.5 $\Omega$ –1 $\Omega$ ).

The temperature stability of Tantalums is typically very good, with a total variation of only about 2:1 over the temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (ESR increases at colder temperatures).

Off-brand capacitors should be avoided, as some poor quality Tantalums are seen with ESR's > 10 $\Omega$ , and this usually causes oscillation problems.

One caution about Tantalums if they are used on the input: the ESR of a Tantalum is low enough that it can be destroyed by surge current if powered up from a low impedance source (like a battery) that has no limit on inrush current. In these cases, use a ceramic input capacitor which does not have this problem.

**CERAMIC:** Ceramics are generally larger and more costly than Tantalums for a given amount of capacitance. Also, they have a very low ESR which is quite stable with temperature.



Be warned that the ESR of a ceramic capacitor is typically low enough to make an LDO oscillate: a 2.2  $\mu\text{F}$  ceramic demonstrated an ESR of about 15 m $\Omega$  when tested. If used as an output capacitor, this will cause instability (see ESR Curves).

If a ceramic is used on the output of an LDO, a small resistance (about 1 $\Omega$ ) should be placed in series with the capacitor. If it is used as an input capacitor, no resistor is needed as there is no requirement for ESR on capacitors used on the input.

## EXTERNAL RESISTORS

The output voltage is set using two external resistors (see [Basic Application Circuit](#)). It is recommended that the resistor from the ADJ pin to ground be 51.1 k $\Omega$ .

The other resistor ( $R_{\text{ADJ}}$ ) which connects between  $V_{\text{OUT}}$  and the ADJ pin is selected to set  $V_{\text{OUT}}$  as given by the formula:

$$V_{\text{OUT}} = V_{\text{REF}} + (V_{\text{REF}} \times (R_{\text{ADJ}} / 51.1 \text{ k}\Omega))$$

## REVERSE CURRENT PATH

The PNP power transistor used as the pass element in the LP2980-ADJ has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse biased (See [Figure 21](#)).

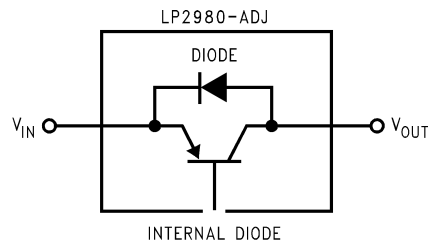


Figure 21. LP2980-ADJ Reverse Current Path

However, if the input voltage is more than a  $V_{\text{BE}}$  below the output voltage, this diode will turn ON and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into the  $V_{\text{IN}}$  pin and out the ground pin, which can damage the part.

The internal diode can also be turned on if the input voltage is abruptly stepped down to a voltage which is a  $V_{\text{BE}}$  below the output voltage.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from  $V_{\text{IN}}$  to  $V_{\text{OUT}}$  (cathode on  $V_{\text{IN}}$ , anode on  $V_{\text{OUT}}$ ). See [Figure 22](#), to limit the reverse voltage across the LP2980-ADJ to 0.3V (see [Absolute Maximum Ratings](#)).

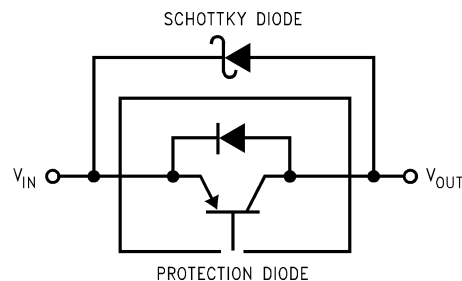


Figure 22. Adding External Schottky Diode Protection

## ON/OFF INPUT OPERATION

The LP2980-ADJ is shut off by driving the ON/OFF input low, and turned on by pulling the ON/OFF input high. If this feature is not to be used, the ON/OFF input must be tied to  $V_{IN}$  to keep the regulator output on at all times (the ON/OFF input must not be left floating).

To ensure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds which specify an ON or OFF state (see [Electrical Characteristics](#)).

It is also important that the turn-on (and turn-off) voltage signals applied to the ON/OFF input have a slew rate which is greater than 40 mV/ $\mu$ s.



**IMPORTANT:** The ON/OFF function will not operate correctly if a slow-moving signal is used to drive the ON/OFF input.

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**REVISION HISTORY**

| <b>Changes from Revision D (April 2013) to Revision E</b>  | <b>Page</b>           |
|--|-----------------------|
| <hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul> <hr/> | <hr/> <b>10</b> <hr/> |

**PACKAGING INFORMATION**

| Orderable Device    | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|---------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| LP2980IM5-ADJ       | NRND          | SOT-23       | DBV             | 5    | 1000        | TBD                     | Call TI                 | Call TI              | -40 to 125   | L06B                    |   |
| LP2980IM5-ADJ/NOPB  | ACTIVE        | SOT-23       | DBV             | 5    | 1000        | Green (RoHS & no Sb/Br) | SN                      | Level-1-260C-UNLIM   | -40 to 125   | L06B                    |  |
| LP2980IM5X-ADJ      | NRND          | SOT-23       | DBV             | 5    | 3000        | TBD                     | Call TI                 | Call TI              | -40 to 125   | L06B                    |   |
| LP2980IM5X-ADJ/NOPB | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | Green (RoHS & no Sb/Br) | SN                      | Level-1-260C-UNLIM   | -40 to 125   | L06B                    |  |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device              | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP2980IM5-ADJ       | SOT-23       | DBV             | 5    | 1000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LP2980IM5-ADJ/NOPB  | SOT-23       | DBV             | 5    | 1000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LP2980IM5X-ADJ      | SOT-23       | DBV             | 5    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LP2980IM5X-ADJ/NOPB | SOT-23       | DBV             | 5    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device              | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP2980IM5-ADJ       | SOT-23       | DBV             | 5    | 1000 | 210.0       | 185.0      | 35.0        |
| LP2980IM5-ADJ/NOPB  | SOT-23       | DBV             | 5    | 1000 | 210.0       | 185.0      | 35.0        |
| LP2980IM5X-ADJ      | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| LP2980IM5X-ADJ/NOPB | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |

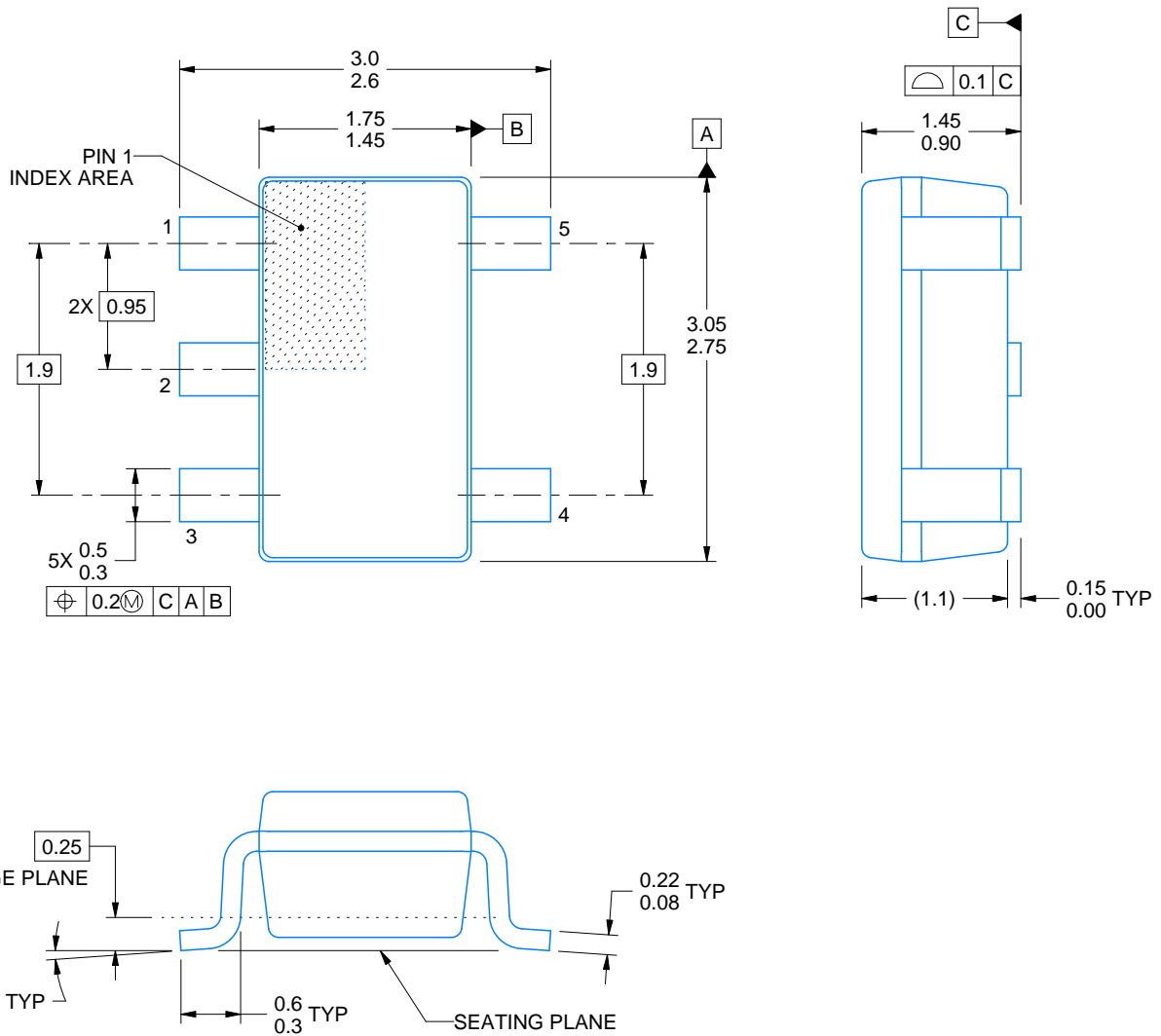
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

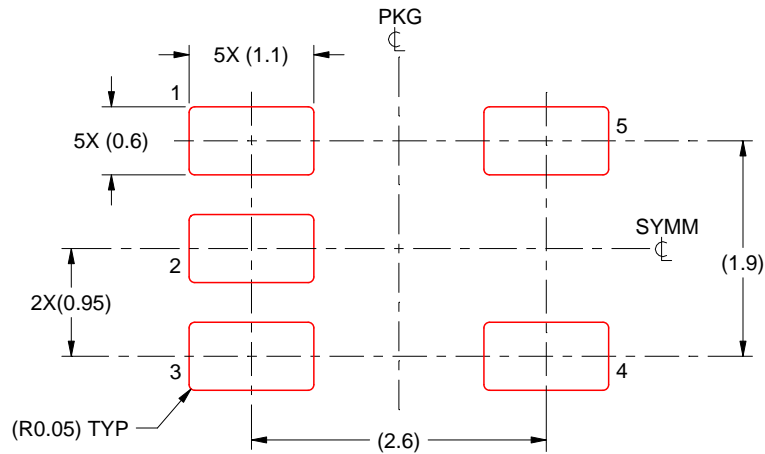
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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