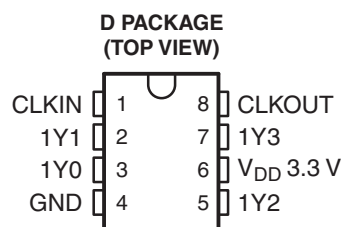


3.3-V CLOCK PHASE-LOCKED LOOP CLOCK DRIVER

FEATURES

- Qualified for Automotive Applications
- Phase-Locked Loop Clock Driver for Synchronous DRAM and General-Purpose Applications
- Spread-Spectrum Clock Compatible
- Operating Frequency: 24 MHz to 200 MHz
- Low Jitter (Cycle-to-Cycle): <150 ps Over the Range 66 MHz to 200 MHz
- Distributes One Clock Input to One Bank of Five Outputs (CLKOUT Is Used to Tune the Input-Output Delay)
- Three-States Outputs When There Is No Input Clock
- Operates From Single 3.3-V Supply
- Available in 8-Pin SOIC Package
- Consumes Less Than 100 μ A (Typically) in Power Down Mode
- Internal Feedback Loop Is Used to Synchronize the Outputs to the Input Clock
- 25- Ω On-Chip Series Damping Resistors
- Integrated RC PLL Loop Filter Eliminates the Need for External Components



DESCRIPTION

The CDCVF2505 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks (1Y[0–3] and CLKOUT) to the input clock signal (CLKIN). The CDCVF2505 operates at 3.3 V. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs provides low-skew, low-jitter copies of CLKIN. Output duty cycles are adjusted to 50 percent, independent of duty cycle at CLKIN. The device automatically goes in power-down mode when no input signal is applied to CLKIN.

Unlike many products containing PLLs, the CDCVF2505 does not require an external RC network. The loop filter for the PLLs is included on-chip, minimizing component count, space, and cost.

Because it is based on the PLL circuitry, the CDCVF2505 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN, and following any changes to the PLL reference.

The CDCVF2505 is characterized for operation from –40°C to 85°C.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Reel of 2500	CDCVF2505IDRQ1	CKV05Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



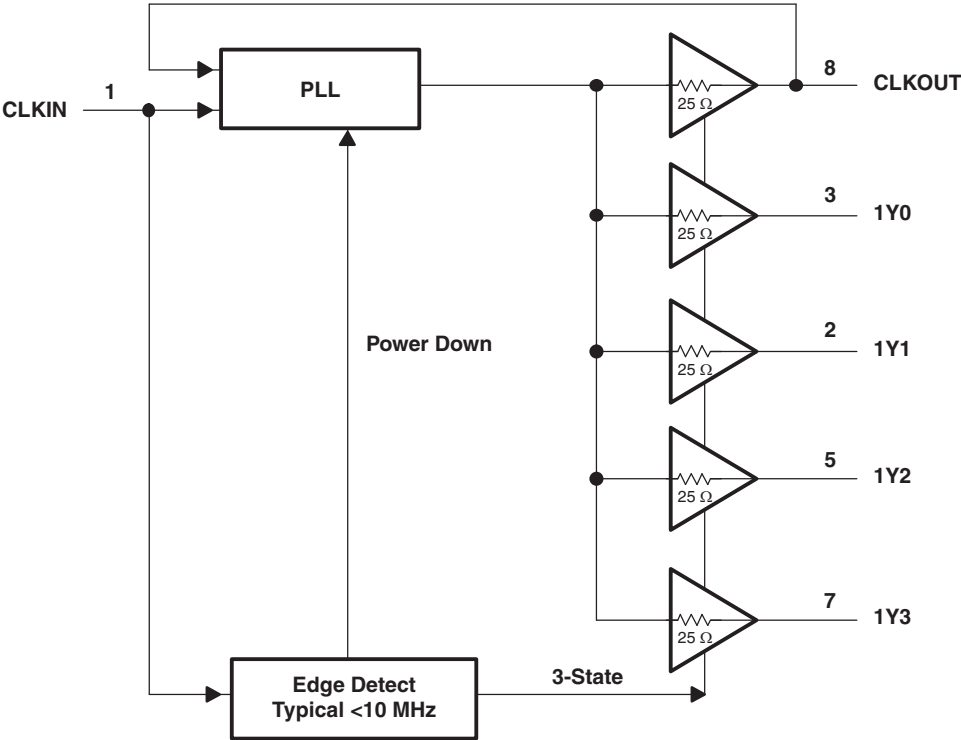
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE

INPUT	OUTPUTS	
CLKIN	1Y[0–3]	CLKOUT
L	L	L
H	H	H
<10 MHz ⁽¹⁾	Z	Z

- (1) Below 2 MHz (typical) the device goes into power-down mode, during which the PLL is turned off and the outputs enter into Hi-Z mode. If a >10-MHz signal is applied at CLKIN, the PLL turns on, reacquires lock, and stabilizes after approximately 100 μs. The outputs are then enabled.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
1Y0	3	O	Clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series damping resistor.
1Y1	2		
1Y2	5		
1Y3	7		
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDCVF2505 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid signal is applied, a stabilization time (100 μs) is required for the PLL to phase lock the feedback signal to CLKIN.
CLKOUT	8	O	Feedback output. CLKOUT completes the internal feedback loop of the PLL. This connection is made inside the chip and an external feedback loop should NOT be connected. CLKOUT can be loaded with a capacitor to achieve zero delay between CLKIN and the Y outputs.
GND	4	Power	Ground
V _{DD} 3.3V	6	Power	3.3-V supply

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage range		–0.5 V to 4.3 V
V_I	Input voltage range ⁽²⁾⁽³⁾		–0.5 V to $V_{DD} + 0.5$ V
V_O	Output voltage range ⁽²⁾⁽³⁾		–0.5 V to $V_{DD} + 0.5$ V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	±50 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	±50 mA
I_O	Continuous total output current	$V_O = 0$ to V_{DD}	±50 mA
θ_{JA}	Package thermal impedance ⁽⁴⁾		97.1°C/W
T_{stg}	Storage temperature range		–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 4.3 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTROSTATIC DISCHARGE INFORMATION

ESD MODEL		LIMIT
HBM	Human-Body Model	2000 V
MM	Machine Model	300 V
CDM	Charged-Device Model	1000 V

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V_{DD}	3	3.3	3.6	V
V_{IH}	$0.7 \times V_{DD}$			V
V_{IL}	$0.3 \times V_{DD}$			V
V_I	0		V_{DD}	V
I_{OH}			–12	mA
I_{OL}			12	mA
T_A	–40		85	°C

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	MIN	NOM	MAX	UNIT
f_{clk}	24		200	MHz
Input clock duty cycle	30		85	%
	40	50	60	
Stabilization time ⁽²⁾			100	μs

- (1) Specified by design.
- (2) Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{DD}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input voltage	I _I = –18 mA	3 V			–1.2	V
V _{OH}	High-level output voltage	I _{OH} = –100 µA	MIN to MAX	V _{DD} – 0.2			V
		I _{OH} = –12 mA	3 V	2.1			
		I _{OH} = –6 mA	3 V	2.4			
V _{OL}	Low-level output voltage	I _{OL} = 100 µA	MIN to MAX			0.2	V
		I _{OL} = 12 mA	3 V			0.8	
		I _{OL} = 6 mA	3 V			0.55	
I _{OH}	High-level output current	V _O = 1 V	3 V	–27			mA
		V _O = 1.65 V	3.3 V	–36			
I _{OL}	Low-level output current	V _O = 2 V	3 V	27			mA
		V _O = 1.65 V	3.3 V	40			
I _I	Input current	V _I = 0 V or V _{DD}				±5	µA
C _i	Input capacitance	V _I = 0 V or V _{DD}	3.3 V	4.2			pF
C _O	Output capacitance	Yn CLKOUT	3.3 V	2.8			pF
				5.2			

(1) All typical values are at nominal V_{DD} and T_A = 25°C.

SWITCHING CHARACTERISTICS⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

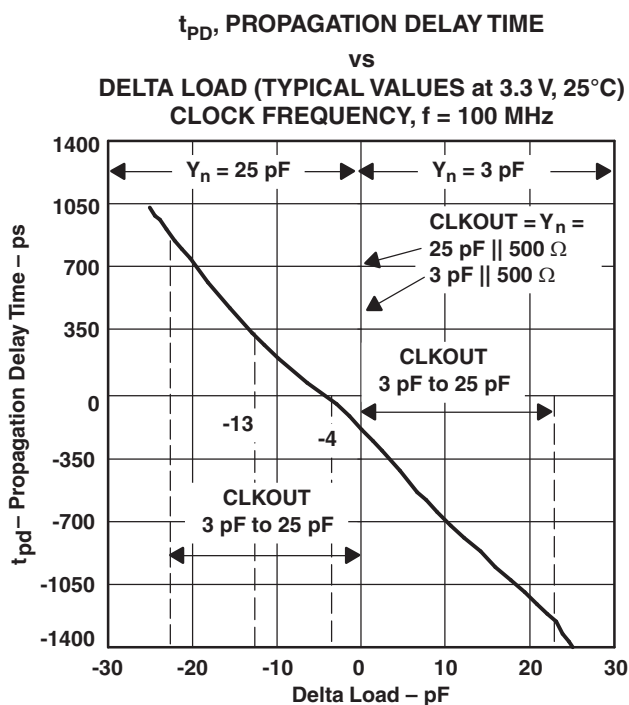
PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
t _{pd}	Propagation delay, normalized (see Figure 1)	CLKIN to Yn, f = 66 MHz to 200 MHz	–150		150	ps
t _{sk(o)}	Output skew ⁽³⁾	Yn to Yn			150	ps
t _{c(jit_cc)}	Jitter (cycle to cycle) (see Figure 5)	f = 66 MHz to 200 MHz		70	150	ps
		f = 24 MHz to 50 MHz		200	400	
odc	Output duty cycle (see Figure 4)	f = 24 MHz to 200 MHz at 50% V _{DD}	45		55	%
t _r	Rise time	V _O = 0.4 V to 2 V	0.5		2	ns
t _f	Fall time	V _O = 2 V to 0.4 V	0.5		2	ns

(1) Not production tested

(2) All typical values are at nominal V_{DD} and T_A = 25°C.

(3) The t_{sk(o)} specification is only valid for equal loading of all outputs.

TYPICAL CHARACTERISTICS



NOTE: Delta Load = CLKOUT Load - Y_n Load

Figure 1.

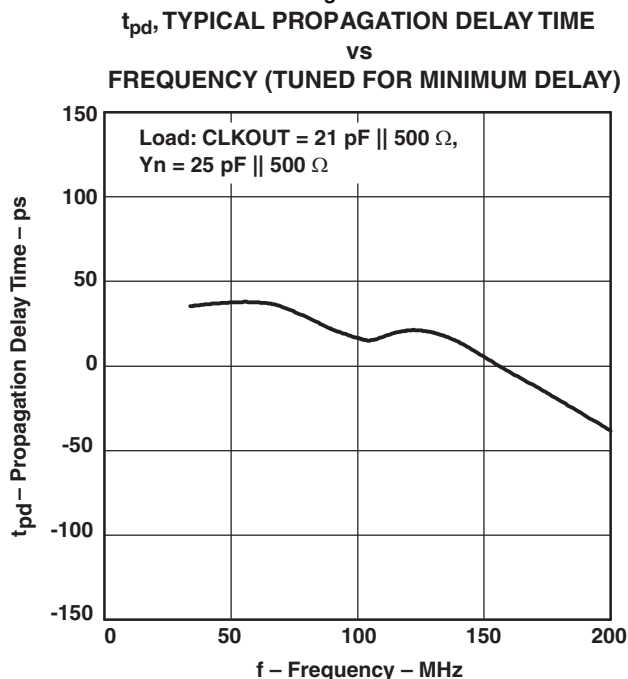


Figure 3.

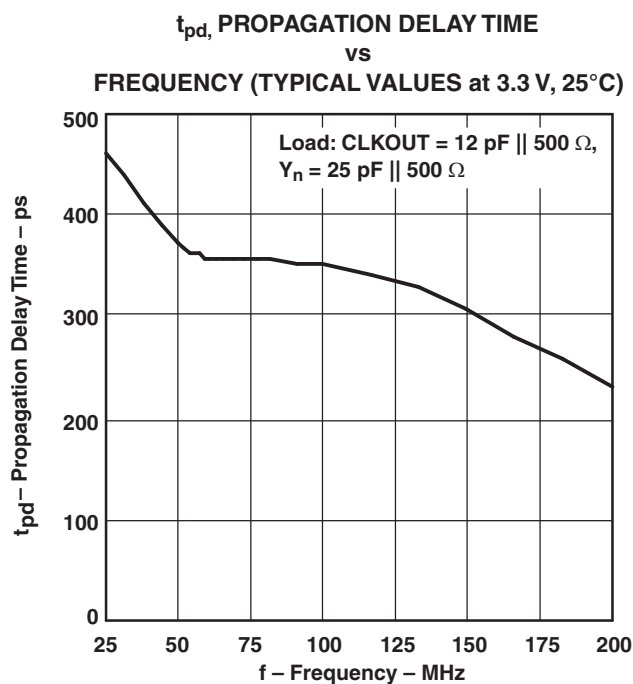


Figure 2.

DUTY CYCLE vs FREQUENCY

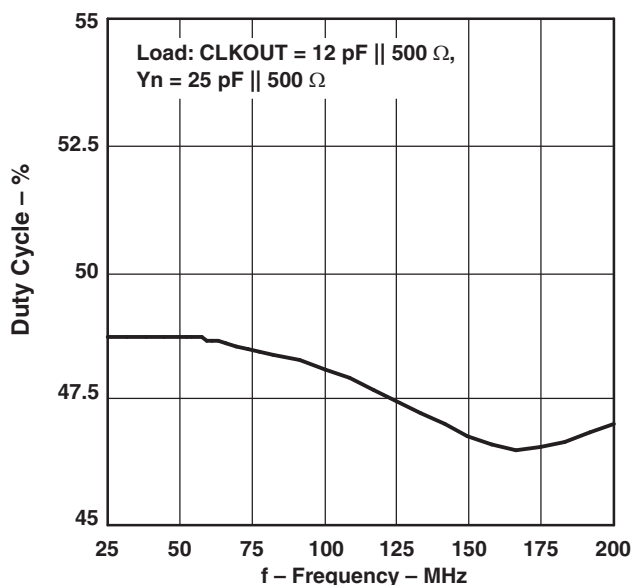


Figure 4.

TYPICAL CHARACTERISTICS (continued)

**CYCLE-to-CYCLE JITTER
vs
FREQUENCY**

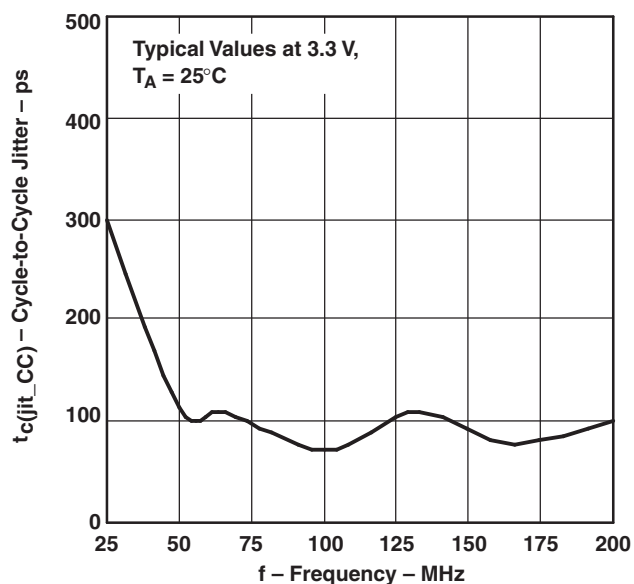


Figure 5.

**I_{CC} , SUPPLY CURRENT
vs
FREQUENCY**

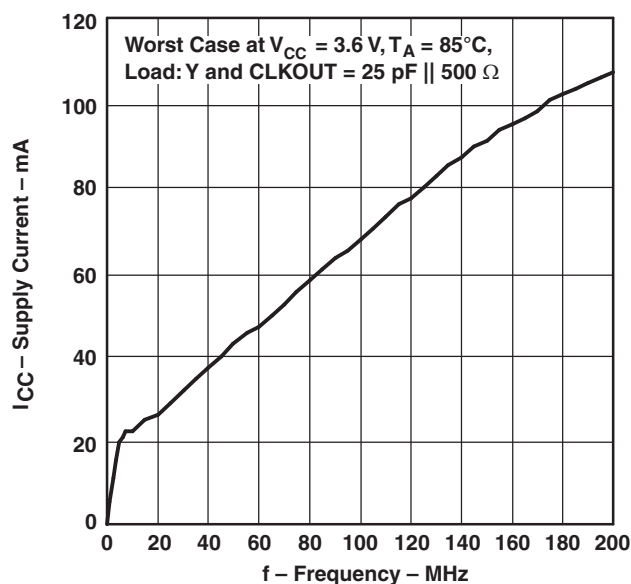


Figure 6.

PARAMETER MEASUREMENT INFORMATION

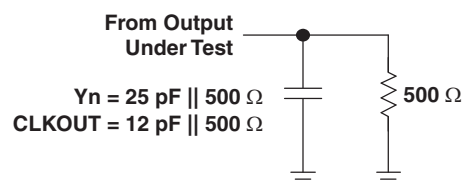


Figure 7. Test Load Circuit

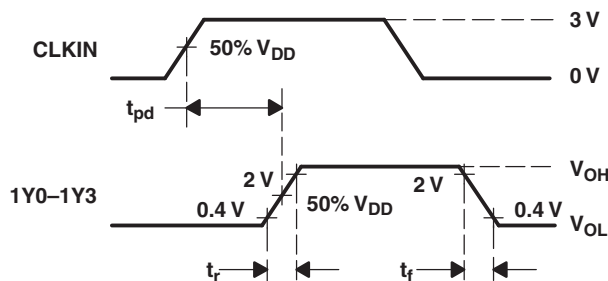


Figure 8. Voltage Threshold for Measurements, Propagation Delay (t_{pd})

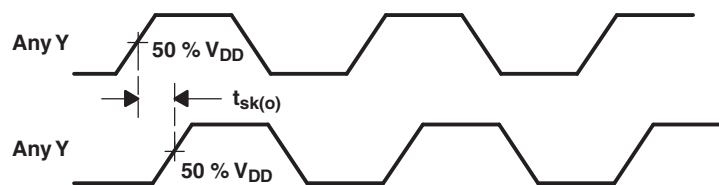


Figure 9. Output Skew

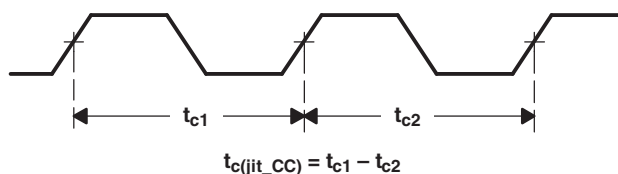


Figure 10. Cycle-to-Cycle Jitter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF2505IDRQ1	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05Q	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CDCVF2505-Q1 :

-
- Catalog: [CDCVF2505](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2505IDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2505IDRQ1	SOIC	D	8	2500	350.0	350.0	43.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



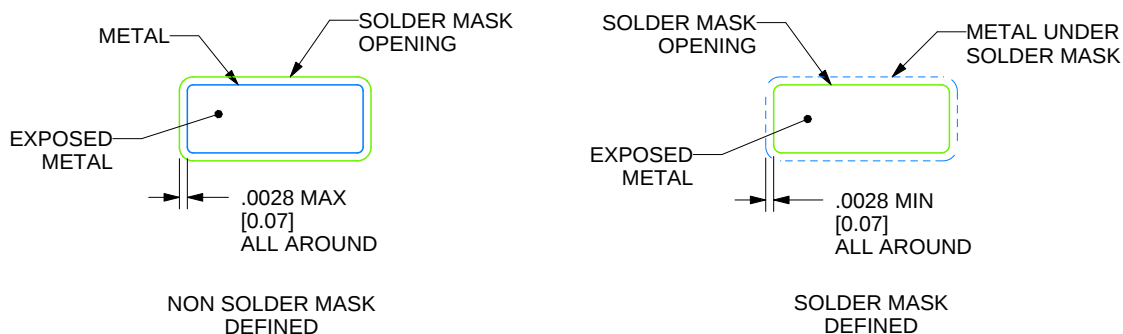
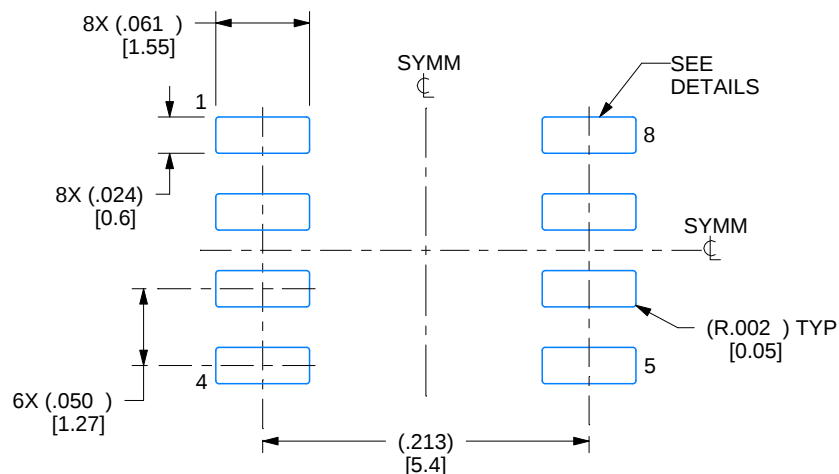
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

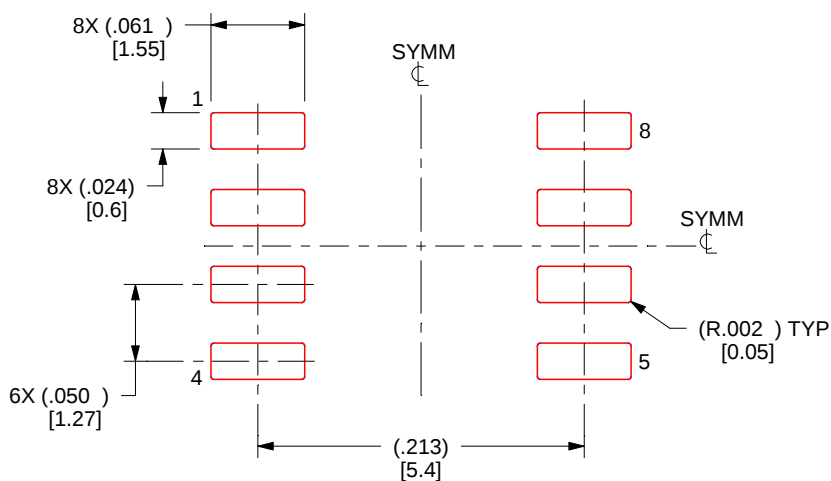
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated