



# SN74HCS595-Q1 Automotive 8-Bit Shift Register With Schmitt-Trigger Inputs and 3-State Output Registers

## 1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical  $I_{CC}$  of 100 nA
  - Typical input leakage current of  $\pm 100$  nA
- $\pm 7.8\text{-mA}$  output drive at 5 V

## 2 Applications

- [Output expansion](#)
- [LED matrix control](#)
- [7-segment display control](#)
- 8-bit data storage

## 3 Description

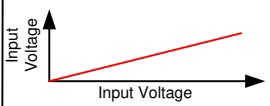
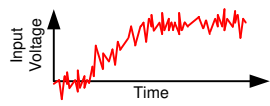
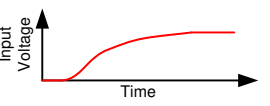
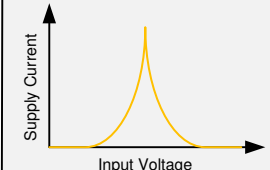
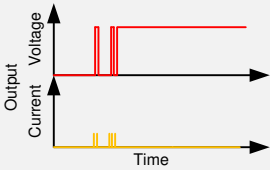
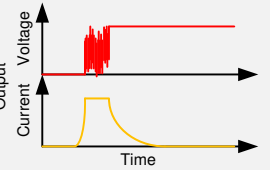
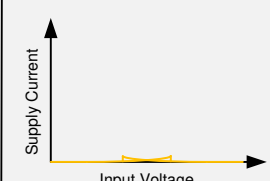
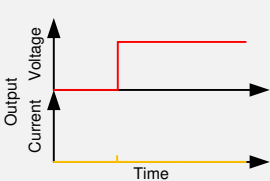
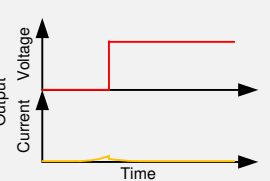
The SN74HCS595-Q1 device contains an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. All inputs include Schmitt-triggers, eliminating any erroneous data outputs due to slow-edged or noisy input signals. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and a serial output ( $Q_H$ ) for cascading. When the output-enable ( $\overline{OE}$ ) input is high, the outputs are in a high-impedance state. Internal register data is not impacted by the operation of the  $\overline{OE}$  input.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCS595QPWRQ1	TSSOP (16)	5.00 mm x 4.40 mm
SN74HCS595QDRQ1	SOIC (16)	9.90 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Benefits of Schmitt-trigger Inputs

	Low Power	Noise Rejection	Supports Slow Inputs
Input Voltage Waveforms			
Standard CMOS Input Response Waveforms			
Schmitt-trigger CMOS Input Response Waveforms			



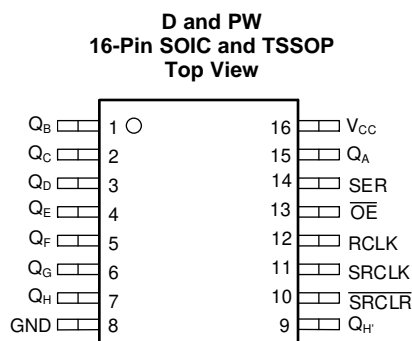
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## 4 Revision History

Changes from Original (December 2019) to Revision A	Page
• Added D package orderable .....	1
• Added D Package to Thermal Table .....	4

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
$Q_B$	1	Output	$Q_B$ output
$Q_C$	2	Output	$Q_C$ output
$Q_D$	3	Output	$Q_D$ output
$Q_E$	4	Output	$Q_E$ output
$Q_F$	5	Output	$Q_F$ output
$Q_G$	6	Output	$Q_G$ output
$Q_H$	7	Output	$Q_H$ output
GND	8	—	Ground
$Q_{H'}$	9	Output	Serial output, can be used for cascading
SRCLR	10	Input	Shift register clear, active low
SRCLK	11	Input	Shift register clock, rising edge triggered
RCLK	12	Input	Output register clock, rising edge triggered
$\overline{OE}$	13	Input	Output Enable, active low
SER	14	Input	Serial input
$Q_A$	15	Output	$Q_A$ output
$V_{CC}$	16	—	Positive supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		–0.5	7	V
$I_{IK}$	Input clamp current <sup>(2)</sup>	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$		±20	mA
$I_{OK}$	Output clamp current <sup>(2)</sup>	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$		±20	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		±35	mA
	Continuous current through $V_{CC}$ or GND			±70	mA
$T_J$	Junction temperature <sup>(3)</sup>			150	°C
$T_{stg}$	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2	5	6	V
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$T_A$	Ambient temperature	–40		125	°C

### 6.4 Thermal Information

THERMAL METRIC		SN74HCS595-Q1		UNIT
		PW (TSSOP)	D (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.2	122.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	80.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.8	80.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	27.7	40.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	85.5	80.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{T+}$	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
$V_{T-}$	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ ) <sup>(1)</sup>			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\ \mu\text{A}$	2 V to 6 V	$V_{CC} - 0.1$	$V_{CC} - 0.002$		V
			$I_{OH} = -6\ \text{mA}$	4.5 V	4.0	4.3		
			$I_{OH} = -7.8\ \text{mA}$	6 V	5.4	5.75		
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\ \mu\text{A}$	2 V to 6 V		0.002	0.1	V
			$I_{OL} = 6\ \text{mA}$	4.5 V		0.18	0.30	
			$I_{OL} = 7.8\ \text{mA}$	6 V		0.22	0.33	
$I_I$	Input leakage current	$V_I = V_{CC}$ or 0		6 V		$\pm 100$	$\pm 1000$	nA
$I_{CC}$	Supply current	$V_I = V_{CC}$ or 0, $I_O = 0$		6 V		0.1	2	$\mu\text{A}$
$C_i$	Input capacitance			2 V to 6 V			5	pF

(1) Guaranteed by design.

## 6.6 Timing Characteristics

$C_L = 50\ \text{pF}$ ; over operating free-air temperature range (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER			V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )				UNIT
				25°C		−40°C to 125°C		
				MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	SRCLK or RCLK high or low	2 V	7		9	ns	
			4.5 V	7		7		
			6 V	7		7		
		$\overline{\text{SRCLR}}$ low	2 V	8		10		
			4.5 V	7		7		
			6 V	7		7		
t <sub>su</sub>	Setup time	SER before SRCLK↑	2 V	8		13	ns	
			4.5 V	4		5		
			6 V	3		4		
		SRCLK↑ before RCLK↑	2 V	11		18		
			4.5 V	5		7		
			6 V	4		6		
		$\overline{\text{SRCLR}}$ low before RCLK↑	2 V	8		13		
			4.5 V	4		6		
			6 V	4		5		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	2 V	8		13		
			4.5 V	4		6		
			6 V	4		5		
t <sub>h</sub>	Hold time	SER after SRCLK↑	2 V	0		0	ns	
			4.5 V	0		0		
			6 V	0		0		

## 6.7 Switching Characteristics

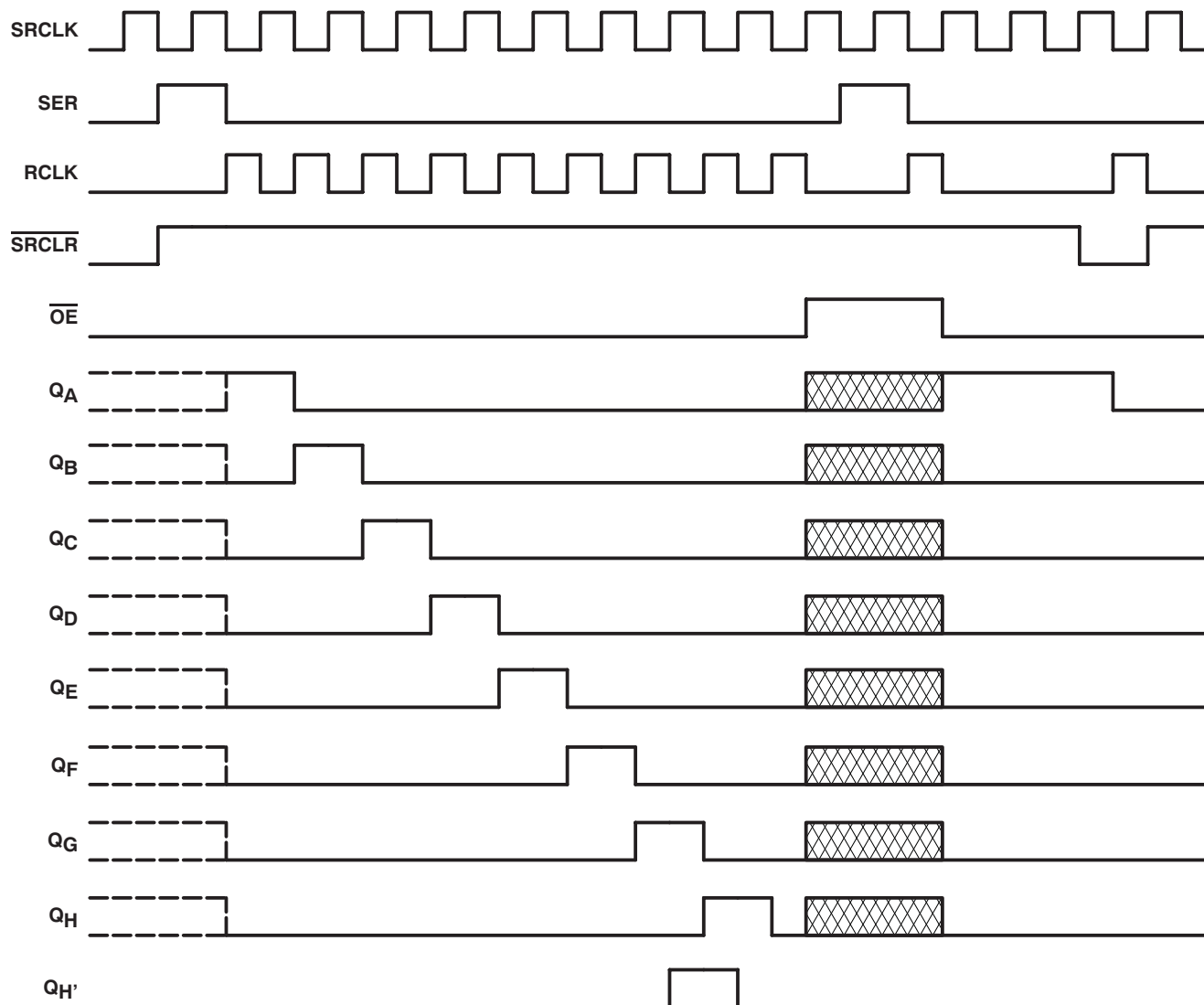
$C_L = 50$  pF; over operating free-air temperature range (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER		FROM	TO	V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )						UNIT
					25°C			−40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>	Max switching frequency			2 V	35			19			MHz
				4.5 V	110			60			
				6 V	130			75			
t <sub>pd</sub>	Propagation delay	SRCLK	Q <sub>H</sub> '	2 V	14		19	28			ns
				4.5 V	6		8	10			
				6 V	5		7	9			
		RCLK	Q <sub>A</sub> - Q <sub>H</sub>	2 V	16		21	37			
				4.5 V	6		9	12			
				6 V	6		8	10			
t <sub>PHL</sub>	Propagation delay	$\overline{\text{SRCLR}}$	Q <sub>H</sub> '	2 V	13		19	27			ns
				4.5 V	6		8	11			
				6 V	6		8	10			
t <sub>en</sub>	Enable time	$\overline{\text{OE}}$	Q <sub>A</sub> - Q <sub>H</sub>	2 V	12		18	27			ns
				4.5 V	6		9	13			
				6 V	5		8	11			
t <sub>dis</sub>	Disable time	$\overline{\text{OE}}$	Q <sub>A</sub> - Q <sub>H</sub>	2 V	13		16	20			ns
				4.5 V	9		11	13			
				6 V	8		10	12			
t <sub>t</sub>	Transition-time		Any output	2 V	9			16			ns
				4.5 V	5			9			
				6 V	4			8			

## 6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

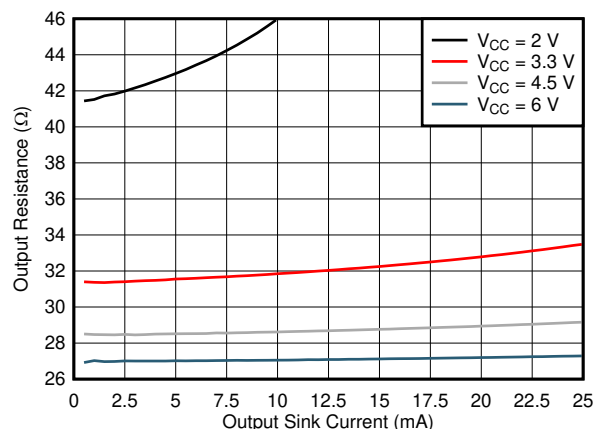
PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance per gate	No load	2 V to 6 V		40		pF



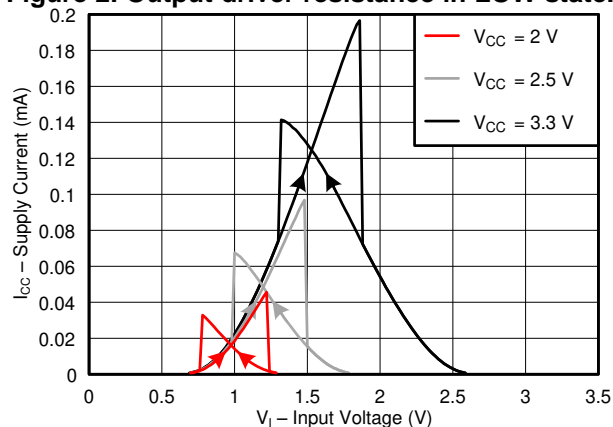
NOTE:  implies that the output is in 3-State mode.

**Figure 1. Timing Diagram**

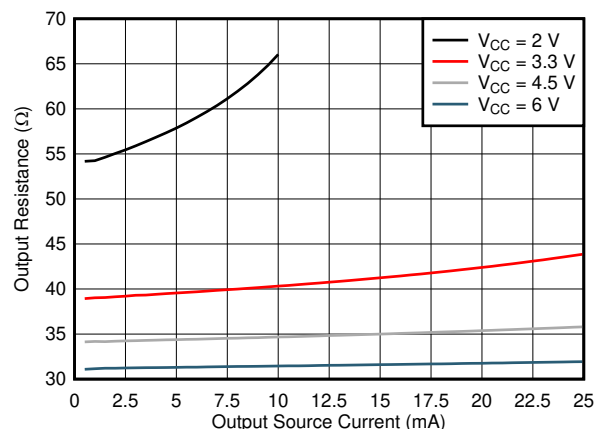
## 6.9 Typical Characteristics

 $T_A = 25^\circ\text{C}$ 


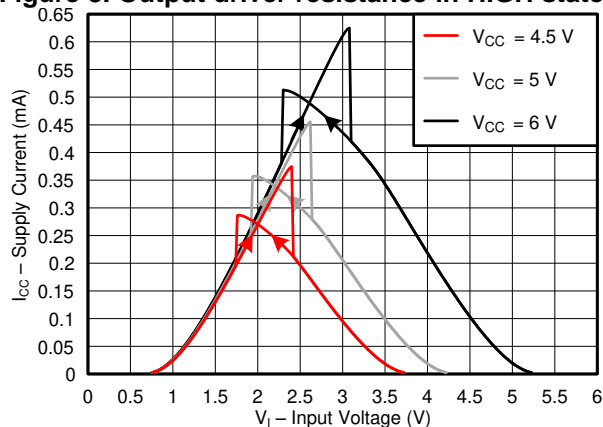
**Figure 2. Output driver resistance in LOW state.**



**Figure 4. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply**



**Figure 3. Output driver resistance in HIGH state.**



**Figure 5. Supply current across input voltage, 4.5-, 5-, and 6-V supply**

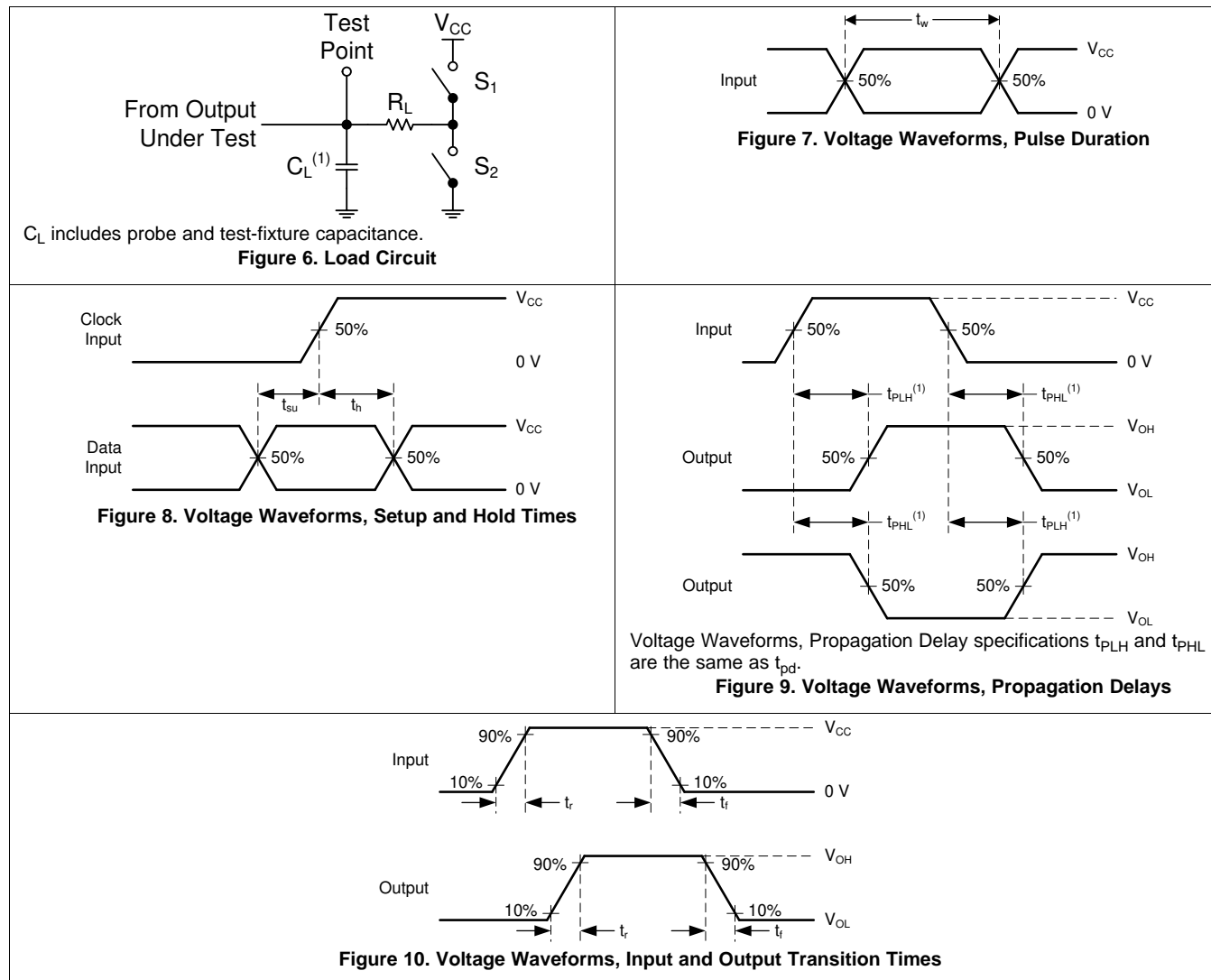


## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50\ \Omega$ ,  $t_f < 2.5\text{ ns}$ .

For clock inputs,  $f_{\max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



## 8 Detailed Description

### 8.1 Overview

Figure 11 describes the SN74HCS595-Q1, an 8-bit shift register that feeds an 8-bit D-type storage register. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register. All inputs include Schmitt-triggers allowing for slow input transitions and providing more noise margin.

### 8.2 Functional Block Diagram

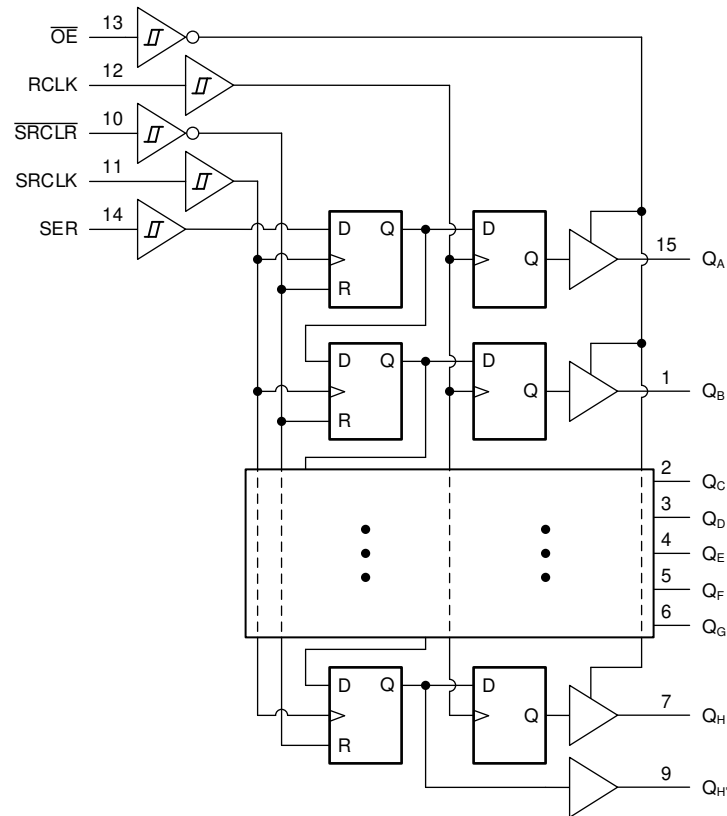


Figure 11. Logic Diagram (Positive Logic) for SN74HCS595-Q1

### 8.3 Feature Description

#### 8.3.1 Balanced CMOS 3-State Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

3-State outputs can be placed into a high-impedance state. In this state, the output will neither source nor sink current, and leakage current is defined by the  $I_{OZ}$  specification in the [Electrical Characteristics](#). A pull-up or pull-down resistor can be used to ensure that the output remains HIGH or LOW, respectively, during the high-impedance state.

## Feature Description (continued)

### 8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ( $R = V \div I$ ).

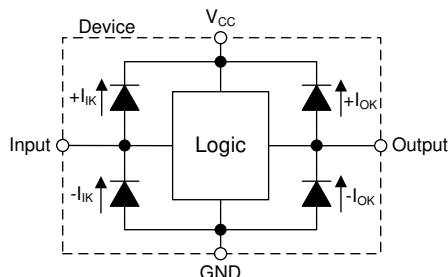
The Schmitt-trigger input architecture provides hysteresis as defined by  $\Delta V_T$  in the [Electrical Characteristics](#), which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

### 8.3.3 Positive and Negative Clamping Diodes

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Figure 12](#).

**CAUTION**

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**Figure 12. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74HCS595-Q1.

**Table 1. Function Table**

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs $Q_A - Q_H$ are disabled.
X	X	X	X	L	Outputs $Q_A - Q_H$ are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	H	↑	X	Shift-register data is stored in the storage register.
X	↑	H	↑	X	Data in shift register is stored in the storage register, the data is then shifted through

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

In this application, the SN74HCS595-Q1 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74HCS595-Q1 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The  $\overline{OE}$  pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74HCS595-Q1 can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many SN74HCS595-Q1 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register. An RC can be connected to the SRCLR pin as shown in Figure 13 to initialize the shift register to all zeros. With the  $\overline{OE}$  pin pulled up with a resistor, this process can be performed while the outputs are in a high impedance state eliminating any erroneous data causing issues with the displays.

### 9.2 Typical Application

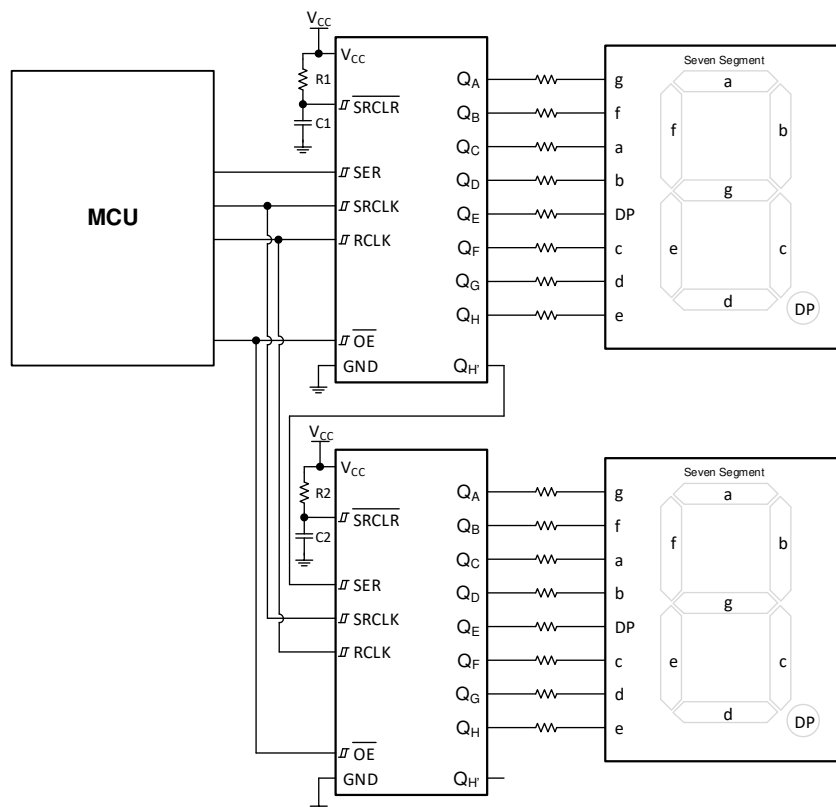


Figure 13. Output Expansion for 7-segment Display control

## Typical Application (continued)

### 9.2.1 Design Requirements

- All signals in the system operate at 5 V
- The RC values for the  $\overline{\text{SRCLR}}$  pin should be chosen such that the signal doesn't reach  $V_{\text{t+}}(\text{min})$  until the supply settles
- The resistors at the outputs should be chosen such that the total current through the  $V_{\text{CC}}$  or GND pin doesn't exceed the maximum value in [Absolute Maximum Ratings](#)
- Follow timing requirements given in

#### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS595-Q1 plus the maximum supply current,  $I_{\text{CC}}$ , listed in the [Electrical Characteristics](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or  $V_{\text{CC}}$  listed in the [Absolute Maximum Ratings](#).

The SN74HCS595-Q1 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and  \$C\_{\text{pd}}\$  Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{\text{J}}(\text{max})$  listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

#### 9.2.1.2 Input Considerations

Input signals must cross  $V_{\text{t}}(\text{min})$  to be considered a logic LOW, and  $V_{\text{t+}}(\text{max})$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the [Absolute Maximum Ratings](#).

Unused inputs must be terminated to either  $V_{\text{CC}}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS595-Q1, as specified in the [Electrical Characteristics](#), and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74HCS595-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the  $\Delta V_{\text{T}}(\text{min})$  in the [Electrical Characteristics](#). This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than  $V_{\text{CC}}$  or ground is plotted in the .

Refer to the [Feature Description](#) for additional information regarding the inputs for this device.

## Typical Application (continued)

### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the [Electrical Characteristics](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the [Electrical Characteristics](#).

Unused outputs can be left floating.

Refer to [Feature Description](#) for additional information regarding the outputs for this device.

### 9.2.1.4 Timing Considerations

The SN74HCS595-Q1 is a clocked device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Maximum clock frequency: the maximum operating clock frequency defined in is the maximum frequency at which the device is guaranteed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the .
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the .
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the .

### 9.2.2 Detailed Design Procedure

#### 1. Recommended Input Conditions:

- Input signals to Schmitt-trigger inputs, like those found on the HCS family of devices, can support unlimited edge rates.
- Input thresholds are listed in the [Electrical Characteristics](#).
- Inputs include positive clamp diodes. Input voltages can exceed the device's supply so long as the clamp current ratings are observed from the [Absolute Maximum Ratings](#). Do not exceed the absolute maximum voltage rating of the device or it could be damaged.

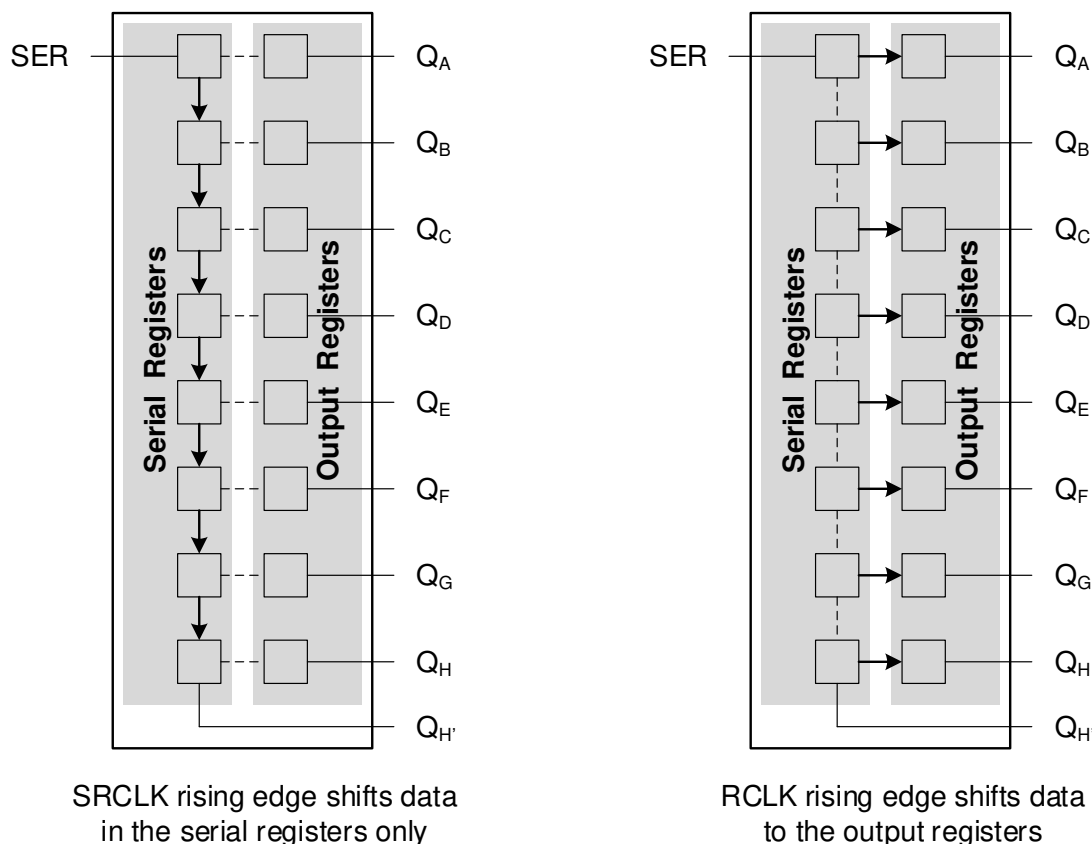
#### 2. Recommended Output Conditions:

- Load currents should not exceed the value listed in the [Absolute Maximum Ratings](#).
- Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

## Typical Application (continued)

### 9.2.3 Application Curve

Figure 14 illustrates the functionality of the SN74HCS595-Q1.



**Figure 14. Simplified Functionality of the SN74HCS595-Q1 Registers**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Absolute Maximum Ratings](#) table. Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. For this device, a 0.1- $\mu$ F capacitor is recommended. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminals as possible for best results.



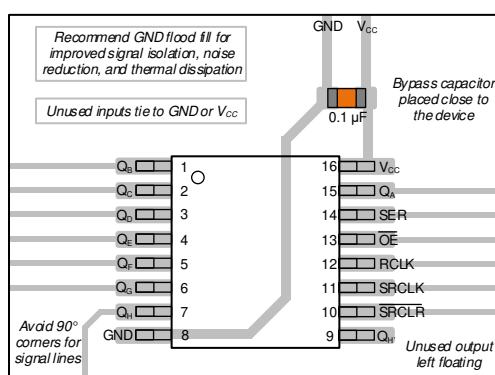
## 11 Layout

### 11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 channels are used. Such input pins should not be left completely unconnected because the unknown voltages result in undefined operational states.

Specified in [Figure 15](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is recommended to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.

### 11.2 Layout Example



**Figure 15. Layout Example**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Documentation Support

##### 12.1.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#) application report
- Texas Instruments, [Reduce Noise and Save Power with the New HCS Logic Family](#) application report
- Texas Instruments, [Understanding Schmitt Triggers](#) application report

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS595QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595Q	<a href="#">Samples</a>
SN74HCS595QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS595QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCS595QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

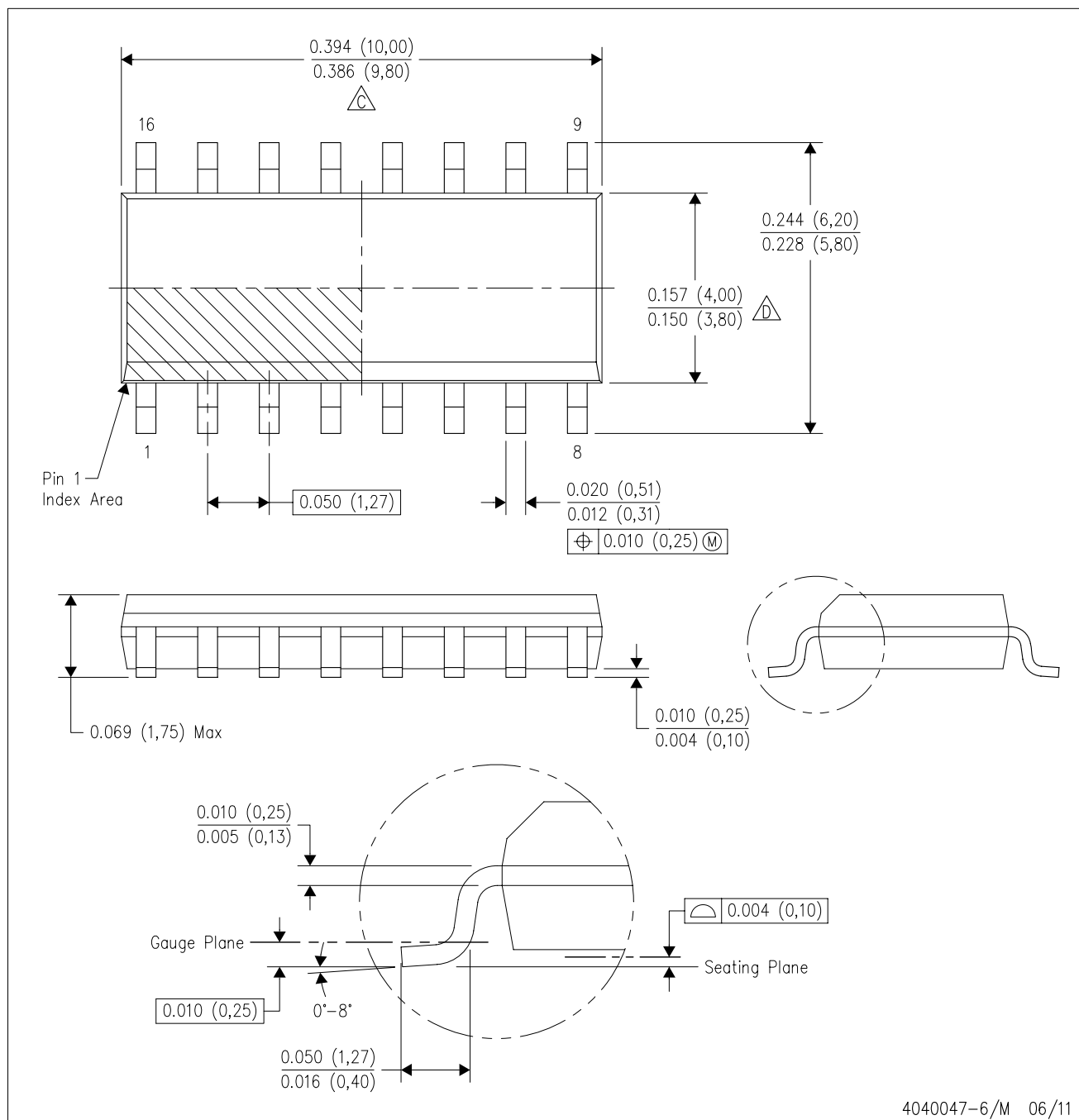


\*All dimensions are nominal

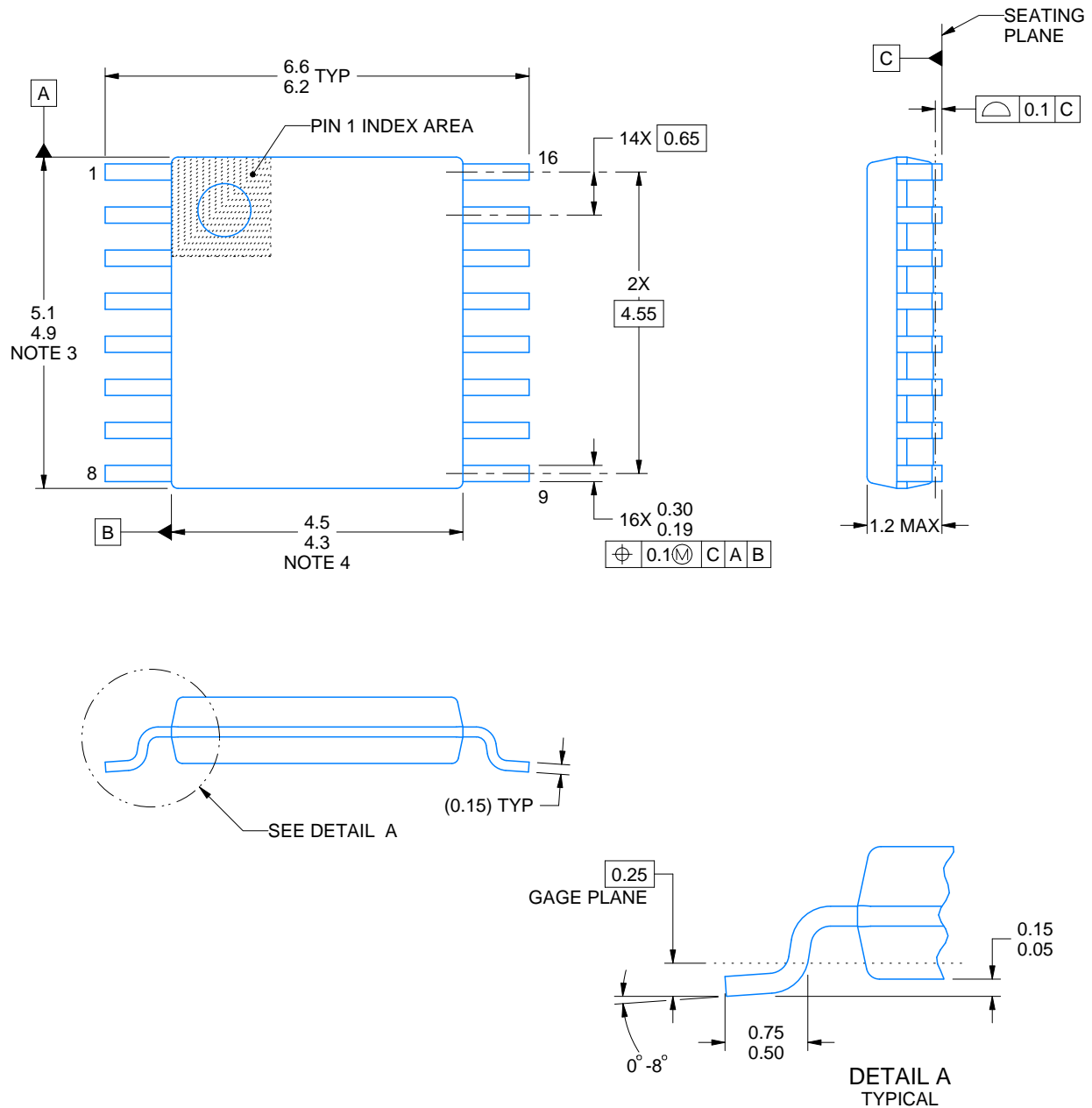
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS595QDRQ1	SOIC	D	16	2500	367.0	367.0	38.0
SN74HCS595QPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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