

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for pulsed wideband applications operating at frequencies between 3100 and 3500 MHz.

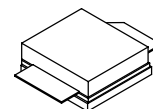
- Typical Pulsed Performance: $V_{DD} = 32$ Volts, $I_{DQ} = 50$ mA,
 $P_{out} = 15$ Watts Peak (3 Watts Avg.), Pulsed Signal, $f = 3500$ MHz,
Pulse Width = 100 μ sec, Duty Cycle = 20%
Power Gain — 16 dB
Drain Efficiency — 41%
- Typical WiMAX Performance: $V_{DD} = 32$ Volts, $I_{DQ} = 150$ mA,
 $P_{out} = 1.8$ Watts Avg., $f = 3500$ MHz, 802.16d, 64 QAM $3/4$, 4 Bursts,
10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01%
Probability on CCDF
Power Gain — 18 dB
Drain Efficiency — 16%
RCE — -33 dB (EVM — 2.2% rms)
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 3300 MHz, 15 Watts Peak Power
- Capable of Handling 3 dB Overdrive @ 32 Vdc

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13 inch Reel.

MRF7S35015HSR3

**3100-3500 MHz, 15 W PEAK, 32 V
PULSED
LATERAL N-CHANNEL
RF POWER MOSFET**



**CASE 465J-02, STYLE 1
NI-400S-240**

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	$^{\circ}$ C
Case Operating Temperature	T_C	150	$^{\circ}$ C
Operating Junction Temperature (1,2)	T_J	225	$^{\circ}$ C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80 $^{\circ}$ C, 15 W Pulsed, 100 μ sec Pulse Width, 20% Duty Cycle Case Temperature 81 $^{\circ}$ C, 15 W Pulsed, 500 μ sec Pulse Width, 10% Duty Cycle	$R_{\theta JC}$	0.60 0.73	$^{\circ}$ C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics

Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	2	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 33.5\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ($V_{DD} = 32\text{ Vdc}$, $I_D = 50\text{ mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	1.8	2.5	3.3	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 300\text{ mAdc}$)	$V_{DS(on)}$	0.1	1.7	0.3	Vdc

Dynamic Characteristics ⁽¹⁾

Reverse Transfer Capacitance ($V_{DS} = 32\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	0.12	—	pF
Output Capacitance ($V_{DS} = 32\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	92	—	pF
Input Capacitance ($V_{DS} = 32\text{ Vdc}$, $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz)	C_{iss}	—	46	—	pF

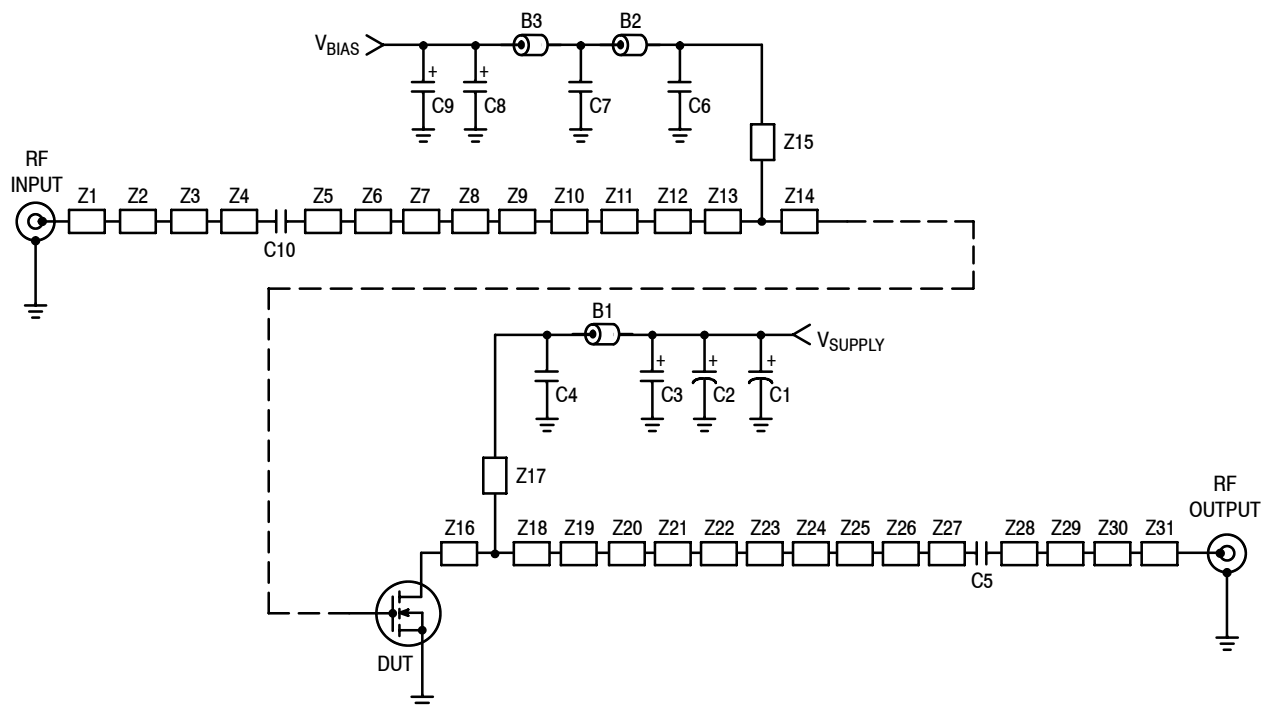
Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 32\text{ Vdc}$, $I_{DQ} = 50\text{ mA}$, $P_{out} = 15\text{ W Peak}$ (3 W Avg.), $f = 3100\text{ MHz}$ and $f = 3500\text{ MHz}$, Pulsed, 100 μsec Pulse Width, 20% Duty Cycle, 25 ns Input Rise Time

Power Gain	G_{ps}	13	16	19	dB
Drain Efficiency	η_D	38	41	—	%
Input Return Loss	IRL	—	-12	-7	dB

Pulsed RF Performance (In Freescale Application Test Fixture, 50 ohm system) $V_{DD} = 32\text{ Vdc}$, $I_{DQ} = 50\text{ mA}$, $P_{out} = 15\text{ W Peak}$ (3 W Avg.), $f = 3100\text{ MHz}$ and $f = 3500\text{ MHz}$, Pulsed, 100 μsec Pulse Width, 20% Duty Cycle, 25 ns Input Rise Time

Output Pulse Droop (500 μsec Pulse Width, 10% Duty Cycle)	DRP_{out}	—	0.2	—	dB
Load Mismatch Tolerance (VSWR = 10:1 at all Phase Angles)	VSWR-T	No Degradation in Output Power			

1. Part internally matched both on input and output.



Z1	0.375" x 0.071" Microstrip	Z18	0.078" x 0.454" Microstrip
Z2	0.126" x 0.524" Microstrip	Z19	0.055" x 0.244" Microstrip
Z3	0.079" x 0.016" Microstrip	Z20	0.630" x 0.073" Microstrip
Z4	0.153" x 0.071" Microstrip	Z21	0.218" x 0.038" Microstrip
Z5	0.076" x 0.520" Microstrip	Z22	0.060" x 0.552" Microstrip
Z6	0.037" x 0.252" Microstrip	Z23	0.079" x 0.038" Microstrip
Z7	0.322" x 0.073" Microstrip	Z24	0.062" x 0.526" Microstrip
Z8	0.123" x 0.440" Microstrip	Z25	0.032" x 0.070" Microstrip
Z9	0.048" x 0.073" Microstrip	Z26	0.110" x 0.526" Microstrip
Z10	0.081" x 0.184" Microstrip	Z27	0.053" x 0.072" Microstrip
Z11	0.030" x 0.262" Microstrip	Z28	0.028" x 0.070" Microstrip
Z12	0.525" x 0.336" Microstrip	Z29	0.098" x 0.148" Microstrip
Z13	0.182" x 0.466" Microstrip	Z30	0.062" x 0.526" Microstrip
Z14	0.077" x 0.466" Microstrip	Z31	0.529" x 0.070" Microstrip
Z15*	0.603" x 0.048" Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$
Z16	0.063" x 0.618" Microstrip		
Z17*	0.534" x 0.040" Microstrip		

* Line length includes microstrip bends

Figure 1. MRF7S35015HSR3 Test Circuit Schematic

Table 5. MRF7S35015HSR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1*	Long Ferrite Bead	2743021447	Fair-Rite
B2, B3	Short Ferrite Beads	2743019447	Fair-Rite
C1	470 μ F, 63 V Electrolytic Capacitor	477KXM063M	Illinois Cap
C2	47 μ F, 50 V Electrolytic Capacitor	476KXM050M	Illinois Cap
C3, C9	22 μ F, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C4, C5, C10	2.7 pF Chip Capacitors	ATC100B2R7BT500XT	ATC
C6	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C7	0.1 μ F Chip Capacitor	CDR33BX104AKYS	AVX
C8	22 μ F, 25 V Tantalum Capacitor	T491D226K025AT	Kemet

*B1 is removed for WiMAX circuit performance.

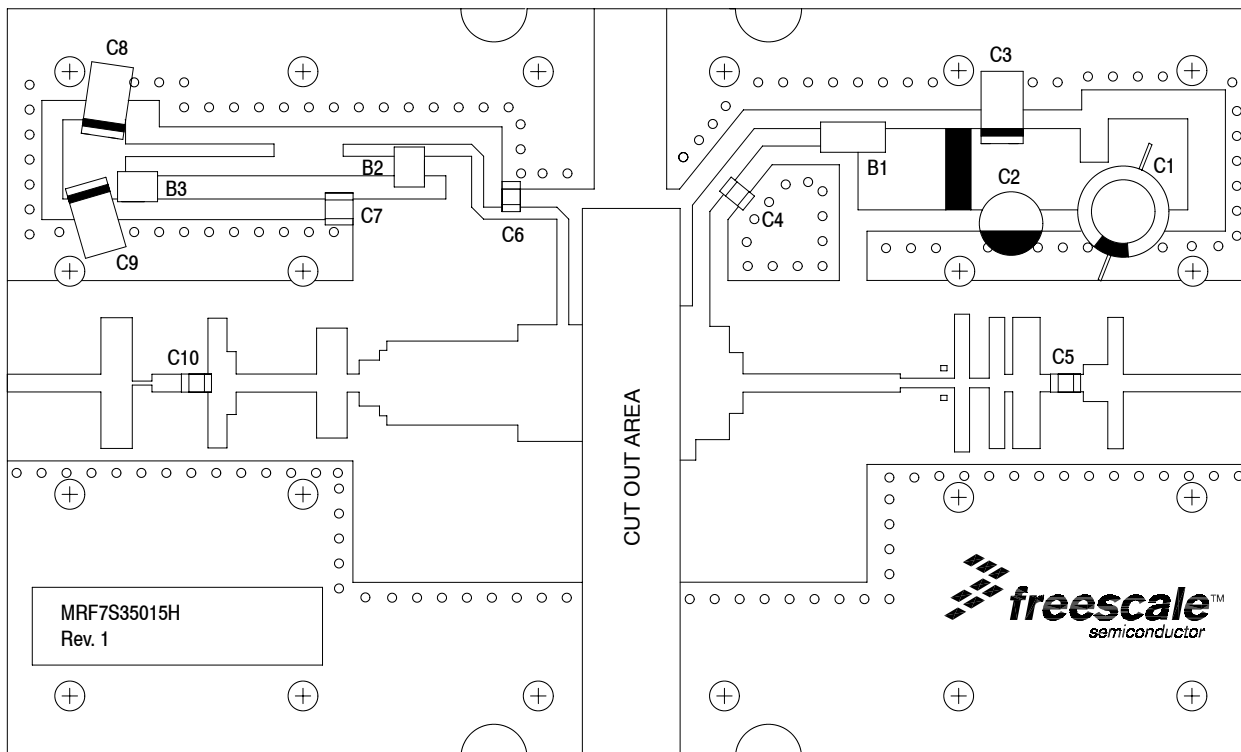


Figure 2. MRF7S35015HSR3 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

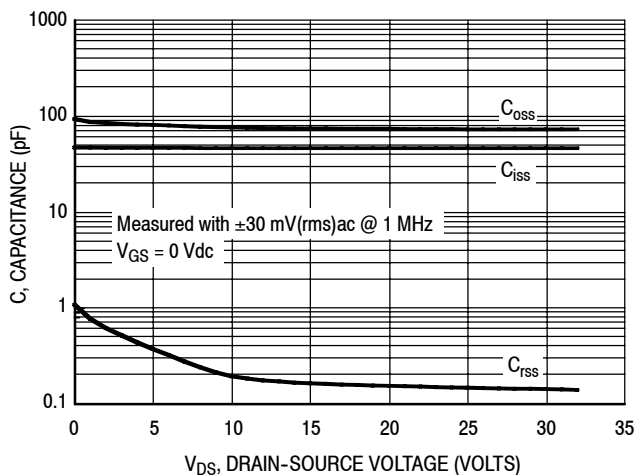


Figure 3. Capacitance versus Drain-Source Voltage

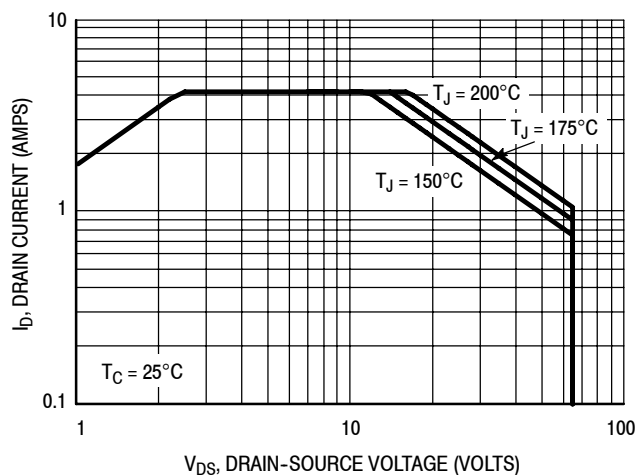


Figure 4. DC Safe Operating Area

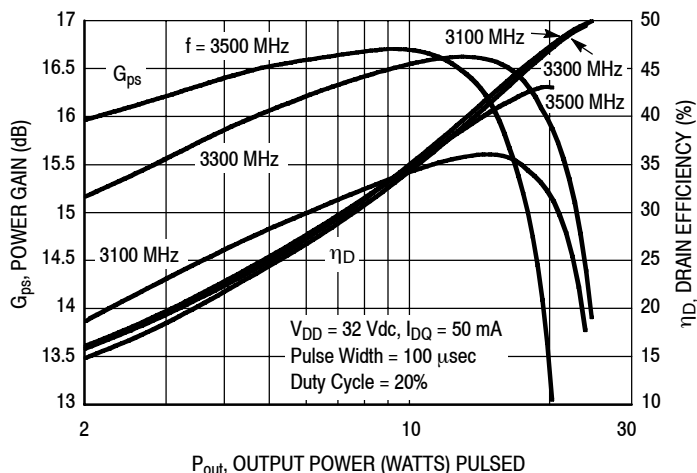


Figure 5. Pulsed Power Gain and Drain Efficiency versus Output Power

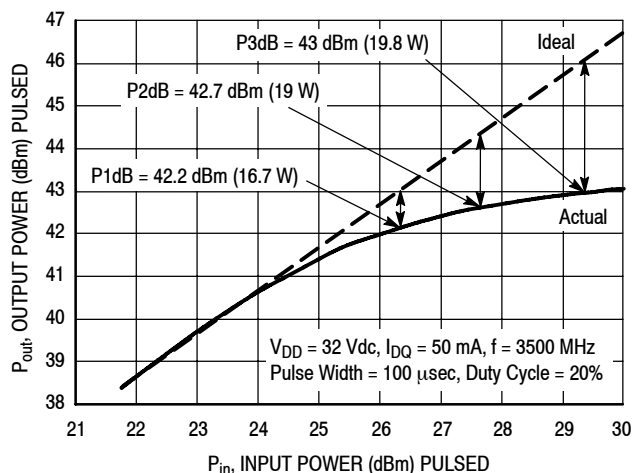


Figure 6. Pulsed Output Power versus Input Power

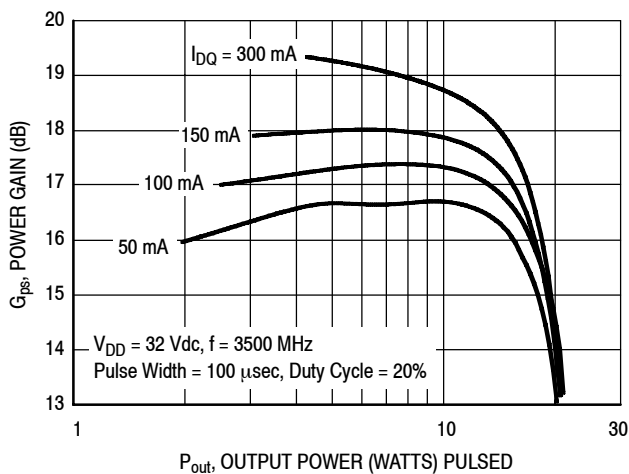


Figure 7. Pulsed Power Gain versus Output Power

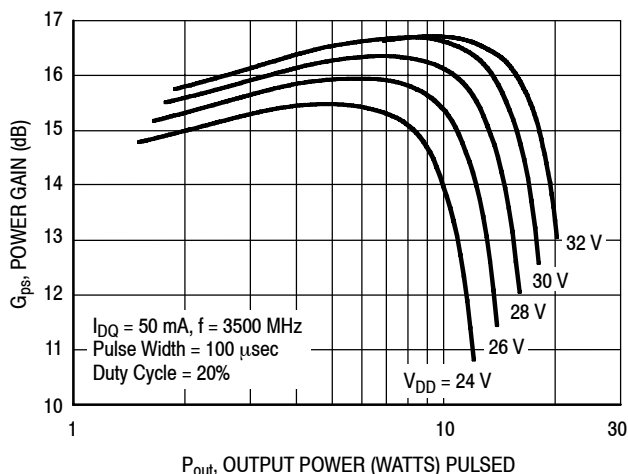


Figure 8. Pulsed Power Gain versus Output Power

TYPICAL CHARACTERISTICS

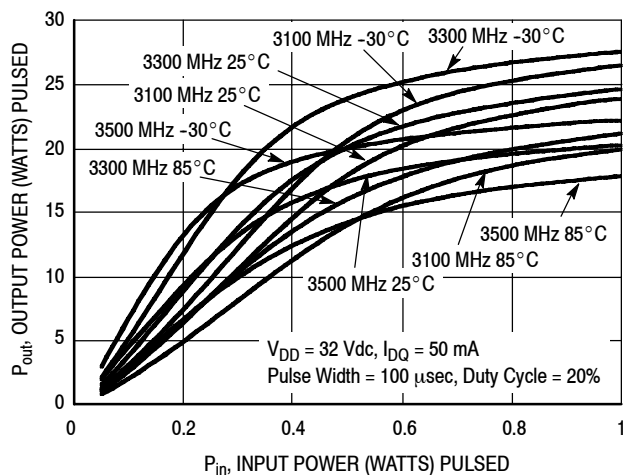


Figure 9. Pulsed Output Power versus Input Power

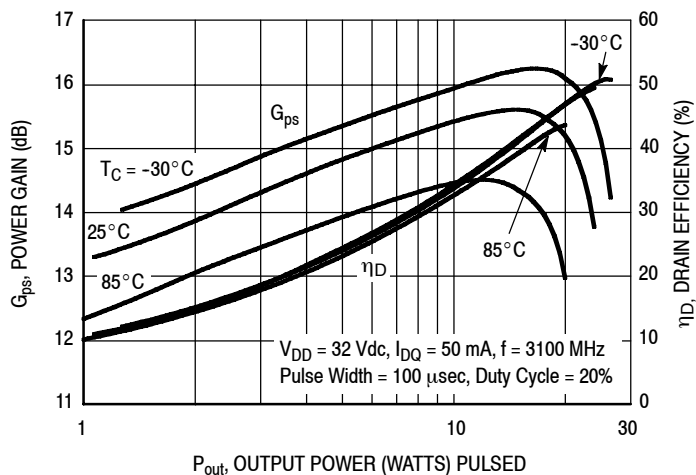


Figure 10. Pulsed Power Gain and Drain Efficiency versus Output Power — 3100 MHz

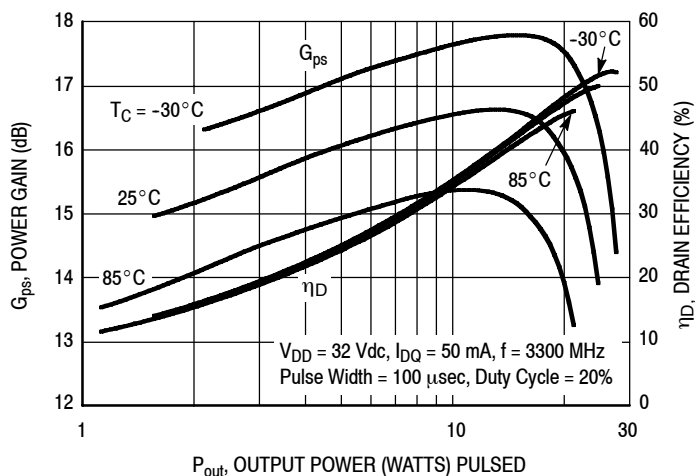


Figure 11. Pulsed Power Gain and Drain Efficiency versus Output Power — 3300 MHz

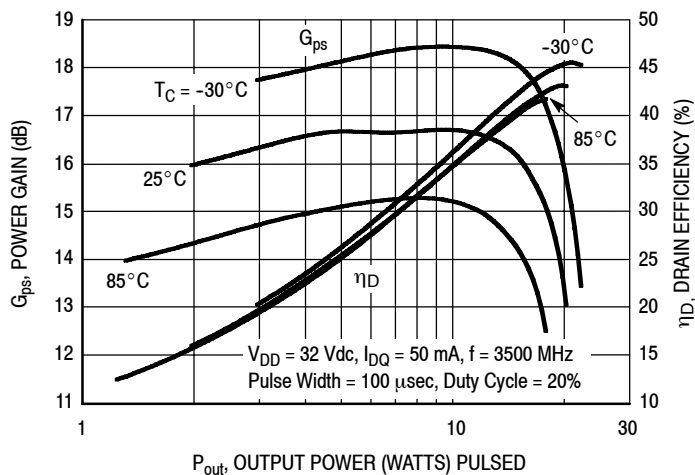


Figure 12. Pulsed Power Gain and Drain Efficiency versus Output Power — 3500 MHz

TYPICAL CHARACTERISTICS

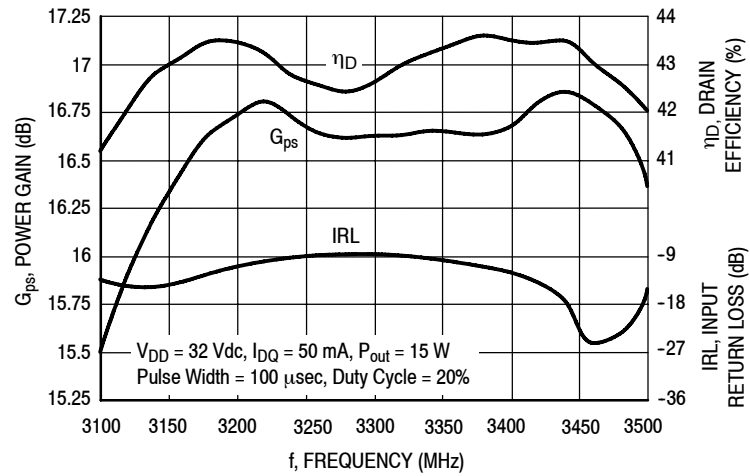


Figure 13. Pulsed Power Gain, Drain Efficiency and IRL versus Frequency

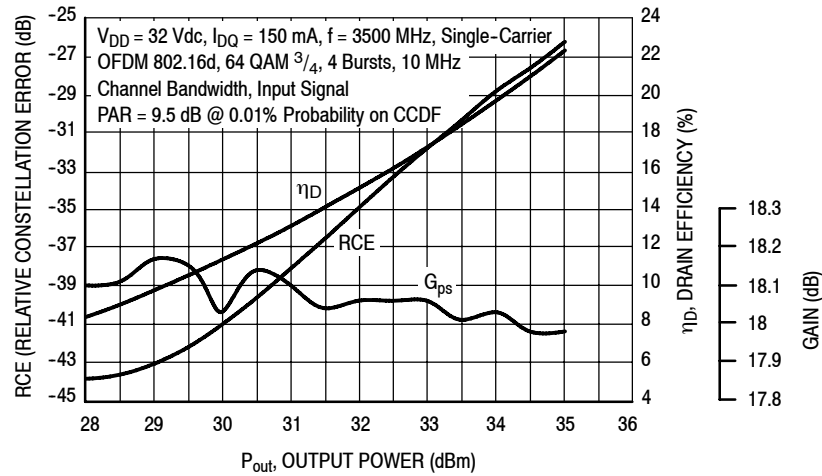
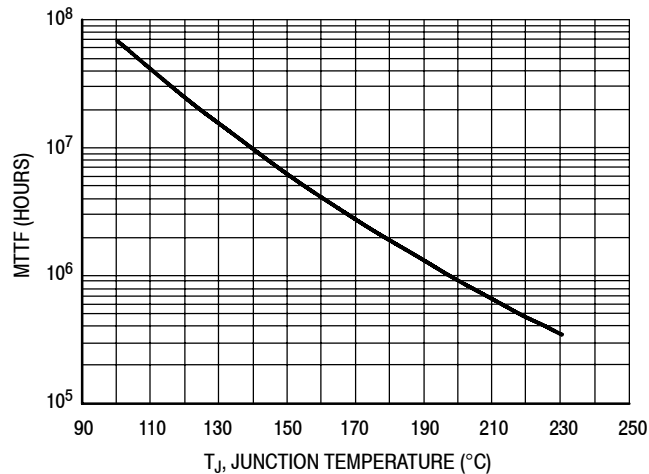


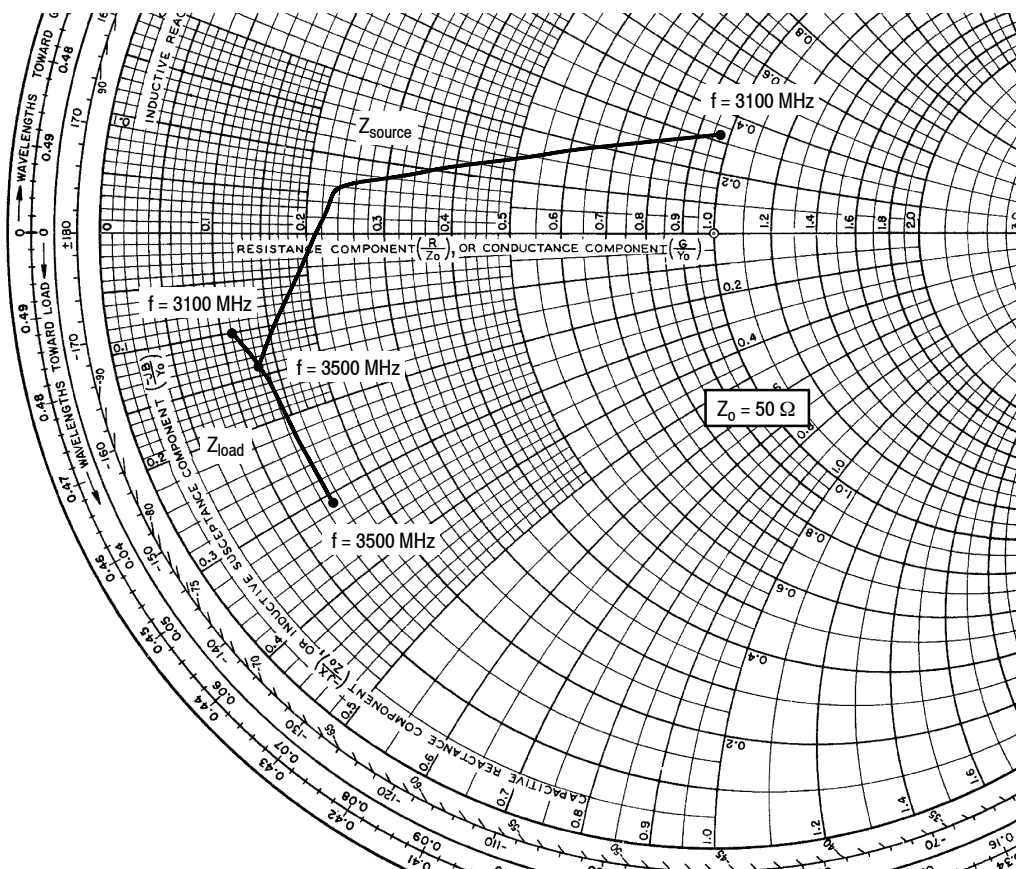
Figure 14. Single-Channel OFDM Relative Constellation Error, Drain Efficiency and Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 32$ Vdc, $P_{out} = 15$ W Peak, Pulse Width = 100 μ sec, Duty Cycle = 20%, and $\eta_D = 41\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 15. MTTF versus Junction Temperature



$V_{DD} = 32 \text{ Vdc}$, $I_{DQ} = 50 \text{ mA}$, $P_{out} = 15 \text{ W Peak}$

f MHz	Z_{source} Ω	Z_{load} Ω
3100	$48.6 + j16.1$	$5.6 - j5.2$
3300	$11.8 + j3.15$	$6.36 - j6.83$
3500	$6.43 - j6.79$	$7.41 - j15.5$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

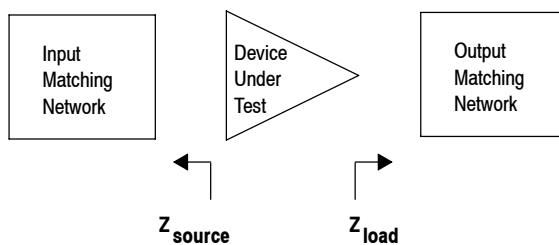
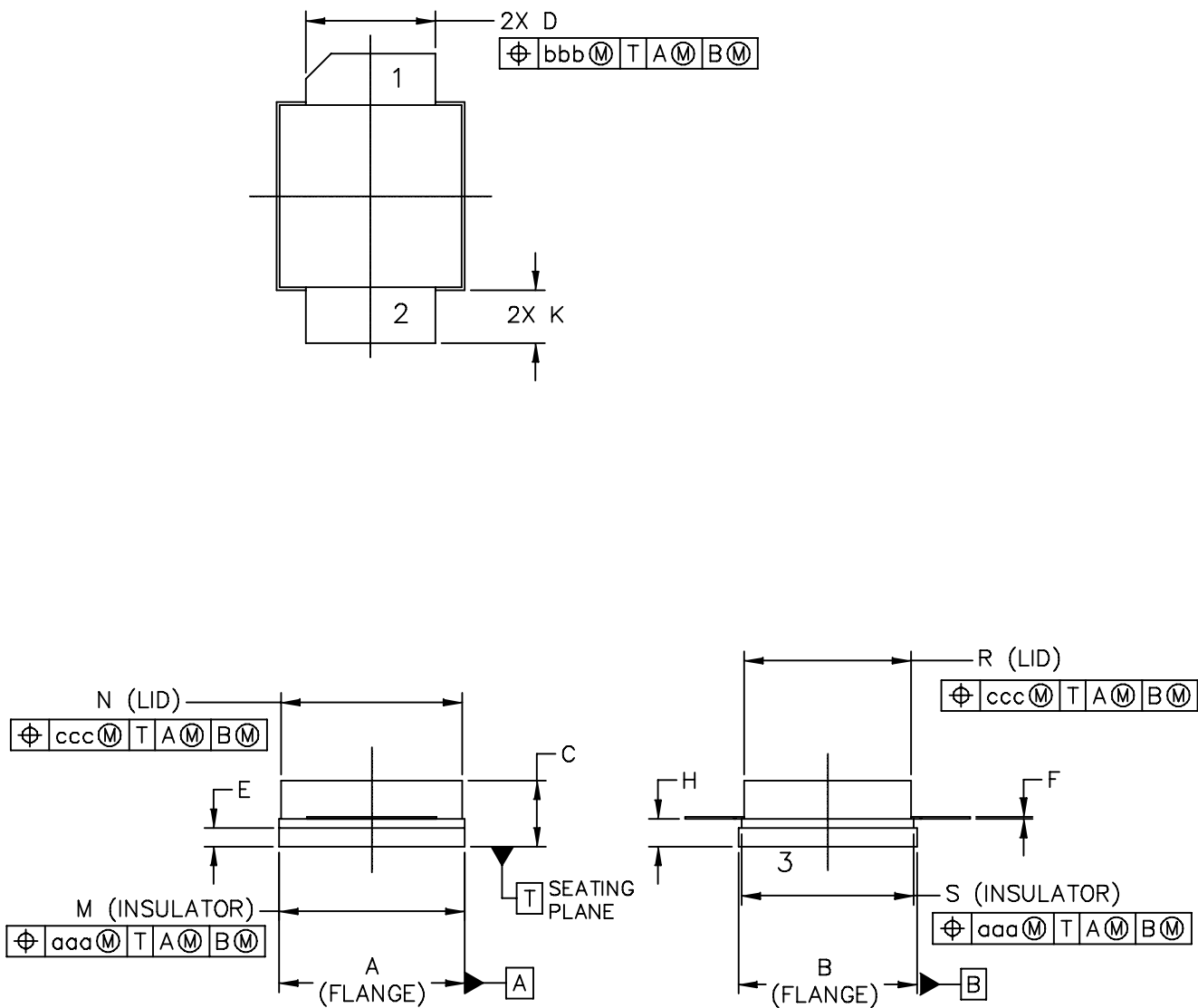


Figure 16. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI-400S-240		DOCUMENT NO: 98ASA10732D	REV: A
		CASE NUMBER: 465J-02	09 MAY 2006
		STANDARD: NON-JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY

STYLE 1:

- PIN 1 - DRAIN
- 2 - GATE
- 3 - SOURCE

STYLE 2:

- PIN 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29	aaa	.005		0.127	
B	.380	.390	9.65	9.91	bbb	.010		0.254	
C	.125	.163	3.18	4.14	ccc	.015		0.381	
D	.275	.285	6.98	7.24					
E	.035	.045	0.89	1.14					
F	.004	.006	0.10	0.15					
H	.057	.067	1.45	1.70					
K	.0995	.1295	2.53	3.29					
M	.395	.405	10.03	10.29					
N	.385	.395	9.78	10.03					
R	.355	.365	9.02	9.27					
S	.365	.375	9.27	9.53					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: NI-400S-240					DOCUMENT NO: 98ASA10732D			REV: A	
					CASE NUMBER: 465J-02			09 MAY 2006	
					STANDARD: NON-JEDEC				

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	June 2008	• Initial Release of Data Sheet
1	Aug. 2008	• Added p. 1 of Case 465J-02 Mechanical Outline drawing, p. 9
2	Apr. 2011	• Fig. 1, Test Circuit Schematic, Z-list, changed Z7 from 0.084" x 0.73" Microstrip to 0.322" x 0.073" Microstrip and moved footnote reference from Z2 and Z3 to Z15 and Z17, p. 3

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2008, 2011. All rights reserved.