LMH7322 Dual 700 ps High Speed Comparator with RSPECL Outputs

Check for Samples: LMH7322

FEATURES

- **(V_{CCI} = +5V, V_{CCO} = +5V)**
- **Propagation Delay 700 ps**
- **Overdrive Dispersion 20 mV-1V 75 ps**
- **Fast Rise and Fall Times 160 ps**
- **Wide Supply Range 2.7V to 12V**
- **Input Common Mode Range Extends 200 mV Below Negative Rail**
- **Adjustable Hysteresis**
- **(RS)PECL Outputs (see Application Information)**
- **(RS)PECL Latch Inputs (see Application Information)**

APPLICATIONS

- **Digital Receivers**
- **High-Speed Signal Restoration**
- **Zero-Crossing Detectors**
- **High-Speed Sampling**
- **Window Comparators**
- **High-Speed Signal Triggering**

DESCRIPTION

The LMH7322 is a dual comparator with 700 ps propagation delay, low dispersion of 75 ps and an input voltage range that extends from V_{CC}-1.5V to V_{EE}. The devices can be operated from a wide supply voltage range of 2.7V to 12V. The adjustable hysteresis adds flexibility and prevents oscillations. Both the outputs and latch inputs of the LMH7322 are RSPECL compatible. When used in combination with a V_{CCO} supply voltage of 2.5V the outputs have LVDS compatible levels.

The LMH7322 is available in a 24-pin WQFN package.

Typical Application

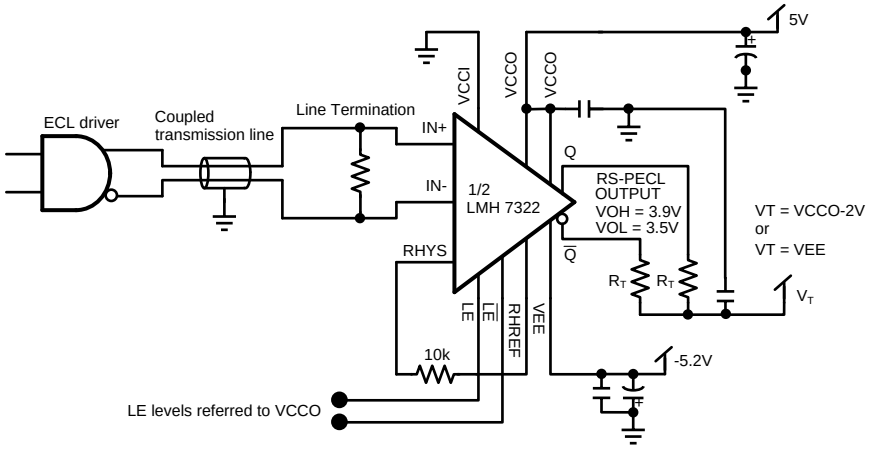


Figure 1. (RS)ECL to RSPECL Converter

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	2.5 kV
Machine Model	250V
Output Short Circuit Duration	See (4)(5)(6)
Supply Voltages (V_{CCx}–V_{EE})	13.2V
Differential Voltage at Input Pins	±13V
Voltage at Input Pins	V_{EE}-0.2V to V_{CCI} + 0.2V
Voltage at LE Pins	V_{EE}-0.2V to V_{CCO}+0.2V
Current at Output Pins	25mA
Soldering Information:	
See Product Folder at www.ti.com and SNOA549	
Storage Temperature Range	−65°C to +150°C
Junction Temperature (7)	+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) Short circuit test is a momentary test. See next note.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(7) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Operating Conditions (1)

Supply Voltage (V_{CCx}–V_{EE})	2.7V to 12V
Operating Temperature Range (2)(3)	−40°C to +125°C
Package Thermal Resistance (2)(3)	
24-Pin WQFN	38°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(3) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information on temperature de-rating of this device.

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12V DC Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CCI} = V_{CCO} = 12V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV, R_{HYS} = 1 kΩ. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
INPUT CHARACTERISTICS						
I_B	Input Bias Current	V_{IN} Differential = 0V; R_{HYS} = 8 kΩ Biased at V_{CM}	−5	−2.9		µA
I_{OS}	Input Offset Current	V_{IN} Differential = 0V	−250	40	+250	nA
TC I_{OS}	Input Offset Current TC	V_{IN} Differential = 0V		0.2		nA/°C
V_{OS}	Input Offset Voltage		−8	−2	+8	mV
TC V_{OS}	Input Offset Voltage TC			12		µV/°C
V_{RI}	Input Voltage Range	for CMRR ≥ 50 dB	V_{EE}−0.2		V_{CCI}−1.5	V
V_{RID}	Input Differential Voltage Range		−1		+1	V
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ V_{CC1}−0.2		80		dB
PSRR	Power Supply Rejection Ratio			80		dB
A_V	Active Gain			53		dB
Hyst	Hysteresis	V_{HYS} = $V_{(HYS^+)}$ -$V_{(HYS^-)}$, R_{HYS} = 0Ω	25	50	75	mV
LATCH ENABLE CHARACTERISTICS						
$I_{B\text{-}LE}$	Latch Enable Bias Current	Biased at RSPECL Level		3	10	µA
$V_{OS\text{-}LE}$	Latch Enable Offset Voltage	Biased at RSPECL Level		−5		mV
$V_{RI\text{-}LE}$	Latch Enable Voltage Range	for CMRR ≥ 50 dB	V_{EE}+1.4		V_{CCO}-0.8	V
$V_{RID\text{-}LE}$	Latch Enable Differential Voltage Range			±0.4		V
OUTPUT CHARACTERISTICS						
V_{OH}	Output Voltage High	V_{IN} Differential = 50 mV		V_{CCO}−1.1 V		mV
V_{OL}	Output Voltage Low	V_{IN} Differential = 50 mV		V_{CCO}−1.5 V		mV
V_{OD}	Output Voltage Differential	V_{IN} Differential = 50 mV		360		mV
POWER SUPPLIES						
I_{VCCI}	V_{CCI} Supply Current/ Channel			6.5	10 **12**	mA
I_{VCCO}	V_{CCO} Supply Current/ Channel	Load Current Excluded		16.3	20 **25**	mA

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

12 AC Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CCI} = V_{CCO} = 12V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV, R_{HYS} = none.**Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
TR	Maximum Toggle Rate	Overdrive = ±50 mV; C_L = 2 pF @ 50% of Output Swing		4		Gb/s
	Minimum Pulse Width	Overdrive = ±50 mV; C_L = 2 pF @ 50% of Output Swing		255		ps

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12 AC Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CCI} = V_{CCO} = 12V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV, R_{HYS} = none.**Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
$t_{jitter\text{-}RMS}$	RMS Random Jitter	Overdrive = ±100 mV; C_L = 2 pF Center Frequency = 140 MHz Bandwidth = 10 Hz–20 MHz		702		fs
t_{PDH}	Propagation Delay. (see Figure 19 application note)	Overdrive 20 mV		818		ps
		Overdrive 50 mV		723		
	Input SR = Constant V_{IN} Startvalue = V_{REF} −100 mV	Overdrive 100 mV		708		ps
		Overdrive 1V		703		
$t_{OD\text{-}disp}$	Input Overdrive Dispersion	t_{PDH} @ Overdrive 20 mV ↔ 100 mV		110		ps
		t_{PDH} @ Overdrive 100 mV ↔ 1V		5		
$t_{SR\text{-}disp}$	Input Slew Rate Dispersion	0.1 V/ns to 1 V/ns; Overdrive = 100 mV		48		ps
$t_{CM\text{-}disp}$	Input Common Mode Dispersion	SR = 1 V/ns; Overdrive = 100 mV; 0V ≤ V_{CM} ≤ V_{CCI}- 1.5V		43		ps
Δt_{PDLH}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDH} - t_{PD\overline{L}}\rvert$	Overdrive = 100 mV; C_L = 2 pF		24		ps
Δt_{PDHL}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDL} - t_{PD\overline{H}}\rvert$	Overdrive = 100 mV; C_L = 2 pF		45		ps
t_r	Output Rise Time (20%–80%)	Overdrive = 100 mV; C_L = 2 pF		155		ps
t_f	Output Fall Time (20%–80%)	Overdrive = 100 mV; C_L = 2 pF		155		ps
t_{sLE}	Latch Setup Time			77		ps
t_{hLE}	Latch Hold Time			33		ps
t_{PD_LE}	Latch to Output Delay Time			944		ps

5V DC Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CCI} = V_{CCO} = 5V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV, R_{HYS} = 1 kΩ.**Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
INPUT CHARACTERISTICS						
I_B	Input Bias Current	V_{IN} Differential = 0V; R_{HYS} = 8 kΩ Biased at V_{CM}	−5	−2.6		µA
I_{OS}	Input Offset Current	V_{IN} Differential = 0V	−250	40	+250	nA
TC I_{OS}	Input Offset Current TC	V_{IN} Differential = 0V		0.3		nA/°C
V_{OS}	Input Offset Voltage		−8	−2	+8	mV
TC V_{OS}	Input Offset Voltage TC			12		µV/°C
V_{RI}	Input Voltage Range	for CMRR ≥ 50 dB	V_{EE}−0.2		V_{CCI}−1.5	V
V_{RID}	Input Differential Voltage Range		−1		+1	V
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ V_{CC1}−0.2		80		dB
PSRR	Power Supply Rejection Ratio			80		dB
A_V	Active Gain			53		dB
Hyst	Hysteresis	V_{HYS} = $V_{(HYS^+)}$ -$V_{(HYS^-)}$, R_{HYS} = 0Ω	25	50	75	mV
LATCH ENABLE CHARACTERISTICS						
$I_{B\text{-}LE}$	Latch Enable Bias Current	Biased at RSPECL Level		3	10	µA
$V_{OS\text{-}LE}$	Latch Enable Offset Voltage	Biased at RSPECL Level		+5		mV
$V_{RI\text{-}LE}$	Latch Enable Voltage Range	for CMRR ≥ 50 dB	V_{EE}+1.4		V_{CCO}-0.8	V

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5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CCI} = V_{CCO} = 5V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV, R_{HYS} = 1 kΩ.**Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{RID-LE}	Latch Enable Differential Voltage Range			±0.4		V
OUTPUT CHARACTERISTICS						
V_{OH}	Output Voltage High			V_{CCO}−1.1 V		mV
V_{OL}	Output Voltage Low			V_{CCO}−1.5 V		mV
V_{OD}	Output Voltage Differential			355		mV
POWER SUPPLIES						
I_{VCCI}	V_{CCI} Supply Current/ Channel			6.3	10 **12**	mA
I_{VCCO}	V_{CCO} Supply Current/ Channel	Load Current Excluded		15.8	20 **25**	mA

5V AC Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CCI} = V_{CCO} = 5V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV, R_{HYS} = none. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
TR	Maximum Toggle Rate	Overdrive = ±50 mV; C_L = 2 pF @ 50% of Output Swing		3.9		Gb/s
	Minimum Pulse Width	Overdrive = ±50 mV; C_L = 2 pF @ 50% of Output Swing		260		ps
t_{jitter_RMS}	RMS Random Jitter	Overdrive = ±100 mV; C_L = 2 pF Center Frequency = 140 MHz Bandwidth = 10 Hz–20 MHz		572		fs
t_{PDLH}	Propagation Delay. (see Figure 19 application note)	Overdrive 20 mV		783		ps
		Overdrive 50 mV		718		
	Input SR = Constant V_{IN} startvalue = V_{REF} – 100 mV	Overdrive 100 mV		708		ps
		Overdrive 1V		708		
$t_{OD-disp}$	Input Overdrive Dispersion	t_{PDH} @ Overdrive 20 mV ↔ 100 mV		75		ps
		t_{PDH} @ Overdrive 100 mV ↔ 1V		5		
$t_{SR-disp}$	Input Slew Rate Dispersion	0.1 V/ns to 1 V/ns; Overdrive = 100 mV		50		ps
$t_{CM-disp}$	Input Common Mode Dispersion	SR = 1 V/ns; Overdrive = 100 mV; 0V ≤ V_{CM} ≤ V_{CCI}- 1.5V		24		ps
Δt_{PDLH}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDH} - t_{PD\overline{L}}\rvert$	Overdrive = 100 mV; C_L = 2 pF		29		ps
Δt_{PDHL}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDL} - t_{PD\overline{H}}\rvert$	Overdrive = 100 mV; C_L = 2 pF		47		ps
t_r	Output Rise Time (20%–80%)	Overdrive = 100 mV; C_L = 2 pF		160		ps
t_f	Output Fall Time (20%–80%)	Overdrive = 100 mV; C_L = 2 pF		160		ps
t_{sLE}	Latch Setup Time			95		ps
t_{hLE}	Latch Hold Time			29		ps
t_{PD_LE}	Latch to Output Delay Time			893		ps

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2.7V DC Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CCI} = V_{CCO} = 2.7V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV, R_{HYS} = 1 kΩ. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
INPUT CHARACTERISTICS						
I_B	Input Bias Current	V_{IN} Differential = 0V; R_{HYS} = 8 kΩ Biased at V_{CM}	−5	−2.5		µA
I_{OS}	Input Offset Current	V_{IN} Differential = 0V	−250	40	+250	nA
TC I_{OS}	Input Offset Current TC	V_{IN} Differential = 0V		0.2		nA/°C
V_{OS}	Input Offset Voltage		−8	−2	+8	mV
TC V_{OS}	Input Offset Voltage TC			12		µV/°C
V_{RI}	Input Voltage Range	for CMRR ≥ 50 dB	V_{EE}−0.2		V_{CCI}−1.5	V
V_{RID}	Input Differential Voltage Range		−1		+1	V
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ V_{CC1}−2		80		dB
PSRR	Power Supply Rejection Ratio			80		dB
A_V	Active Gain			53		dB
Hyst	Hysteresis	V_{HYS} = $V_{(HYS^+)}$ -$V_{(HYS^-)}$, R_{HYS} = 0Ω	25	50	75	mV
LATCH ENABLE CHARACTERISTICS						
$I_{B\text{-}LE}$	Latch Enable Bias Current	Biased at RSPECL Level		3	10	µA
$V_{OS\text{-}LE}$	Latch Enable Offset Voltage	Biased at RSPECL Level		−5		mV
$V_{RI\text{-}LE}$	Latch Enable Voltage Range	for CMRR ≥ 50 dB	V_{EE}+1.4		V_{CCO}-0.8	V
$V_{RID\text{-}LE}$	Latch Enable Differential Voltage Range			±0.4		V
OUTPUT CHARACTERISTICS						
V_{OH}	Output Voltage High			V_{CCO}−1.1 V		mV
V_{OL}	Output Voltage Low			V_{CCO}−1.5 V		mV
V_{OD}	Output Voltage Differential			350		mV
POWER SUPPLIES						
I_{VCCI}	V_{CCI} Supply Current/ Channel			6.2	10 **12**	mA
I_{VCCO}	V_{CCO} Supply Current/ Channel	Load Current Excluded		15.5	20 **25**	mA

(1) All limits are specified by testing or statistical analysis.
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2.7V AC Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CCI} = V_{CCO} = 2.7V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV, R_{HYS} = none. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
TR	Maximum Toggle Rate	Overdrive = ±50 mV; C_L = 2 pF @ 50% of Output Swing		3.8		Gb/s
	Minimum Pulse Width	Overdrive = ±50 mV; C_L = 2 pF @ 50% of Output Swing		265		ps

(1) All limits are specified by testing or statistical analysis.
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2.7V AC Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CCI} = V_{CCO} = 2.7V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV, R_{HYS} = none. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
t_{jitter_RMS}	RMS Random Jitter	Overdrive = ±50 mV; C_L = 2 pF Center Frequency = 140 MHz Bandwidth = 10 Hz–20 MHz		551		fs
t_{PDH}	Propagation Delay. (see Figure 19 application note)	Overdrive 20 mV		783		ps
		Overdrive 50 mV		728		
	Input SR = Constant V_{IN} startvalue = V_{REF} – 100 mV	Overdrive 100 mV		713		ps
		Overdrive 1V		718		
$t_{OD\text{-}disp}$	Input Overdrive Dispersion	t_{PDH} @ Overdrive 20 mV ↔ 100 mV		70		ps
		t_{PDH} @ Overdrive 100 mV ↔ 1V		5		
$t_{SR\text{-}disp}$	Input Slew Rate Dispersion	0.1 V/ns to 1 V/ns; Overdrive = 100 mV		54		ps
$t_{CM\text{-}disp}$	Input Common Mode Dispersion	SR = 1 V/ns; Overdrive = 100 mV; 0V ≤ V_{CM} ≤ V_{CCI}- 1.5V		12		ps
Δt_{PDLH}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDH} - t_{PD\overline{L}}\rvert$	Overdrive = 100 mV; C_L = 2 pF		35		ps
Δt_{PDHL}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDL} - t_{PD\overline{H}}\rvert$	Overdrive = 100 mV; C_L = 2 pF		53		ps
t_r	Output Rise Time (20%–80%)	Overdrive = 100 mV; C_L = 2 pF		165		ps
t_f	Output Fall Time (20%–80%)	Overdrive = 100 mV; C_L = 2 pF		165		ps
t_{sLE}	Latch Setup Time			102		ps
t_{hLE}	Latch Hold Time			37		ps
t_{PD_LE}	Latch to Output Delay Time			906		ps

Connection Diagrams

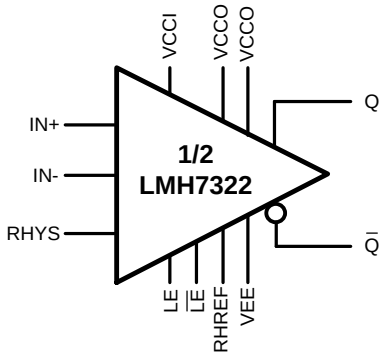


Figure 2. Schematic

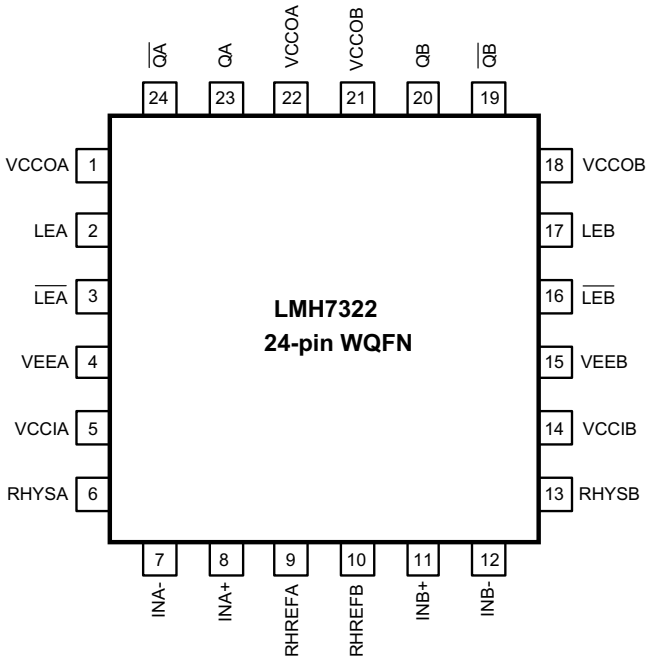


Figure 3. Footprint

Typical Performance Characteristics

At T_J = 25°C; V_{CCI} = +5V; V_{CCO} = +3.3V; V_{EE} = −5V; unless otherwise specified.

Propagation Delay vs. Supply Voltage

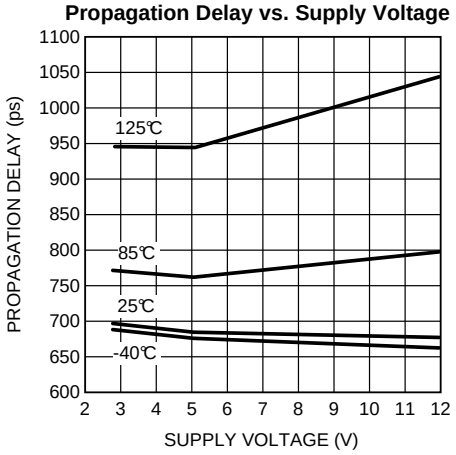


Figure 4.

Propagation Delay vs. Temperature

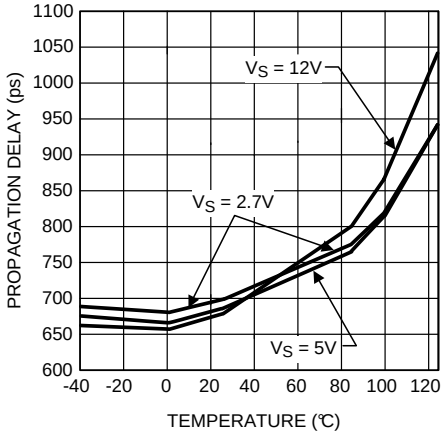


Figure .

Propagation Delay vs. Supply Voltage

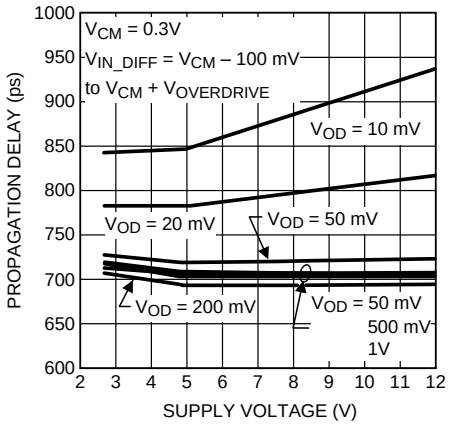


Figure 5.

Propagation Delay vs. Overdrive Voltage

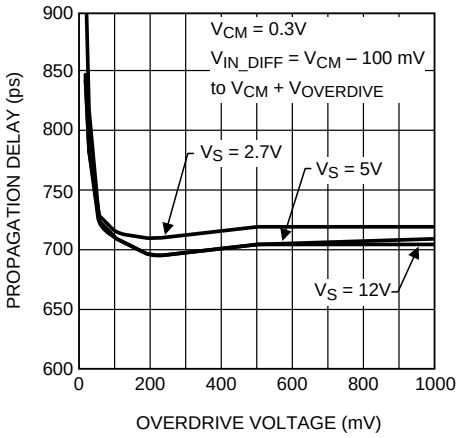


Figure 6.

Propagation Delay vs. Common Mode Voltage

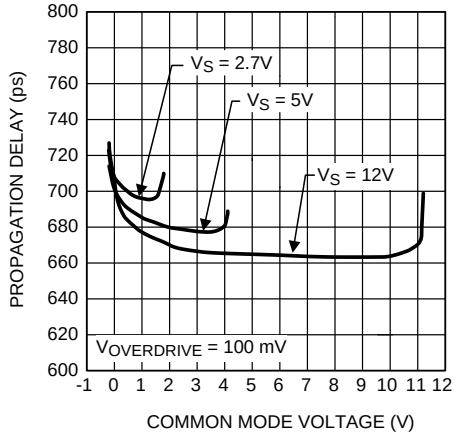


Figure 7.

Propagation Delay vs. Slew Rate

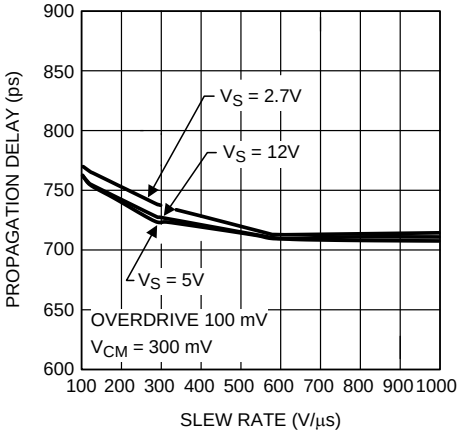


Figure 8.

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Typical Performance Characteristics (continued)

At T_J = 25°C; V_{CCI} = +5V; V_{CCO} = +3.3V; V_{EE} = −5V; unless otherwise specified.

T_{PD} Dispersion vs. Supply Voltage

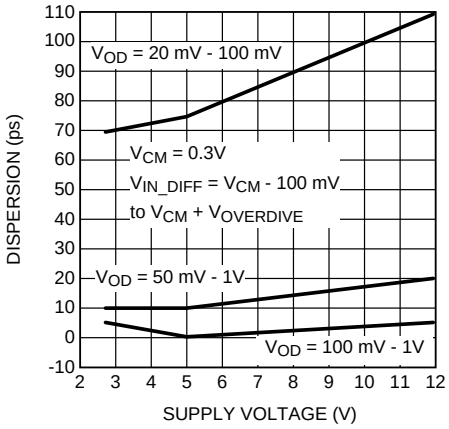


Figure 9.

Slew Rate Dispersion vs. Voltage Supply

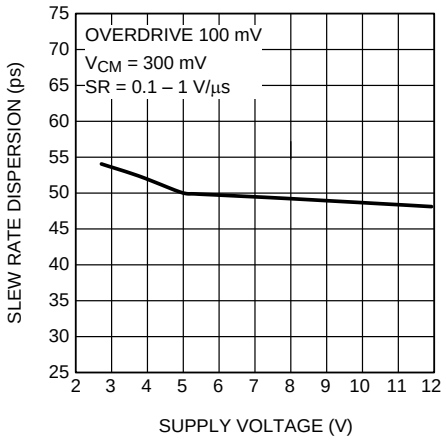


Figure 10.

Common Mode Dispersion vs. Supply Voltage

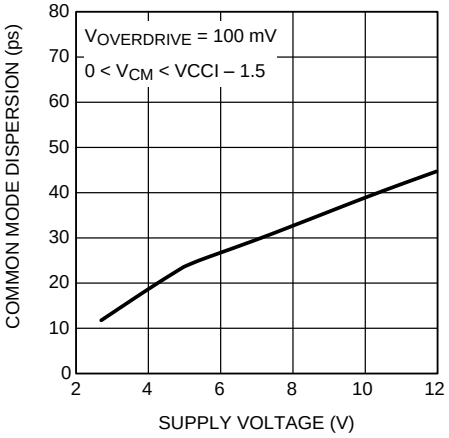


Figure 11.

Bias Current vs. Temperature

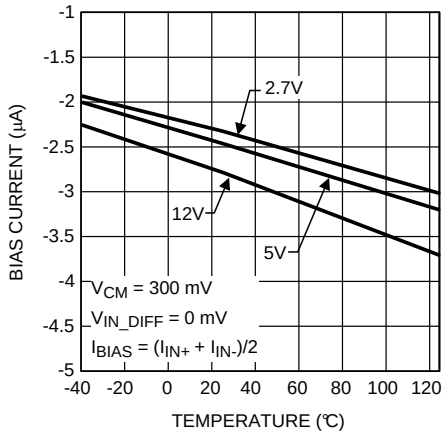


Figure 12.

Input Current vs. Differential Input Voltage

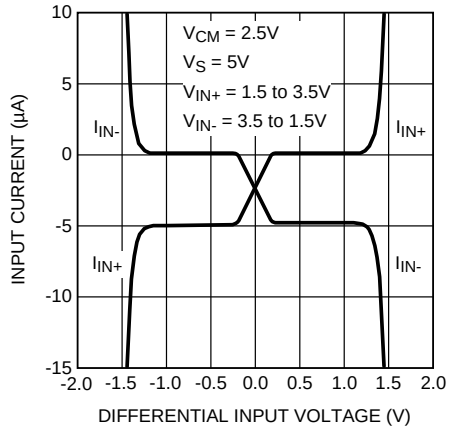


Figure 13.

Maximum Toggle Rate

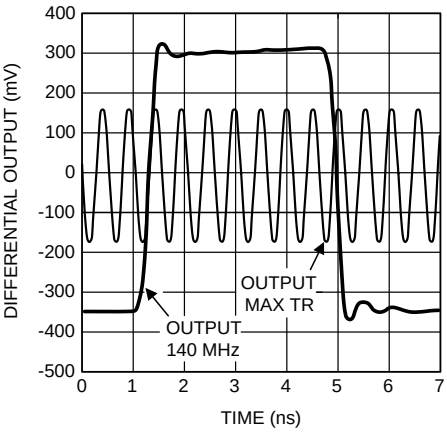


Figure 14.

Typical Performance Characteristics (continued)

At T_J = 25°C; V_{CCI} = +5V; V_{CCO} = +3.3V; V_{EE} = −5V; unless otherwise specified.

Output Voltage vs. Input Voltage

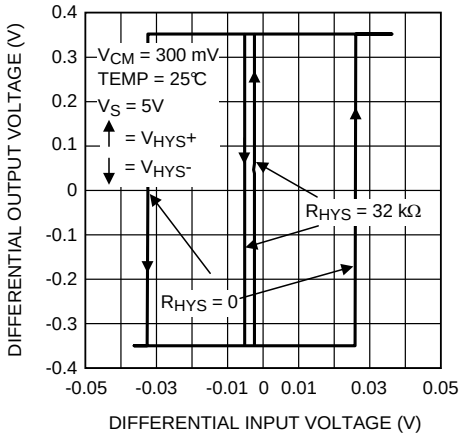


Figure 15.

Hysteresis Voltage vs. Hysteresis Resistor

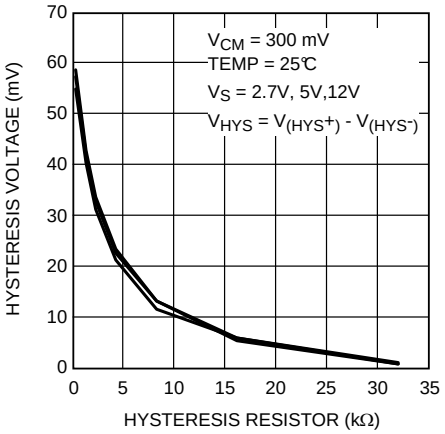


Figure 16.

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APPLICATION INFORMATION

Introduction

The LMH7322 is a high speed comparator with RS(P)ECL (**R**educed **S**wing **P**ositive **E**mitter Coupled Logic) outputs, and is compatible with LVDS (**L**ow **V**oltage **D**ifferential **S**ignaling) if V_{CCO} is set to 2.5V. The use of complementary outputs gives a high level of suppression for common mode noise. The very fast rise and fall times of the LMH7322 enable data transmission rates up to several Gigabits per second (Gbps). The LMH7322 inputs have a common mode voltage range that extends 200 mV below the negative supply voltage thus allowing ground sensing in case of single supply. The rise and fall times of the LMH7322 are about 160 ps, while the propagation delay time is about 700 ps. The LMH7322 can operate over the full supply voltage range of 2.7V to 12V, while using single or dual supply voltages. This is a very useful feature because it provides a flexible way to interface between several high speed logic families. Several setups are shown in the application information section "Interface Between Logic Families". The outputs are referenced to the positive V_{CCO} supply rail. The supply current is 23 mA at 5V (per comparator, load current excluded.) The LMH7322 is available in a 24-Pin WQFN package.

The following topics will be discussed in this application section.

- Input and output topology
- Specification definitions
- Propagation delay and dispersion
- Hysteresis and oscillations
- Output
- Applying transmission lines
- PCB layout

Input & Output Topology

All input and output pins are protected against excessive voltages by ESD diodes. These diodes are conducting from the negative supply to the positive supply. As can be seen in Figure 17, both inputs are connected to these diodes. Further protection of the inputs is provided by the two resistors of 250Ω, in conjunction with the string of anti-parallel diodes connected between both bases of the input stage. This combination of resistors and diodes reduces excessive input voltages over the input stage, but is low enough to maintain switching speed to the output signal.

Protection against excessive supply voltages is provided by a power clamp between V_{CC} and GND.

When using this part be aware of situations in which the differential input voltage level is such that these diodes are conducting. In this case the input current is raised far above the normal value stated in the datasheet tables because input current is flowing through the bypass diode string between both inputs.

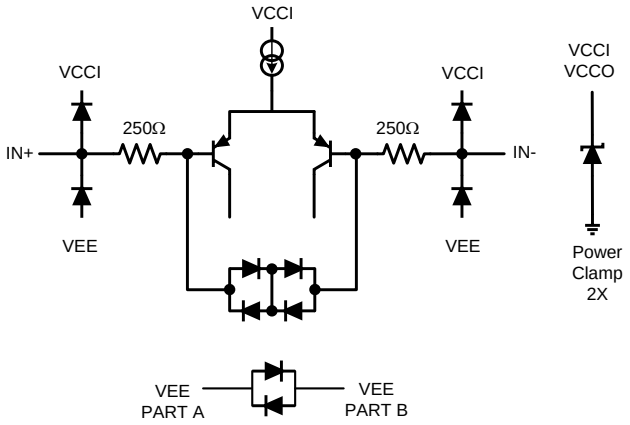


Figure 17. Equivalent Input Circuitry

The output stage of the LMH7322 is built using two emitter followers, which are referenced to the V_{CCO} (see Figure 18.) Each of the output transistors is active when a current is flowing through any external output resistor connected to a lower supply rail. The output structure is actually the same as for all other ECL devices. Activating the outputs is done by connecting the emitters to a termination voltage which lies 2V below the V_{CCO}. In this case a termination resistor of 50Ω can be used and a transmission line of 50Ω can be driven. Another method is to connect the emitters through a resistor to the most negative supply by calculating the right value for the emitter current in accordance with the datasheet tables. Both methods are useful, and it is up to the customer which method is used. Using 50Ω to the termination voltage means the introduction of an extra supply in the system, while using resistors to a negative supply means the use of resistors that are much larger than 50Ω and a more constant output current per stage. The following calculation will show the difference. In this example a V_{CCO} of 2.5V is used and a V_T of V_{CCO}-2V and a negative supply of −5V. When connecting the outputs through a 50Ω resistor to the V_T, the output currents for the high and the low state are respectively 18 mA and 10 mA. Connecting the outputs through a 400Ω resistor to the −5V supply the output currents for the high and the low state are respectively 16 mA and 15 mA. Higher resistor values to the V_{EE} will further reduce power consumption but will cause a slower transition of the output stage. In the case that this will not harm your application it is a useful method to reduce power consumption.

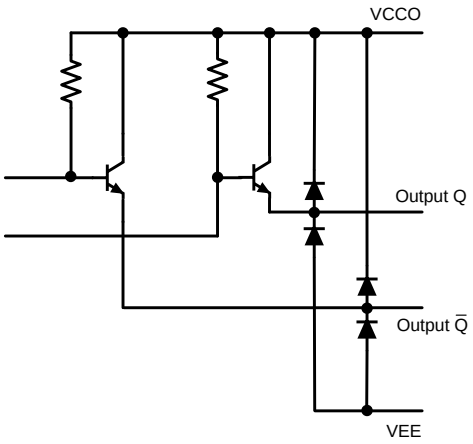


Figure 18. Equivalent Output Circuitry

The output voltages for '1' and '0' have a difference of approximately 400 mV and are respectively 1.1V (for the '1') and 1.5V (for the '0') below the V_{CCO}. This swing of 400 mV is enough to drive any LVDS input but can also be used to drive any ECL or PECL input, when the right supply voltage is chosen, especially the right level for the V_{CCO}.

Table 1. Definitions

Symbol	Text	Description
I_B	Input Bias Current	Current flowing in or out of the input pins, when both are biased at the V_{CM} voltage as specified in the tables.
I_{OS}	Input Offset Current	Difference between the input bias current of the inverting and non-inverting inputs.
TC I_{OS}	Average Input Offset Current Drift	Temperature coefficient of I_{OS}.
V_{OS}	Input Offset Voltage	Voltage difference needed between IN+ and IN- to make the outputs change state, averaged for H to L and L to H transitions.
TC V_{OS}	Average Input Offset Voltage Drift	Temperature coefficient of V_{OS} .
V_{RI}	Input Voltage Range	Voltage which can be applied to the input pin maintaining normal operation.
V_{RID}	Input Differential Voltage Range	Differential voltage between positive and negative input at which the input clamp is not working. The difference can be as high as the supply voltage but excessive input currents are flowing through the clamp diodes and protection resistors.
CMRR	Common Mode Rejection Ratio	Ratio of input offset voltage change and input common mode voltage change.
PSRR	Power Supply Rejection Ratio	Ratio of input offset voltage change and supply voltage change from $V_{S\text{-}MIN}$ to $V_{S\text{-}MAX}$.
A_V	Active Gain	Overall gain of the circuit.

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Table 1. Definitions (continued)

Symbol	Text	Description
Hyst	Hysteresis	Difference between the switching point '0' to '1' and vice versa.
I_{B-LE}	Latch Enable Bias Current	Current flowing in or out of the input pins, when both are biased at normal PECL levels.
I_{OS-LE}	Latch Enable Offset Current	Difference between the input bias current of the LE and $\overline{LE}$ pin.
TC I_{OS-LE}	Temp Coefficient Latch Enable Offset Current	Temperature coefficient of I_{OS-LE}.
V_{OS-LE}	Latch Enable Offset Voltage	Voltage difference needed between LE and $\overline{LE}$ to place the part in the latched or the transparent state.
TC V_{OS-LE}	Temp Coefficient Latch Enable Offset Voltage	Temperature coefficient of V_{OS-LE}.
V_{RI-LE}	Latch Enable Voltage Range	Voltage which can be applied to the LE input pins without damaging the device.
V_{RID-LE}	Latch Enable Differential Voltage Range	Differential Voltage between LE and $\overline{LE}$ at which the clamp isn't working. The difference can be as high as the supply voltage but excessive input currents are flowing through the clamp diodes and protection resistors.
V_{OH}	Output Voltage High	High state single ended output voltage ($\overline{Q}$ or Q) (see Figure 34).
V_{OL}	Output Voltage Low	Low state single ended output voltage ($\overline{Q}$ or Q) (see Figure 34).
V_{OD}	average of V_{ODH} and V_{ODL}	$(V_{ODH} + V_{ODL})/2$.
I_{VCCI}	Supply Current Input Stage	Supply current into the input stage.
I_{VCCO}	Supply Current Output Stage	Supply current into the output stage while current through the load resistors is excluded.
I_{VEE}	Supply Current V_{EE} pin	Current flowing to the negative supply pin.
TR	Maximum Toggle Rate	Maximum frequency at which the outputs can toggle between the nominal V_{OH} and V_{OL}.
PW	Pulse Width	Time from 50% of the rising edge of a signal to 50% of the falling edge.
t_{PDH} resp t_{PDL}	Propagation Delay	Delay time between the moment the input signal crosses the switching level L to H and the moment the output signal crosses 50% of the rising edge of Q output (t_{PDH}), or delay time between the moment the input signal crosses the switching level H to L and the moment the output signal crosses 50% of the falling edge of Q output (t_{PDL}).
$t_{PD\overline{L}}$ resp $t_{PD\overline{H}}$		Delay time between the moment the input signal crosses the switching level L to H and the moment the output signal crosses 50% of the falling edge of $\overline{Q}$ output ($t_{PD\overline{L}}$), or delay time between the moment the input signal crosses the switching level H to L and the moment the output signal crosses 50% of the rising edge of $\overline{Q}$ output ($t_{PD\overline{H}}$).
t_{PDLH}		Average of t_{PDH} and $t_{PD\overline{L}}$.
t_{PDHL}		Average of t_{PDL} and $t_{PD\overline{H}}$.
t_{PD}		Average of t_{PDLH} and t_{PDHL}.
t_{PDHd} resp t_{PDLd}		Delay time between the moment the input signal crosses the switching level L to H and the zero crossing of the rising edge of the differential output signal (t_{PDHd}), or delay time between the moment the input signal crosses the switching level H to L and the zero crossing of the falling edge of the differential output signal (t_{PDLd}).
$t_{OD-disp}$	Input Overdrive Dispersion	Change in t_{PD} for different overdrive voltages at the input pins.
$t_{SR-disp}$	Input Slew Rate Dispersion	Change in t_{PD} for different slew rates at the input pins.
$t_{CM-disp}$	Input Common Mode Dispersion	Change in t_{PD} for different common mode voltages at the input pins.
Δt_{PDLH} resp Δt_{PDHL}	Q to $\overline{Q}$ Time Skew	Time skew between 50% levels of the rising edge of $\overline{Q}$ output and the falling edge of output (Δt_{PDLH}), or time skew between 50% levels of falling edge of Q output and rising edge of $\overline{Q}$ output (Δt_{PDHL}).
Δt_{PD}	Average Q to $\overline{Q}$ Time Skew	Average of t_{PDLH} and t_{PDHL} for L to H and H to L transients.
ΔtP_{Dd}	Average Diff. Time Skew	Average of t_{PDHd} and t_{PDLd} for L to H and H to L transients.
t_r / t_{rd}	Output Rise Time (20% - 80%)	Time needed for the (single ended or differential) output voltage to change from 20% of its nominal value to 80%.
t_f / t_{fd}	Output Fall Time (20% - 80%)	Time needed for the (single ended or differential) output voltage to change from 80% of its nominal value to 20%.
t_sLE	Latch Setup Time	Time the input signal has to be stable before enabling the latch functionality.

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Table 1. Definitions (continued)

Symbol	Text	Description
t_hLE	Latch Hold Time	Time the input signal has to remain stable after enabling the latch functionality.
t_{PD-LE}	Latch to Output Delay Time	Delay time between the moment the latch input crosses the switching level H to L and the moment the differential output signal crosses the 50% level. Note: input signal is opposite to output signal when latch becomes enabled.

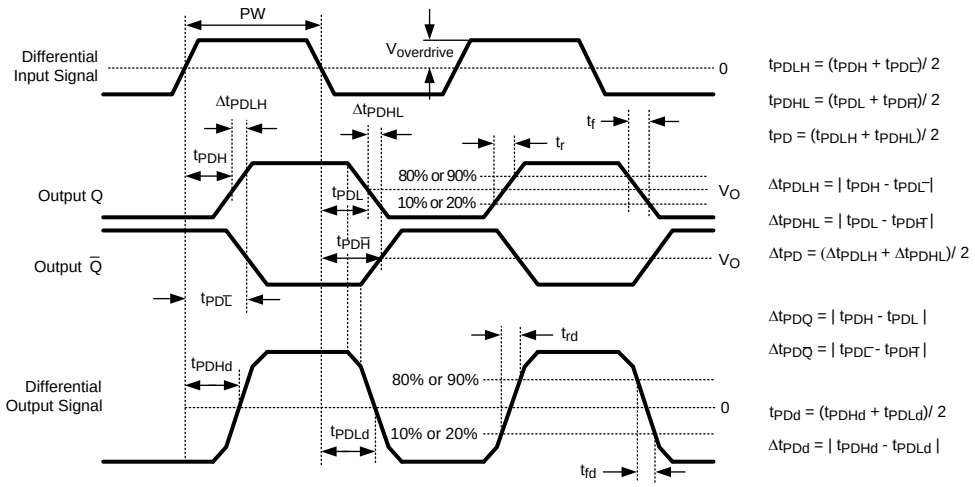


Figure 19. Timing Definitions

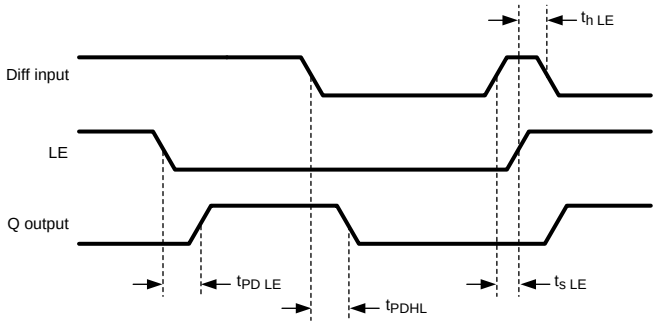


Figure 20. LE Timing

Table 2. PIN DESCRIPTIONS

Pin	Name	Description		Comment
1.	VCCOA	Positive Supply Output Stage	part A	The supply pin for the output stage is independent of the supply pin for the input pin. This allows output levels of different logic families.
2.	LEA	Latch Enable Input	part A	Logic '1' sets the part on hold. Logic levels are RSPECL (Reduced Swing PECL) compatible.
3.	$\overline{LEA}$	Latch Enable Input Not	part A	Logic '0' sets the part on hold. Logic levels are RSPECL compatible.
4.	VEEA	Negative Supply	part A	The supply pin for the negative supply is connected to the VEEB via a string of two anti-parallel diodes (see Figure 17)
5.	VCCIA	Positive Supply for Input Stage	part A	The supply pin for the input stage is independent of the supply for the output stage.
6.	RHYSA	Hysteresis Resistor	part A	The hysteresis voltage is determined by connecting a resistor from this pin to RHREFA.
7.	INA-	Negative Input	part A	Input for analog voltages between 200 mV below VEEA and 2V below VCCIA.

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Table 2. PIN DESCRIPTIONS (continued)

Pin	Name	Description		Comment
8.	INA+	Positive Input	part A	Input for analog voltages between 200 mV below VEEA and 2V below VCCIA.
9.	RHREFA	Reference Voltage Hysteresis Resistor	part A	The hysteresis voltage is determined by connecting a resistor from this pin to RHYSA.
10.	RHREFB	Reference Voltage Hysteresis Resistor	part B	The hysteresis voltage is determined by connecting a resistor from this pin to RHYSB.
11.	INB+	Positive Input	part B	Input for analog voltages between 200 mV below VEEB and 2V below VCCIB.
12.	INB−	Negative Input	part B	Input for analog voltages between 200 mV below VEEB and 2V below VCCIB.
13.	RHYSB	Hysteresis Resistor	part B	The hysteresis voltage is determined by connecting a resistor from this pin to RHREFB.
14.	VCCIB	Positive Supply for Input Stage	part B	The supply pin for the input stage is independent of the supply for the output stage.
15.	VEEB	Negative Supply	part B	The supply pin for the negative supply is connected to the VEEA via a string of two anti-parallel diodes (see Figure 17).
16.	$\overline{\text{LEB}}$	Latch Enable Input Not	part B	Logic '0' sets the part on hold. Logic levels are RSPECL compatible.
17.	LEB	Latch Enable Input Logic	part B	'1' sets the part on hold. Logic levels are RSPECL compatible.
18.	VCCOB	Positive Supply for Output Stage	part B	The supply pin for the output stage is independent of the supply pin for the input pin. This allows output levels of different logic families.
19.	$\overline{\text{QB}}$	Inverted Output	part B	Output levels are determined by the choice of VCCOB.
20.	QB	Output	part B	Output levels are determined by the choice of VCCOB.
21.	VCCOB	Positive Supply for Output Stage	part B	See other VCCOB
22.	VCCOA	Positive Supply for Output Stage	part A	See other VCCOA.
23.	QA	Output	part A	Output levels are determined by the choice of VCCOA.
24.	$\overline{\text{QA}}$	Inverted Output	part A	Output levels are determined by the choice of VCCOA.
25.	DAP	Central pad at the bottom of the package	A & B	This pad is connected to the VEE pins and its purpose is to transfer heat outside the part.

Tips & Tricks Using the LMH7322

In this section several aspects are discussed concerning special applications using the LMH7322.

This concerns the LE function, the connection of the DAP in conjunction to the V_{EE} pins and the use of this part as an interface between several logic families.

The Latch Enable Pins

The latch function is intended to stop the device from comparing the signals on both input pins. If the latch function is enabled, the output is frozen and the logic information on the output pins, present at that moment, is held until the latch function is disabled. The timing of this process can be seen in Figure 20. The input levels for the latch pins should comply with RSPECL, but can also be driven with PECL type of signals if the minimum supply (V_{CCO} –V_{EE}) is larger or equal to 3.3V. The minimum differential latch input voltage should be 100 mV. Another possibility to set the LE function in a steady state is to connect the pins via a resistor to the power supply. If the LE pin is connected to V_{EE} via a resistor of 10 kΩ and the LE-not pin is connected via 10 kΩ to the V_{CCO} pin the part is continuously on. Since the latch input stage is referenced to V_{CCO}, the resistors to set the LE function should be connected to this voltage. This is very important when working with different voltages for V_{CCI} and V_{CCO}. If connected to the wrong supply, the latch function will not work.

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The DAP and the VEE Pins

To ensure that both VEE pins are operating at the same voltage, both pins are connected to the DAP, and thus to each other, through bond wires. As a consequence, the DAP is at the same potential as the VEE pins and can be used to connect the device to the minimum supply voltage. A more solid VEE connection is obtained if the two VEE pins and the DAP are all connected to the minimum supply on the PCB, rather than an indirect connection through the internal bond wires.

To protect the device during handling and production two anti-parallel connected diodes are connected between both VEE pins. Under normal operating conditions these diodes are shorted via the DAP.

The DAP (Die Attach Paddle) functions as a heat sink which means that heat can be transferred using vias below this pad to the copper plane VEE is connected to.

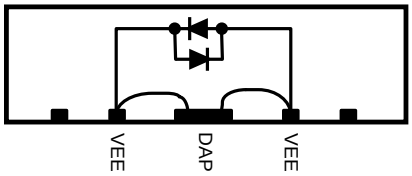


Figure 21. DAP Connection

Interface Between Logic Families

As can be seen in the typical schematics (see Figure 1) the LMH7322 can be used to interface between different logic families. The feature that facilitates this property is the fact that the input stage and the output stage use different positive power supply pins which can be used at different supply voltages. The negative supply pins are connected together for both parts. Using the power pins at different supply voltages makes it possible to create several translations for logic families. It is possible to translate from logic at negative voltage levels such as ECL to logic at positive levels such as RSPECL and LVDS and vice versa. The drawings in the next paragraphs do not show the output resistors except the first one. This is intentionally done for simplicity. All outputs need an output resistor to a termination voltage or to the negative rail as can be seen on the front page in the Typical Application of an ECL to RSPECL converter.

Interface from ECL to RSPECL

The supply pin V_{CCI} can be connected to ground because the input levels are negative and the V_{CCO} pin must operate at 5V to create the RSPECL levels (see Figure 22). When working with ECL, the negative supply pin (V_{EE}) can be connected to the −5.2V ECL supply voltage.

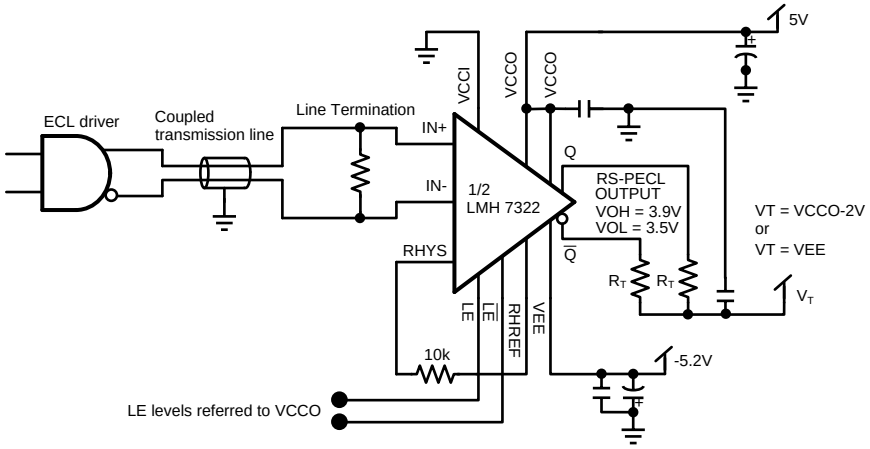


Figure 22. ECL TO RSPECL

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Interface from PECL to (RS)ECL

The conversion from PECL to RS-ECL is possible when connecting the V_{CCI} pin to +5V, which allows the input stage to handle these positive levels. The V_{CCO} pin must be connected to the ground level in order to create the RSECL levels. The high level of the output of the LMH7322 is normally 1.1V below the V_{CCO} supply voltage, and the low level is 1.5V below this supply. The output levels are now −1100 mV for the logic '1' and −1500 mV for the logic '0' (see Figure 23). In the same way the V_{EE} can be connected to the ECL supply voltage of −5.2V.

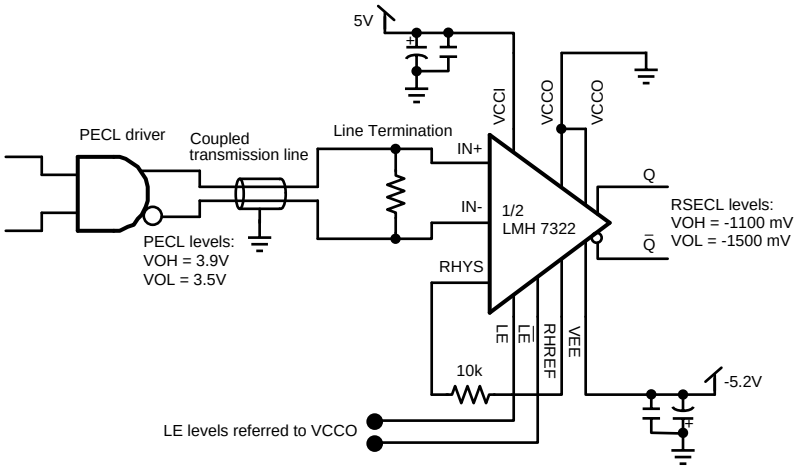


Figure 23. PECL TO RSECL

Interface from Analog to LVDS

As seen in Figure 24, the LMH7322 can be configured to create LVDS levels. This is done by connecting the V_{CCO} to 2.5V. As discussed before the output levels are now at V_{CCO} –1.1V for the logic '1' and at V_{CCO} −1.5V for the logic '0'. These levels of 1000 mV and 1400 mV comply with the LVDS levels. As can be seen in this setup, an AC coupled signal via a transmission line is used. This signal is terminated with 50Ω.

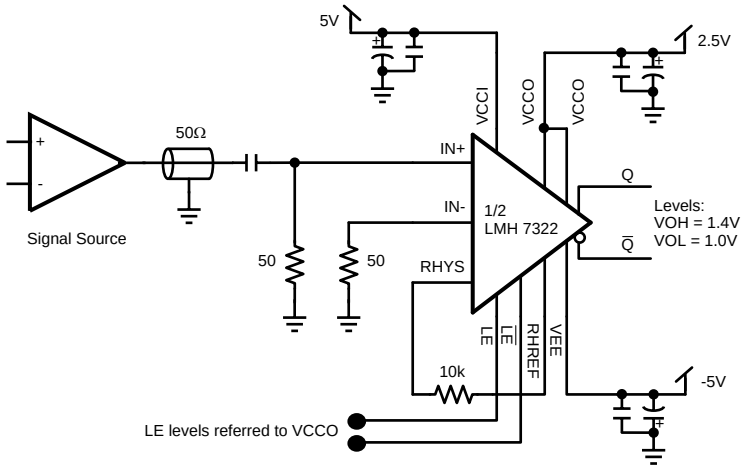


Figure 24. ANALOG TO LVDS

Figure 25 shows a standard comparator setup which creates RSPECL levels because the V_{CCO} supply voltage is +5V. In this case the V_{EE} pin is connected to the ground level. The V_{CCI} pin is connected to the V_{CCO} pin because there is no need to use different positive supply voltages. The input signal is AC coupled to the positive input. To maintain reliable results the input pins IN+ and IN− are biased at 1.4V through a resistive divider using a resistor of 1 kΩ to ground and a resistor of 2.5 kΩ to the V_{CC} and by adding two decoupling capacitors. Both inputs are connected to the bias level by the use of a 10 kΩ resistor. With this input configuration the input stage can work in a linear area with signals of approximately 3 V_{PP} (see Input Voltage Range or V_{RI} in the Electrical Characteristics tables.)

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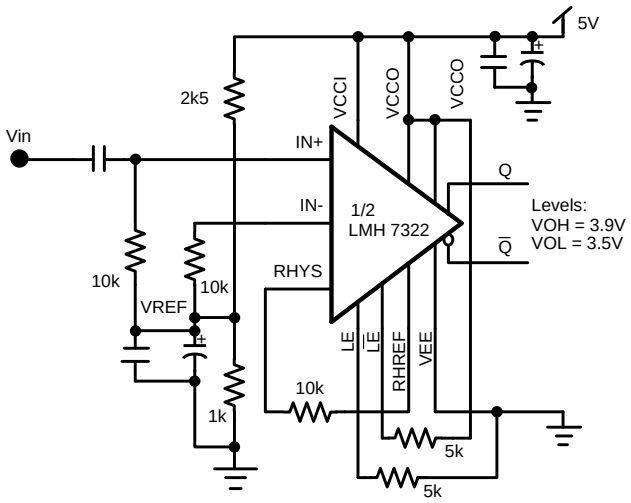


Figure 25. Standard Setup

Delay and Dispersion

Comparators are widely used to connect the analog world to the digital one. The accuracy of a comparator is dictated by its DC properties, such as offset voltage and hysteresis, and by its timing aspects, such as rise and fall times and delay. For low frequency applications most comparators are much faster than the analog input signals they handle. The timing aspects are less important here than the accuracy of the input switching levels. The higher the frequencies, the more important the timing properties of the comparator become, because the response of the comparator can make a noticeable change in critical parameters such as time frame or duty cycle. A designer has to know these effects and has to deal with them. In order to predict what the output signal will do, several parameters are defined which describe the behavior of the comparator. For a good understanding of the timing parameters discussed in the following section, a brief explanation is given and several timing diagrams are shown for clarification.

Propagation Delay

The propagation delay parameter is described in the Table 1 section. Due to this definition there are two parameters, t_{PDH} and t_{PDL} (Figure 26). Both parameters do not necessarily have the same value. It is possible that differences will occur due to a different response of the internal circuitry. As a derivative of this effect another parameter is defined: Δt_{PD}. This parameter is defined as the absolute value of the difference between t_{PDH} and t_{PDL}.

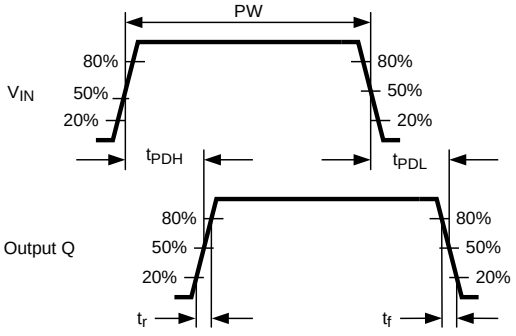


Figure 26. Propagation Delay

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If Δt_{PD} is not zero, duty cycle distortion will occur. For example when applying a symmetrical waveform (e.g. a sinewave) at the input, it is expected that the comparator will produce a symmetrical square wave at the output with a duty cycle of 50%. When t_{PDH} and t_{PDL} are different, the duty cycle of the output signal will not remain at 50%, but will be increased or decreased. In addition to the propagation delay parameters for single ended outputs discussed before, there are other parameters in the case of complementary outputs. These parameters describe the delay from input to each of the outputs and the difference between both delay times (See Figure 27.) When the differential input signal crosses the reference level from L to H, both outputs will switch to their new state with some delay. This is defined as t_{PDH} for the Q output and t_{PDL} for the $\overline{Q}$ output, while the difference between both signals is defined as Δt_{PDLH}. Similar definitions for the falling slope of the input signal can be seen in Figure 19.

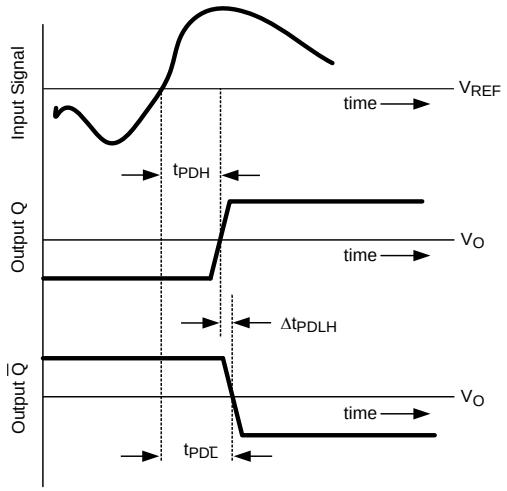


Figure 27. t_{PD} with Complementary Outputs

Both output circuits should be symmetrical. At the moment one output is switching 'on' the other is switching 'off' with ideally no skew between both outputs. The design of the LMH7322 is optimized so that this timing difference is minimized. The propagation delay, t_{PD}, is defined as the average delay of both outputs at both slopes: (t_{PDLH} + t_{PDHL})/2.

Both overdrive and starting point should be equally divided around the V_{REF} (absolute values).

Dispersion

There are several circumstances that will produce a variation of the propagation delay time. This effect is called dispersion.

Amplitude Overdrive Dispersion

One of the parameters that causes dispersion is the amplitude variation of the input signal. Figure 28 shows the dispersion due to a variation of the input overdrive voltage. The overdrive is defined as the 'go to' differential voltage applied to the inputs. Figure 28 shows the impact it has on the propagation delay time if the overdrive is varied from 10 mV to 100 mV. This parameter is measured with a constant slew rate of the input signal.

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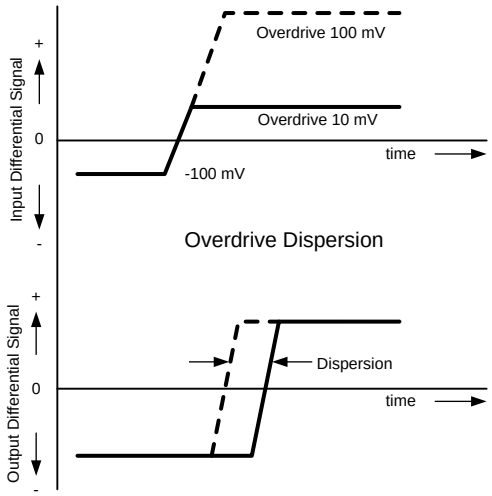


Figure 28. Overdrive Dispersion

The overdrive dispersion is caused by the switching currents in the input stage which is dependent on the level of the differential input signal.

Slew Rate Dispersion

The slew rate is another parameter that affects propagation delay. The higher the input slew rate, the faster the input stage switches (See Figure 29).

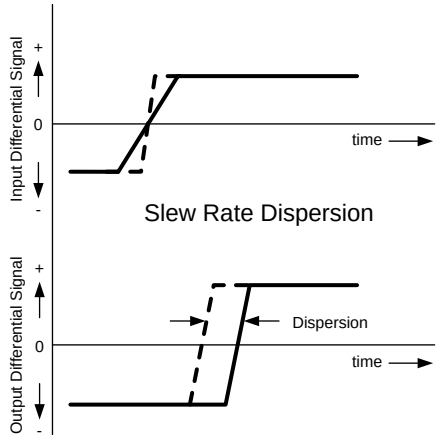


Figure 29. Slew Rate Dispersion

A combination of overdrive and slew rate dispersion occurs when applying signals with different amplitudes at constant frequency. A small amplitude will produce a small voltage change per time unit (dV/dt) but also a small maximum switching current (overdrive) in the input transistors. High amplitudes produce a high dV/dt and a larger overdrive.

Common Mode Dispersion

Dispersion will also occur when changing the common mode level of the input signal (Figure 30). When V_{REF} is swept through the CMVR (Common Mode Voltage Range), It results in a variation of the propagation delay time. This variation is called Common Mode Dispersion.

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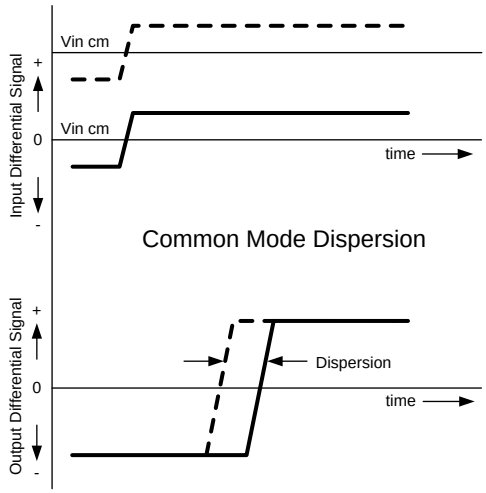


Figure 30. Common Mode Dispersion

All of the dispersion effects described previously influence the propagation delay. In practice the dispersion is often caused by a combination of more than one varied parameter.

Hysteresis & Oscillations

In contrast to an op amp, the output of a comparator has only two defined states '0' or '1.' Due to finite comparator gain however, there will be a small band of input differential voltage where the output is in an undefined state. An input signal with fast slopes will pass this band very quickly without problems. During slow slopes however, passing the band of uncertainty can take a relatively long time. This enables the comparators output to switch back and forth several times between '0' and '1' on a single slope. The comparator will switch on its input noise, ground bounce (possible oscillations), ringing etc. Noise in the input signal will also contribute to these undesired switching actions. The next sections explain these phenomena in situations where no hysteresis is applied, and discuss the possible improvement hysteresis can give.

Using No Hysteresis

Figure 31 shows what happens when the input signal rises from just under the threshold V_{REF} to a level just above it. From the moment the input reaches the lowest dotted line around V_{REF} at t=0, the output toggles on noise etc. Toggling ends when the input signal leaves the undefined area at t=1. In this example the output was fast enough to toggle three times. Due to this behavior digital circuitry connected to the output will count a wrong number of pulses. One way to prevent this is to choose a very slow comparator with an output that is not able to switch more than once between '0' and '1' during the time the input state is undefined.

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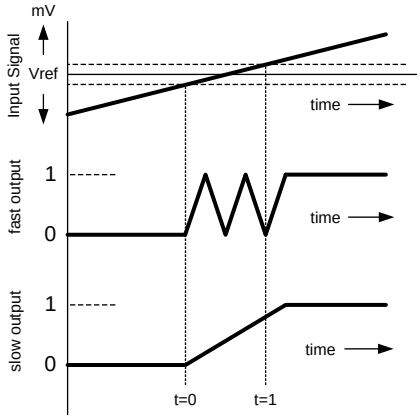


Figure 31. Oscillations on Output Signal

In most circumstances this is not an option because the slew rate of the input signal will vary.

Using Hysteresis

Hysteresis can be introduced to avoid oscillations, e.g. due to noise on the input signal, especially for slow edges. For this purpose the switching level without hysteresis (V_{REF}) is forced to a new level (A or B) at the moment the input signal crosses one of these levels. This can be seen in Figure 32.

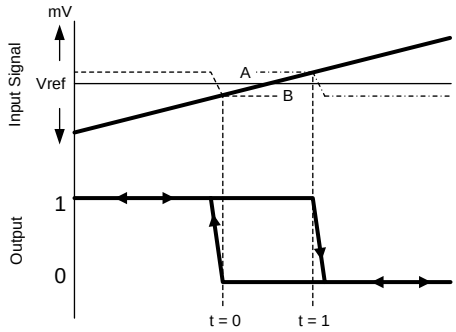


Figure 32. Hysteresis

In this picture the two dotted lines A and B, represent the resulting reference level at which the comparator will compare the input level against. Assume that for this situation the input signal is connected to the negative input and the switching level (V_{REF}) to the positive input. The input level drawn in Figure 32 starts much lower as the reference level and this means that the input stage is well defined with the inverting input much lower than the non-inverting input. As a result the output will be in the high state. Internally the switching level is at level A, with the input signal sloping up, this situation remains until V_{IN} crosses level A at t=1. Now the output toggles, and the internal switching level is lowered to level B. So before the output has the possibility to toggle again, the voltage difference between the inputs is sufficient to have a stable situation again. When the input signal comes down from high to low, the situation is stable until level B is reached at t=0. At this moment the output will toggle back, and the circuit returns to the starting situation with the inverting input at a much lower level than the non inverting input. Varying the levels A and B due to the change of the hysteresis resistor will also vary the timing of t=0 and t=1. When designing a circuit be aware of this effect. Introducing hysteresis will cause some time shift between output and input (e.g. duty cycle variations), but will eliminate undesired switching of the output.

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Configuring Hysteresis for the LMH7322

The LMH7322 offers the possibility to introduce hysteresis by connecting a resistor between the RHYS pin and the RHREF pin. This hysteresis setting resistor may vary between zero ohm and infinite. The current drawn from the RHYS pin determines the setting of the internal reference voltage. When no resistor is present the internal used reference voltage is set to zero (the difference between A and B level is zero, see explanation Using Hysteresis) and no hysteresis is configured. This means the output will change state when the difference between the positive en negative input signals crosses zero level. Connecting a resistor between the RHYS pin and the RHREF pin produces a difference for the A and B levels which means hysteresis is introduced and the output will change state at different levels for an up or down transition of the input signal. Due to the internal structure a current must be drawn from the RHYS pin. This can be done by connecting a resistor to the lowest supply voltage. In order to assure the RHYS pin is connected to the correct voltage level, and unwanted current variations in the hysteresis level are avoided, the RHREF and VEE are connected internally within the LMH7322. Therefore, the hysteresis resistor should only be connected between RHYS and RHREF or left open if no hysteresis is required. To select the correct resistor for the desired hysteresis voltage see Figure 33.

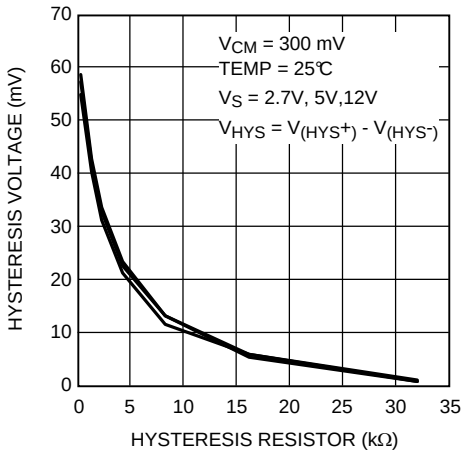


Figure 33. Hysteresis Voltage vs. Hysteresis Resistor

With the use of a resistor to set the hysteresis voltage no external conditions will effect these setting as long as they stay within the normal operating ranges. Temperature changes may cause a variation of the hysteresis resistor dictated by the temperature coefficient of the used type. Connecting the RHYS pin to another voltage as provided by the RHREF pin is not covered in the resistor selection plot and the designer of such a circuit must be aware of abnormal behavior.

The Output

Output Swing Properties

The LMH7322 has differential outputs which means that both outputs have the same swing but in opposite directions (See Figure 34). Both outputs swing around the common mode output voltage (V_O). This voltage can be measured at the midpoint between two equal resistors connected to each output. The absolute value of the difference between both voltages is called V_{OD}. The outputs cannot be held at the V_O level because of their digital nature. They only cross this level during a transition. Due to the symmetrical structure of the circuit, both output voltages cross at V_O regardless of whether the output changes from '0' to '1' or vise versa.

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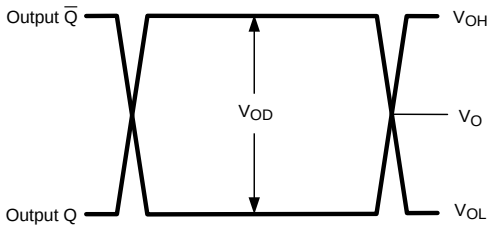


Figure 34. Output Swing

Loading the Output

Both outputs are activated when current is flowing through a resistor that is externally connected to V_T. The termination voltage should be set 2V below the V_{CCO}. This makes it possible to terminate each of the outputs directly with 50Ω, and if needed to connect through a transmission line with the same impedance (see Figure 35). Due to the low ohmic nature of the output emitter followers and the 50Ω load resistor, a capacitive load of several pF does not dramatically affect the speed and shape of the signal. When transmitting the signal from one output to any input the termination resistor should match the transmission line. The capacitive load (C_P) will distort the received signal. When measuring this input with a probe, a certain amount of capacitance from the probe is parallel to the termination resistor. The total capacitance can be as large as 10 pF. In this case there is a pole at:

$$f = 1/(2*\pi*C*R) \quad (1)$$

$$f = 1e9/ \pi \quad (2)$$

$$f = 318 \text{ MHz} \quad (3)$$

In this case the current I_P has the same value as the current through the termination resistor. This means that the voltage drops at the input and the rise and fall times are dramatically different from the specified numbers for this part.

Another parasitic capacitance that can affect the output signal is the capacitance directly between both outputs, called C_{PAR} (see Figure 35). The LMH7322 has two complementary outputs so there is the possibility to transport the output signal by a symmetrical transmission line. In this case both output tracks form a coupled line with their own parasitics and both receiver inputs connected to the transmission line. Actually the line termination looks like 100Ω and the input capacitances, which are in series, are parallel to the 100Ω termination. The best way to measure the input signal is to use a differential probe directly across both inputs. Such a probe is very suitable for measuring these fast signals because it has good high frequency characteristics and low parasitic capacitance.

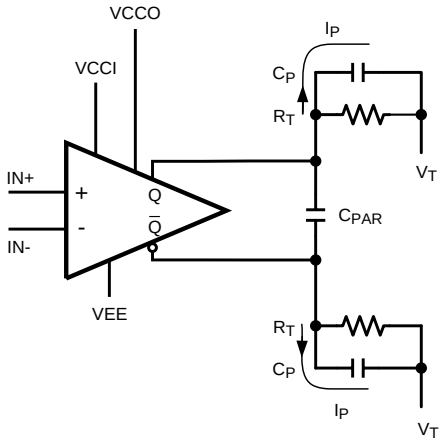


Figure 35. Parasitic Capacitance

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Transmission Lines & Termination Technologies

The LMH7322 uses complementary RSPECL outputs and emitter followers, which means high output current capability and low sensitivity to parasitic capacitance. The use of Reduced Swing Positive Emitter Coupled Logic reduces the supply voltage to 2.7V, being the lowest possible value, and raises the maximum frequency response. Data rates are growing, which requires increasing speed. Data is not only connected to other IC's on a single PCB board but, in many cases, there are interconnections from board to board or from equipment to equipment. Distances can be short or long but it is always necessary to have a reliable connection, which consumes low power and is able to handle high data rates. The complementary outputs of the LMH7322 make it possible to use symmetrical transmission lines The advantage over single ended signal transmission is that the LMH7322 has higher immunity to common mode noise. Common mode signals are signals that are equally apparent on both lines and because the receiver only looks at the difference between both lines, this noise is canceled.

Maximum Bit Rates

The maximum toggle rate is defined at an amplitude of 50% of the nominal output signal. This toggle rate is a number for the maximum transfer rate of the part and can be given in Hz or in Bps. When transmitting signals in a NRZ (Non Return to Zero) format the bitrate is double this frequency number, because during one period two bits can be transmitted. (See Figure 36.) The rise and fall times are very important specifications in high speed circuits. In fact these times determine the maximum toggle rate of the part. Rise and fall times are normally specified at 20% and 80% of the signal amplitude (60% difference). Assuming that the edges at 50% amplitude are coming up and down like a sawtooth it is possible to calculate the maximum toggle rate but this number is too optimistic. In practice the edges are not linear while the pulse shape is more or less a sinewave.

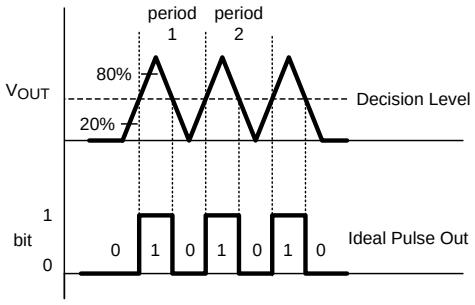


Figure 36. Bit Rates

Need for Terminated Transmission Lines

During the 1980's and 90's, TI fabricated the 100K ECL logic family. The rise and fall time specifications were 0.75 ns, which are considered very fast. If sufficient care has not been given in designing the transmission lines and choosing the correct terminations, then errors in digital circuits are introduced. To be helpful to designers that use ECL with "old" PCB-techniques, the 10K ECL family was introduced with a rise and fall time specification of 2 ns. This was much slower and easier to use. The RSPECL output signals of the LMH7322 have transition times that extend the fastest ECL family. A careful PCB design is needed using RF techniques for transmission and termination. Transmission lines can be formed in several ways. The most commonly used types are the coaxial cable and the twisted pair telephony cable (Figure 37).

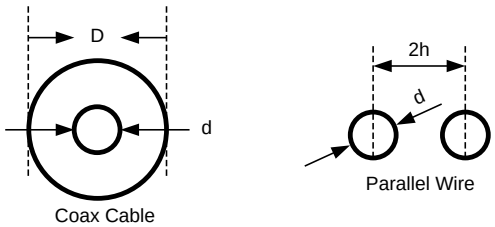


Figure 37. Cable Types

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These cables have a characteristic impedance determined by their geometric parameters. Widely used impedances for the coaxial cable are 50Ω and 75Ω. Twisted pair cables have impedances of about 120Ω to 150Ω.

Other types of transmission lines are the strip line and the micro strip line. These last types are used on PCB boards. They have the characteristic impedance dictated by the physical dimensions of a track placed over a metal ground plane (see Figure 38).

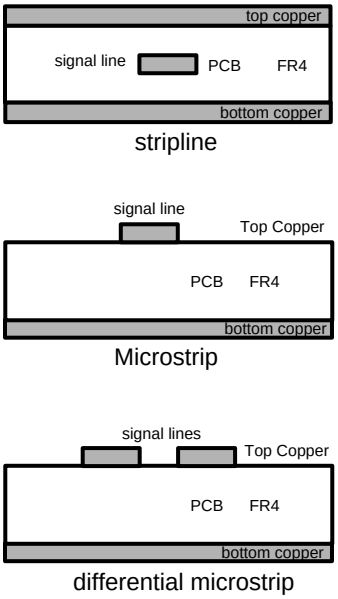


Figure 38. PBC Lines

Differential Microstrip

Line The transmission line which is ideally suited for complementary signals is the differential microstrip line. This is a double microstrip line with a narrow space in between. This means both lines have strong coupling and this determines the characteristic impedance. The fact that they are routed above a copper plane does not affect differential impedance, only CM-capacitance is added. Each of the structures above has its own geometric parameters, so for each structure there is different formula to calculate the right impedance. For calculations on these transmission lines visit the TI website or order RAPIDESIGNER. At the end of the transmission line there must be a termination having the same impedance as that of the transmission line itself. It does not matter what impedance the line has, if the load has the same value no reflections will occur. When designing a PCB board with transmission lines on it, space becomes an important item especially on high density boards. With a single microstrip line, line width is fixed for given impedance and a board material. Other line widths will result in different impedances.

Advantages of Differential MicrostripLines

Impedances of transmission lines are always dictated by their geometric parameters. This is also true for differential microstrip lines. Using this type of transmission line, the distance of the track determines the resulting impedance. So, if the PCB manufacturer can produce reliable boards with low track spacing the track width for a given impedance is also small. The wider the spacing, the wider tracks are needed for a specific impedance. For example two tracks of 0.2 mm width and 0.1 mm spacing have the same impedance as two tracks of 0.8 mm width and 0.4 mm spacing. With high-end PCB processes, it is possible to design very narrow differential microstrip transmission lines. It is desirable to use these to create optimal connections to the receiving part or the terminating resistor, in accordance to their physical dimensions. Seen from the comparator, the termination resistor must be connected at the far end of the line. Open connections after the termination resistor (e.g. to an input of a receiver) must be as short as possible. The allowed length of such connections varies with the received transients. The faster the transients, the shorter the open lines must be to prevent signal degradation.

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PCB Layout Considerations and Component Value Selection

High frequency designs require that both active and passive components be selected from those that are specially designed for this purpose. The LMH7322 is fabricated in a 24-pin WQFN package intended for surface mount design. For reliable high speed design it is highly recommended to use small surface mount passive components because these packages have low parasitic capacitance and low inductance simply because they have no leads to connect them to the PCB. It is possible to amplify signals at frequencies of several hundreds of MHz using standard through-hole resistors. Surface mount devices however, are better suited for this purpose. Another important issue is the PCB itself, which is no longer a simple carrier for all the parts and a medium to interconnect them. The PCB becomes a real component itself and consequently contributes its own high frequency properties to the overall performance of the circuit. Good practice dictates that a high frequency design have at least one ground plane, providing a low impedance path for all decoupling capacitors and other ground connections. Care should be given especially that on-board transmission lines have the same impedance as the cables to which they are connected. Most single ended applications have 50Ω impedance (75Ω for video and cable TV applications). Such low impedance, single ended microstrip transmission lines usually require much wider traces (2 to 3 mm) on a standard double sided PCB board than needed for a ‘normal’ trace. Another important issue is that inputs and outputs should not ‘see’ each other. This occurs if input and output tracks are routed in parallel over the PCB with only a small amount of physical separation, particularly when the difference in signal level is high. Furthermore, components should be placed as flat and low as possible on the surface of the PCB. For higher frequencies a long lead can act as a coil, a capacitor or an antenna. A pair of leads can even form a transformer. Careful design of the PCB minimizes oscillations, ringing and other unwanted behavior. For ultra high frequency designs only surface mount components will give acceptable results. (For more information see OA-15 [SNOA367]).

TI suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing:

LMH7322EVAL

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REVISION HISTORY

Changes from Revision H (March 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	27

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH7322SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	L7322SQ	Samples
LMH7322SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	L7322SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

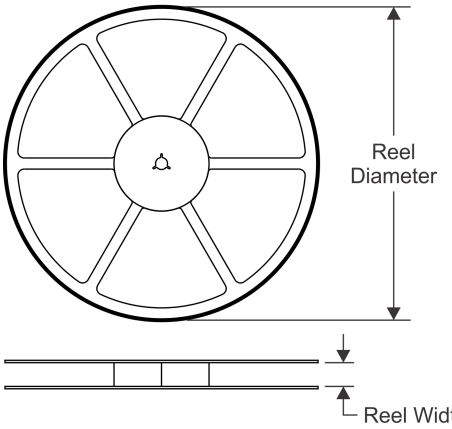
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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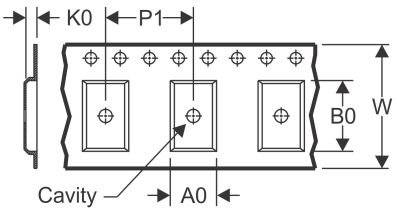
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

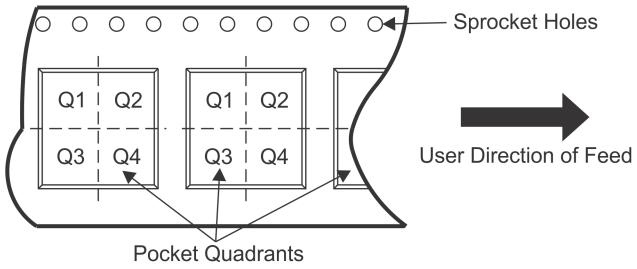


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

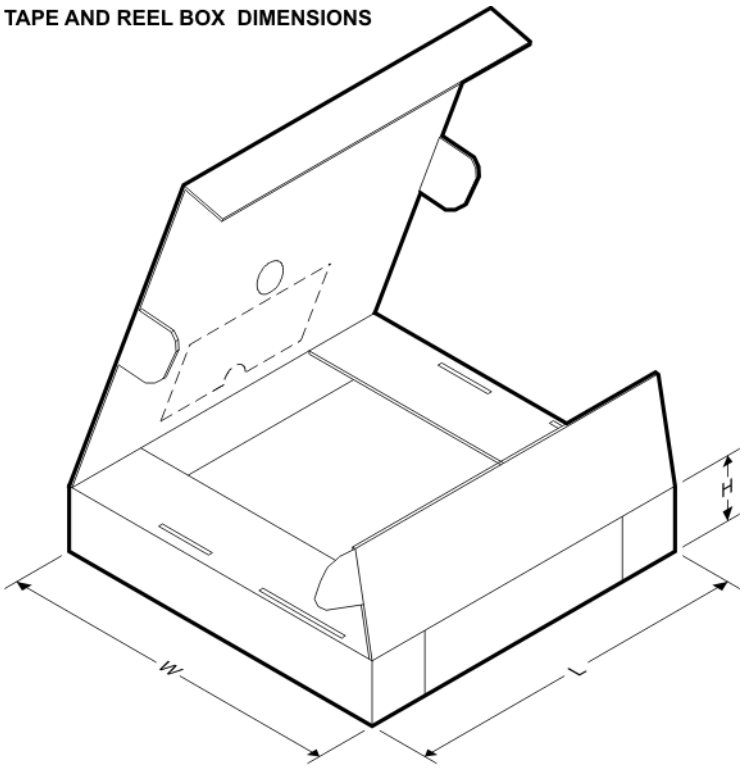
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH7322SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH7322SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

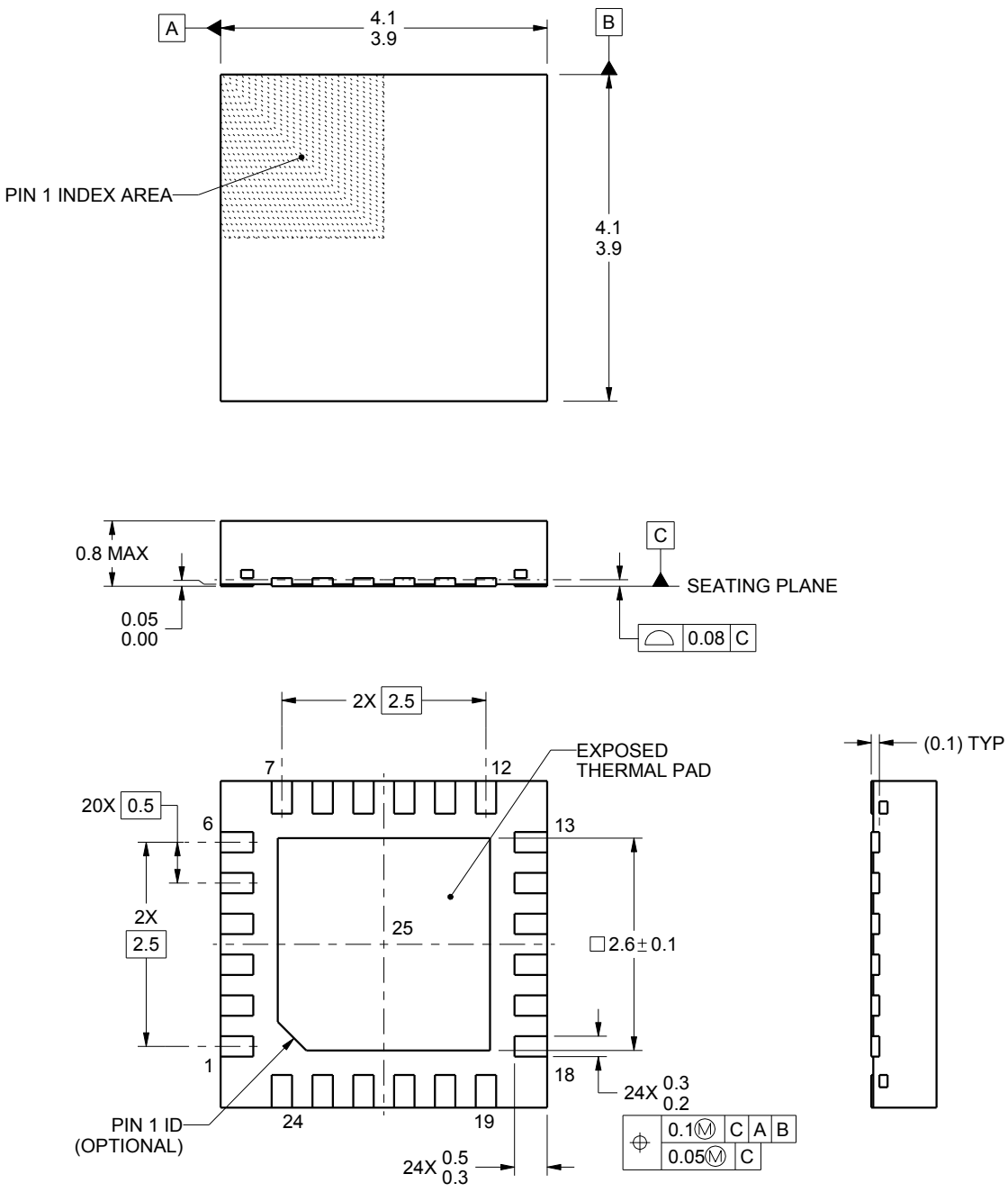
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH7322SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LMH7322SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

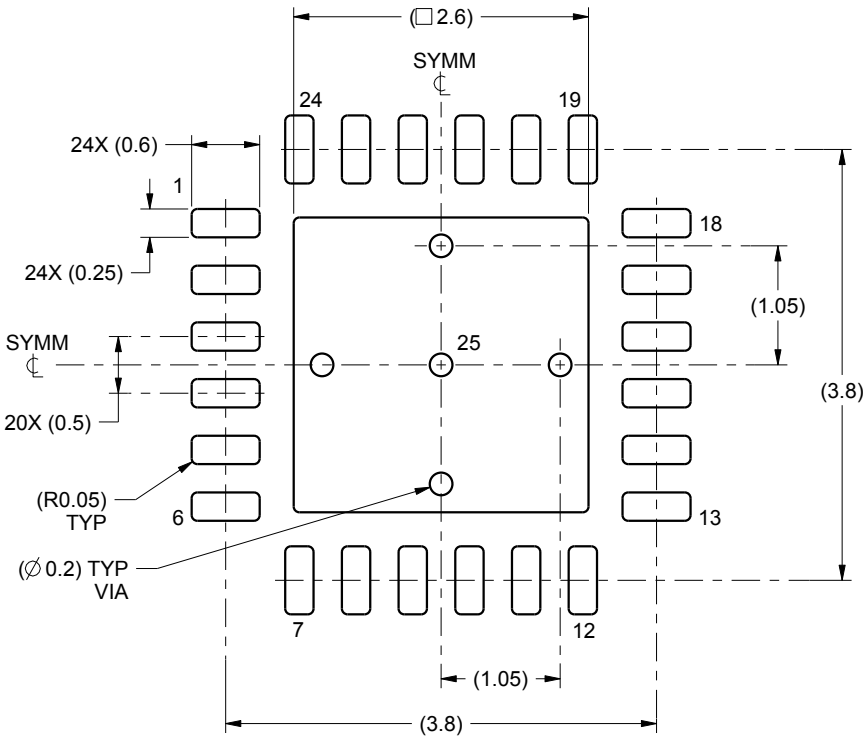
PLASTIC QUAD FLATPACK - NO LEAD



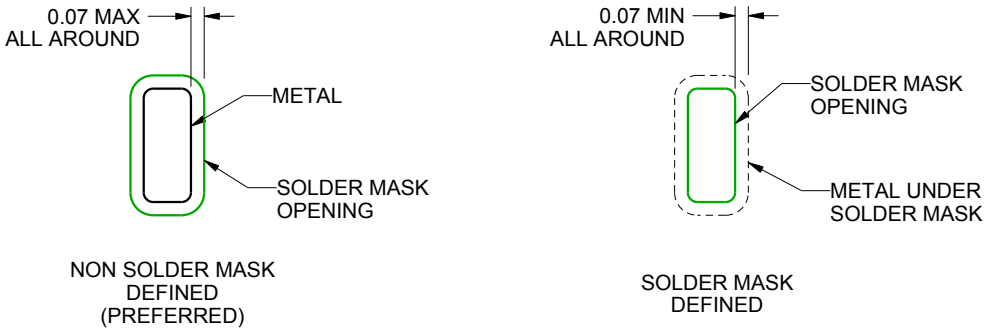
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

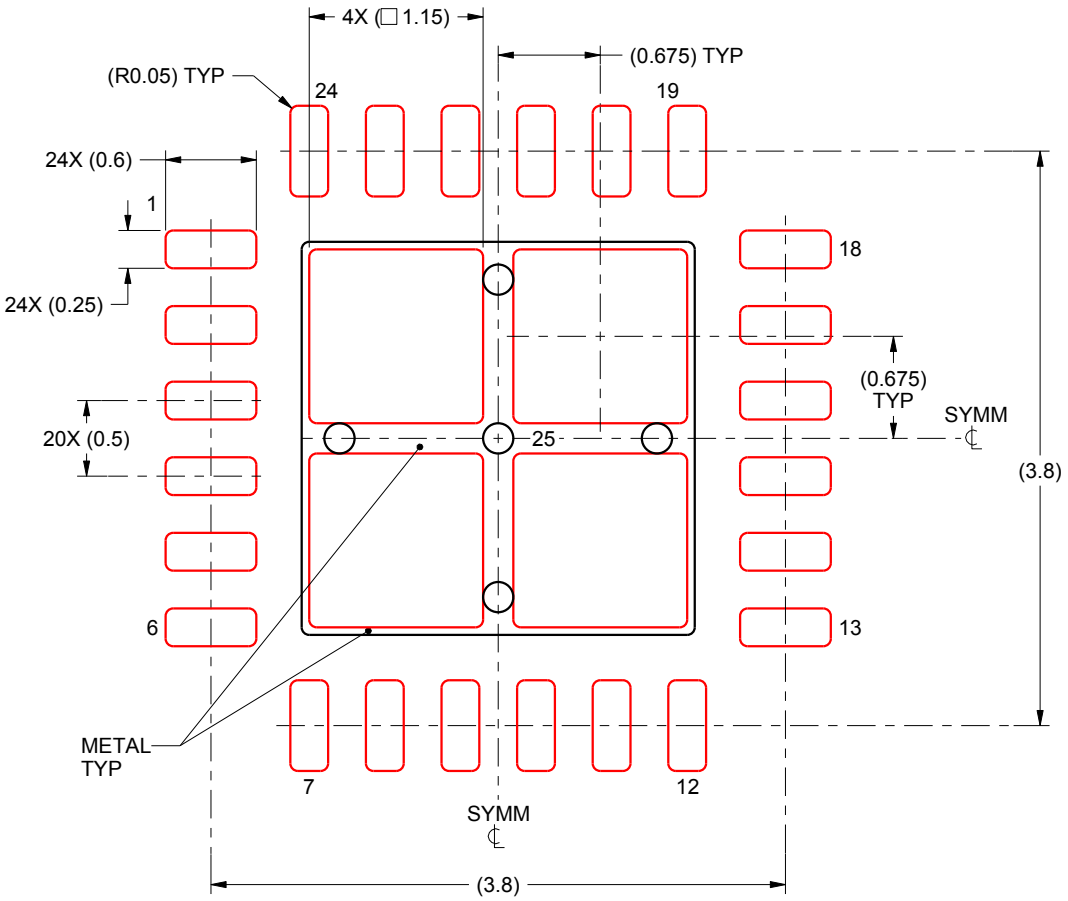


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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