PL360G55CF-EK

PL360G55CF-EK User Guide

Introduction

PL360G55CF-EK is an evaluation kit for the PL360 modem. PL360 is a programmable modem for narrow-band Power Line Communication (PLC) from Microchip Technology Inc, able to run any PLC protocol in the frequency band below 500 kHz. The PL360 has been conceived to be driven by external Microchip host controller devices; in this case a SAMG55 ARM® Cortex®-M4 RISC processor is used. The Microchip host device loads the corresponding PLC-protocol firmware and then controls the PL360 modem operation.

The PL360G55CF-EK board has been conceived to communicate in CENELEC A-Band (35 kHz to 91 kHz) and in FCC band (151 kHz to 472 kHz). It complies with CENELEC standard EN 50065 regulations in CENELEC A-Band. It can be connected directly to AC mains or DC power rails.

Contents

- Welcome letter
- Board:
  - One PL360G55CF-EKv1 board
- Cable:
  - One Micro A/B-type USB cable
- Jumpers:
  - Two jumpers with pitch 1.27 mm
- Pin Headers:
  - Two 8-pin headers with pitch 2.54 mm

Features

- PL360G55CF-EK board mounts a PL360 PLC transceiver and a SAMG55J19 ARM Cortex M4 microcontroller.
- PL360G55CF-EK board provides a full-featured platform to develop a complete communications system based on PLC technology working in CENELEC A-Band and FCC band.
- PL360 is a compact and highly efficient device for a wide range of Smart Grid applications such as lighting control, industrial/home automation and renewable-energy management, among others.
- PL360G55CF-EK board provides support for:
  - PLC band characterization and noise level measurement
  - PLC sensitivity level measurement
  - Power consumption
  - Power fail detection
- PL360G55CF-EK board includes a SWD/JTAG interface for MCU debugging and programming purposes. Firmware is also upgradable via USB/serial interface.
- USB 2.0 full-speed interface.

- mikroBUS™ add-on connectors to integrate the board itself as a module for interfacing with other microcontrollers or microprocessors (mikroBUS main board).
- PL360G55CF-EK board can be supplied from the following connectors:
  - mikroBUS connector
  - Micro-B USB connector
  - DC Jack connector

Table of Contents

1. Evaluation Kit Specifications

1.1 Safety Recommendations

This evaluation board must only be used by expert technicians. The PL360G55CF-EK board is powered from a DC power source, so only the PLC coupling stage could have a hazardous voltage when is connected to mains. The risk of electric shock is minimized since all required connectors and configuration jumpers are galvanically isolated from the coupling stage.

⚠ CAUTION Be careful, there is risk of electric shock in the PLC coupling stage. A normal use of the PL360G55CF-EK board is for indoor use only.

This evaluation board does not have any switch on mains connection to switch it on or off.

To avoid damage of measurement instruments, do not connect any probe to the high voltage sections if the board is not isolated from the mains supply.

Temperature operating range should be from 0ºC to +85ºC. Running extended periods at minimum and maximum values may cause permanent damage to the board. Quartz crystal components could not cover previous temperature range with desired performance due to aging.

The evaluation board is intended for further engineering, development, demonstration, or evaluation purposes only. It is not a finished product, unless otherwise noted on the board/kit.

Important: Microchip does not assume any responsibility for the consequences arising from any improper use of this board.

1.2 Electrical Specifications

This section shows the electrical characteristics of the PL360G55CF-EK board.

Table 1-1. Power Supply Requirements

Parameter	Condition	Min.	Typ.	Max.	Unit
DC Mains Voltage Range	DC Jack Connector, J8	6	-	30	V_{DC}
Maximum Input Current	DC Jack Connector, J8	-	370[1]	-	mA
Isolation Voltage	PLC coupling transformer	-	-	3000	V_{AC}

Note that the PL360G55CF-EK can be supplied with several power sources. For more information about the power supply system, see section 3.3.6 Power Supply System.

Note:

1. Board supplied with 6 V_{DC}, transmission against very low impedance (2Ω) and all peripherals are on.

Table 1-2. Power Consumption

Parameter	Condition	Consumption	Unit
TX Power Consumption	FW: G3 CENELEC A PHY TX Test Console Application. Low Impedance Load (2Ω LISN, see Figure C.1 of ITU-T G.9901). Measured on 12V DC/DC output.	1390[1]	mW
	FW: G3 CENELEC A PHY TX Test Console Application. High Impedance Load (CISPR LISN, see Figure 5 of EN 50065-1). Measured on 12V DC/DC output.	318[1]	mW
RX Power Consumption	Measured on 3.3V DC/DC output	238[1]	mW

Notes:

1. These measurements were taken running the PHY TX Test Console project with a default configuration in TX and RX modes, and correspond to the whole PCBA design and not only to PL360 and SAMG55J19 devices. All PCB is supplied in the worst consumption conditions (board is supplied with a minimum input voltage, 6 V_{DC}) and emitting in CENELEC A-band. Refer to *PL360* and *SAMG55 datasheets* for their respective power consumption.

2. Getting Started

2.1 Powering-Up the Board

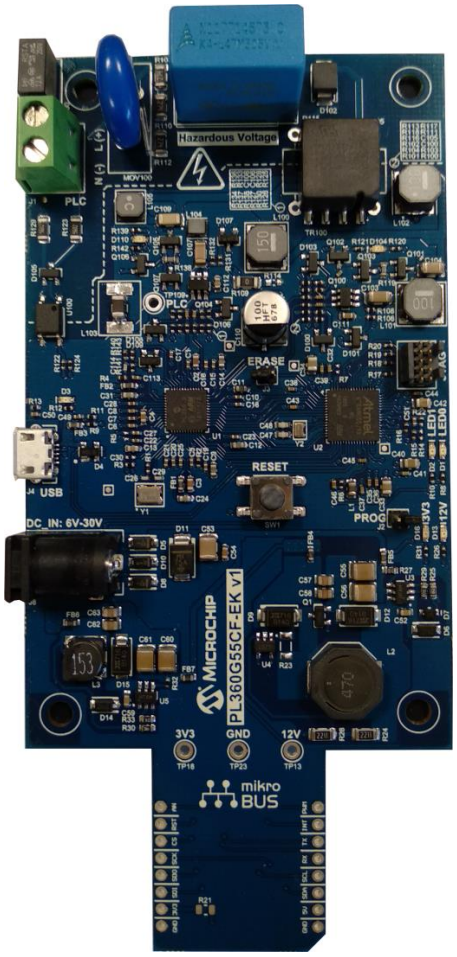
Unpack and inspect the kit carefully.

Figure 2-1. Unpacked PL360G55CF-EK

Kit contents are covered by anti-static foam. The PL360G55CF-EK board is shipped in an anti-static shielding bag.

⚠WARNING The board must not be subject to high electrostatic discharge. We recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments. Avoid touching the components' pins or any other metallic elements on the board.

Figure 2-2. PL360G55CF-EKv1 Board Top View



Take into account that the connectors to supply the board are different than the one for PLC signals. The board can be supplied by three different ways:

- +5V from USB Micro-B connector (J4)
- +5V from mikroBUS connector (J6)
- DC voltage (from +6V to +30V) from DC Jack connector (J8)

2.2 Running Preloaded Firmware

Once the board is supplied, LEDs will show activity. The PL360G55CF-EK board is delivered with a preprogrammed application in SAMG55 Flash memory: the G3-PLC PHY Tester for CENELEC A-Band. PLC communications are developed for CENELEC A-Band in AC or DC voltage grid.

The kit includes a USB 2.0 type A to Micro-B cable that can be used to connect the board to a computer. Connect a suitable cable in the PLC connector (J1) and plug it to an AC/DC voltage grid to communicate.

By means of the PLC PHY Tester PC application, it is possible to send and receive PLC messages using the G3 PHY layer in the CENELEC A-Band according to the binary flashed in PL360G55CF-EK board.

2.3 Code and Technical Support

Firmware developers can not only run the given example code, but also implement their own applications based on the provided firmware stacks.

Please note that the latest software code, documentation and support materials are available online. Follow instructions described in the welcome letter for more information.

For any technical support requests, please visit http://support.microchip.com.

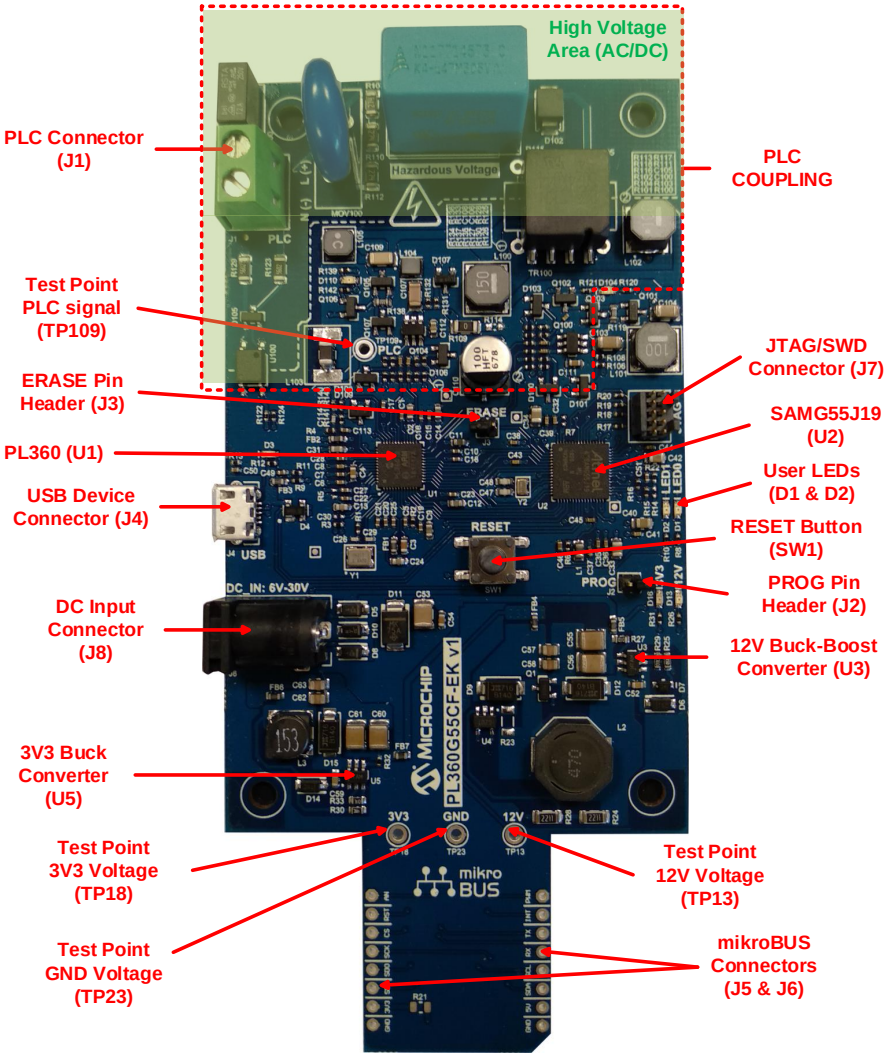
3. PL360G55CF-EK Board

3.1 Overview

This section summarizes the PL360G55CF-EK board design. It introduces system-level concepts, such as power supply, MCU, PLC coupling, peripherals and interface board.

PL360G55CF-EK is a PLC modem board based on the PL360 transceiver and on the SAMG55 ARM Cortex-M4 RISC processor. This evaluation board can be used as a PLC modem reference design for modular smart meter architectures; or, in any case to provide a platform to develop a complete communications system over PLC technology.

Figure 3-1. PL360G55CF-EKv1 Board Description



3.2 Features List

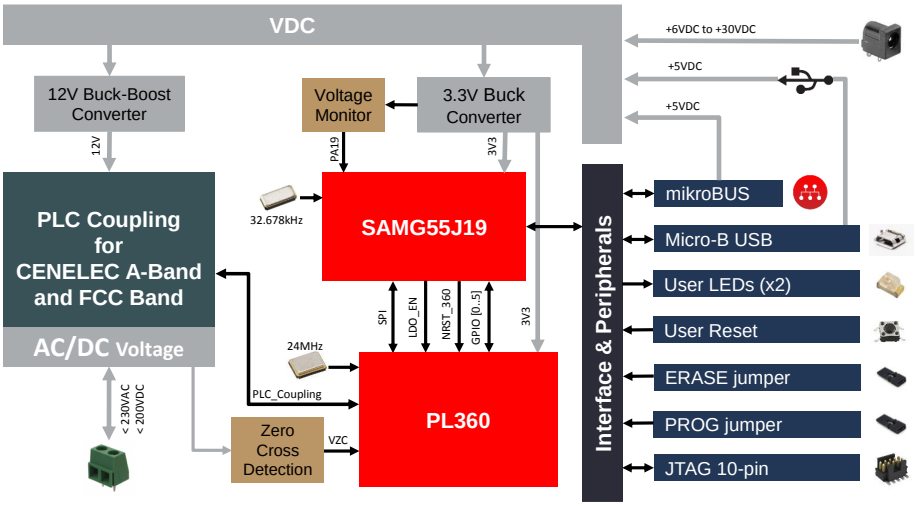
The PL360G55CF-EK board includes the following features:

- PL360 PLC Transceiver:
  - Multi-protocol PLC modem:
    - G3-PLC
    - PRIME 1.3 and PRIME 1.4
  - One SPI peripheral to external MCU
  - Zero-Cross Detection
  - Embedded PLC Analog Front End (AFE)
  - Low-power consumption in transmission and reception
- SAMG55 MCU:
  - Core:
    - ARM Cortex-M4 running at up to 120 MHz
    - Memory Protection Unit (MPU)
    - DSP instruction set
    - Floating-Point Unit (FPU)
    - Thumb® -2 instruction set
    - Instruction and Data Cache Controller with 2 Kbytes cache memory
    - Up to 512 Kbytes of embedded Flash, 176 Kbytes of embedded SRAM, 8 Kbytes of ROM
  - Memories:
    - Up to 512 Kbytes of embedded Flash
    - Up to 176 Kbytes of embedded SRAM
    - Up to 8 Kbytes of ROM with embedded boot loader, single-cycle access at full speed
- PLC Coupling designed to communicate in CENELEC A-Band (35 kHz to 91 kHz) or FCC band (151 kHz to 472 kHz)
- A 3.3V buck converter for the digital circuitry and a 12V Buck-Boost converter for supplying the PLC Power Amplifier. It allows supply of the board with any of the three different power sources
- Mains Zero-Crossing Detector Circuit
- Peripherals:
  - Supply monitor
  - User LEDs
  - Reset button
  - Chip Erase jumper
  - Chip Programming jumper
- Interfaces:
  - USB Device
  - mikroBUS add-on connectors
  - SWD/JTAG debugging port

3.2.1 PL360G55CF-EK Block Diagram

The following figure shows the block diagram of the PL360G55CF-EK board.

Figure 3-2. PL360G55CF-EK Block Diagram

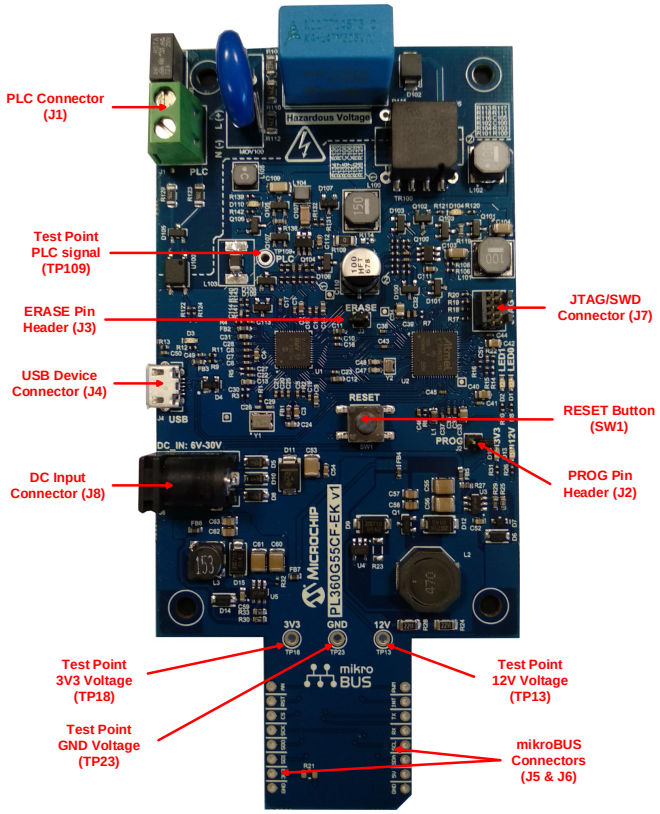


3.2.2 Interface Connection

The PL360G55CF-EK board includes hardware interfaces such as jumpers, connectors and a button.

Following figure shows an overview of the connectors, jumpers and button of the PL360G55CF-EK board.

Figure 3-3. PL360G55CF-EK Connectors, Button and Jumpers Overview



3.2.2.1 Connectors

The PL360G55CF-EK board includes the following connectors:

1. PLC connector (for an AC/DC grid), J1.

Table 3-1. PLC Connector (for an AC/DC grid), J1

Pin	Signal Name	Description
1	L / +VDC	Line / Positive Voltage
2	N / -VDC	Neutral / Negative Voltage

2. Micro-B female USB connector, J4.

Table 3-2. USB Device Connector, J4

Pin	Signal Name	Description
1	VUSB	5V power
2	D+	Data Plus
3	D-	Data Minus
4	ID	On the Go Identification
5	GND	Ground

3. mikroBUS add-on connectors, J5 and J6.

Table 3-3. mikroBUS Connector, J5

Pin	Mnemonic	Description
1	AN	Analog
2	RST	Reset
3	CS	SPI Chip Select
4	SCK	SPI Clock
5	SDO	SPI Master Input Slave Output
6	SDI	SPI Master Output Slave Input
7	3V3	VCC - 3.3V power
8	GND	Reference Ground

Table 3-4. mikroBUS Connector, J6

Pin	Mnemonic	Description
1	PWM	PWM
2	INT	Hardware Interrupt
3	TX	UART Transmit
4	RX	UART Receive
5	SCL	I^2C Clock

.....continued		
Pin	**Mnemonic**	**Description**
6	SDA	I^2C Data
7	5V	VCC - 5V power
8	GND	Reference Ground

4. JTAG/SWD 10-pin connector for SAMG55J19, J7.

Table 3-5. SW-DP Connector, J7

Pin	Mnemonic	Description
1	VCC	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from V_{CC} on the target board and must not have a series resistor.
2	SWDIO/TMS	Serial Wire Input Output / Test Mode Select. JTAG mode set input of target CPU. This pin should be pulled up on the target. Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
3	GND	Ground.
4	SWDCLK/TCK	Serial Wire Clock / Test Clock. JTAG clock signal to target CPU (output timing signal, for synchronizing test logic and control register access).
5	GND	Ground.
6	SWO/TDO	Test Asynchronous Data Out from target CPU.
7	KEY	-
8	NC/TDI	Not Connected / Test Data Input. JTAG data input of target CPU (serial data output line, sampled on the rising edge of the TCK signal). It is recommended that this pin is pulled to a defined state on the target board.
9	GND Detect	Ground.
10	nRESET	JTAG Reset (active-low output signal that resets the target). Output from SAM-ICE™ to the Reset signal on the target JTAG port. This pin is normally pulled HIGH on the target to avoid unintentional resets when there is no connection.

5. DC Input connector, J8.

Table 3-6. DC Input Connector, J8

Pin	Signal Name	Description
1	DC_IN	DC Input voltage (6 - 30V)
2	GND	Ground

.....continued		
Pin	**Signal Name**	**Description**
3	-	-

3.2.2.2 Jumper Configurations

The following table describes the functionality of the jumpers.

Table 3-7. Jumper Configuration

Jumper	Label	Default Setting	Function
J3	ERASE	Open	SAMG55J19 Flash memory code erase (closed = erase).
J2	PROG	Open	SAMG55J19 Flash memory upgrade (closed = programming).

Note: Pitch jumpers are 1.27 mm (0.050").

3.2.2.3 Test Points

Some test points (probes and pads) have been placed on the PL360G55CF-EK board for the verification of the main signals.

Table 3-8. Test Point Probes

Reference	Function
TP13	12V
TP18	3V3
TP23	GND
TP109	PLC signal

Table 3-9. Test Point Pads

Reference	Function	Reference	Function
TP1	PL360 pin PA6	TP19	3V3
TP2	PL360 pin PA7	TP20	Ground
TP3	PL360 pin PA8	TP21	Ground
TP4	PL360 pin PA9	TP22	Ground
TP5	PL360 pin PA0	TP100	P0 Channel MOSFET (CEN-A)
TP6	PL360 pin PA3	TP101	Line
TP7	PROG	TP103	N0 Channel MOSFET (CEN-A)
TP9	ERASE	TP104	Neutral
TP10	SAMG55J19 pin PA12, LED D1	TP105	PL360 pin TXRX0
TP11	SAMG55J19 pin PA15, LED D2	TP106	Zero cross signal, VZC
TP12	NRST	TP107	P1 Channel MOSFET (FCC)

.....continued			
Reference	**Function**	**Reference**	**Function**
TP14	12V	TP108	N1 Channel MOSFET (FCC)
TP15	DC_IN	TP110	PLC RX
TP16	VDC	TP111	PL360 pin TXRX1
TP17	Ground	-	-

3.3 Hardware Description – System

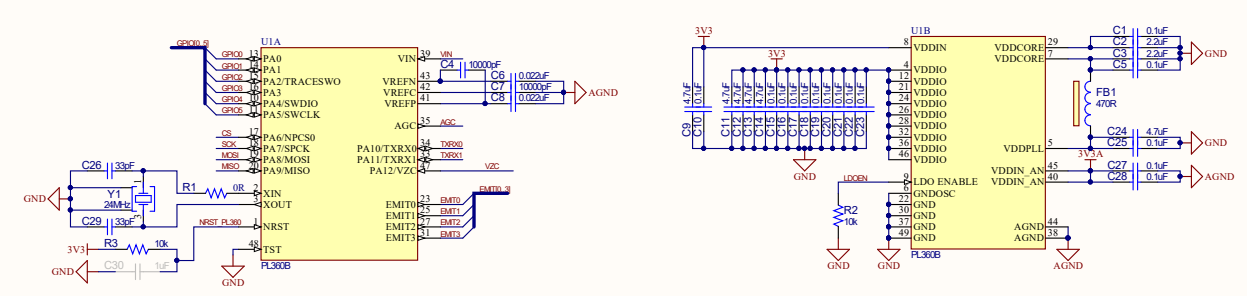
3.3.1 PL360

The PL360G55CF-EK board is equipped with a PL360 device in 48-pin QFN (0.4 mm pitch package).

PL360 is a multi-protocol (G3-PLC, PRIME 1.3 and PRIME 1.4) modem for Power Line Communication implementing a very flexible architecture, which allows implementation of standard and customized PLC solutions.

PL360 transceiver has been conceived to be easily managed by an external Microchip MCU through a 4-line standard Serial Peripheral Interface (SPI) accessing the internal peripheral registers. Two additional signals are used by the host microcontroller to control the PL360 transceiver: LDO enable and NRST.

Figure 3-4. PL360 PLC Modem

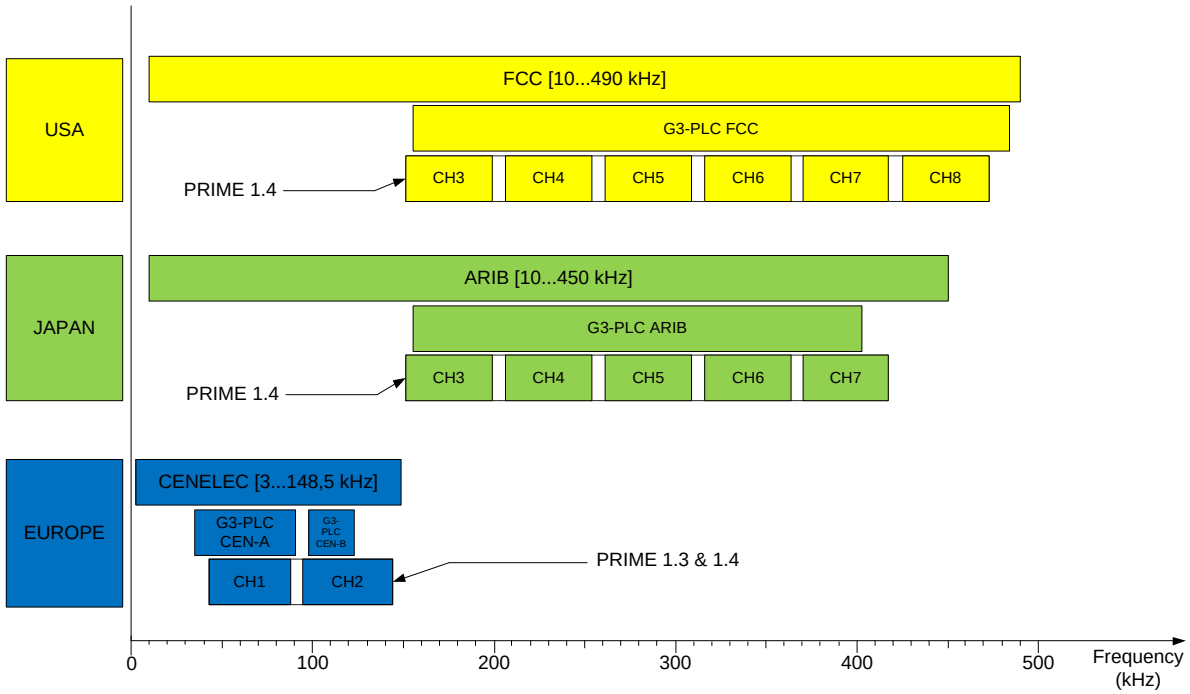


Important: Some GPIOs of PL360 device must be connected to the external MCU for the right implementation of the firmware of the PLC standard. G3-PLC requires a GPIO for an external interrupt line (EINT) and PRIME requires two GPIOs for an external interrupt and carrier detect indication lines (EINT and CD). Please check this point with the firmware user guide.

Remember: The PL360 control lines from MCU perspective (SPI lines, EINT in GPIO3 and CD in GPIO0) are accessible via test points.

Microchip provides highly efficient, reduced BOM reference designs for different coupling options, targeting common configurations in all PLC bands (<500 kHz) complying with existing regulations.

Figure 3-5. PLC Bands Supported by PL360



For a further description of the PL360 device, please refer to the PL360 datasheet.

3.3.2 SAMG55J19

The PL360G55CF-EK board is equipped with a SAMG55J19 device in 64-pin QFN. The SAM G55 devices are general-purpose low-power microcontrollers which offer high performance, processing power and small package options combined with a rich and flexible peripheral set.

The Microchip's SAM G55 embeds a Cortex-M4 CPU with an FPU (floating point unit). This ensures maximum throughput. This is very important as it allows minimization of the active power consumption and getting to sleep faster in order to reduce the overall power consumption. Additionally, the device has 30 DMA channels, which gives extremely high throughput.

The SAMG55J19 operates at a maximum speed of 120 MHz and features 512 Kbytes of Flash and up to 176 Kbytes of SRAM. The peripheral set includes eight flexible communication units comprising of USARTs, SPIs and I^2C-bus interfaces (TWIs),two three-channel general-purpose 16-bit timers, two I^2S controllers, one-channel pulse density modulation, one 8-channel 12-bit ADC, one Real-Time Timer (RTT) and one Real-Time Clock (RTC), both located in the ultra-low power backup area.

Figure 3-6. SAMG55 Microcontroller

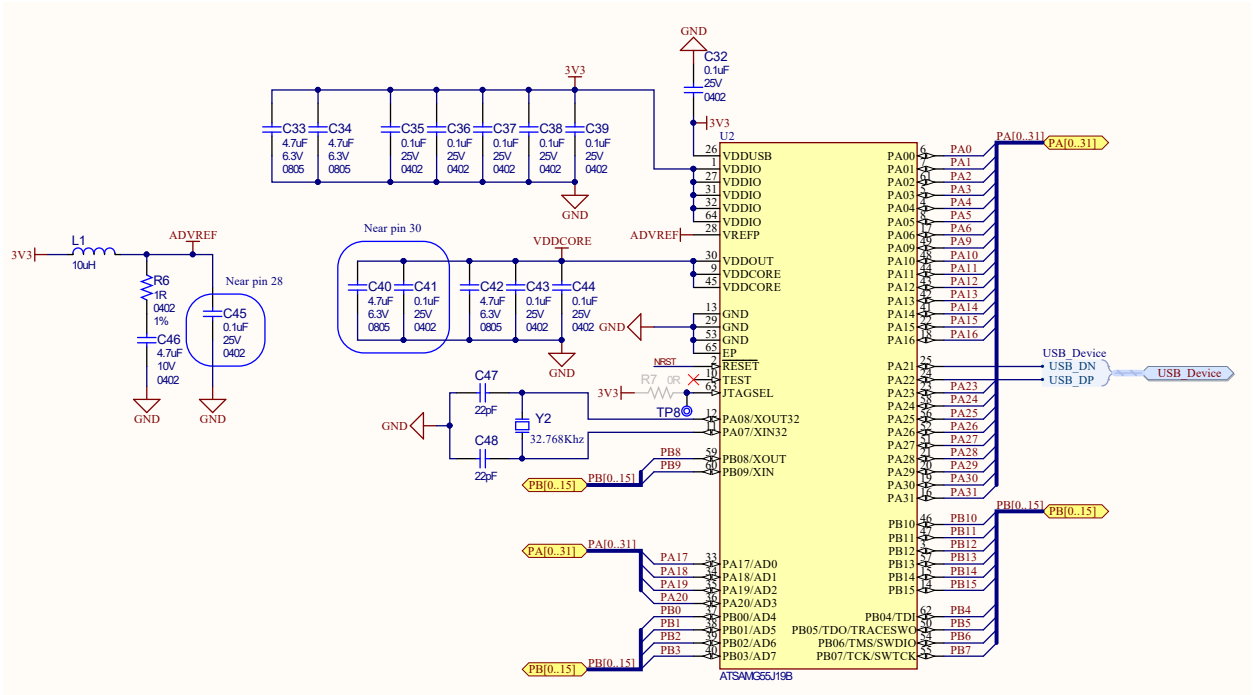


Table 3-10 and Table 3-11 summarize the functionality of each input/output line of the SAMG55J19 microcontroller in the PL360G55CF-EK board.

Table 3-10. Pinout of SAMG55J19 PortA in PL360G55CF-EK Board

I/O LINE	Function	I/O LINE	Function
PA0	PL360 GPIO3	PA16	PL360 GPIO4
PA1	PL360 GPIO2	PA17	AD0 (mikroBUS)
PA2	Not Connected	PA18	PROG
PA3	PL360 MOSI	PA19	Voltage Monitor
PA4	PL360 MISO	PA20	Not Connected
PA5	PL360 GPIO1	PA21	USB Device Diff Negative
PA6	PL360 GPIO5	PA22	USB Device Diff Positive
PA7	XIN32	PA23	TIOA1 (mikroBUS)
PA8	XOUT32	PA24	Not Connected
PA9	SPI0 MISO (mikroBUS)	PA25	SPI0 CS0 (mikroBUS)
PA10	SPI0 MOSI (mikroBUS)	PA26	Not Connected
PA11	USB Detect	PA27	Not Connected
PA12	User LED0	PA28	Not Connected
PA13	Not Connected	PA29	PL360 NRST

.....continued			
I/O LINE	**Function**	**I/O LINE**	**Function**
PA14	WKUP8 (mikroBUS)	PA30	PL360 LDO_EN
PA15	User LED1	PA31	PL360 GPIO0

Table 3-11. Pinout of SAMG55J19 PortB in PL360G55CF-EK Board

I/O LINE	Function	I/O LINE	Function
PB0	SPI0 CLK (mikroBUS)	PB8	Not Connected
PB1	Not Connected	PB9	Not Connected
PB2	TWCK1 (mikroBUS)	PB10	TXD4 (mikroBUS)
PB3	TWD1 (mikroBUS)	PB11	RXD4 (mikroBUS)
PB4	TDI	PB12	ERASE
PB5	TDO/TRACESWO	PB13	PL360 SCK
PB6	TMS/SDWIO	PB14	PL360 CS
PB7	TCK/SWCLK	PB15	Not Connected

The right implementation of the PLC standards require some GPIOs of the transceiver PL360 connected to the SAMG55. G3-PLC requires a GPIO for an external interrupt line (PA0 of SAMG55) and PRIME requires two GPIOs for an external interrupt and carrier detect (PA0 and PA31 of SAMG55) indication lines. Please check this point with the firmware user guide.

For a further description of the SAMG55J19 capabilities see the corresponding SAMG55 datasheet.

3.3.3 Clock Circuitry

Besides the embedded RC oscillators of SAMG55J19, two crystal oscillators are assembled on the PL360G55CF-EK board to obtain a more precise and stable system clock reference:

- A 24 MHz clock signal, Y1, generated for the PLC transceiver PL360
- A low-power 32.768 kHz crystal oscillator, Y2, for the SAMG55J19

Figure 3-7. 24 MHz Crystal Oscillator Scheme

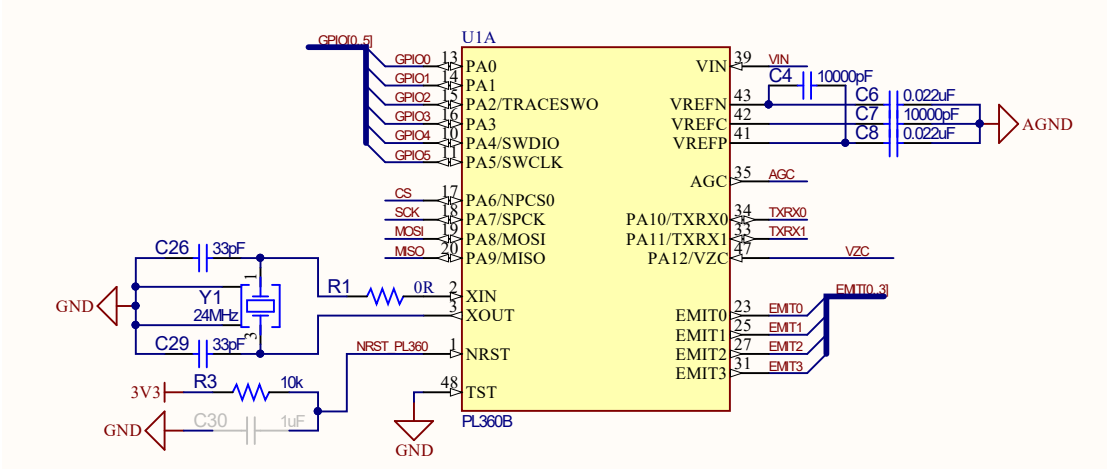
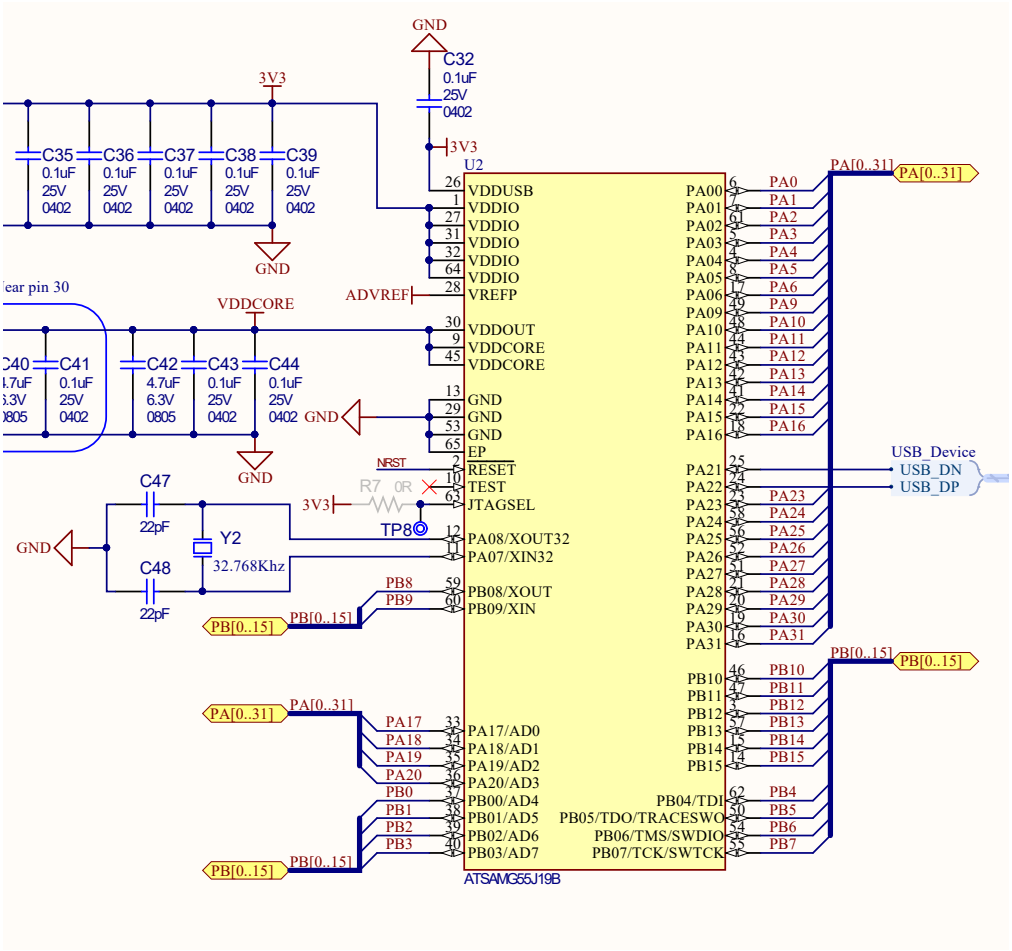


Figure 3-8. 32.768 kHz Crystal Oscillator Scheme



3.3.4 Reset

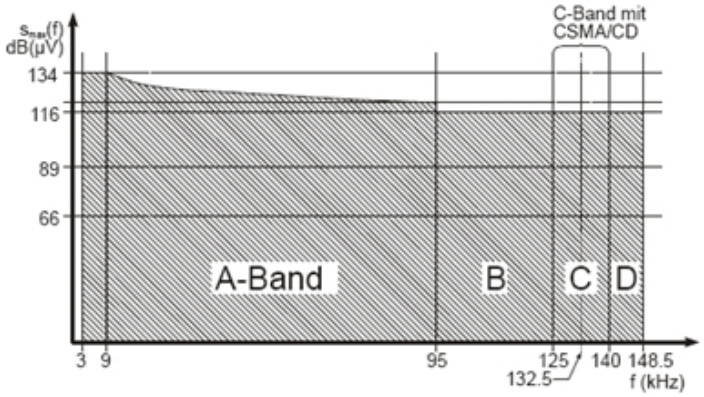
The reset sources of the PL360G55CF-EK board are:

- Power-on Reset function, embedded in the SAMG55 device.
- Push button reset. Both devices, SAMG55J19 and PL360, have a NRST pin: “NRST” for SAMG55J19 and “NRST_360” for PL360. The user can manually reset the SAMG55J19, which manages the PL360 reset, by using the push button SW1. See section 3.4.2.2 Push Buttons.
- JTAG reset from an in-circuit emulator.

3.3.5 PLC Coupling Circuitry Description

The European regulations concerning Power Line Communications are described in CENELEC standard EN 50065. This standard applies to electrical equipment using signals in the frequency range 3 kHz to 148,5 kHz to transmit information on low voltage electrical systems, either on the public supply system or within installations in consumers' premises. The following figure shows the different frequency bands allocated to the different applications.

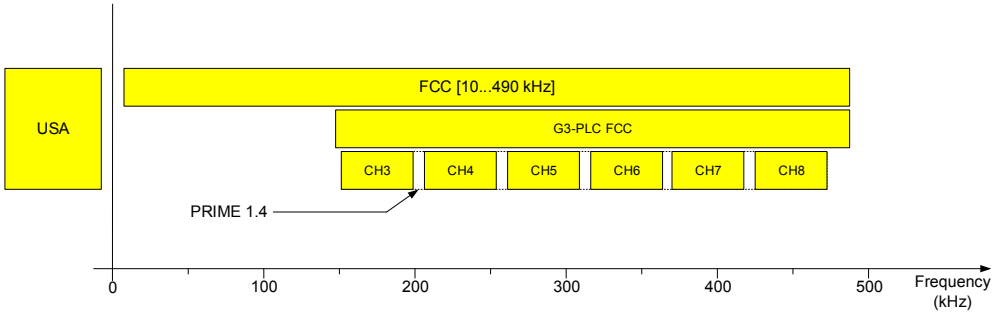
Figure 3-9. CENELEC Frequency Bands



FCC section 15 defined 10-490 kHz frequency band for PLC in North America and Canada. The FCC band (10-490 kHz), is not yet regulated in Europe.

PLC COUP011 is designed to communicate in FCC band, from 151 to 471 kHz.

Figure 3-10. FCC Frequency Bands



The PL360G55CF-EK evaluation board communicates in the CENELEC A-Band and FCC Band frequencies. The use of frequencies in these bands shall be restricted to consumer use; for example, for end-user applications such as industrial applications.

Microchip has designed four coupling reference designs for this frequency range with variations in the BOM cost and the communication performance. Table 3-12 summarizes the main features of the available designs.

Table 3-12. Characteristics of PLCOUPxxx Boards for CENELEC A-Band and FCC Band

Board Name	Description	Frequency Band (kHz)	Branch	Electrical Isolation	PRIME Channel	G3-PLC Band	Applicable Regulation
PLCOUP007-ISO	G3-PLC CENELEC A & PRIME Channel 1 compliant	35 - 91	Single	Yes	1	G3 CENELEC A	CENELEC EN 50065
PLCOUP008-NONISO	Non-Isolated G3-PLC CENELEC A & PRIME Channel 1 compliant	35 - 91	Single	No	1	G3 CENELEC A	CENELEC EN 50065
PLCOUP011-ISO	Dual PRIME / G3 for CENELEC A and FCC bands	35 - 91 151-472	Double	Yes	1, 3, 4, 5, 6, 7 and 8	G3 CENELEC A and FCC	CENELEC EN 50065

.....continued

Board Name	Description	Frequency Band (kHz)	Branch	Electrical Isolation	PRIME Channel	G3-PLC Band	Applicable Regulation
PLCOUP011-NONISO	Non-Isolated Dual PRIME / G3 for CENELEC A and FCC bands	35 - 91 151-472	Double	No	1, 3, 4, 5, 6, 7 and 8	G3 CENELEC A and FCC	CENELEC EN 50065

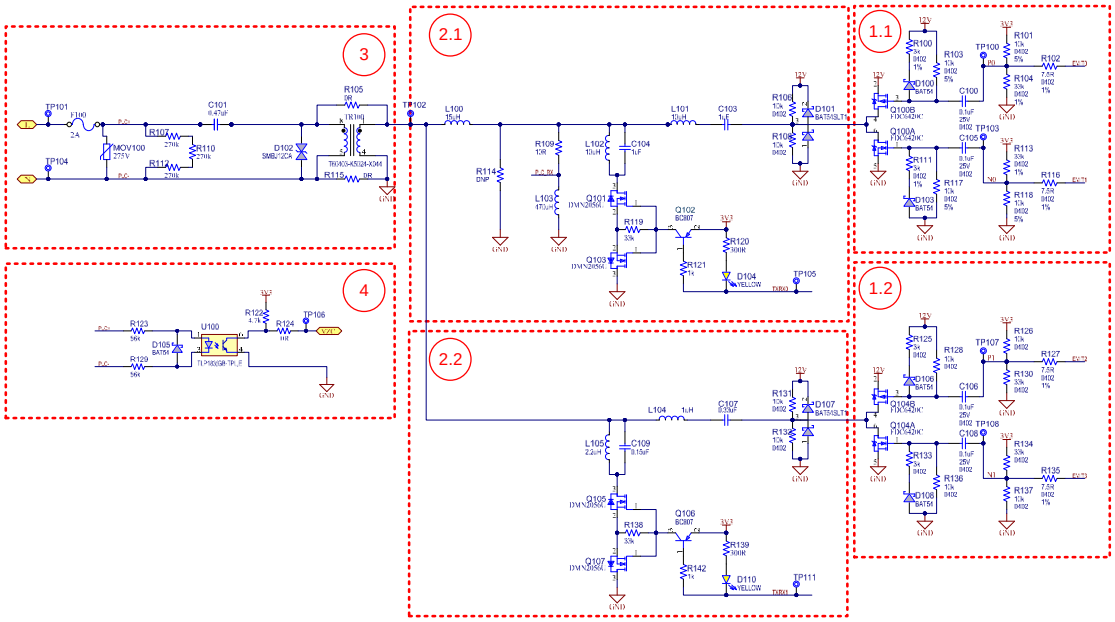
The PL360G55CF-EK board is assembled with the PLCOUP011-ISO coupling design. The goal is to provide a cost-optimized fully-featured design according to the G3-PLC and PRIME requirements. Still, the PL360G55CF-EK board is designed to allow using all the other coupling designs by changing the corresponding components and firmware configurations.

Important: Check the online resources from the Microchip website to download the proper files according to your desired CENELEC A-Band and FCC Band design.

The following figure shows the PLC Coupling assembled (PLCOUP011-ISO) which is composed of four sub-circuits:

1. Transmission Stage
   1.1. Transmission Stage for CENELEC A-Band
   1.2. Transmission Stage for FCC Band
2. Filtering Stage
   2.1. Filtering Stage for CENELEC A-Band
   2.2. Filtering Stage for FCC Band
3. Coupling Stage
4. Reception Stage

Figure 3-11. PLC Coupling Schematic on PL360G55CF-EK Board



Remember: PLC Coupling circuitry includes two yellow LEDs, D104 and D110, for visual indication of PLC frames transmission through the corresponding branch.

The following sections describe the purpose of every sub-circuit assembled in the PL360G55CF-EK board.

3.3.5.1 PLC Transmission Circuit

The transmission stage adapts the EMIT signals and amplifies them. In the PL360G55CF-EK board, see Figure 3-11, it is a single branch composed of:

- Driver: It adapts the EMIT signals to either control the amplifier or to be filtered by the next stage
- Amplifier: A Class-D amplifier generating a square waveform from 0 to 12V
- Bias and protection: It provides a DC component and provides protection from received disturbances

The transmission stage is followed by a filtering stage.

3.3.5.2 PLC Filtering Circuit

The in-band flat response filtering stage reduces spurious emission to the limits set by the corresponding regulation and blocks potential interferences from other transmission channels without distorting the injected signal.

The filtering stage used in PL360G55CF-EK, see Figure 3-11, has three aims:

- Band-pass filtering of high frequency components of the square waveform generated by the transmission stage
- Adapt Input/Output impedance for optimal reception/transmission. This is controlled by TXRX0 and TXRX1 signal
- A band-pass filtering for received signals

3.3.5.3 PLC Coupling Circuit

PLC coupling circuit connects the PLC signal directly to the mains grid or even to DC power rails without requiring any hardware adaptation. The main purpose of the circuit is to block the mains voltage of the grid to/from which the signal is injected/received. This is carried out in PL360G55CF-EK, see Figure 3-11, by a high voltage capacitor, C101. Resistors R107, R110 and R112 allow the high voltage capacitor to discharge after disconnection from mains.

⚠ CAUTION PLC coupling components are designed for a maximum voltage of 230 V_{AC} or 200 V_{DC}.

The TR100 transformer (with turn ratio 1:1) provides galvanic isolation from mains. A non-isolated version could easily be implemented removing TR100, soldering R105 and R115 resistors and updating the value of L103 and R109 according to the PLCOUP011-NONISO design.

MOV100 varistor, F100 fuse and D102 TVS diode protect the coupling circuit from overvoltages and high transient voltages (surges and spikes) from mains.

3.3.5.4 PLC Reception Circuit

The PLC reception circuit used in PL360G55CF-EK, see Figure 3-11, is the reference design for the reception stage and it is composed of:

- Single-pole low pass filter, R140 and C114
- Automatic Gain Control (AGC) circuit. A resistor, R143, is used to attenuate the incoming PLC signal in case its amplitude is high enough to exceed the input dynamic range of the embedded ADC

- A resistor, R141, for impedance matching
- DC decoupling capacitor, C113

3.3.6 Power Supply System

The PL360G55CF-EK board can be powered by several power sources. Supply the board via:

- the DC jack 2.0 mm connector J8, *DC_IN*, with a DC source from 6V to 30V (±5%) and 4.2W
- USB connector (+5V), J4
- the power supply pin (+5V) of mikroBUS standard

Table 3-13. Power Sources for PL360G55CF-EK Board

Power Input	Voltage Requirements	Power Requirements	Connector Marking
DC Jack connector	+6V to +30V (±5%)	4.2W	DC_IN
Target USB	+5V	According to USB specifications	USB
mikroBUS Power pin (+5V)	+5V	According to mainboard specifications	+5V

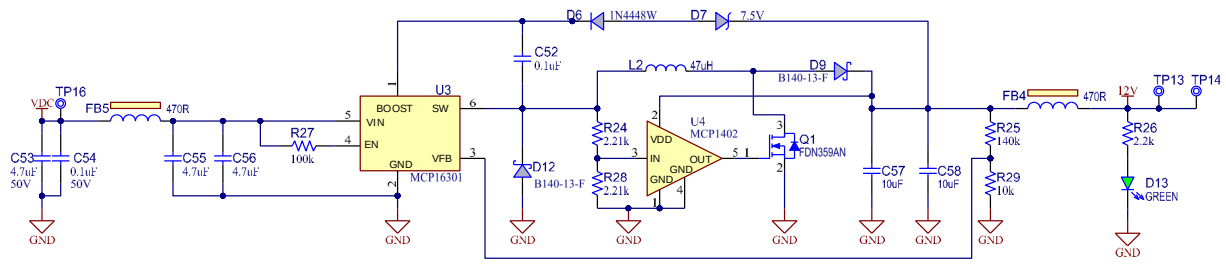
The PL360G55CF-EK board has two voltage rails:

- +3.3V for the digital part of the PLC modem, PL360, and the SAMG55J19 MCU
- +12V to power the class-D amplifier of the PLC coupling circuit

⚠ CAUTION Note that the PL360G55CF-EK board does not provide a power supply protection circuit; only a TVS diode is used to protect from voltage spikes at the DC rail.

The 12V voltage rail is obtained from the Microchip MC16301 buck-boost converter. For a further description about the buck-boost converter see the MCP16301 Buck-Boost Converter User's Guide. If the VDC voltage is always higher than 12V, it is possible to improve the power efficiency by transforming the converter mode from buck-boost to buck, see MCP16301 datasheet for a further explanation.

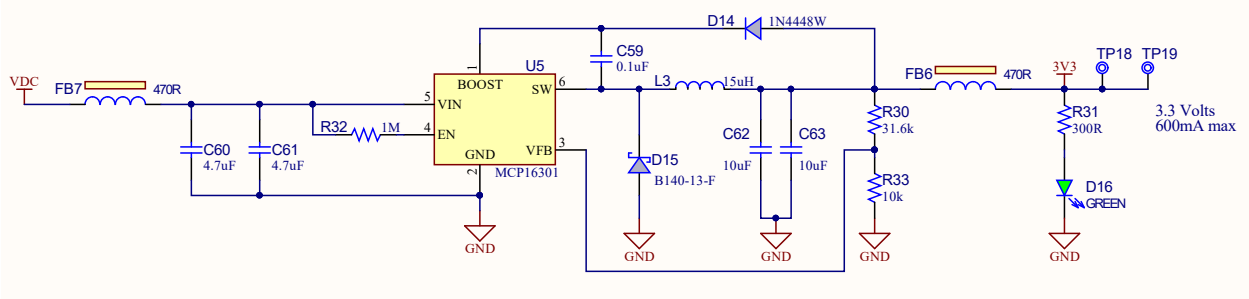
Figure 3-12. 12V Voltage Design



Restriction: Note that some power sources, such as USB port and mikroBUS rail, might have limited current capabilities and they could not supply enough current for the class-D amplifier transmitting against low impedance values. In this case, an external AC/DC power supply with enough current rating is recommended to maintain the PLC performance at its best. If using one, we recommend a module complying to national regulations or CISPR 32:2015.

Another buck converter, MC16301, is used to generate a regulated 3.3V voltage rail required by the PL360 modem and the SAMG55J19 MCU. For a further description about the buck converter see the MCP16301 Buck Converter User's Guide.

Figure 3-13. 3.3V Buck Converter Design



There are one LED and two test points on each voltage rail to check whether all power supplies are operating properly.

To avoid on board self-generated disturbances within the PLC signal band, both converters are switching at 500 kHz fixed frequency, out of the PLC band (35 to 472 kHz).

Tip: If choosing a different SMPS in the customer design, it is important to analyze its potential interference on the PLC frequency band.

Attention: To avoid noise interferences, the switching frequency of the SMPS must be out of the PLC band and preferably in frequencies above it to avoid harmonics influence. This is essential to obtain a good reception performance.

3.3.6.1 PLC Rejection Filter

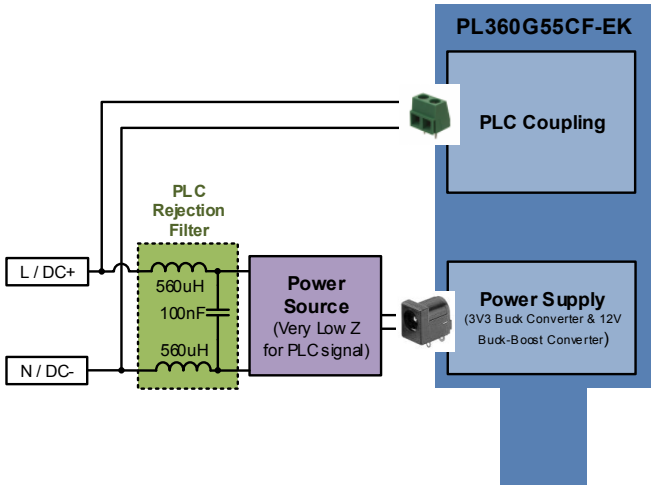
When the PLC coupling circuit is in parallel with the power supply circuit, the input impedance of the final equipment could be affected. If the requirements about total input impedance are not satisfied, an appropriate input filter is needed at the power supply input to increase the input impedance.

Apart from the input filter, it is also recommended to add a PLC rejection filter to avoid the absorption of the PLC signals by the power supply circuit. This filter also increases the input impedance, so it helps to achieve the requisites about input impedance.

Notice: The PL360G55CF-EK board has PLC coupling and power supply circuits separated, so the PLC rejection filter is not included. A PLC rejection filter is needed in case of low input impedance after connecting in the same point the PLC Coupling connector J1 and the power source of the board.

An example of PLC rejection filter is composed of two inductance in-series (L = 560 µH) and a capacitor in-parallel (C = 100 nF) at the power supply input as shown in the following picture.

Figure 3-14. PLC Rejection Filter Example



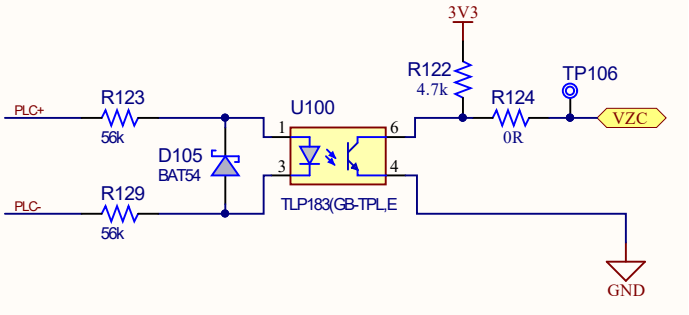
3.3.7 Zero-Crossing Detector Circuit

Phase identification is an important feature of devices that are connected to Smart Grid networks, such as smart meters. A typical implementation is based on measuring the time difference between a specific PLC frame reception and the last zero crossing event of the mains single-phase to which the device is connected.

Important: The phase identification feature is mandatory for G3-PLC and PRIME1.4, but not for PRIME1.3.

Figure 3-15 shows the Zero-Crossing Detection circuit used in the PL360G55CF-EK board, which features detection of rising edges of the mains voltage. The output signal of the detection circuit “VZ CROSS” is connected to VZ pin of PL360 and a synchronization algorithm is applied in order to obtain an accurate measurement of the time between PLC frame reception and zero crossing events.

Figure 3-15. Zero-Crossing Detection Circuit



Notice: Designs that do not require galvanic isolation can use a simpler Zero-Crossing Detector circuit, such as a Zener diode, instead of the previous circuit.

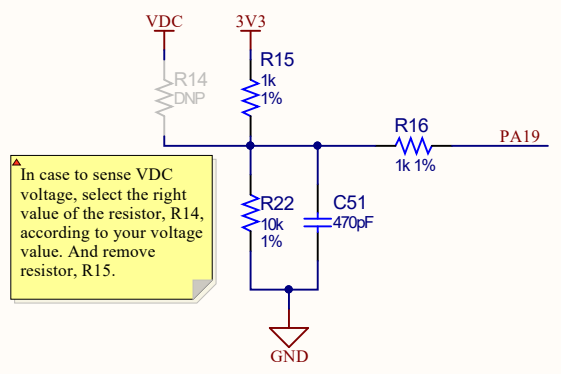
3.4 Hardware Description – MCU Peripherals

3.4.1 Voltage Monitor

The input pin PA19 of SAMG55J19 is used to monitor the 3.3V voltage rail through external voltage divisors. It can be used to monitor the VDC voltage rail mounting R14 and removing R15 resistor.

Important: The R14 resistor value depends on the voltage value of the input source power.

Figure 3-16. Voltage Monitor Circuit



The voltage monitor circuit allows the implementation of multiple applications such as:

- Detection of fault conditions
- Detection of Low-Power mode entering conditions
- Detection of wake-up situations

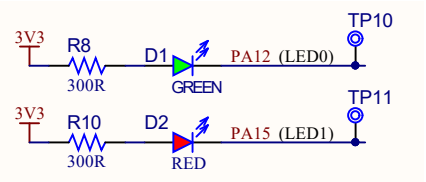
3.4.2 LEDs and Buttons

The PL360G55CF-EK board is equipped with several LEDs and one user push button.

3.4.2.1 User LEDs

The PL360G55CF-EK board includes two general purpose LEDs, one green connected to PA12 (LED0) and one red connected to PA15 (LED1).

Figure 3-17. User LEDs

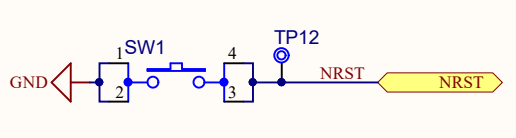


In addition, this board disposes of two green LEDs, D13 and D16, connected to 12V and 3.3V supplies for visual status of these voltages, and two yellow LEDs, D104 and D110, for PLC transmissions indication.

3.4.2.2 Push Buttons

The PL360G55CF-EK board is equipped with a momentary push button switch mounted directly to the board. When the button is pressed it will drive the SAMG55 reset line, NRST, to GND. And PA29 will drive the PL360 reset line, NRST_PL360, to GND.

Figure 3-18. Reset Button



3.4.3 Chip Programming

The 1x2 pin-header J2 marked as “PROG” is connected to the SAMG55J19 chip input pin (PA18) and GND. This header can be used to upgrade (using a bootloader binary file of the SAMG55J19) the PLC stack running on the SAMG55 by the USB/serial port. See *Smart Energy: Serial Bootloader User Guide* for more information.

3.4.4 Chip Erase

The 1x2 pin-header J3 marked as “ERASE” is connected to the SAMG55J19 chip erase pin (PB12) and 3.3V. This header can be used to re-initialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1) by placing a jumper on the header and pressing the reset switch button. Shortly after, the erase jumper should be removed and the PCBA must be turned off and turned on by disconnecting and connecting it again to the selected power supply. See section “ERASE Pin” in the *SAMG55J19* datasheet for more information.

Notice: Take into account that when Flash is erased, the bootloader application will also be removed; therefore the SAMG55J19 device will be programmable only via JTAG.

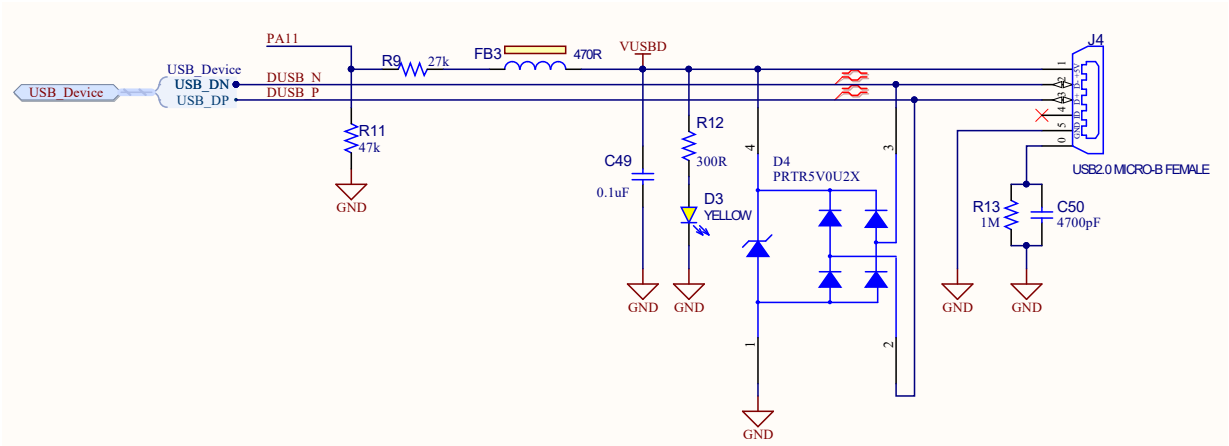
3.5 Hardware Description – MCU Interface Ports

3.5.1 USB Device Port

The USB Device Port (UDP) is compliant with the Universal Serial Bus (USB) 2.0 full-speed device specification. There is a USB available on the PL360G55CF-EK board that can act as both host and device. It has a Micro-B female USB connector with the silk screen USB.

The I/O line PA11 allows the application to check if VUSBD is available.

Figure 3-19. USB Circuit



Important: Check online resources from the Microchip website to download the drivers according to your Operating System.

⚠ CAUTION The USB connector is not isolated from mains. Please make use of proper isolation (i.e.: USB isolator device) if using this connector when the board is not galvanically isolated (using a PLC Coupling design which it is not isolated from mains). Take into account the possible noise interference that these isolators could be adding to the PLC network. For instance, you can use the UH401.

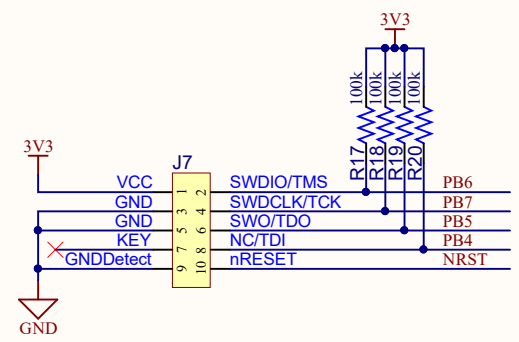
3.5.2 SAMG55J SWD/JTAG Port

The PL360G55CF-EK board includes an SWD (Serial Wire Debug) / JTAG interface port to provide debug level access to the system-on-chip. It also embeds a serial wire trace. This connector provides the required interface for in-circuit emulators, like the Atmel-ICE or SAM-ICE. The SW-DP/JTAG port is a 10-pin, dual row, 0.1-inch male connector (J7). When using the SAM-ICE, a JTAG adapter for 20 to 10 pins is necessary, e.g., this one.

Important: Note that the PL360G55CF-EK kit does not include either SAM-ICE or Atmel-ICE JTAG emulators.

Please refer to the SAMG55 datasheet for further description of the JTAG debug port.

Figure 3-20. JTAG/SWD Interface Schematic



⚠ CAUTION The USB JTAG/SWD connector is not isolated from mains. Please make use of proper isolation (i.e.: USB isolator device) if using this connector when the board is not galvanically isolated (using a PLC Coupling design which it is not isolated from mains). Take into account the possible noise interference that these isolators could be adding to the PLC network. For instance, you can use the UH401.

3.5.3 mikroBUS Connector

The PL360G55CF-EK board incorporates mikroBUS add-on connectors (J5 and J6) to integrate the board itself as a module which is able to interface with other microcontrollers or microprocessors (main board).

The mikroBUS standard specifies the size and shape of the add-on boards, but because of special constraints, the board exceeds those limits although keeping the smallest size model S as a reference for the plug-in area.

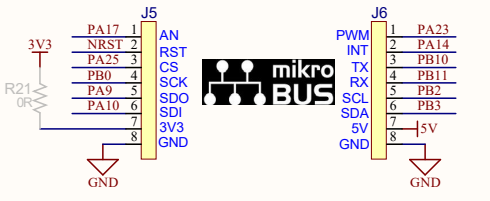
The PL360G55CF-EK board is designed to operate only from the +5V power supply rail of the mikroBUS socket. Therefore, +3.3V power supply pin is not connected.

Important: By default, J5 and J6 headers are not populated in the board. The 8-pin headers are included in a zip bag as kit contents.

The mikroBUS standard has a pair of 1x8 male headers with the following pinout:

- SPI
- UART
- I^2C
- PWM
- Interrupt
- Analog input
- Reset
- Chip Select
- +3.3V
- +5V
- Two GND pins

Figure 3-21. mikroBUS Connector



Notice: The mikroBUS Xplained Pro is an extension board that contains the female header to connect the mikroBUS add-on boards to the Xplained Pro MCU boards.

3.6 PL360G55CF-EK Schematics

This section contains the schematics for the PL360G55CF-EKv1 board:

- Top Level Schematic, Figure 3-22
- PL360 Schematic, Figure 3-23
- SAMG55 MCU Schematic, Figure 3-24
- Interface and Peripherals SAMG55 Schematic, Figure 3-25
- Power Supply Schematic, Figure 3-26
- PLC Coupling Schematic, Figure 3-27

Figure 3-22. Top Level Schematic

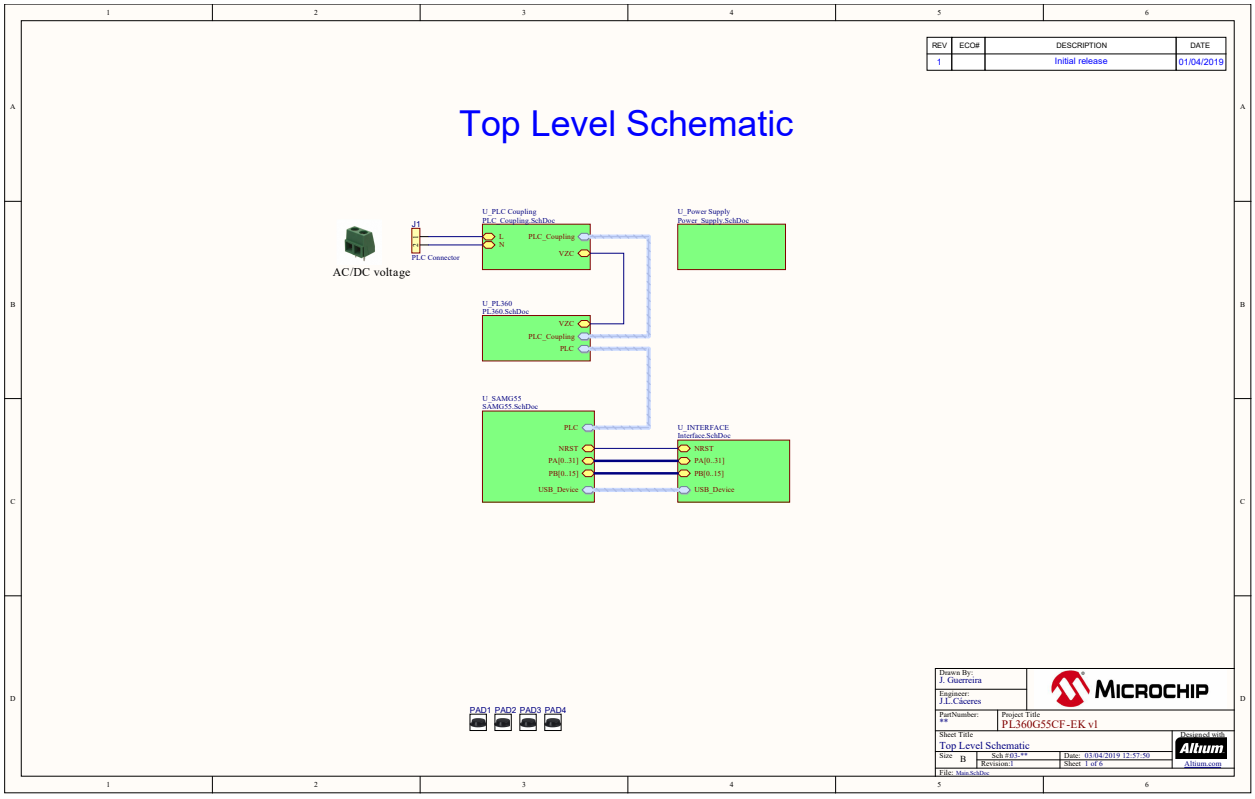


Figure 3-23. PL360 Schematic

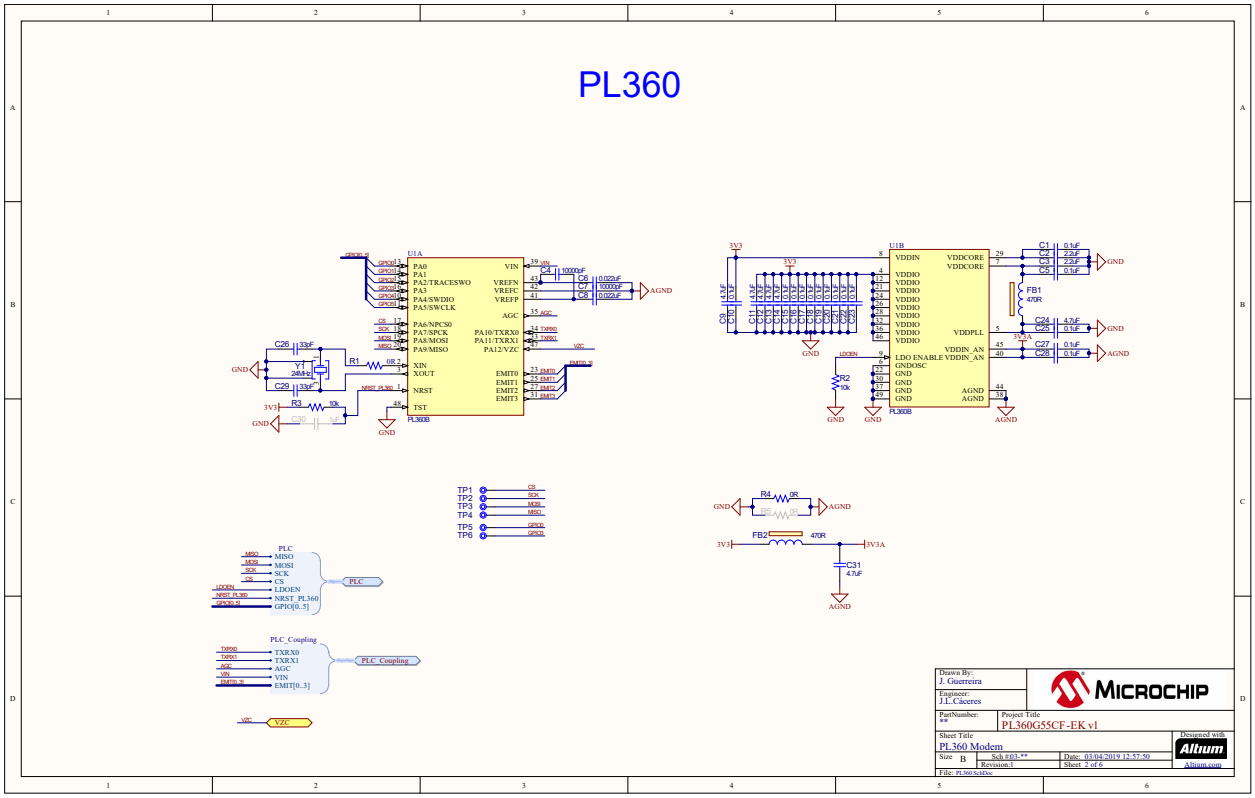


Figure 3-24. SAMG55 MCU Schematic

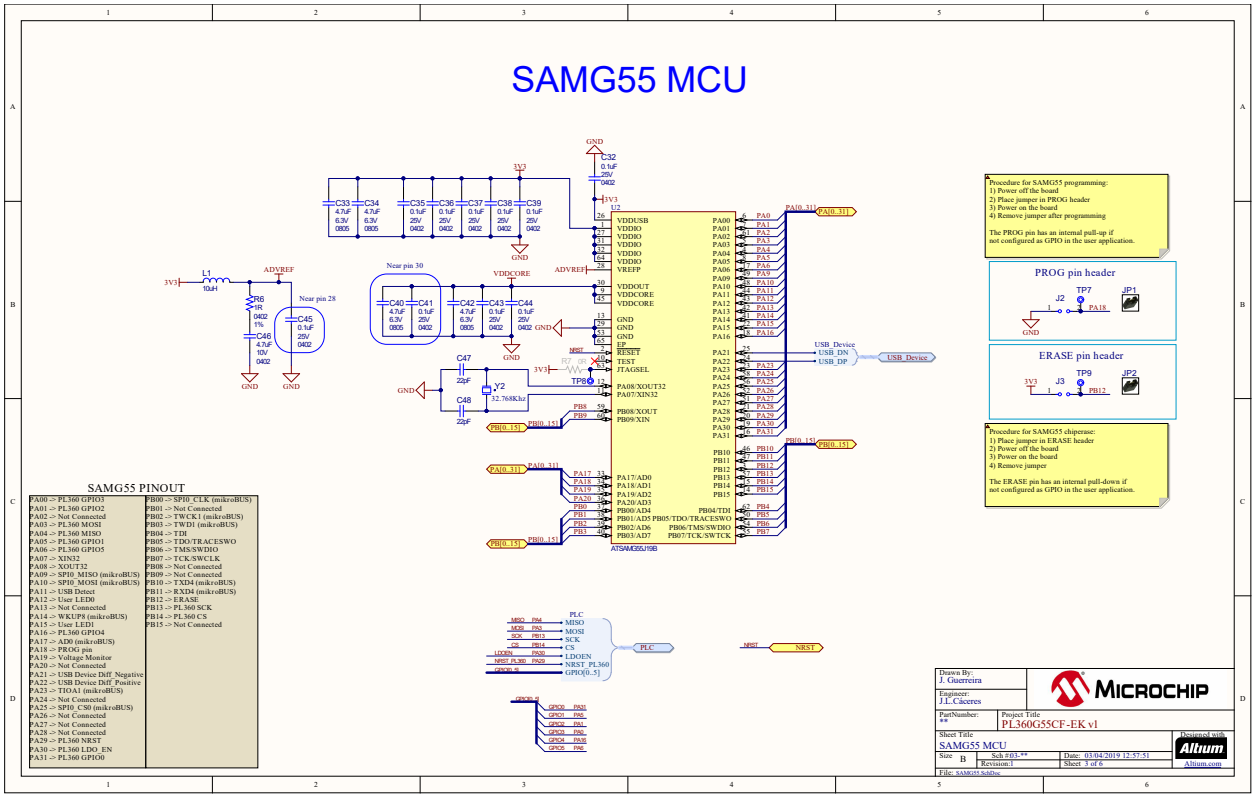


Figure 3-25. Interface and Peripherals SAMG55 Schematic

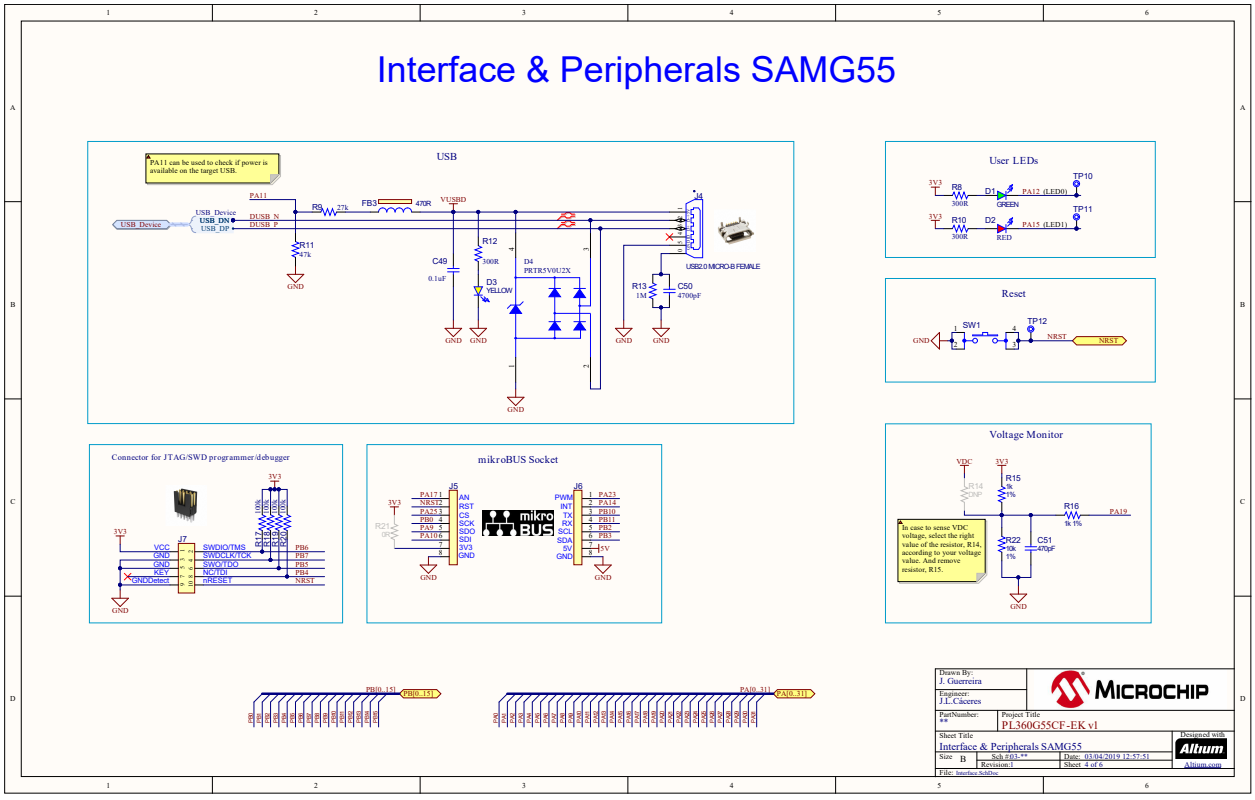


Figure 3-26. Power Supply Schematic

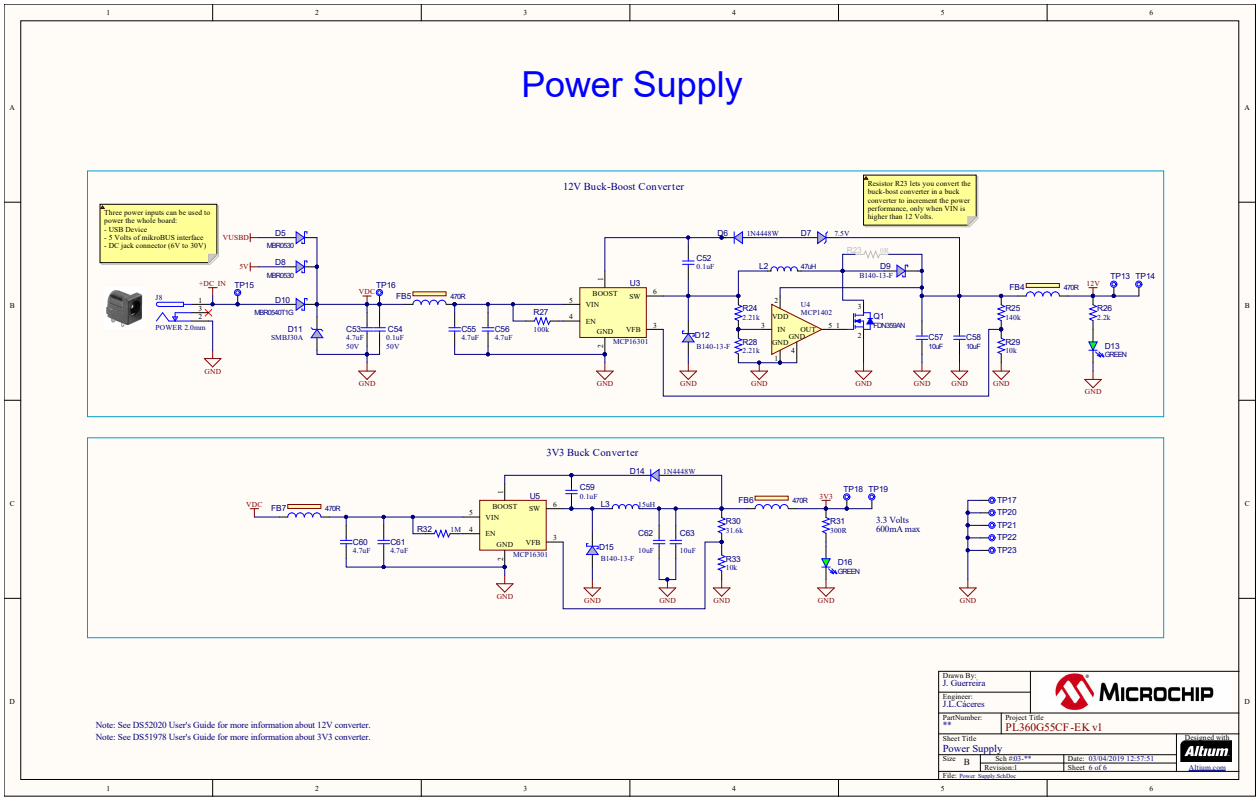
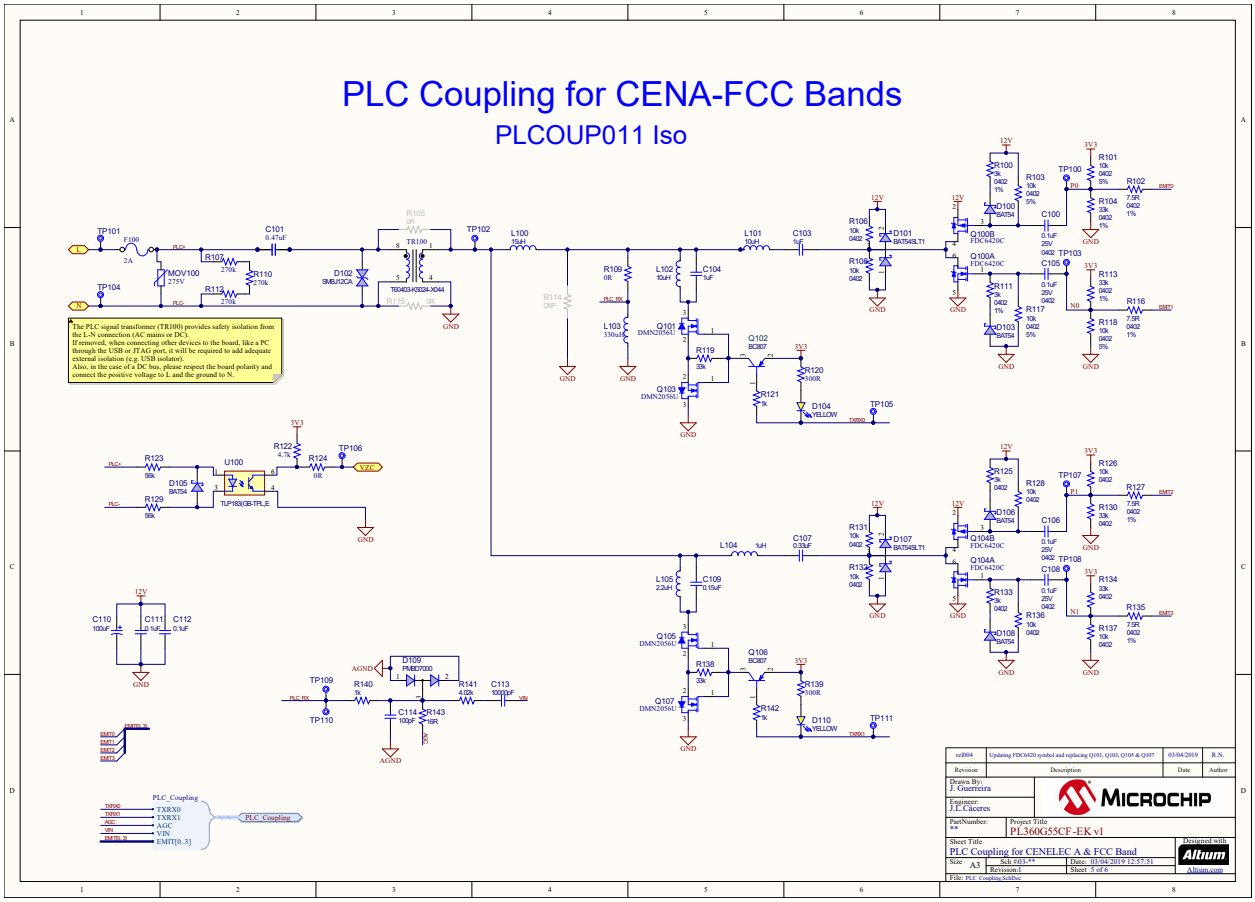


Figure 3-27. PLC Coupling Schematic



3.7 PL360G55CF-EK Layout

This section contains the layout graphics for the PL360G55CF-EKv1 board:

- Layer 1: Top Layer, Figure 3-28
- Layer 2: Mid Layer 1 (Ground), Figure 3-29
- Layer 3: Mid Layer 2 (Power Supplies), Figure 3-30
- Layer 4: Bottom Layer, Figure 3-31
- Top Components Placement, Figure 3-32
- Bottom Components Placement, Figure 3-33

Figure 3-28. PL360G55CF-EKv1 Layout: Top Layer

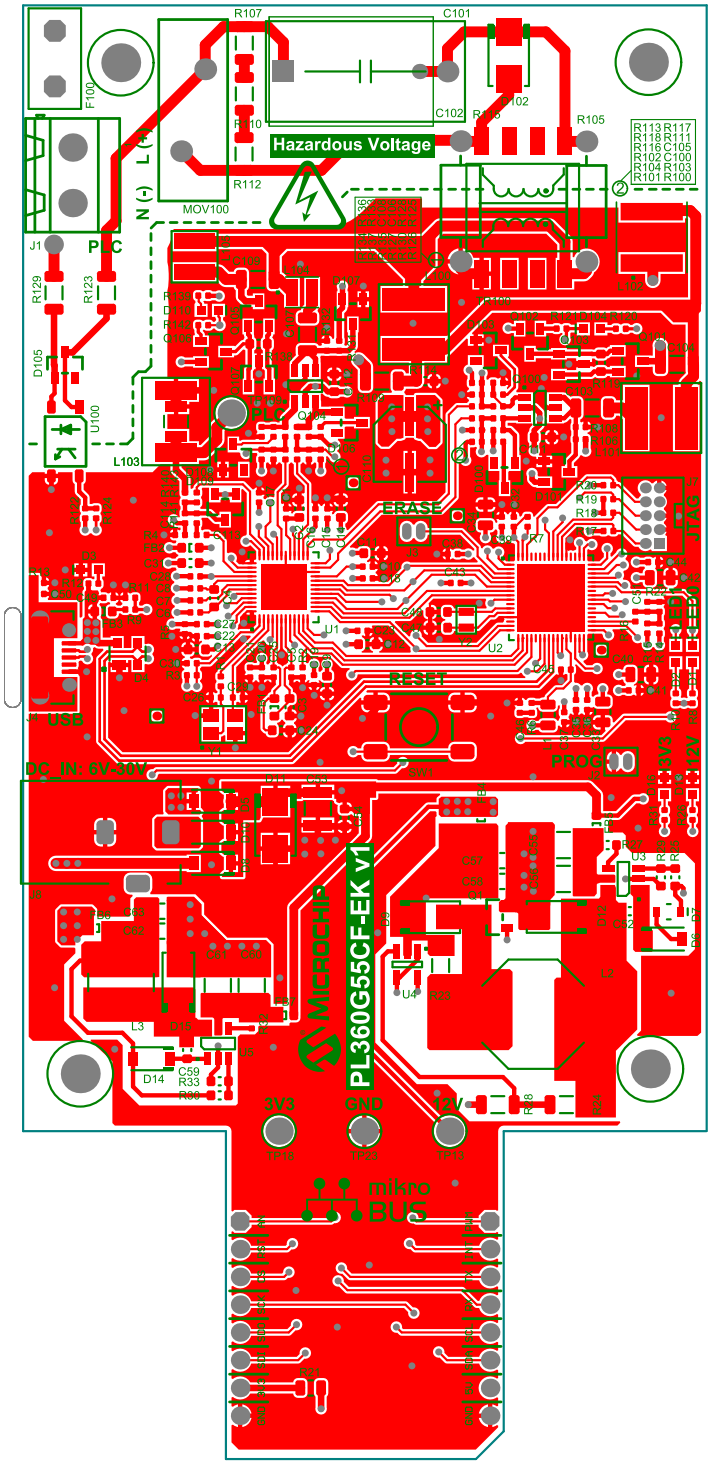


Figure 3-29. PL360G55CF-EKv1 Layout: Mid Layer 1 (Ground)

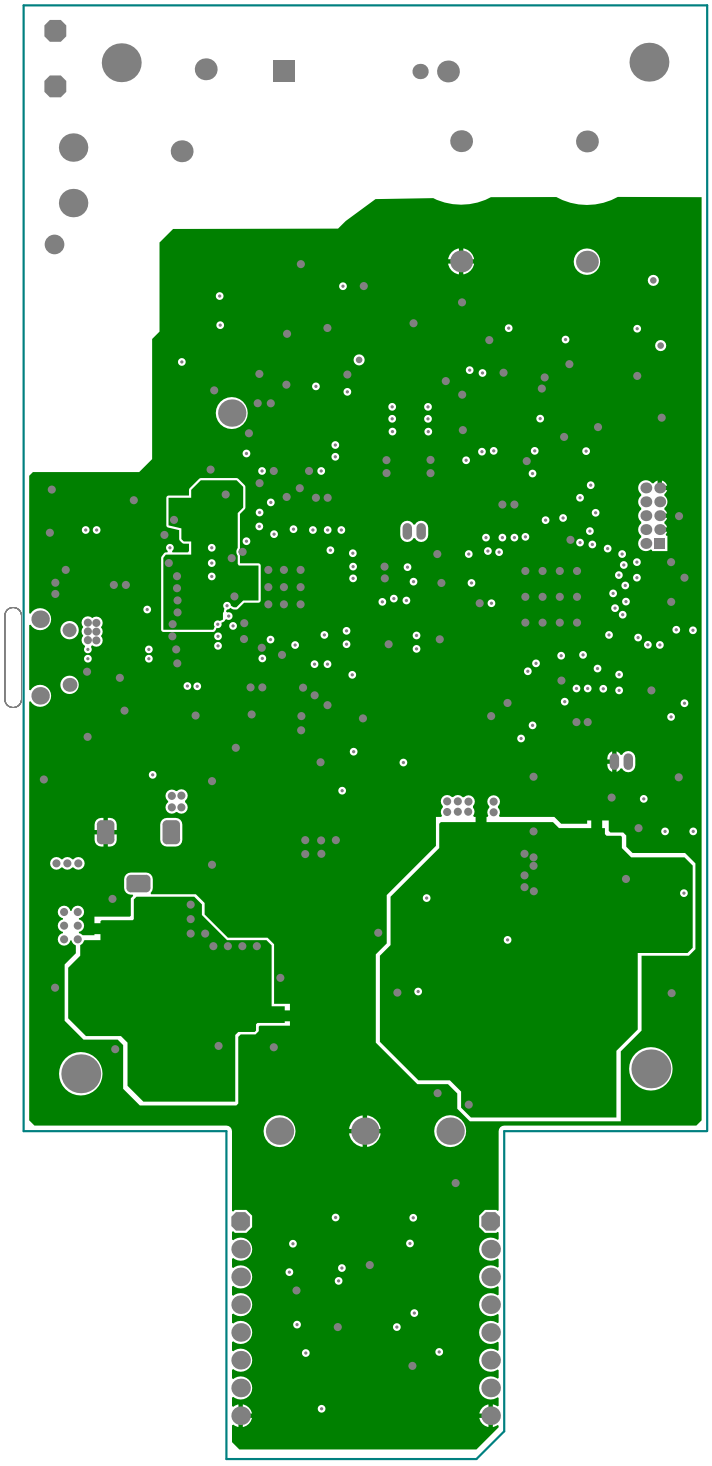


Figure 3-30. PL360G55CF-EKv1 Layout: Mid Layer 2 (Power Supplies)

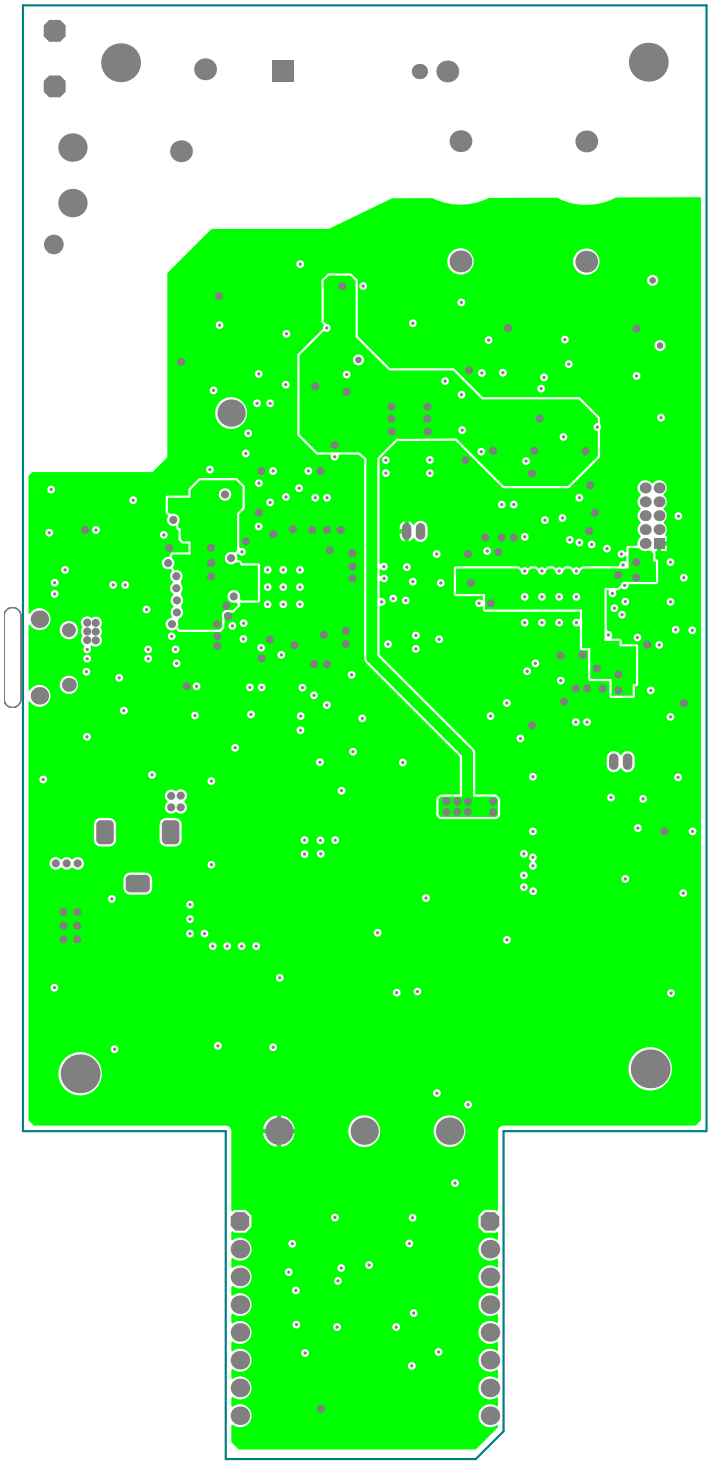


Figure 3-31. PL360G55CF-EKv1 Layout: Bottom Layer

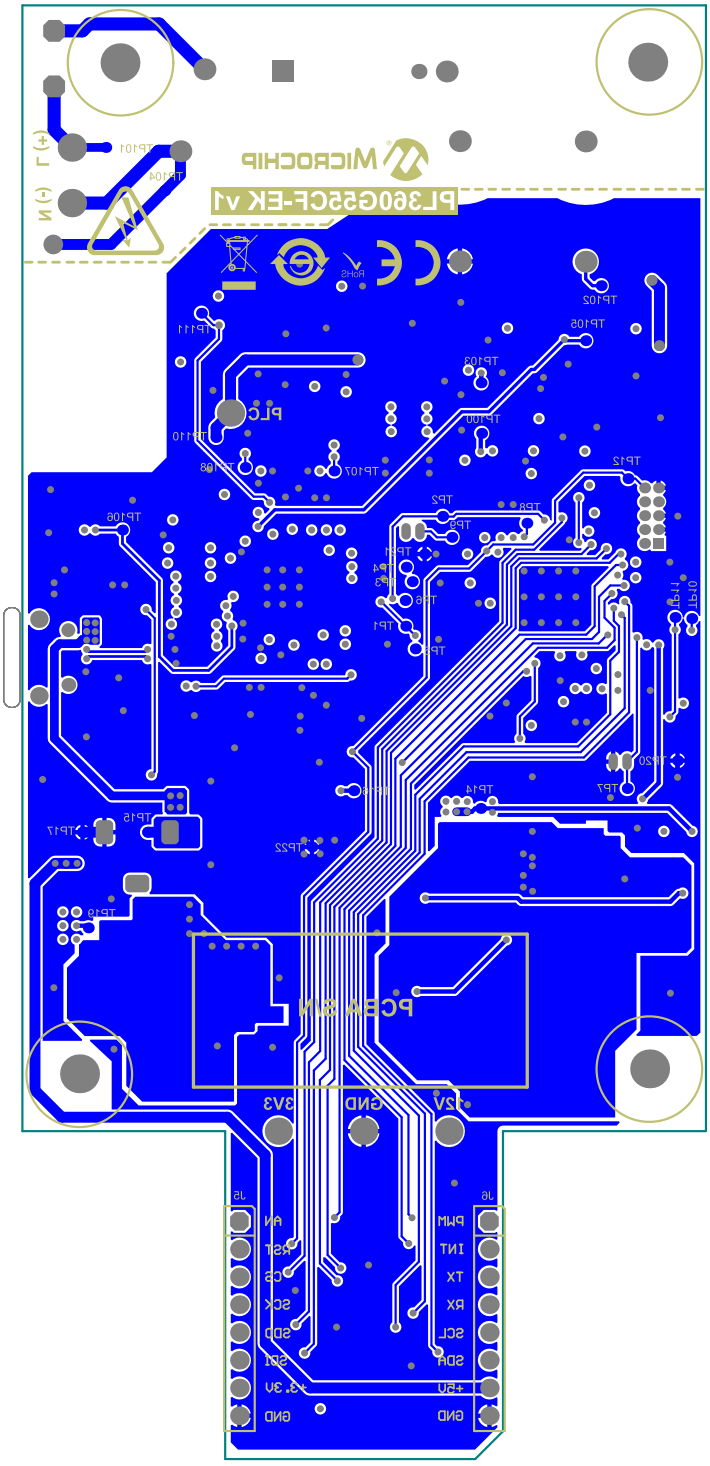


Figure 3-32. PL360G55CF-EKv1 Layout: Top Silkscreen

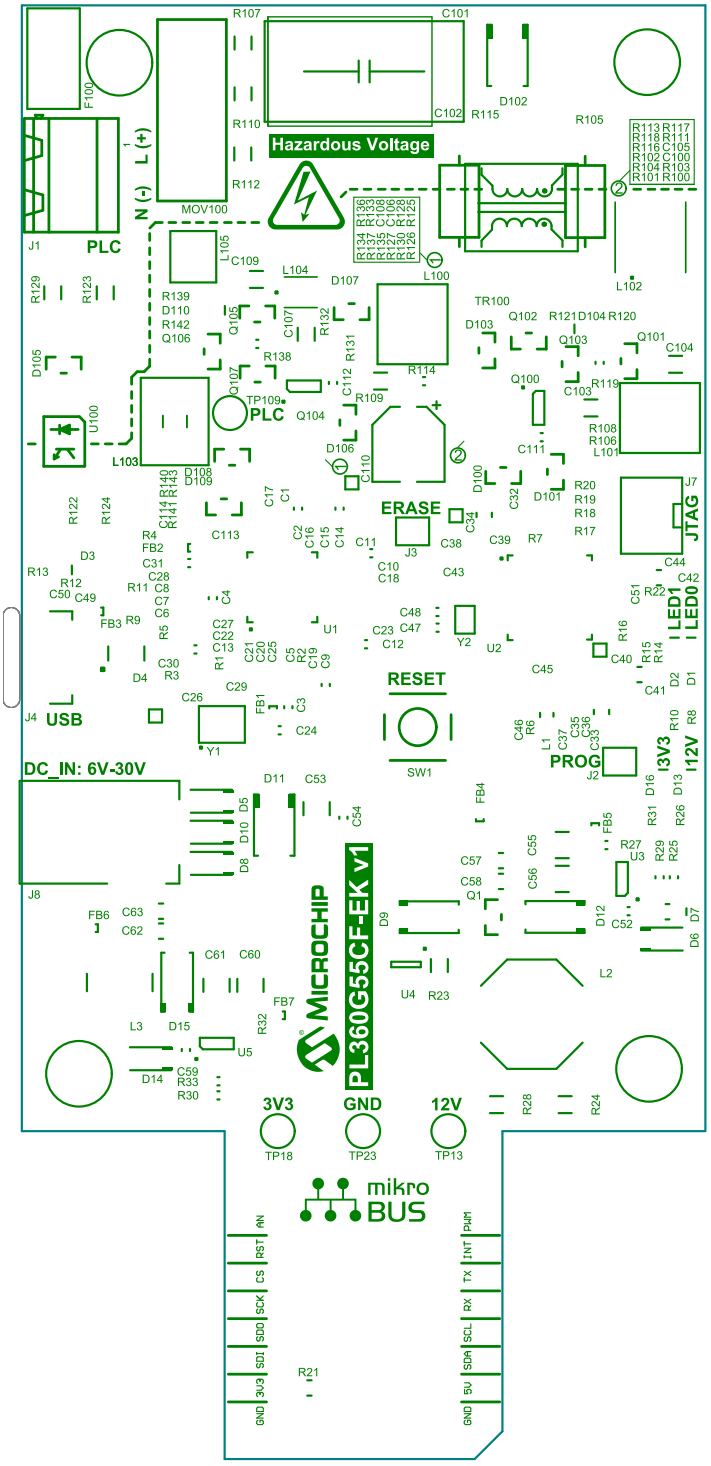
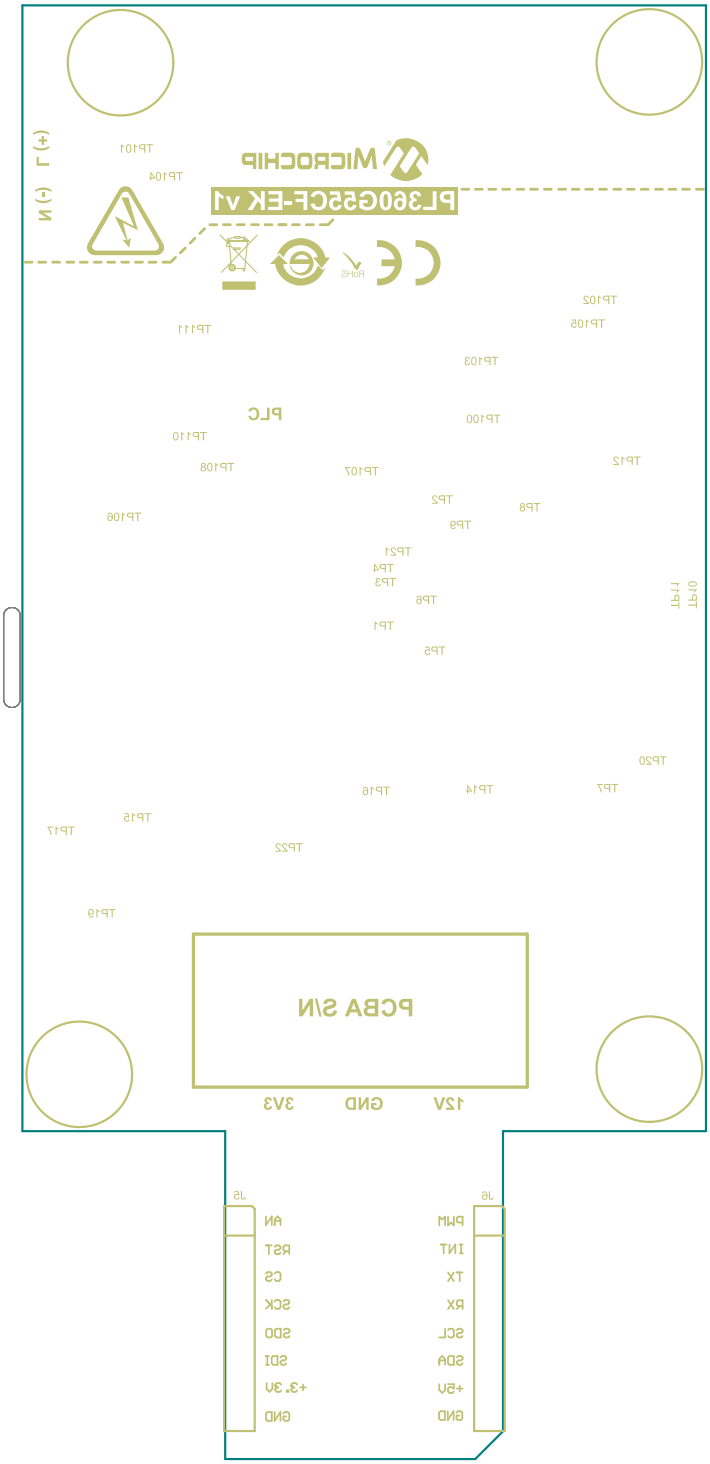


Figure 3-33. PL360G55CF-EKv1 Layout: Bottom Silkscreen



4. Compliance for Specific Standards

The development/evaluation tool is designed to be used for research and development in a laboratory environment. This development/evaluation tool is not intended to be a finished appliance, nor is it intended for incorporation into finished appliances that are made commercially available as single functional units to end users.

The PL360G55CF-EK board is a CE mark product which passes the EN 50065-1, EN 50065-2-3 and EN 50065-7 EMC standards. It also satisfies the Pb-Free and ROHS directive.

5. References

- CENELEC, EN 50065. Signaling on low-voltage electrical installations in the frequency range 3 kHz to 148.5 kHz, 2002
- PL360 Datasheet, 2018
- SAMG55 Datasheet, 2016
- MCP16301 High-Voltage Input Integrated Switch Step-Down Regulator, 2015
- MCP16301 High Voltage Buck-Boost Demo Board User's Guide, 2012
- MCP16301 High Voltage Buck Converter 600mA Demo Board User's Guide, 2011

6. Revision History

6.1 Rev A - 04/2019

Document	Initial release.

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