CSD95372AQ5M Synchronous Buck NexFET™ Power Stage

1 Features

- 60 A Continuous Operating Current Capability
- 92.4% System Efficiency at 30 A
- Ultra-Low Power Loss of 3.3 W at 30 A
- High Frequency Operation (up to 2 MHz)
- High Density - SON 5 x 6 mm Footprint
- Ultra-Low Inductance Package
- System Optimized PCB Footprint
- 3.3 V and 5 V PWM Signal Compatible
- Diode Emulation Mode with FCCM
- Analog Temperature Output
- Input Voltages up to 16 V
- Tri-State PWM Input
- Integrated Bootstrap Switch
- Optimized Dead Time for Shoot Through Protection
- RoHS Compliant – Lead-Free Terminal Plating
- Halogen Free

2 Applications

- Multiphase Synchronous Buck Converter
  - High Frequency Applications
  - High Current, Low Duty Cycle Applications
- Point-of-Load DC-DC Converters
- Memory and Graphic Cards
- Desktop and Server VR11.x and VR12.x for V-Core Synchronous Buck Converters

3 Description

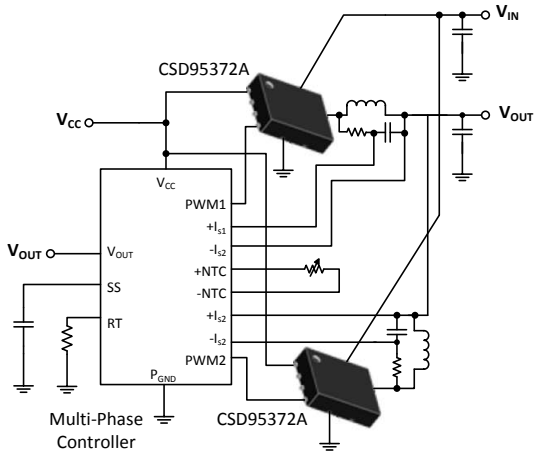
The CSD95372AQ5M NexFET™ Power Stage is a highly optimized design for use in a high power, high density Synchronous Buck converters. This product integrates the driver IC and NexFET technology to complete the power stage switching function. The driver IC has a built-in selectable diode emulation function that enables DCM operation to improve light load efficiency. This combination produces high current, high efficiency, and high speed switching capability in a small 5 x 6 mm outline package. It also integrates the temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

Device Information(1)

Device	Media	Qty	Package	Ship
CSD95372AQ5M	13-Inch Reel	2500	SON 5 mm × 6 mm Package	Tape and Reel
CSD95372AQ5MT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



Typical Power Stage Efficiency and Power Loss

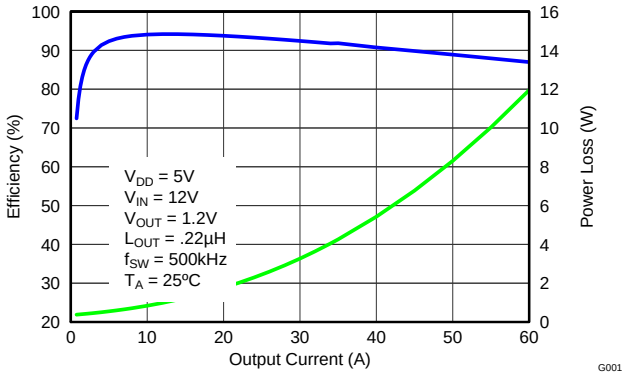


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2014) to Revision C — **Page**

- Corrected typo so f_{SW} reads 2000 kHz in Recommended Operating Conditions ... 4

Changes from Revision A (September 2013) to Revision B — **Page**

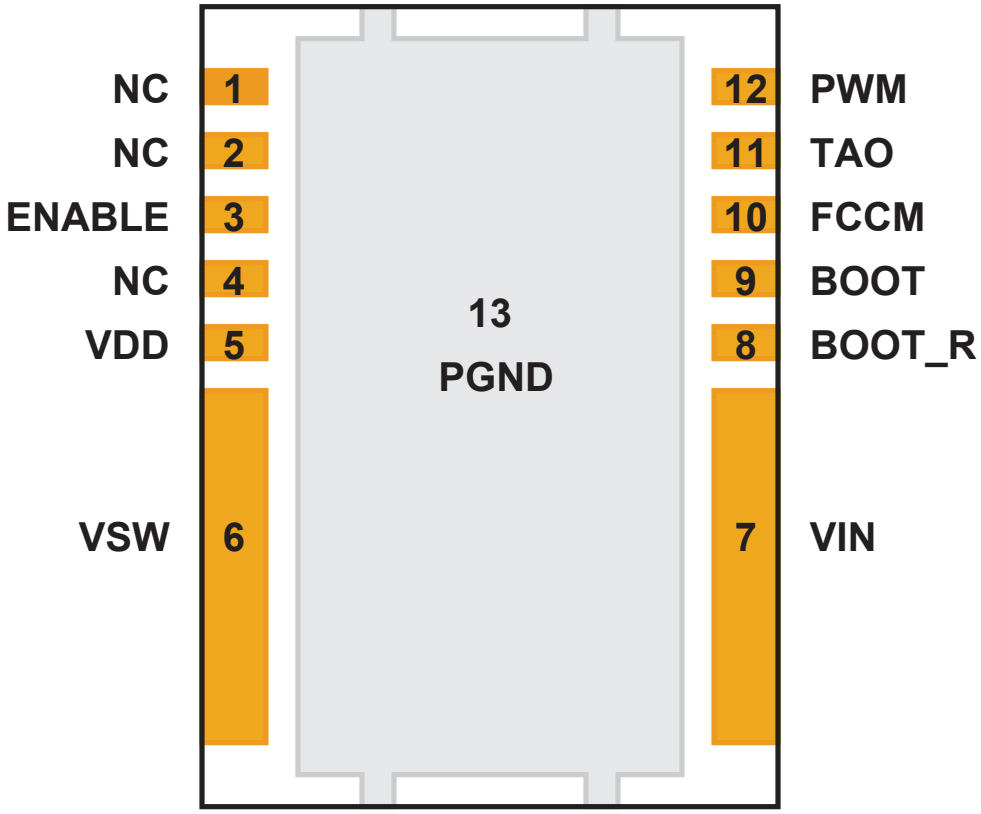
- Added small reel option ... 1
- Fixed TAO/FAULT Pin Function to state that TAO will be pulled up to 3.3 V in the event of thermal shutdown ... 3
- Increased the max LS FET Turn-off Current to 1.125A ... 6

Changes from Original (June 2013) to Revision A — **Page**

- Changed CSD97372AQ5M to CSD95372AQ5M throughout the Functional Description section ... 9

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5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
NC	1, 2, 4	No connect, must leave floating.
ENABLE	3	Enables device operation. If ENABLE = logic HIGH, turns on device. If ENABLE = logic LOW, the device is turned off and both MOSFET gates are actively pulled low. An internal 100 kΩ pull down resistor will pull the ENABLE pin LOW if left floating.
V_{DD}	5	Supply Voltage to Gate Driver and internal circuitry.
V_{SW}	6	Phase node connecting the HS MOSFET Source and LS MOSFET Drain - pin connection to the output inductor.
V_{IN}	7	Input Voltage Pin. Connect input capacitors close to this pin.
BOOT_R	8	Return path for HS gate driver, connected to V_{SW} internally.
BOOT	9	Bootstrap capacitor connection. Connect a minimum of 0.1 µF 16 V X7R, ceramic capacitor from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the Control FET. The bootstrap diode is integrated.
FCCM	10	This pin enables the Diode Emulation function. When this pin is held LOW, Diode Emulation Mode is enabled for Sync FET. When FCCM is HIGH, the device operated in Forced Continuous Conduction Mode. An internal 5µA current source will pull the FCCM pin to V_{DD} if left floating.
TAO/ FAULT	11	Temperature amplifier output. Reports a voltage proportional to the die temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the IC's. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if Thermal Shutdown occurs. TAO should be bypassed to P_{GND} with a 1nF 16V X7R ceramic capacitor.
PWM	12	Pulse-width modulated Tri-state input from external controller. Logic LOW sets Control FET gate low and Sync FET gate high. Logic HIGH sets Control FET gate high and Sync FET gate low. Open or High Z sets both MOSFET gates low if greater than the Tri-State Shutdown Hold-off Time (t_{3HT}).
P_{GND}	13	Power ground.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

T_A = 25°C (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN} to P_{GND}	–0.3	25	V
V_{SW} to P_{GND}	–0.3	25	V
V_{SW} to P_{GND} (<10 ns)	–7	27	V
V_{DD} to P_{GND}	–0.3	7	V
ENABLE, PWM, FCCM, TAO to P_{GND}(2)	–0.3	V_{DD} + 0.3	V
BOOT to BOOT_R(2)	–0.3	V_{DD} + 0.3	V
P_D, Power Dissipation		12	W
T_J, Operating Temperature Range	–55	150	°C
T_{stg}, Storage Temperature Range	–55	150	°C

(1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability.
(2) Should not exceed 7 V.

6.2 ESD Ratings

		VALUE	UNIT
ESD Rating	Human Body Model (HBM)	±2000	V
	Charged Device Model (CDM)	±500	

6.3 Recommended Operating Conditions

T_A = 25° (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Gate Drive Voltage		4.5	5.5	V
V_{IN}	Input Supply Voltage			16	V
V_{OUT}	Output Voltage			5.5	V
I_{OUT}	Continuous Output Current	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.8 V, f_{SW} = 500 kHz, L_{OUT} = 0.22 µH(1)		60	A
I_{OUT-PK}	Peak Output Current(2)			90	A
f_{SW}	Switching Frequency	C_{BST} = 0.1 µF (min)		2000	kHz
	On Time Duty Cycle	f_{SW} = 1 MHz		85	%
	Minimum PWM On Time		20		ns
	Operating Temperature		–40	125	°C

(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) System conditions as defined in Note 1. Peak Output Current is applied for t_p = 50 µs.

6.4 Thermal Information

T_A = 25°C (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance (Top of package)(1)			15	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance(2)			2	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches, 0.06 inch (1.52 mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1 mm of the package.

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6.5 Electrical Characteristics

T_A = 25°C, V_{DD} = POR to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}						
	Power Loss(1)	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 30 A, f_{SW} = 500 kHz, L_{OUT} = 0.22 µH , T_J = 25°C		3.3		W
	Power Loss(2)	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 30 A, f_{SW} = 500 kHz, L_{OUT} = 0.22 µH , T_J = 125°C		3.9		W
V_{IN}						
I_Q	V_{IN} Quiescent Current	ENABLE = 0, V_{DD} = 5 V			10	µA
V_{DD}						
I_{DD}	Standby Supply Current	ENABLE = 0, PWM = 0			250	µA
I_{DD}	Operating Supply Current	ENABLE = 5 V, PWM = 50% Duty cycle, f_{SW} = 500 kHz		23		mA
POWER-ON RESET AND UNDERVOLTAGE LOCKOUT						
V_{DD} Rising	Power-On Reset				3.9	V
V_{DD} Falling	UVLO		3.4			V
	Hysteresis		100		250	mV
	Startup Delay(3)	ENABLE = 5 V		6		µs
ENABLE						
V_{IH}	Logic Level High	Schmitt Trigger Input See Figure 11	2.0			V
V_{IL}	Logic Level Low				0.8	V
	Weak Pulldown Impedance			100		kΩ
t_{PDH}	Rising Propagation Delay			3		µs
t_{PDL}	Falling Propagation Delay			30		ns
FCCM						
V_{IH}	Logic Level High	Schmitt Trigger Input See Figure 13 and Figure 14	2.0			V
V_{IL}	Logic Level Low				0.8	V
	Weak Pullup Current			5		µA
THERMAL SHUTDOWN(2)						
	Start Threshold		150	165		°C
	Temperature Hysteresis			25		°C

(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) Specified by design
(3) POR to V_{SW} Rising

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Electrical Characteristics (continued)

T_A = 25°C, V_{DD} = POR to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM						
I_{PWMH}		PWM = 5 V		500		µA
I_{PWML}		PWM = 0		–500		µA
V_{PWMH}	PWM Logic Level High	C_{PWM} = 10 pF	2.3	2.5	2.7	V
V_{PWML}	PWM Logic Level Low		0.7	0.9	1.1	V
	PWM Tri-State Open Voltage			1.5		V
t_{PDLH} and t_{PDHL}	PWM to V_{SW} Propagation Delay(2)			50		ns
t_{3HT}	Tri-State Shutdown Hold-off Time(2)			30		ns
t_{3SD}	Tri-State Shutdown Propagation Delay(2)			80	160	ns
t_{3RD}	Tri-State Recovery Propagation Delay(2)			50	80	ns
t_{DEM}	Diode Emulation Minimum On Time(2)			150		ns
BOOTSTRAP SWITCH						
V_{FBOOT}	Forward Voltage	Measured from V_{DD} to V_{BOOT}, I_F = 10 mA		200	360	mV
I_{RBOOT}	Reverse Leakage(1)	$V_{BOOT} – V_{DD}$ = 20 V		0.15	1	µA
ZERO CROSSING COMPARATOR						
	LS FET Turn-off Current	Diode Emulation Mode Enabled V_{OUT} = 1.8 V, L = 150 nH	0		1.125	A
THERMAL ANALOG OUTPUT TAO						
	Output Voltage at 25°C		0.56	0.60	0.64	V
	Output Voltage Temperature Coefficient			8		mV/°C

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6.6 Typical Power Stage Characteristics

T_J = 125°C, unless stated otherwise. The typical CSD95372A system characteristic curves are based on measurements made on a PCB design with dimensions of 4 inches (W) x 3.5 inches (L) x 0.062 inch (T) and 6 copper layers of 1 oz. copper thickness. See the *Application Information* section for a detailed explanation.

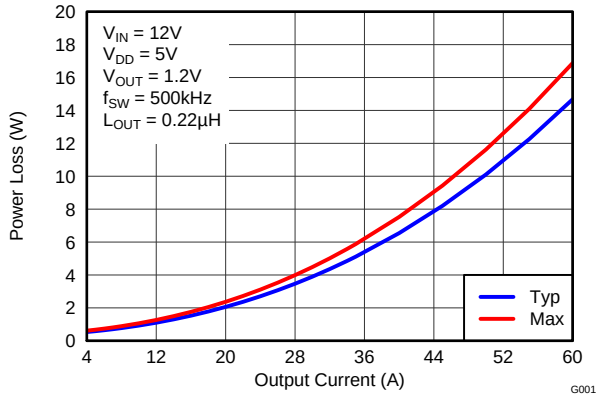


Figure 1. Power Loss vs Output Current

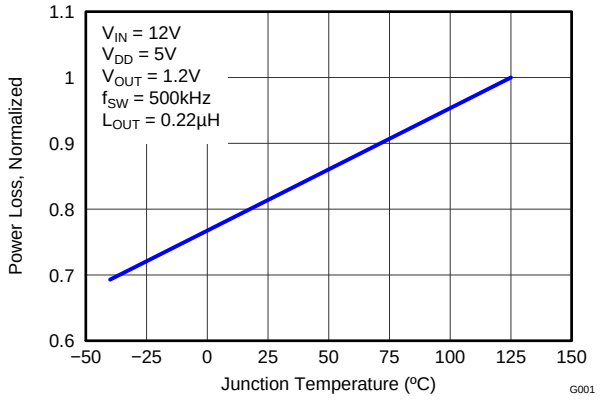


Figure 2. Power Loss vs Temperature

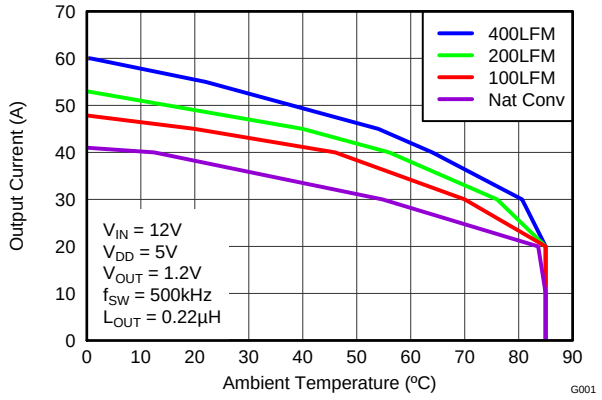


Figure 3. Safe Operating Area – PCB Horizontal Mount (1)

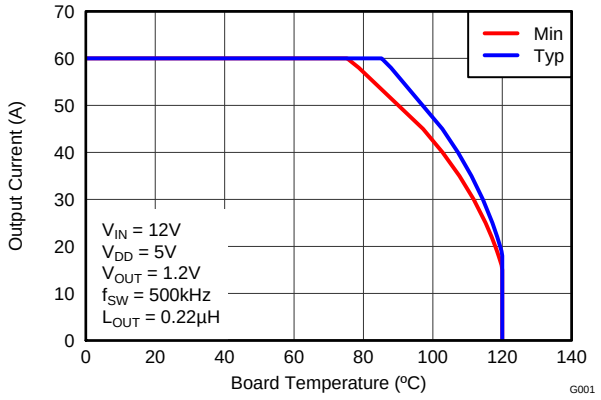


Figure 4. Typical Safe Operating Area (1)

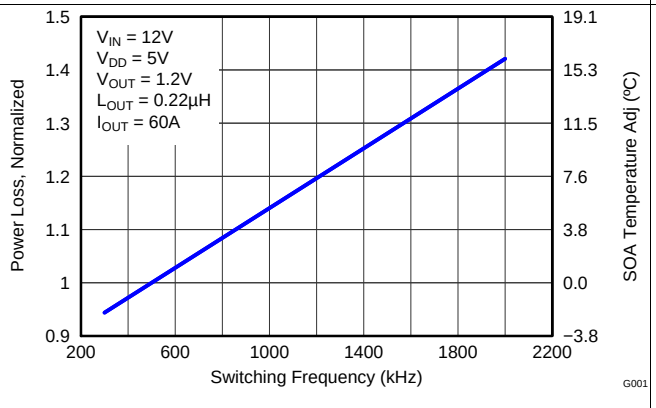


Figure 5. Normalized Power Loss vs Frequency

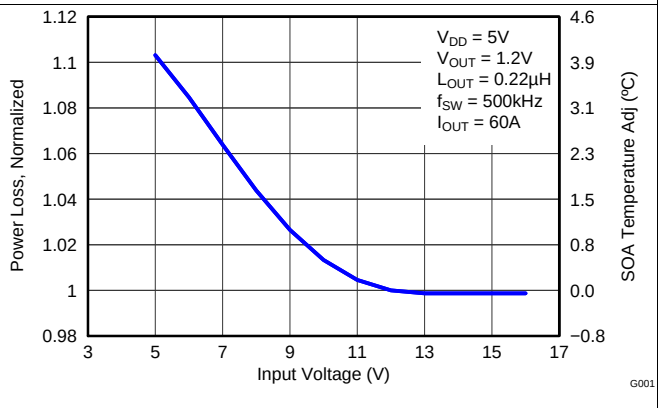


Figure 6. Normalized Power Loss vs Input Voltage

Typical Power Stage Characteristics (continued)

T_J = 125°C, unless stated otherwise. The typical CSD95372A system characteristic curves are based on measurements made on a PCB design with dimensions of 4 inches (W) x 3.5 inches (L) x 0.062 inch (T) and 6 copper layers of 1 oz. copper thickness. See the *Application Information* section for a detailed explanation.

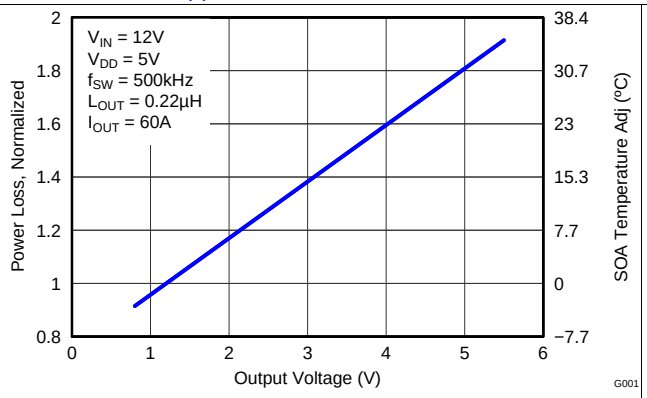


Figure 7. Normalized Power Loss vs Output Voltage

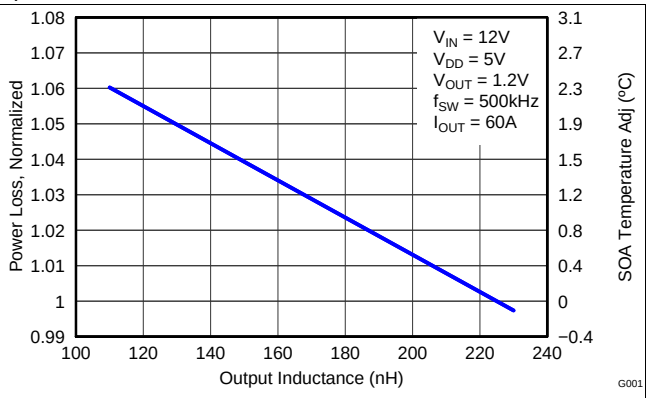


Figure 8. Normalized Power Loss vs Output Inductance

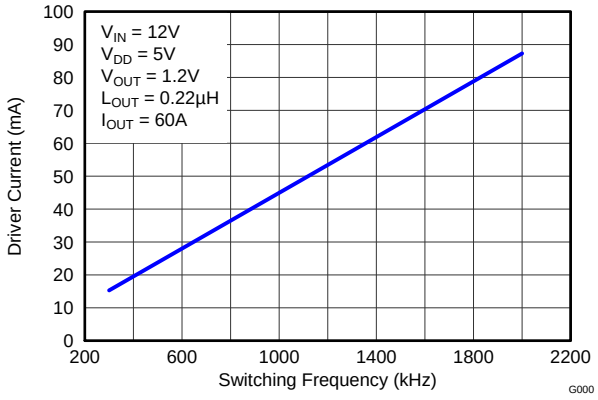
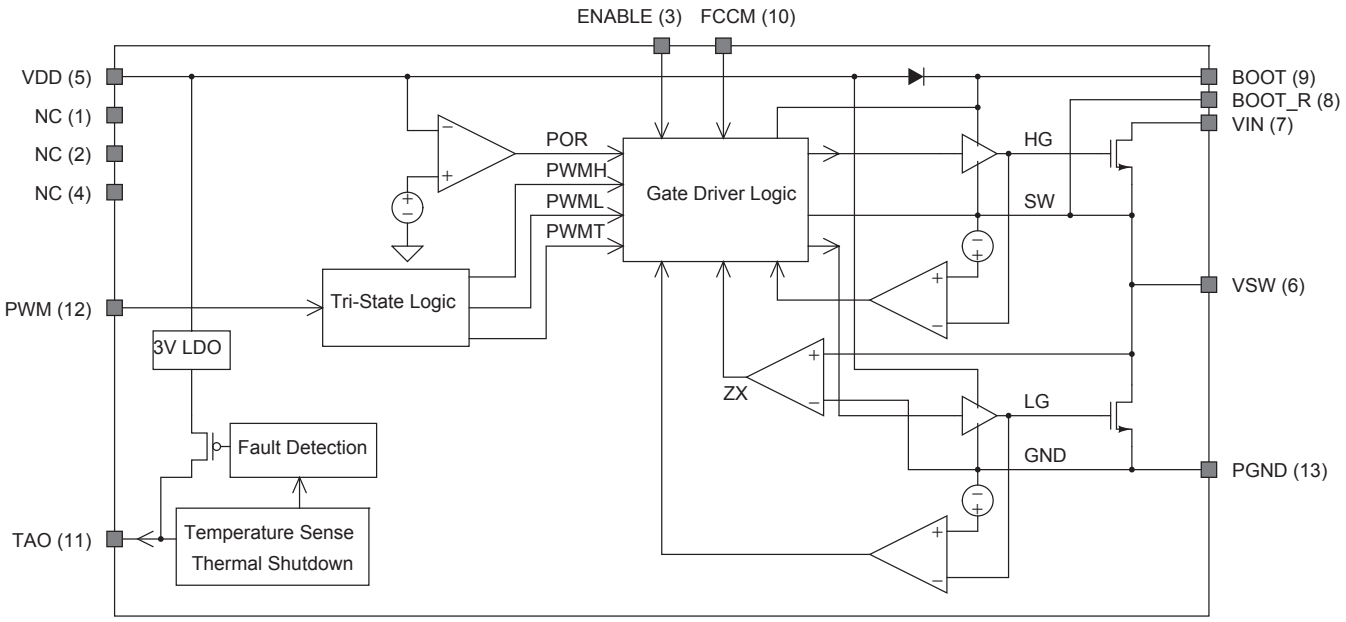


Figure 9. Driver Current vs Frequency

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7 Detailed Description

7.1 Functional Block Diagram



7.2 Functional Description

7.2.1 Powering the CSD95372AQ5M and Gate Drivers

An external V_{DD} voltage is required to supply the integrated gate driver IC and provide the necessary gate drive power for the MOSFETs. The gate driver IC is capable of supplying in excess of 4 A peak current into the MOSFET gates to achieve fast switching. A 1 µF 10 V X5R or higher ceramic capacitor is recommended to bypass V_{DD} pin to P_{GND}. A bootstrap circuit to provide gate drive power for the Control FET is also included. The bootstrap supply to drive the Control FET is generated by connecting a 100 nF 16 V X5R ceramic capacitor between BOOT and BOOT_R pins. An optional R_{BOOT} resistor can be used to slow down the turn on speed of the Control FET and reduce voltage spikes on the V_{SW} node. A typical 1 to 4.7 Ω value is a compromise between switching loss and V_{SW} spike amplitude.

7.2.2 Undervoltage Lockout (UVLO) Protection

The V_{DD} supply is monitored for UVLO conditions and both Control FET and Sync FET gates are held low until adequate supply is available. An internal comparator evaluates the V_{DD} voltage level and if V_{DD} is greater than the Power On Reset threshold (V_{POR}), the gate driver becomes active. If V_{DD} is less than the UVLO threshold, the gate driver is disabled and the internal MOSFET gates are actively driven low. At the rising edge of the V_{DD} voltage, both Control FET and Sync FET gates will be actively held low during V_{DD} transitions between 1.0V to V_{POR}. This region is referred to as the Gate Drive Latch Zone, seen in Figure 10. In addition, at the falling edge of the V_{DD} voltage, both Control FET and Sync FET gates are actively held low during the UVLO to 1 V transition.

The Power Stage CSD95372AQ5M device must be powered up and Enabled before the PWM signal is applied.

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Functional Description (continued)

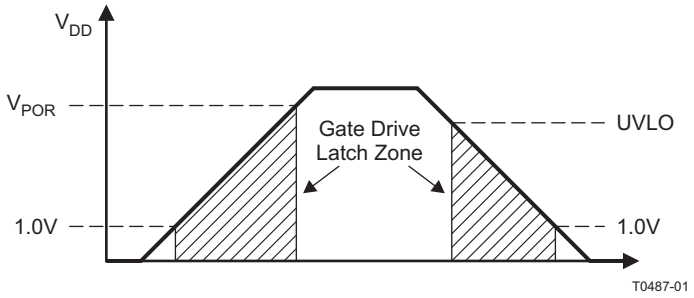


Figure 10. UVLO Operation

7.2.3 ENABLE

The ENABLE pin is TTL compatible. The logic level thresholds are sustained under all V_{DD} operating conditions between V_{POR} to V_{DD}. In addition, if this pin is left floating, a weak internal pull down resistor of 100 kΩ will pull the ENABLE pin below the logic level low threshold. The operational functions of this pin should follow the timing diagram outlined in Figure 11. A logic level low will actively hold both Control FET and Sync FET gates low and V_{DD} pin should typically draw less than 5 µA.

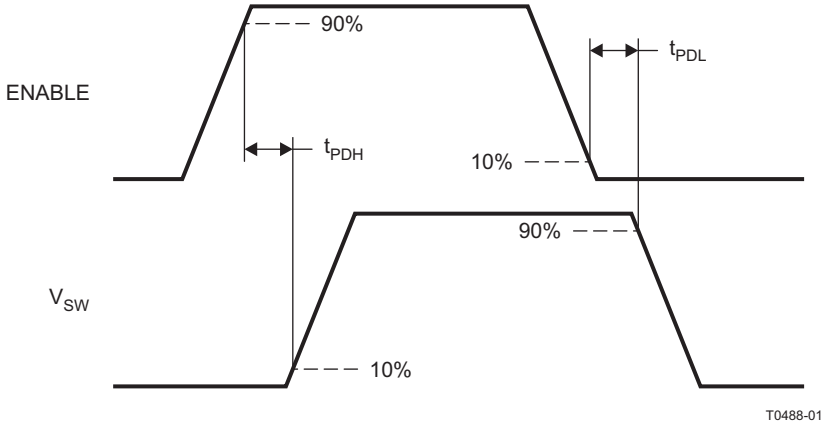


Figure 11. CSD95372AQ5M ENABLE Timing Diagram (V_{DD} = PWM = 5 V)

7.2.4 Power Up Sequencing

If the ENABLE signal is used, it is necessary to ensure proper co-ordination with the ENABLE and soft-start features of the external PWM controller in the system. If the CSD95372AQ5M was disabled through ENABLE without sequencing with the PWM IC controller, the buck converter output will have no voltage or fall below regulation set point voltage. As a result, the PWM controller IC delivers Max duty cycle on the PWM line. If the Power Stage is re-enabled by driving the ENABLE pin high, there will be an extremely large input inrush current when the output voltage builds back up again. The input inrush current might have undesirable consequences such as inductor saturation, driving the input power supply into current limit or even catastrophic failure of the CSD95372AQ5M device. Disabling the PWM controller is recommended when the CSD95372AQ5M is disabled. The PWM controller should always be re-enabled by going through soft-start routine to control and minimize the input inrush current and reduce current and voltage stress on all buck converter components. It is recommended that the external PWM controller be disabled when CSD95372AQ5M is disabled or nonoperational because of UVLO.

When ENABLE signal is toggled, there is an internal 3 µs hold-off time before the driver will respond to PWM events to ensure the analog sensing circuitry is properly powered and stable. This hold-off time should be considered when designing the power-up sequencing of the controller IC and the Power Stage.

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Functional Description (continued)

7.2.5 PWM

The input PWM pin incorporates a Tri-State function. The Control FET and Sync FET gates are forced low if the PWM pin is left floating for more than the Tri-State Hold off time (t_{3HT}). The Tri-state mode can be entered by actively driving the PWM input to the V_{3T} voltage or the PWM input can be made high impedance and internal current sources will driver PWM to V_{3T}. The PWM input can source up to I_{PWMH} and sink down to I_{PWML} current to drive PWM to the V_{3T} voltage, but will consume no current when sitting at the V_{3T} voltage. Operation in and out of Tri-State mode should follow the timing diagram outlined in Figure 12. Both V_{PWML} and V_{PWMH} threshold levels are set to accommodate both 3.3 V and 5 V logic controllers. During normal operation, the PWM signal should be driven to logic levels Low and High with a maximum of 500 Ω sink/source impedance respectively.

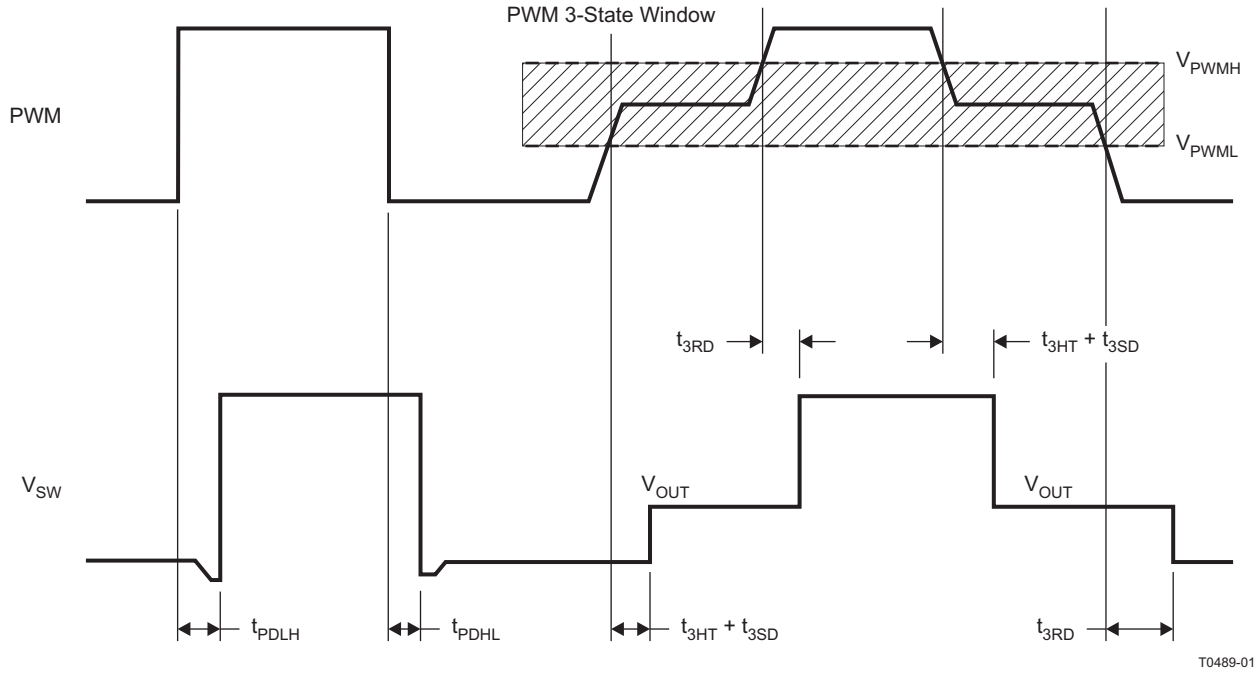


Figure 12. PWM Timing Diagram

7.2.6 FCCM

The input FCCM pin enables the Power Stage device to operate in either continuous current conduction mode or diode emulation mode. When FCCM is driven above its high threshold, the Power Stage will operate in continuous conduction mode regardless of the polarity of the output inductor current. When FCCM is driven below its low threshold, the Power Stage's internal zero-cross detection circuit is enabled. When the zero-cross detection circuit is active, diode emulation mode will be entered on the third consecutive PWM pulse in which a zero-crossing event is detected. If FCCM is driven high after diode emulation mode has been enabled, continuous conduction mode will begin after the next PWM event. See Figure 13 and Figure 14 for FCCM timing.

7.2.7 TAO/FAULT (Thermal Analog Output/Protection Flag)

During normal operation the output TAO pin is a highly accurate analog temperature measurement of the lead-frame temperature of the Power Stage. Because the source junction of the Sync FET sits directly on the lead-frame of the Power Stage, this output can be used as an accurate measurement of the junction temperature of the Sync FET. The TAO pin should be bypassed to P_{GND} using a 1 nF X7R ceramic capacitor to ensure accurate temperature measurement.

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Functional Description (continued)

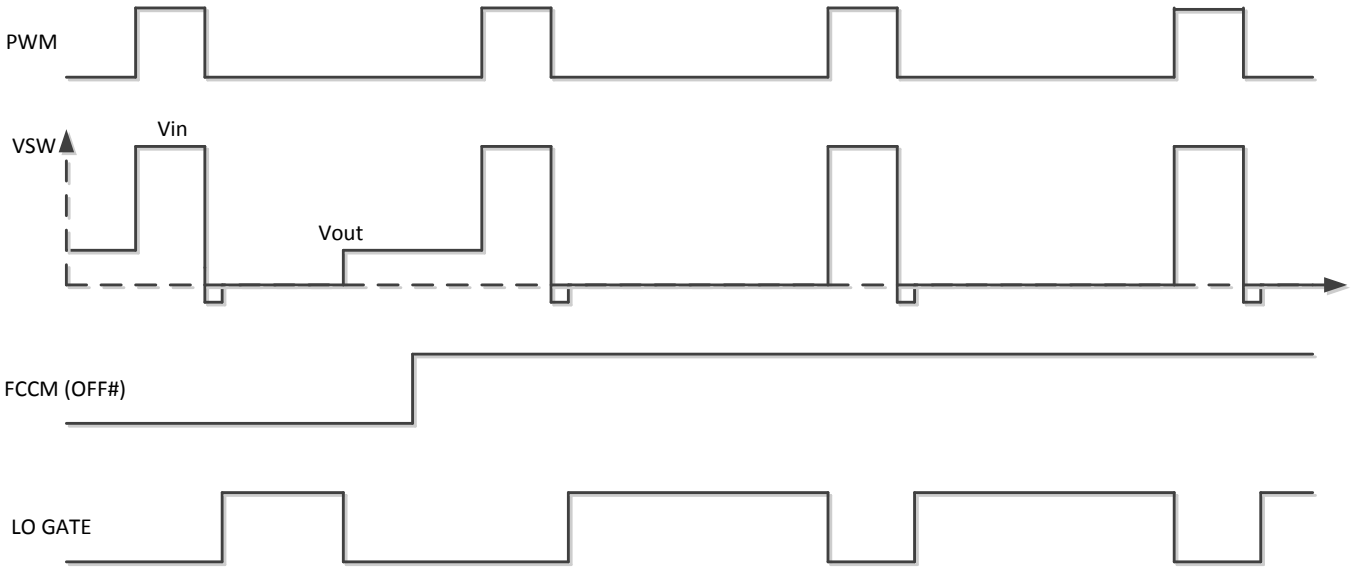
This Power Stage device has built-in over-temperature protection (described below) which is flagged by pulling TAO to 3 V. The TAO pin also includes a built in ORing function. When connecting TAO pins of more than one device together, the TAO bus automatically reads the highest TAO voltage among all devices. This greatly simplifies the temperature sense and fault reporting design for multi-phase applications, where a single line TAO/FAULT bus can be used to tie the TAO pins of all phases together and the system can monitor the temperature of the hottest component.

7.2.8 Over Temperature

An over-temperature fault occurs when the dies temperature reaches Thermal Shutdown Temperature (see the *Electrical Characteristics*). An over-temperature event is the only fault condition to which the Power Stage will automatically react. When the over-temperature event is detected, the Power Stage will automatically turn off both HS and LS MOSFETs and pull TAO to 3.3 V. If the temperature falls below the over-temperature threshold hysteresis band, the driver will again respond to PWM commands and the TAO pin will return to normal operation. A weak pull down is used to pull TAO back from a fault event so there is a significant delay before the TAO output will report the correct temperature.

7.2.9 Gate Drivers

This Power Stage has an internal high-performance gate driver IC that is trimmed to achieve minimum dead-time for lowest possible switching loss and switch-node ringing reduction. To eliminate the possibility of shoot-through at light load conditions, the dead-time is adjusted to a longer period when the inductor current is negative prior to a PWM HIGH input.

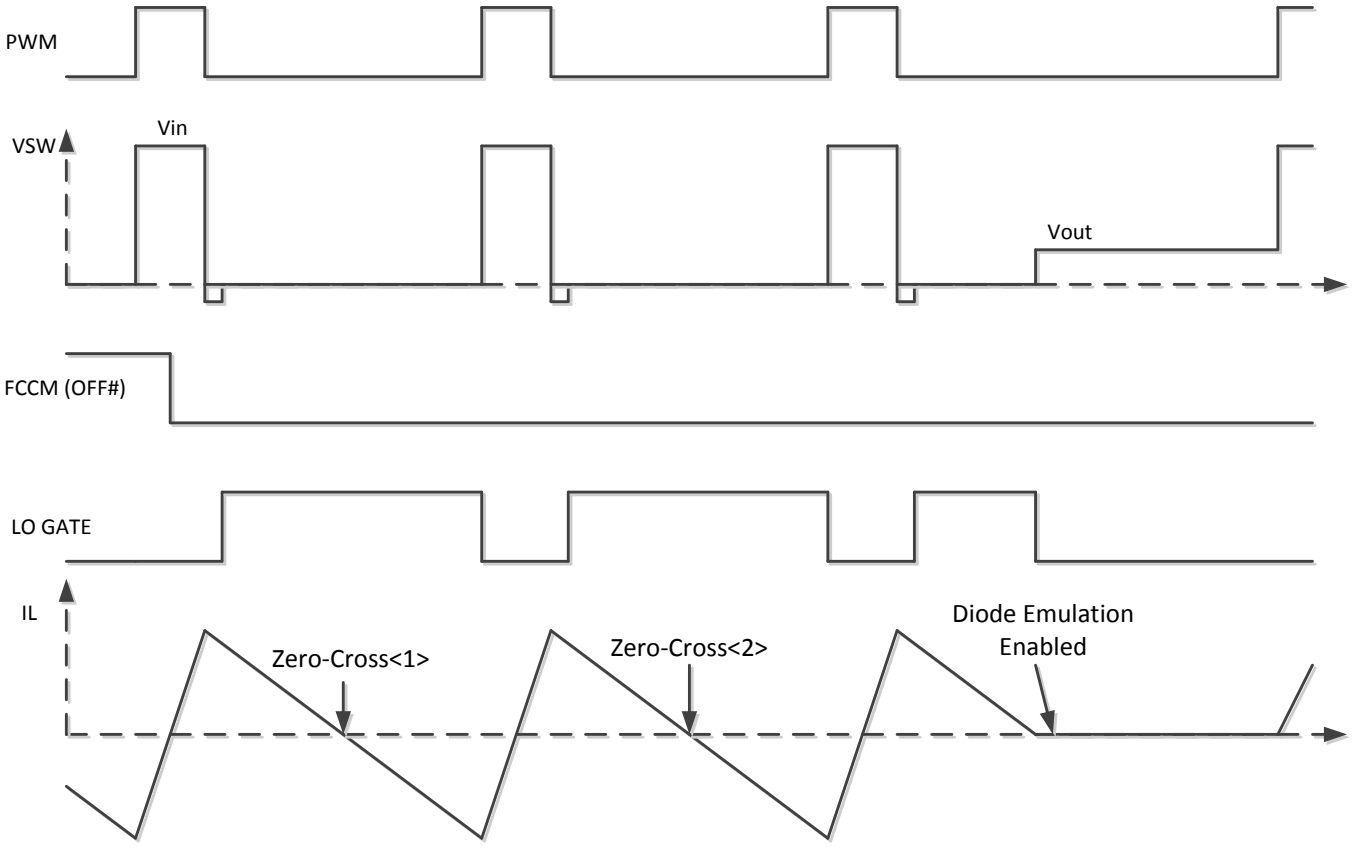


During Diode Emulation Mode (DEM) the Lo Gate signal is latched off by the zero-cross comparator and reset by rising edge of PWM. If FCCM is pulled high after Lo Gate has been latched off, normal CCM operation does not begin until after the next PWM pulse.

Figure 13. FCCM Rising Timing Diagram

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Functional Description (continued)



Zero-cross detection is enabled by FCCM low. Diode-Emulation Mode is entered on the third consecutive PWM pulse in which a zero-crossing event is detected. If at any time no zero-cross event is detected when FCCM is low, the zero-cross counter is reset and diode-emulation mode is not enabled. If FCCM remains low, diode-emulation mode will be re-enabled on the third consecutive PWM pulse in which a zero-cross event is detected.

Figure 14. FCCM Falling Timing Diagram

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The Power Stage CSD95372AQ5M is a highly optimized design for synchronous buck applications using NexFET devices with a 5 V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems centric environment. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the power MOSFETs. System level performance curves such as Power Loss, Safe Operating, Area and normalized graphs allow engineers to predict the product performance in the actual application.

8.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are primarily needed by engineers to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD95372AQ5M as a function of load current. This curve is measured by configuring and running the CSD95372AQ5M as it would be in the final application (see *Application Schematic*). The measured power loss is the CSD95372AQ5M device power loss which consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\textbf{Power Loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperature of T_J = 125°C under isothermal test conditions.

8.3 Safe Operating Curves (SOA)

The SOA curves in the CSD95372AQ5M datasheet give engineers guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 and Figure 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness.

8.4 Normalized Curves

The normalized curves in the CSD95372AQ5M data sheet give engineers guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

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8.5 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Design Example*). Though the Power Loss and SOA curves in this datasheet are taken for a specific set of test conditions, the following procedure will outline the steps engineers should take to predict product performance for any set of system conditions.

8.5.1 Design Example

Operating Conditions: Output Current (I_{OUT}) = 40 A, Input Voltage (V_{IN}) = 7 V, Output Voltage (V_{OUT}) = 1.5 V, Switching Frequency (f_{SW}) = 800 kHz, Output Inductor (L_{OUT}) = 0.2 µH

8.5.2 Calculating Power Loss

- Typical Power Loss at 40 A = 6.5 W (Figure 1)
- Normalized Power Loss for switching frequency ≈ 1.08 (Figure 5)
- Normalized Power Loss for input voltage ≈ 1.06 (Figure 6)
- Normalized Power Loss for output voltage ≈ 1.06 (Figure 7)
- Normalized Power Loss for output inductor ≈ 1.01 (Figure 8)
- **Final calculated Power Loss = 6.5 W × 1.08 × 1.06 × 1.06 × 1.01 ≈ 8.0 W**

8.5.3 Calculating SOA Adjustments

- SOA adjustment for switching frequency ≈ 3.2°C (Figure 5)
- SOA adjustment for input voltage ≈ 2.4°C (Figure 6)
- SOA adjustment for output voltage ≈ -0.8°C (Figure 7)
- SOA adjustment for output inductor ≈ 0.5°C (Figure 8)
- **Final calculated SOA adjustment = 3.2 + 2.4 + 2.4 + 0.5 ≈ 8.5°C**

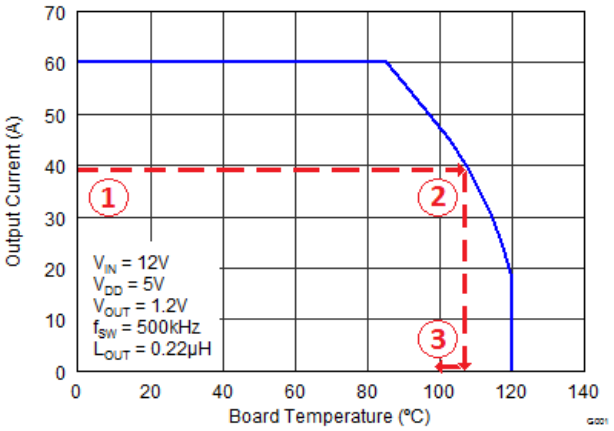


Figure 15. Power Stage CSD95372AQ5M SOA

In the design example above, the estimated power loss of the CSD95372AQ5M would increase to 8.0 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 8.5°C. Figure 15 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 8.5°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

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9 Layout

9.1 Layout Guidelines

9.1.1 Recommended Schematic Overview

There are several critical components that must be used in conjunction with this Power Stage device. Figure 16 shows a portion of a schematic with the critical components needed for proper operation.

- C1: Bootstrap Capacitor
- R1: Bootstrap Resistor
- C4: Bypass Capacitor for TAO
- C3: Bypass Capacitor for V_{DD}
- C5: Bypass Capacitor for V_{IN} to Help with Ringing Reduction
- C6: Bypass Capacitor for V_{IN}

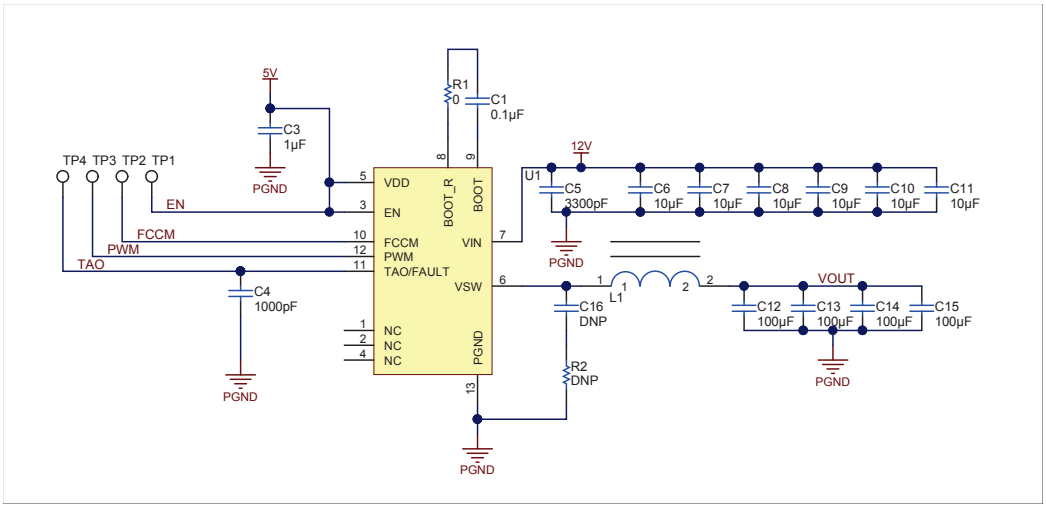


Figure 16. Recommended Schematic

9.1.2 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. Below is a brief description on how to address each parameter.

9.1.2.1 Electrical Performance

The CSD95372AQ5M has the ability to switch at voltage rates greater than 10 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, inductor and output capacitors.

- The placement of the input capacitors relative to V_{IN} and P_{GND} pins of CSD95372AQ5M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the V_{IN} and P_{GND} pins (see Figure 17). The example in Figure 17 uses 1 x 3.3 nF 0402 50 V and 6 x 10 µF 1206 25 V ceramic capacitors (TDK part number C3216X7R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C5, C8 and C6, C19 should follow in order.
- The bootstrap cap C_{BOOT} 0.1 µF 0603 16 V ceramic capacitor should be closely connected between BOOT and BOOT_R pins
- The switching node of the output inductor should be placed relatively close to the Power Stage CSD95372AQ5M V_{SW} pins. Minimizing the V_{SW} node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. (1)

(1) Keong W. Kam, David Pommerenke, “EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis”, University of Missouri – Rolla

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Layout Guidelines (continued)

9.1.2.2 Thermal Performance

The CSD95372AQ5M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 17 uses vias with a 10 mil drill hole and a 26 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

9.1.3 Sensing Performance

The integrated temperature sensing technology built in the driver of the CSD95372AQ5M produces an analog signal that is proportional to the temperature of the lead-frame of the device, which is almost identical to the junction temperature of the Sync FET. To calculate the junction temperature based on the TAO voltage, use Equation 2. TAO should be bypassed to P_{GND} with a 1 nF X7R ceramic capacitor for optimal performance. The TAO pin has limited sinking current capability in order to enable several power stages that are wire OR-ed together to report only the highest temperature (or fault condition if present). In order to ensure accurate temperature reporting, the TAO nets should be routed on a quiet inner layer between ground planes where possible. In addition, the TAO bypass capacitor should have a P_{GND} pour on the layer directly beneath to ensure proper decoupling. The TAO net should always be shielded from V_{SW} and V_{IN} whenever possible.

$$T_J[C°] = (TAO[mV] - 400[mV]) / 8[mV/°C] \quad (2)$$

9.2 Layout Example

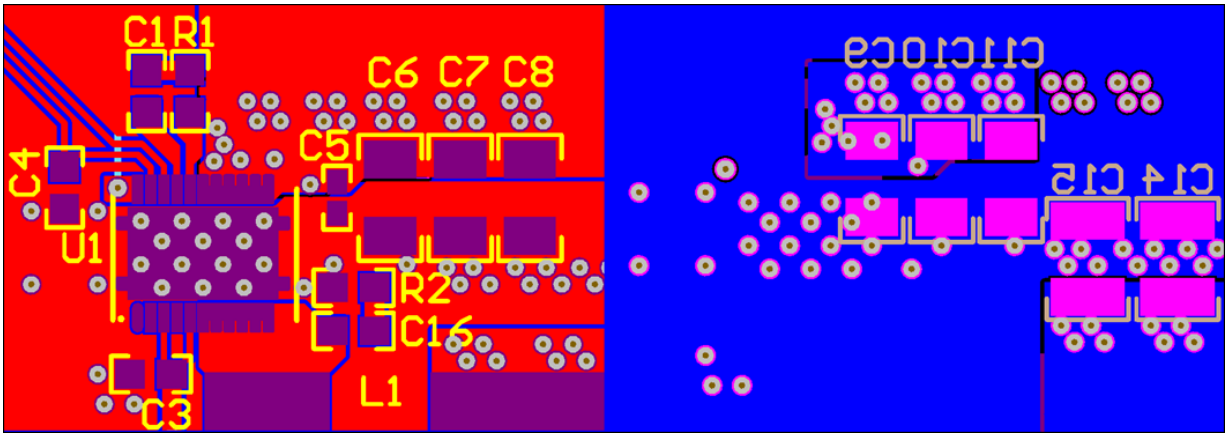
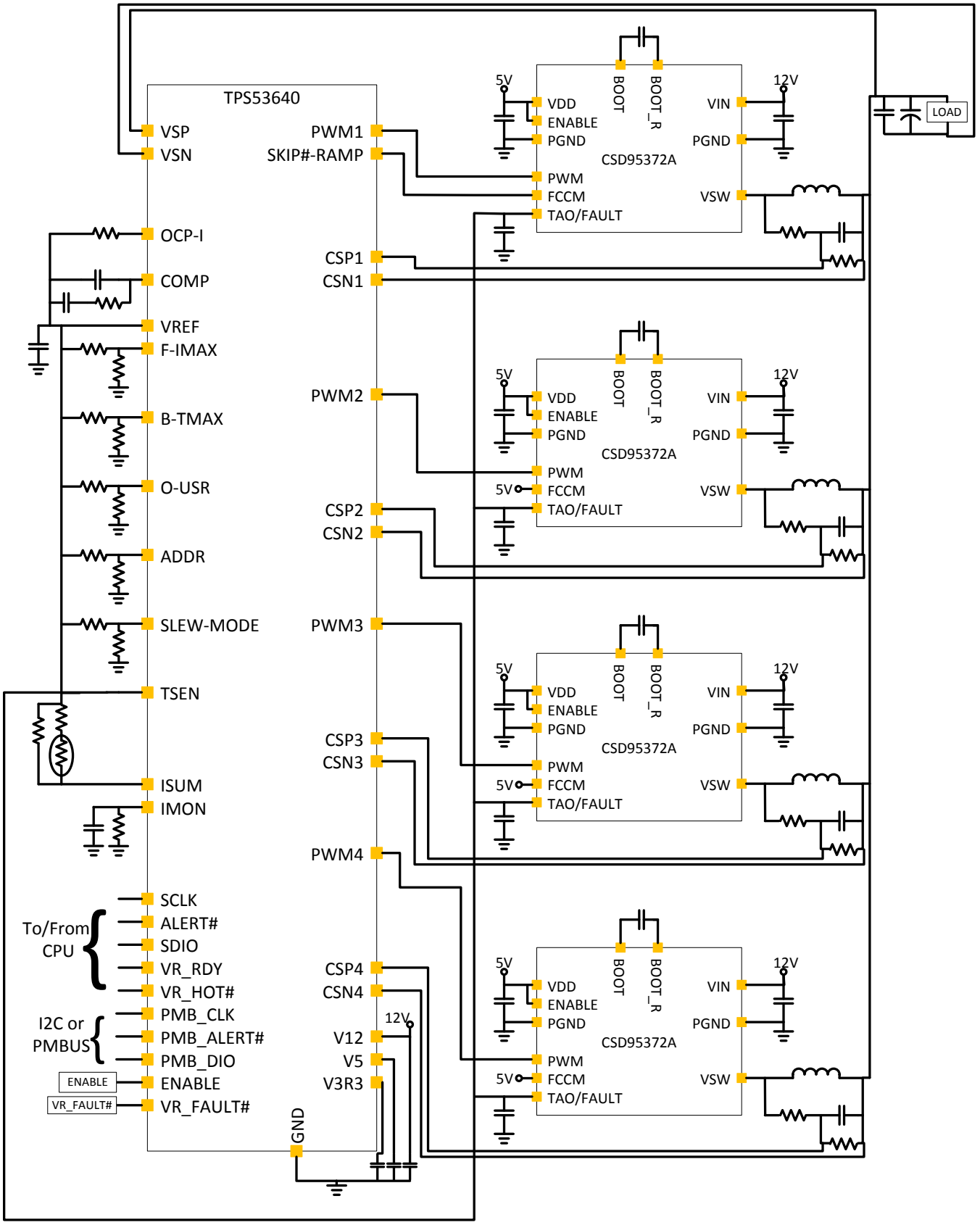


Figure 17. Recommended PCB Layout (Top Down View)

10 Application Schematic



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11 Device and Documentation Support

11.1 Trademarks

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11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

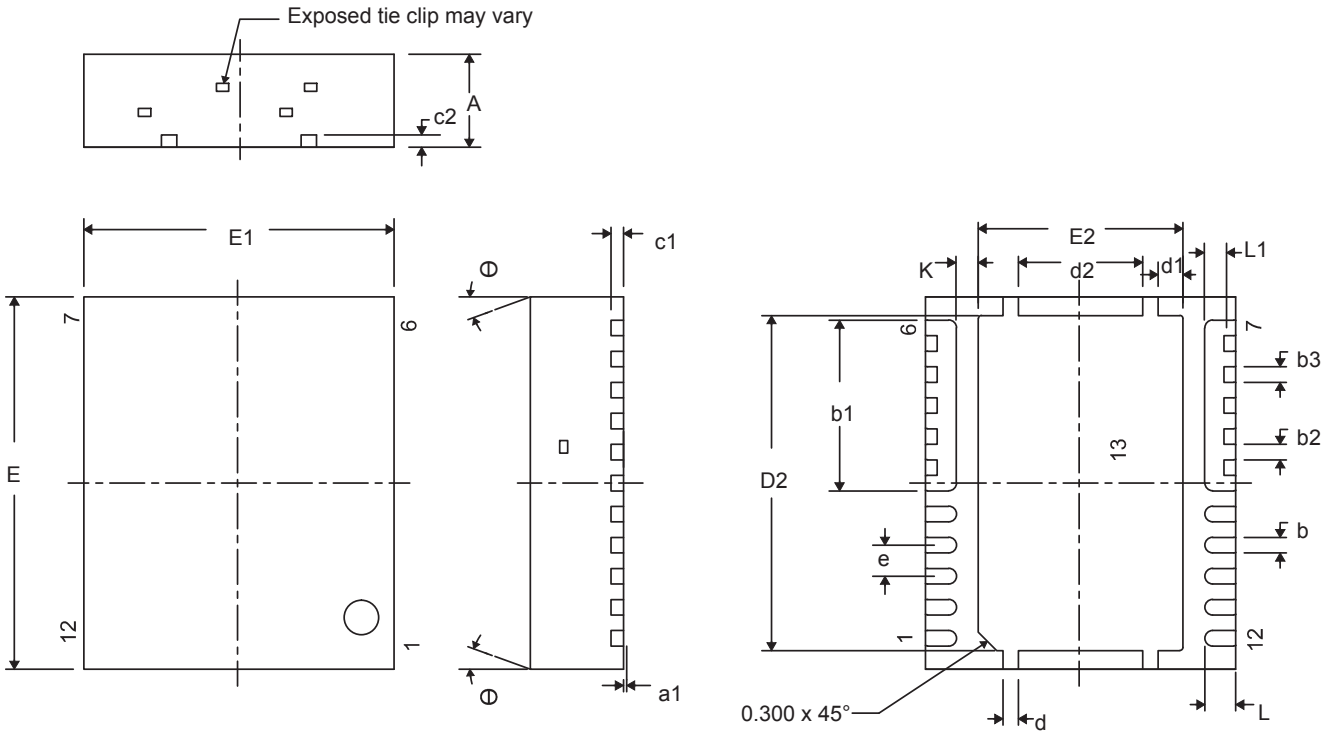
This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

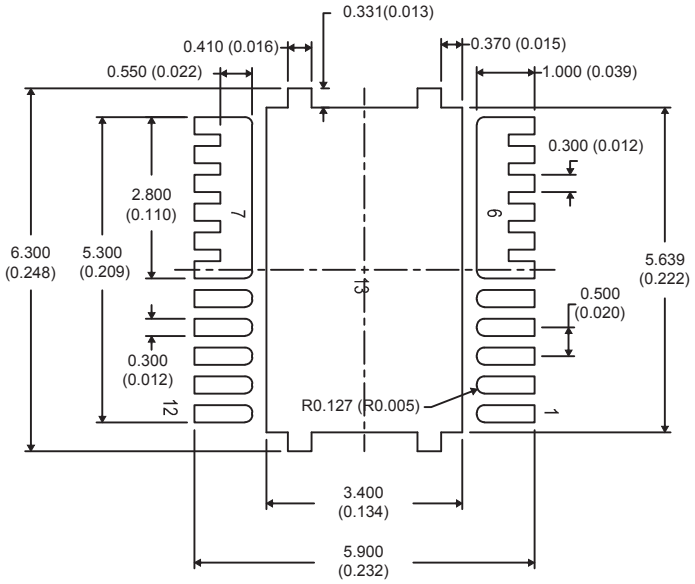
12.1 Mechanical Drawing



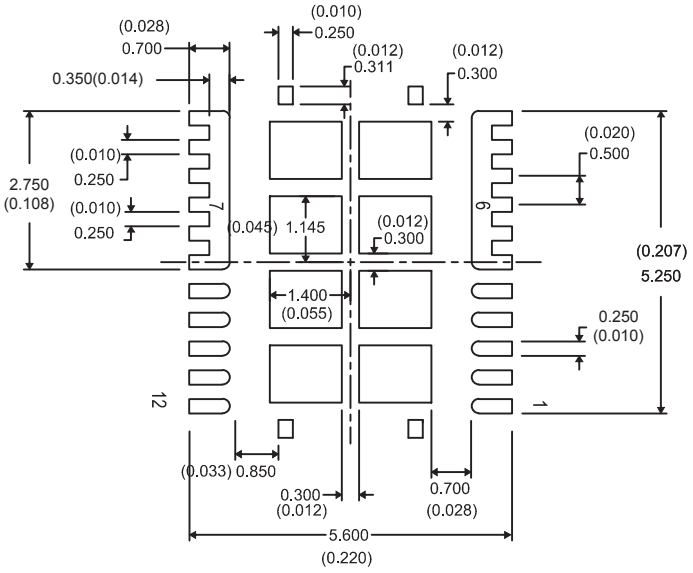
DIM	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.400	1.450	1.500	0.055	0.057	0.059
a1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.320	0.008	0.010	0.013
b1		2.750 TYP			0.108 TYP	
b2	0.200	0.250	0.320	0.008	0.010	0.013
b3		0.250 TYP			0.010 TYP	
c1	0.150	0.200	0.250	0.006	0.008	0.010
D2	5.300	5.400	5.500	0.209	0.213	0.217
d	0.200	0.250	0.300	0.008	0.010	0.012
d1	0.350	0.400	0.450	0.014	0.016	0.018
d2	1.900	2.000	2.100	0.075	0.079	0.083
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.200	3.300	3.400	0.126	0.130	0.134
e		0.500 TYP			0.020 TYP	
K		0.350 TYP			0.014 TYP	
L	0.400	0.500	0.600	0.016	0.020	0.024
L1	0.210	0.310	0.410	0.008	0.012	0.016
θ	0.00	—	—	0.00	—	—

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12.2 Recommended PCB Land Pattern



12.3 Recommended Stencil Opening



1. Dimensions are in mm (inches).
2. Stencil thickness is 100 µm.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD95372AQ5M	ACTIVE	LSON-CLIP	DQP	12	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	95372AM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

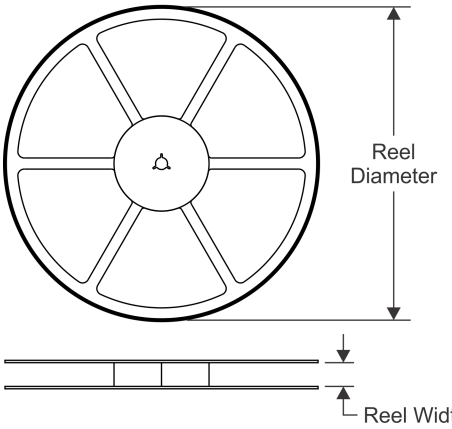
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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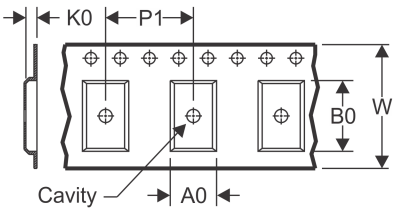
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

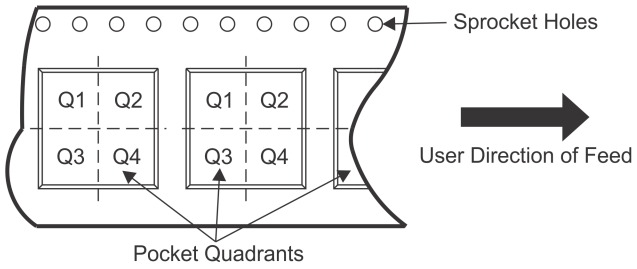


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

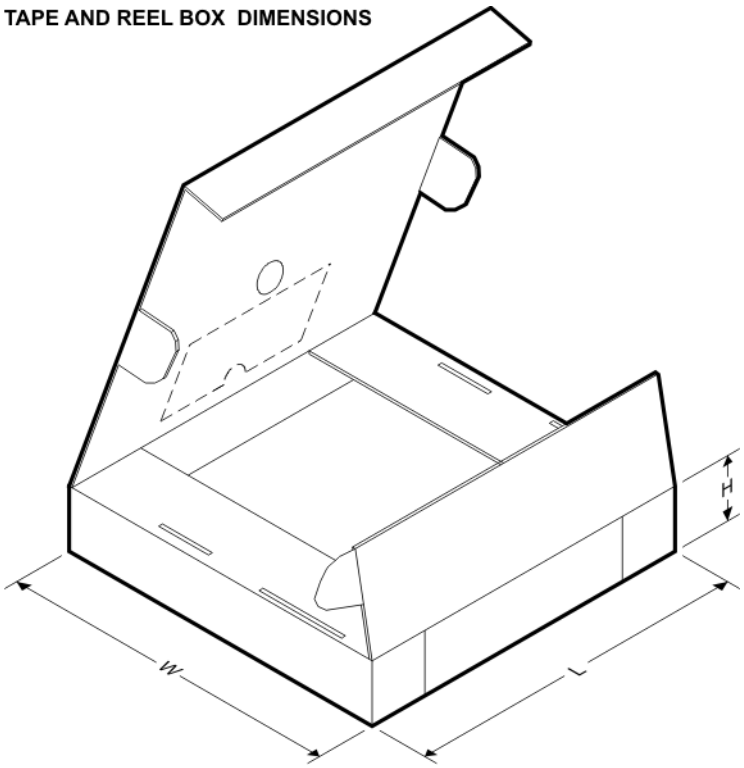
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95372AQ5M	LSON-CLIP	DQP	12	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95372AQ5M	LSON-CLIP	DQP	12	2500	367.0	367.0	35.0

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