

Errata to TFP101(A), TFP201(A), TFP401(A), TFP403, Datasheet Literature Numbers SLDS116A, SLDS119A, SLDS120A, SLDS125A

1. Power pad dimension.

ISSUE

The size of the exposed metal on the PowerPad package figure is shown as larger than on production devices. When providing a thermal land, it may be smaller than assumed from the package drawing. If routing traces under the power pad, some method of protection from shorts between the traces or vias and the PowerPad should be used.

Changes to document:

In the package drawing page, change the package figure as described:

a) Re-size the thermal pad dashed box from its present size to 5.05mm, centered in the package.

b)

Add dimensions to re-sized pad showing: $\frac{5.05}{3.95}$ SQ

c) Change note D to read:

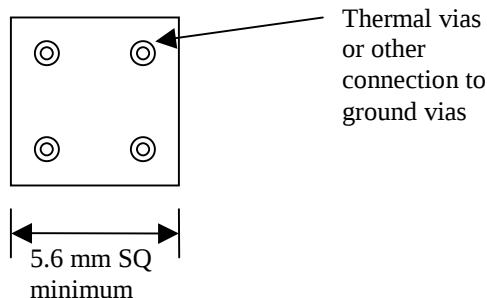
The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is centered on the package and is electrically and thermally connected to the backside of the die.

In the “PowerPAD...” section, add a sentence to paragraph 1, reword paragraph 2 and add figure and paragraphs between existing paragraphs 2 &3 to read:

... Soldering the back side of the ... to the application board is not required thermally as the device power dissipation is well within the package capability when not soldered. If traces or vias are located under the back side pad, they should be protected by suitable solder mask or other assembly technique to prevent inadvertent shorting to the exposed back side pad.

Soldering the back side pad of the device to a thermal land connected to the PCB ground plane is recommended for electrical and EMI considerations. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

The recommended pad size for the grounded thermal land is 5.6mm minimum, centered in the device land pattern. When vias are required to ground the land, multiple vias are recommended for a low impedance connection to the ground plane. Vias in the exposed pad should be small enough or filled to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow.



More information on this package and other requirements for using thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: <http://www.ti.com>

Table 1 outlines the thermal properties of the TI 100-TQFP...

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