Synchronous Buck NexFET™ Power Stage

FEATURES

- 92% System Efficiency at 30A
- High Frequency Operation (Up To 2MHz)
- High Density – SON 5-mm × 6-mm Footprint
- Low Power Loss 3.4W at 30A
- Ultra Low Inductance Package
- System Optimized PCB Footprint
- 3.3V and 5V PWM Signal Compatible
- 3-State PWM Input
- Integrated Bootstrap Diode
- Pre-Bias Start-Up Protection
- Shoot Through Protection
- RoHS Compliant – Lead Free Terminal Plating Halogen Free

APPLICATIONS

- Synchronous Buck Converters
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters
- Memory and Graphic Cards
- Desktop and Server VR11.x and VR12 V-Core Synchronous Buck Converters

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD96371Q5M	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

DESCRIPTION

The CSD96371Q5M NexFET™ Power Stage has an optimized design for use in a high power high density Synchronous Buck converter. This product integrates the gate driver IC and Power MOSFETs to complete the power stage switching function. This combination produces high current, high efficiency, and high speed switching capability in a small 5-mm × 6-mm outline package. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

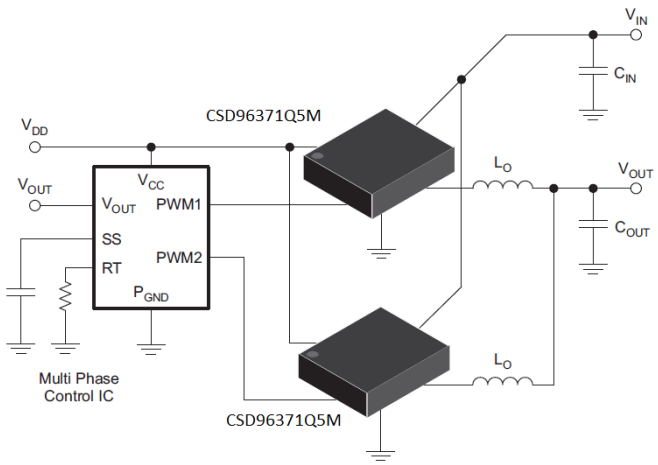


Figure 1. Application Diagram

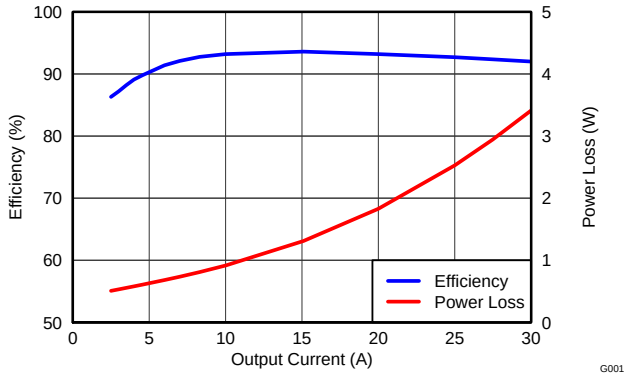


Figure 2. Efficiency and Power Loss

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

T_A = 25°C (unless otherwise noted)

		VALUE	UNIT
V_{IN} to P_{GND} (2)		–0.3 to 16	V
V_{DD} to P_{GND}		–0.3 to 6	V
V_{SW} to P_{GND}		-0.3 to 25	V
V_{SW} to P_{GND}(10ns)		-7 to 27	V
ENABLE to P_{GND} (3)		–0.3 to V_{DD} + 0.3	V
PWM to P_{GND} (3)		–0.3 to V_{DD} + 0.3	V
BOOT to BOOT_R (3)		–0.3 to V_{DD} + 0.3	V
ESD Rating	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	500	V
Power Dissipation, P_D		12	W
Storage Temperature Range, T_{STG}		–55 to 150	°C
Operating Temperature Range,		-40 to 150	°C

(1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability.
(2) V_{IN} to V_{SW} Max = 27V for 10ns
(3) Should not exceed 6V

RECOMMENDED OPERATING CONDITIONS

T_A = 25° (unless otherwise noted)

Parameter	Conditions	MIN	MAX	UNIT
Gate Drive Voltage, V_{DD}		4.5	5.5	V
Input Supply Voltage, V_{IN}		3.3	13.2	V
Output Voltage, V_{OUT}			5.5	V
Continuous Output Current, I_{OUT}	V_{IN} = 12V, V_{DD} = 5V, V_{OUT} = 1.2V, f_{SW} = 500kHz, L_{OUT} = 0.3µH (1)		50	A
Peak Output Current, I_{OUT-PK} (2)			75	A
Switching Frequency, f_{SW}	C_{BST} = 0.1µF (min)	200	2000	kHz
On Time Duty Cycle			85%	
Minimum PWM On Time		40		ns
Operating Temperature		–40	125	°C

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) System conditions as defined in Note 1. Peak Output Current is applied for t_p = 50µs.

THERMAL INFORMATION

T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Top of package) (1)			20	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (2)			2	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2 oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch, 0.06-inch (1.52-mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1mm of the package.

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ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = POR to 5.5V (unless otherwise noted)

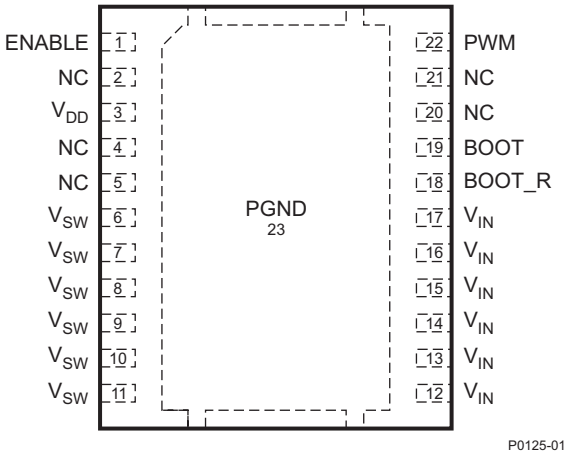
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}					
Power Loss(1)	V_{IN} = 12V, V_{DD} = 5V, V_{OUT} = 1.2V, I_{OUT} = 30A, f_{SW} = 500kHz, L_{OUT} = 0.29µH , T_J = 25°C		3.4	3.7	W
Power Loss(2)	V_{IN} = 12V, V_{DD} = 5V, V_{OUT} = 1.2V, I_{OUT} = 50A, f_{SW} = 500kHz, L_{OUT} = 0.29µH , T_J = 125°C		10.6	11.7	W
V_{IN}					
V_{IN} Quiescent Current (I_Q)	ENABLE = 0V, V_{DD} = 5V			100	µA
V_{DD}					
Standby Supply Current (I_{DD})	ENABLE = 0V, PWM = 0V			5	µA
Operating Supply Current (I_{DD})	ENABLE = 5V, PWM = 50% Duty cycle, f_{SW} = 500kHz		21	25	mA
POWER-ON RESET AND UNDER VOLTAGE LOCKOUT					
Power on Reset (V_{DD} Rising)			3.6	3.9	V
UVLO (V_{DD} Falling)		3.4	3.5		V
Hysteresis		100		250	mV
Startup Delay(3)	ENABLE = PWM = 5V		600	1000	ns
ENABLE					
Logic Level Low Threshold (V_{IL})	Schmitt Trigger Input PWM = 5V (See Figure 5)	0.8	1		V
Logic Level High Threshold (V_{IH})			1.6	2.0	V
Threshold Hysteresis			580		mV
Weak Pull-down Impedance			100		kΩ
Rising Propagation Delay (t_{PDH})			600		ns
Falling Propagation Delay (t_{PDL})			200		ns
PWM					
I_{PWMH}	PWM = 5V		620	800	µA
I_{PWML}	PWM = 0V		–260	–340	µA
PWM Logic Level High (V_{PWMH})	V_{DD} = POR to 5.5V, C_{PWM} = 10pF (See Figure 6)			2.2	V
PWM Logic Level Low (V_{PWML})		0.8			V
PWM 3-State open Voltage			1.5		V
PWM to VSW propagation delay (t_{PDLH} and t_{PDHL})			100		ns
3-State Shutdown Hold-off Time (t_{3HT})			100		ns
3-State Shutdown Propagation Delay (t_{3SD})			650		ns
3-State Recovery Propagation Delay (t_{3RD})			75		ns
BOOTSTRAP SWITCH					
Forward Voltage (V_{FBOOT})	V_{DD} – V_{BOOT}, I_F = 20mA		180	360	mV
Reverse Leakage (I_{RBOOT})(2)	V_{BOOT} – V_{DD} = 20V		0.15	1	µA

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) Specified by design
(3) POR to V_{SW} rising

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PIN CONFIGURATION

SON 5mm × 6mm
22-Pin Package
(Top View)



PIN DESCRIPTION

PIN		DESCRIPTION
NO.	NAME	
1	ENABLE	Enables device operation. If ENABLE=logic HIGH, turns on the device. If ENABLE=logic LOW, the device is turned off and MOSFET gates are actively pulled low. An internal 100kΩ pull down resistor will pull the ENABLE pin LOW if left floating.
2	NC	Not for electrical connection, connect to floating pad only.
3	V_{DD}	Supply Voltage to Gate Drivers and internal circuitry.
4	NC	Not for electrical connection, connect to floating pad only.
5	NC	Not for electrical connection, connect to floating pad only.
6	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
7	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
8	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
9	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
10	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
11	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
12	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
13	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
14	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
15	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
16	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
17	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
18	BOOT_R	Bootstrap capacitor connection. Connect a minimum 0.1µF 16V X5R, ceramic cap from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the Control FET. The bootstrap diode is integrated.
19	BOOT	
20	NC	Not for electrical connection, connect to floating pad only.
21	NC	Not for electrical connection, connect to floating pad only.
22	PWM	Pulse Width modulated 3-state input from external controller. Logic Low sets Control FET gate low and Sync FET gate high. Logic High sets Control FET gate high and Sync FET gate Low. Open or High Z sets both MOSFET gates low if greater than the 3-State Shutdown Hold-off Time (t_{3HT})
23	P_{GND}	Power Ground

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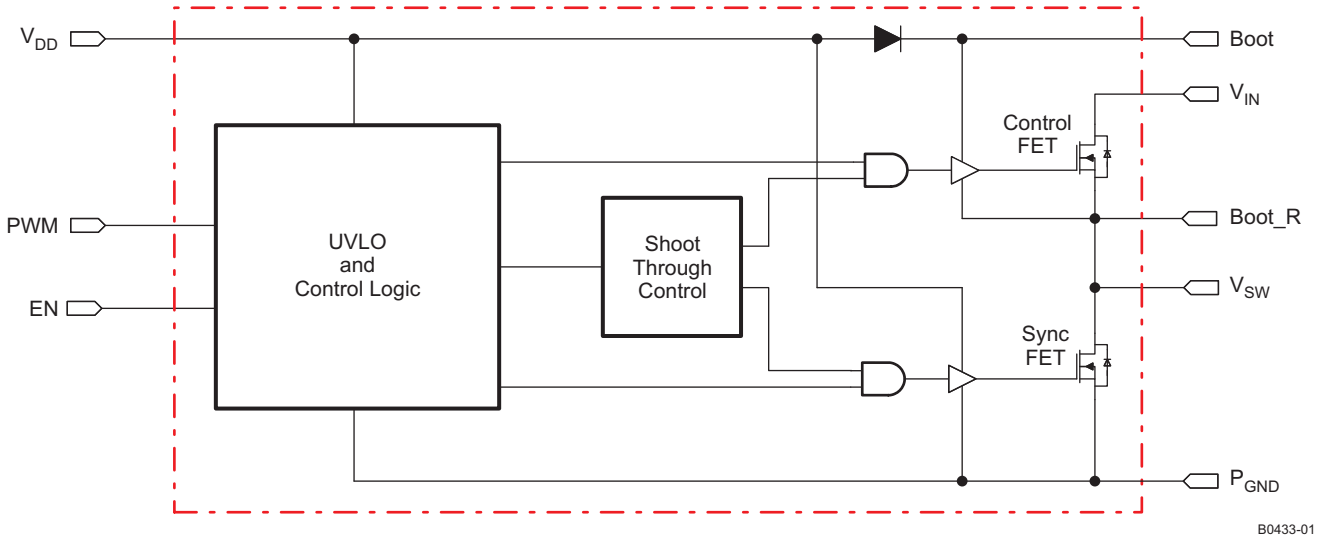


Figure 3. Functional Block Diagram

FUNCTIONAL DESCRIPTION

POWERING CSD96371Q5M AND GATE DRIVERS

An external V_{DD} voltage is required to supply the integrated gate driver IC and provide the necessary gate drive power for the MOSFETS. The gate driver IC is capable of supplying in excess of 4 Amps peak current into the MOSFET gates to achieve fast switching. A 1uF 10V X5R or higher ceramic capacitor is recommended to bypass V_{DD} pin to PGND. A bootstrap circuit to provide gate drive power for the Control FET is also included. The bootstrap supply to drive the Control FET is generated by connecting a 100nF 16V X5R ceramic capacitor between BOOT and BOOT_R pins. An optional R_{BOOT} resistor which can be used to slow down the turn on speed of the Control FET and reduce voltage spikes on the Vsw node. A typical 1Ω to 4.7Ω value is a compromise between switching loss and V_{SW} spike amplitude.

UVLO (Under Voltage Lock Out)

The V_{DD} supply is monitored for UVLO conditions and both Control FET and Sync FET gates are held low until adequate supply is available. An internal comparator evaluates the V_{DD} voltage level and if V_{DD} is greater than the Power On Reset threshold (V_{POR}) the gate driver becomes active. If V_{DD} is less than the UVLO threshold, the gate driver is disabled and the internal MOSFET gates are actively driven low. At the rising edge of the V_{DD} voltage, both Control FET and Sync FET gates will be actively held low during V_{DD} transitions between 1.0V to V_{POR}. This region is referred to the Gate Drive Latch Zone (see Figure 4). In addition, at the falling edge of the V_{DD} voltage, both Control FET and Sync FET gates are actively held low during the UVLO to 1.0V transition.

The Power Stage CSD96371Q5M device must be powered up and Enabled before the PWM signal is applied.

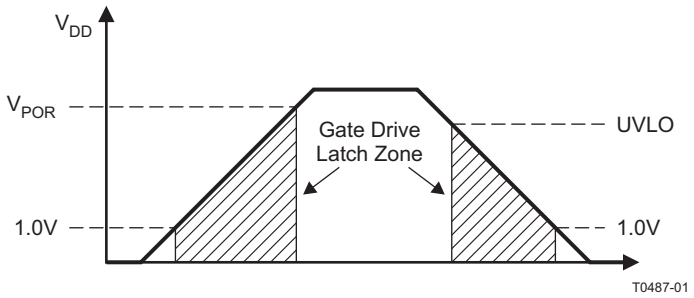


Figure 4. POR and UVLO

ENABLE

The ENABLE pin is TTL compatible. The logic level thresholds are sustained under all V_{DD} operating conditions between V_{POR} to V_{DD}. In addition, if this pin is left floating, a weak internal pull down resistor of 100kΩ will pull the ENABLE pin below the logic level low threshold. The operational functions of this pin should follow the timing diagram outlined in Figure 5. A logic level low will actively hold both Control FET and Sync FET gates low and V_{DD} pin should typically draw less than 5µA.

POWER UP SEQUENCING

If the ENABLE signal is used, it is necessary to ensure proper co-ordination with the ENABLE and soft-start features of the external PWM controller in the system. If the CSD96371Q5M was disabled through ENABLE without sequencing with the PWM IC controller, the buck converter output will have no voltage or fall below regulation set point voltage. As a result, the PWM controller IC delivers Max duty cycle on the PWM line. If the Power Stage CSD96371Q5M is re-enabled by driving the ENABLE pin high, there will be an extremely large input inrush current when the output voltage builds back up again. The input inrush current might have undesirable consequences such as inductor saturation, driving the input power supply into current limit or even catastrophic failure of the CSD96371Q5M device. Disabling the PWM controller is recommended when the CSD96371Q5M is disabled. The PWM controller should always be re-enabled by going through soft-start routine to control and minimize the input inrush current and reduce current and voltage stress on all buck converter components. It is recommended that the external PWM controller be disabled when CSD96371Q5M is disabled or nonoperational because of UVLO.

PWM

The input PWM pin incorporates a 3-State function. The Control FET and Sync FET gates are forced low if the PWM pin is left floating for more than the 3-State Hold off time (t_{3HT}), typically 100ns. This requires the source impedance of the driving PWM signal to be a minimum of 250kΩ when in 3-State mode. Operation in and out of 3-State mode should follow the timing diagram outlined in Figure 6. Both V_{PWML} and V_{PWMH} threshold levels are set to accommodate both 3.3V and 5V logic controllers. During normal operation, the PWM signal should be driven to logic levels Low and High with a maximum of 220Ω/320Ω sink/source impedance respectively.

GATE DRIVERS

The CSD96371Q5M has an internal high-performance gate driver IC that ensures minimum MOSFET dead-time while eliminating potential shoot-through currents. Propagation delays between the Control FET and Sync FET gates are kept to a minimum to minimize body diode conduction and improve efficiency. The gate driver IC incorporates an adaptive shoot through protection scheme which ensures that neither MOSFET is turned on while the other one is still conducting at the same time, preventing cross conduction. See Table 1.

Table 1. Truth Table

ENABLE	PWM	CONTROL FET GATE	SYNC FET GATE	V_{SW}
L	X	L	L	3-State
H	<Min ON time	L	L	3-State
H	L	L	H	P_{GND}
H	3-State	L	L	3-State
H	H	H	L	V_{IN}
L = Logic Low; H = Logic High; X = Don't care; minimum on time = 40ns				

START UP IN PRE-BIASED OUTPUT VOLTAGE

The CSD96371Q5M incorporates a simple pre-bias feature to protect against the discharging of a prebiased output voltage and inducing large negative inductor currents. After the Power On Reset threshold is crossed and the ENABLE pin is set to logic level high, both internal MOSFETs are actively held low until the PWM pin receives a signal that crosses logic level high threshold and meets the minimum on time criteria (see the *Electrical Characteristics Table*). This allows the PWM control IC to provide a soft start routine that creates a monotonic startup of the output voltage. The pre-bias feature is enabled for a single event and subsequent PWM signals creates normal switching of the internal MOSFETs (see Table 1). To reactivate the pre-bias feature, the ENABLE pin needs to be pulled below logic level low or the V_{DD} supply voltage needs to cross UVLO.

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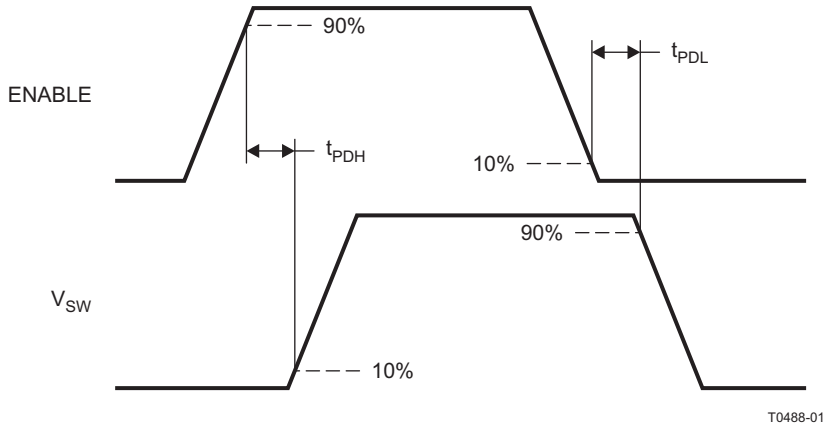


Figure 5. CSD96371Q5M ENABLE Timing Diagram (V_{DD} = PWM = 5V)

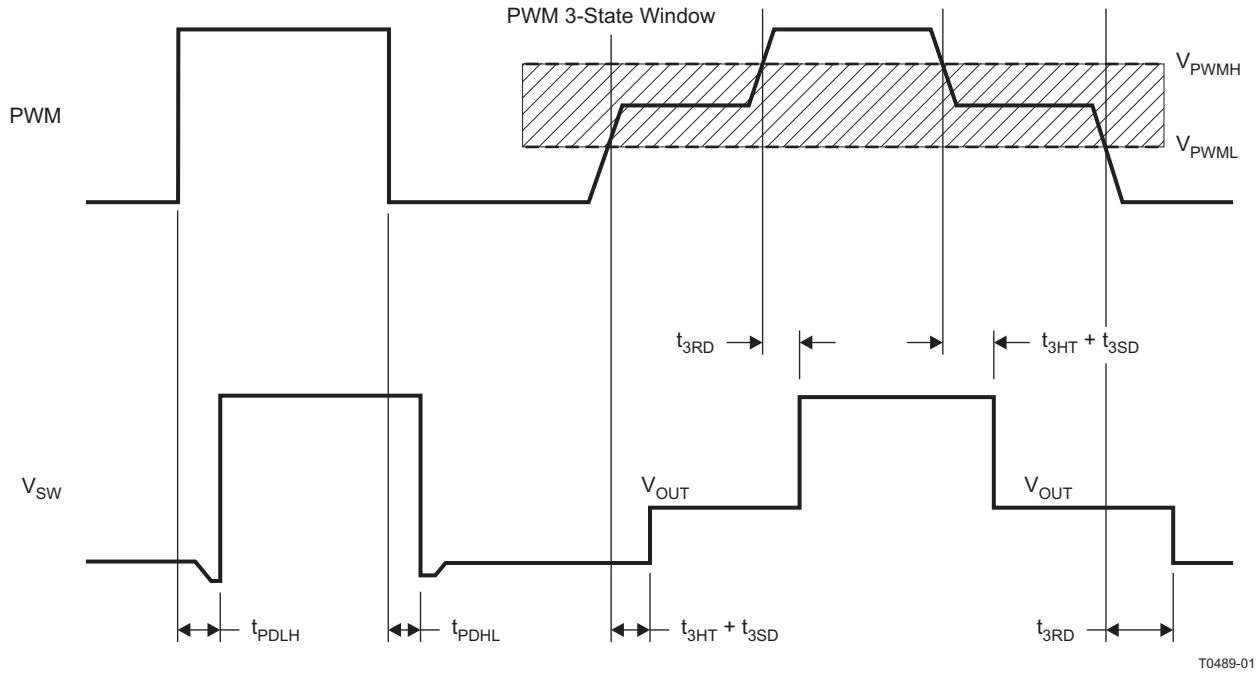


Figure 6. CSD96371Q5M PWM Timing Diagram

TYPICAL CHARACTERISTICS

Test conditions: V_{IN} = 12V, V_{DD} = 5V, f_{SW}= 500kHz, V_{OUT} = 1.2V, L_{OUT} = 0.29µH, DCR = 0.54mΩ, T_J = 125°C (Unless otherwise stated)

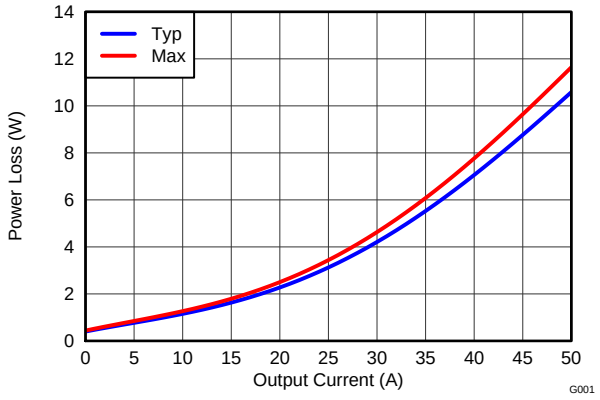


Figure 7. Power Loss vs Output Current

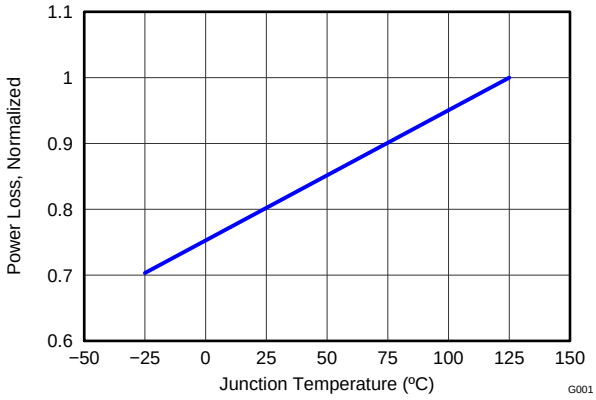


Figure 8. Power Loss vs Temperature

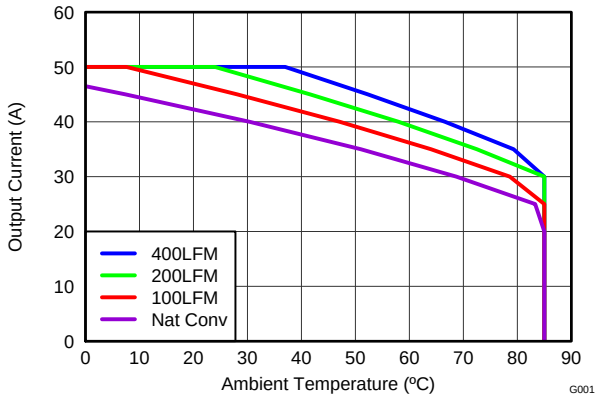


Figure 9. Safe Operating Area – PCB Horizontal Mount (1)

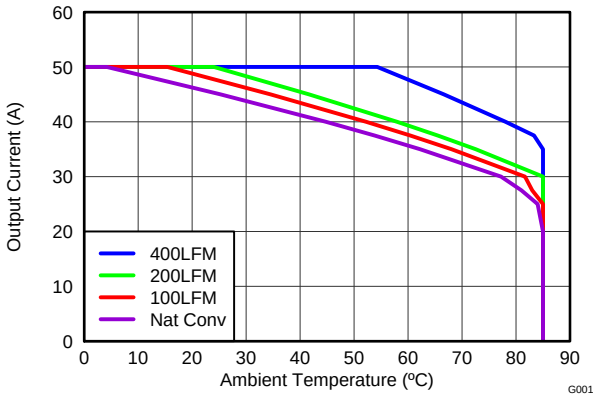


Figure 10. Safe Operating Area – PCB Vertical Mount (1)

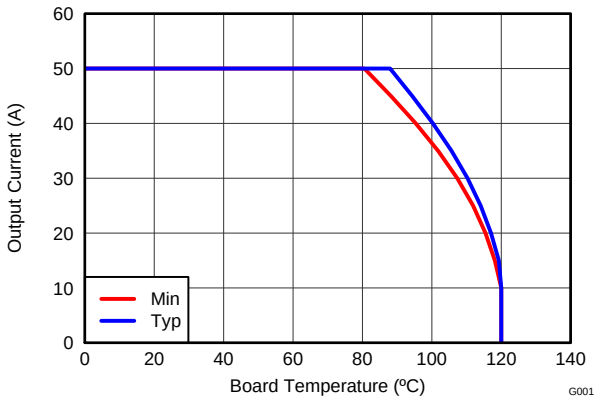


Figure 11. Typical and Min Safe Operating Area (1)

1. The Typical CSD96371Q5M System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness. See the *Application section* for detailed explanation.

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TYPICAL CHARACTERISTICS (continued)

Test conditions: V_{IN} = 12V, V_{DD} = 5V, f_{SW}= 500kHz, V_{OUT} = 1.2V, L_{OUT} = 0.29µH, DCR = 0.54mΩ, T_J = 125°C (Unless otherwise stated)

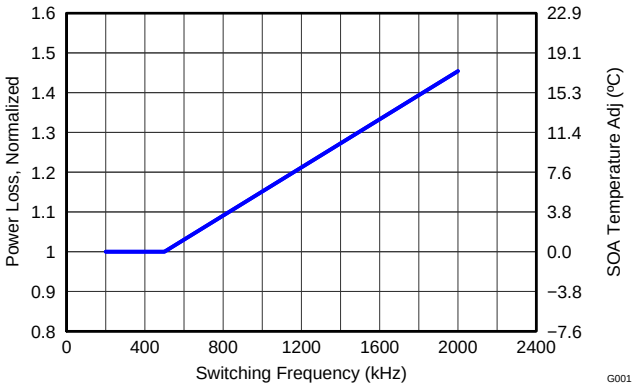


Figure 12. Normalized Power Loss vs Frequency

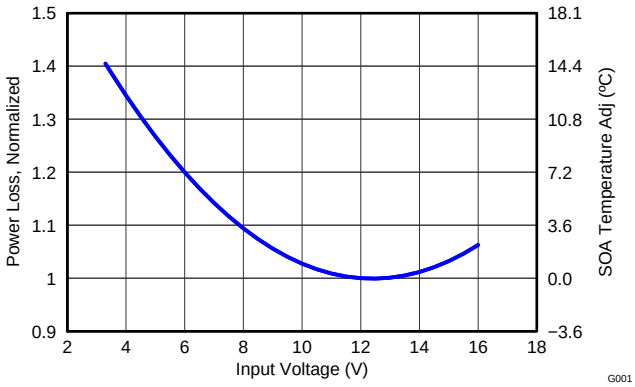


Figure 13. Normalized Power Loss vs Input Voltage

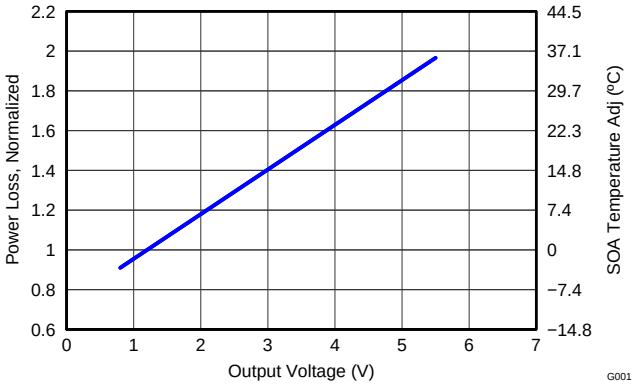


Figure 14. Normalized Power Loss vs Output Voltage

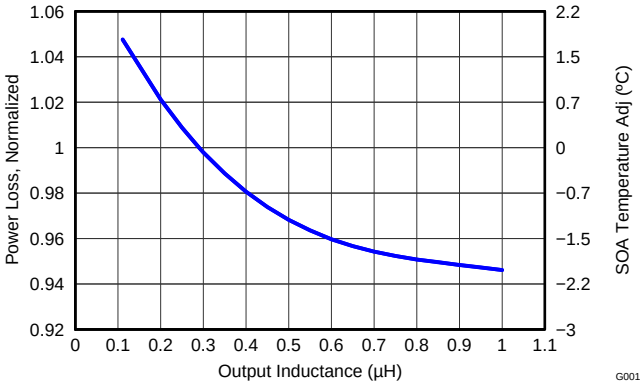


Figure 15. Normalized Power Loss vs Output Inductance

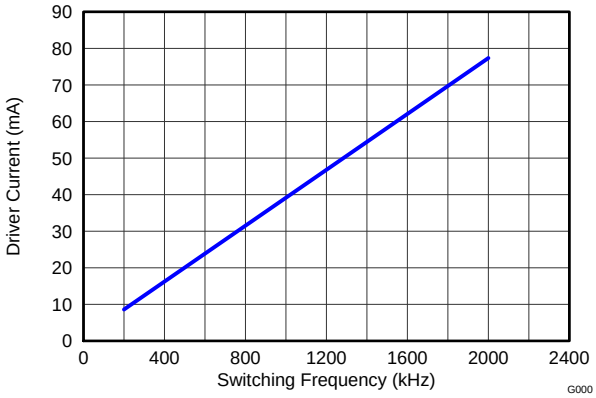


Figure 16. Driver Current vs Frequency

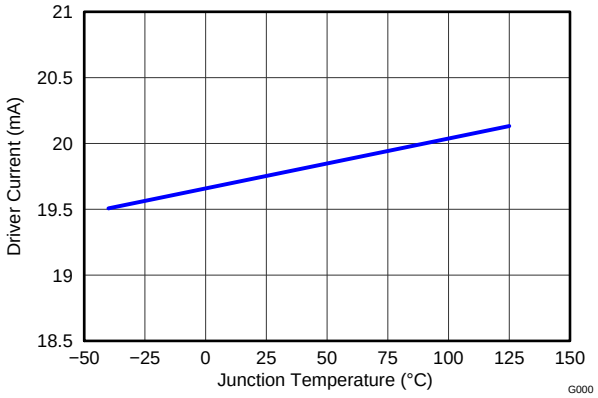


Figure 17. Driver Current vs Temperature

APPLICATION INFORMATION

The Power Stage CSD96371Q5M is a highly optimized design for synchronous buck applications using NexFET devices with a 5V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems centric environment. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the power MOSFETs. System level performance curves such as Power Loss, Safe Operating Area and normalized graphs allow engineers to predict the product performance in the actual application.

Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are primarily needed by engineers to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 7 plots the power loss of the CSD96371Q5M as a function of load current. This curve is measured by configuring and running the CSD96371Q5M as it would be in the final application (see Figure 18). The measured power loss is the CSD96371Q5M device power loss which consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\text{Power Loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 7 is measured at the maximum recommended junction temperature of T_J = 125°C under isothermal test conditions.

Safe Operating Curves (SOA)

The SOA curves in the CSD96371Q5M datasheet give engineers guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 9, Figure 10, and Figure 11 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness.

Normalized Curves

The normalized curves in the CSD96371Q5M data sheet give engineers guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

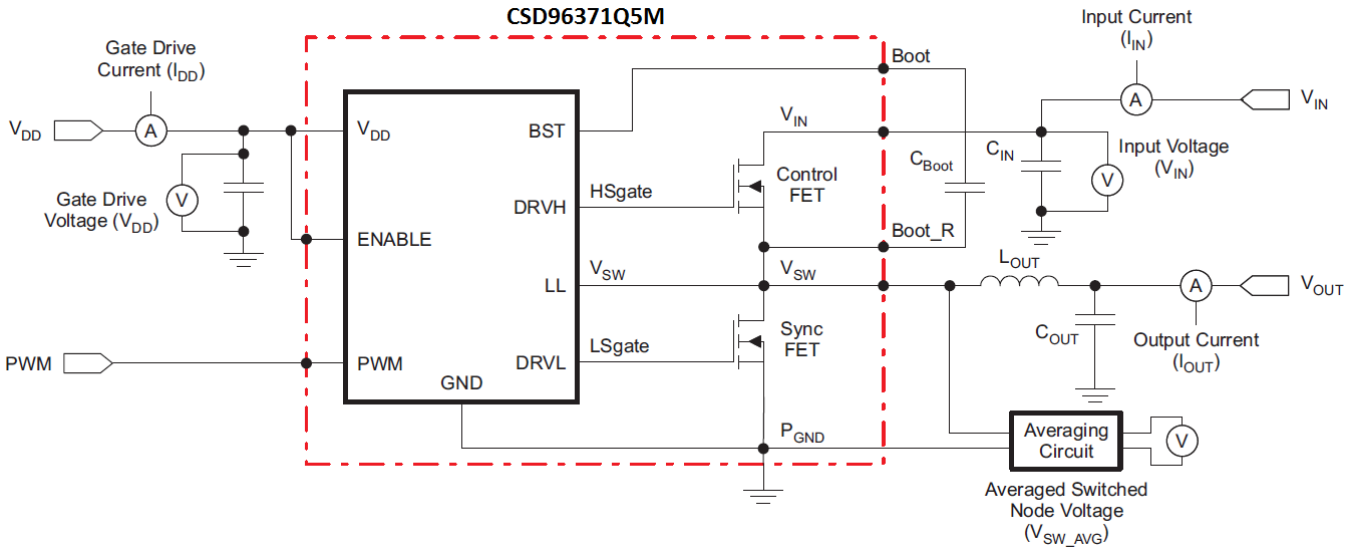


Figure 18. Power Loss Test Circuit

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Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see the Design Example). Though the Power Loss and SOA curves in this datasheet are taken for a specific set of test conditions, the following procedure will outline the steps engineers should take to predict product performance for any set of system conditions.

Design Example

Operating Conditions: Output Current (I_{OUT}) = 25A, Input Voltage (V_{IN}) = 7V, Output Voltage (V_{OUT}) = 1V, Switching Frequency (f_{SW}) = 800kHz, Output Inductor (L_{OUT}) = 0.2µH

Calculating Power Loss

- Power Loss at 25A = 3.1W (Figure 7)
- Normalized Power Loss for switching frequency ≈ 1.09 (Figure 12)
- Normalized Power Loss for input voltage ≈ 1.15 (Figure 13)
- Normalized Power Loss for output voltage ≈ 0.95 (Figure 14)
- Normalized Power Loss for output inductor ≈ 1.02 (Figure 15)
- **Final calculated Power Loss = 3.1W × 1.09 × 1.15 × 0.95 × 1.02 ≈ 3.8W**

Calculating SOA Adjustments

- SOA adjustment for switching frequency ≈ 3.4°C (Figure 12)
- SOA adjustment for input voltage ≈ 5.4°C (Figure 13)
- SOA adjustment for output voltage ≈ –7.7°C (Figure 14)
- SOA adjustment for output inductor ≈ 1.7°C (Figure 15)
- **Final calculated SOA adjustment = 3.4 + 5.4 + (–1.9) + 0.7 ≈ 7.6°C**

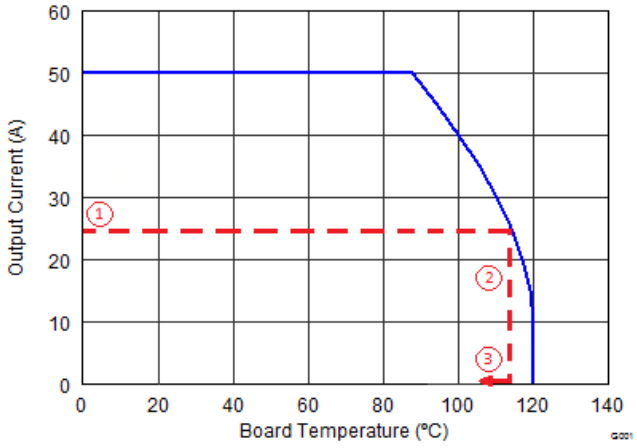


Figure 19. Power Stage CSD96371Q5M SOA

In the design example above, the estimated power loss of the CSD96371Q5M would increase to 3.8W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 7.6°C. Figure 19 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 7.6°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

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RECOMMENDED PCB DESIGN OVERVIEW

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. Below is a brief description on how to address each parameter.

Electrical Performance

The CSD96371Q5M has the ability to switch at voltages rates greater than 10kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, inductor and output capacitors.

- The placement of the input capacitors relative to V_{IN} and P_{GND} pins of CSD96371Q5M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the V_{IN} and P_{GND} pins (see Figure 20). The example in Figure 20 uses 6 x 10µF 1206 25V ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C5, C8 and C7, C19 should follow in order.
- The bootstrap cap C_{BOOT} 0.1µF 0603 16V ceramic capacitor should be closely connected between BOOT and BOOT_R pins
- The switching node of the output inductor should be placed relatively close to the Power Stage CSD96371Q5M V_{SW} pins. Minimizing the V_{SW} node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. (1)

Thermal Performance

The CSD96371Q5M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 20 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

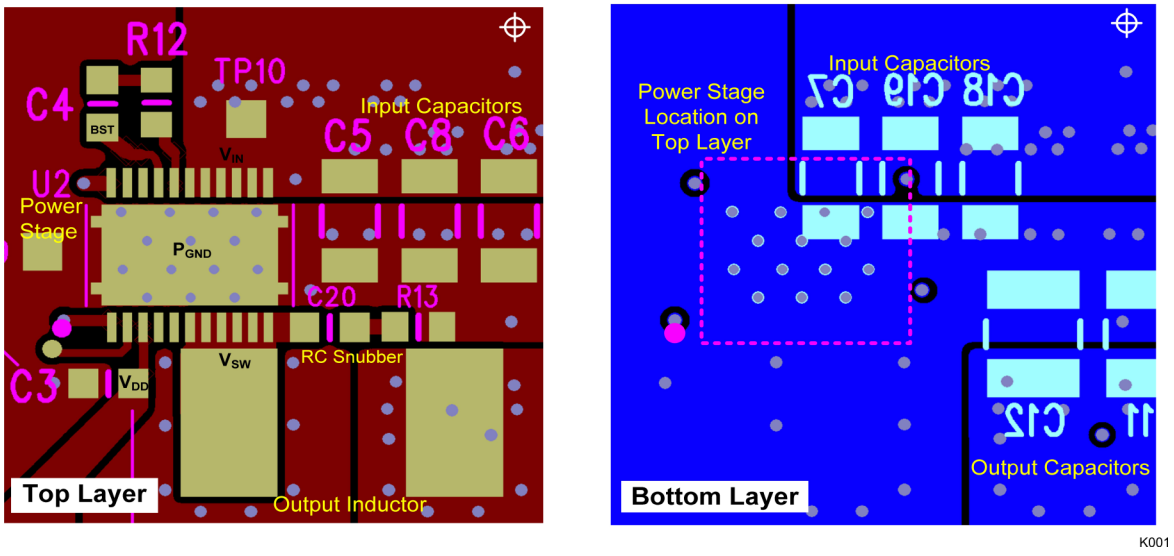
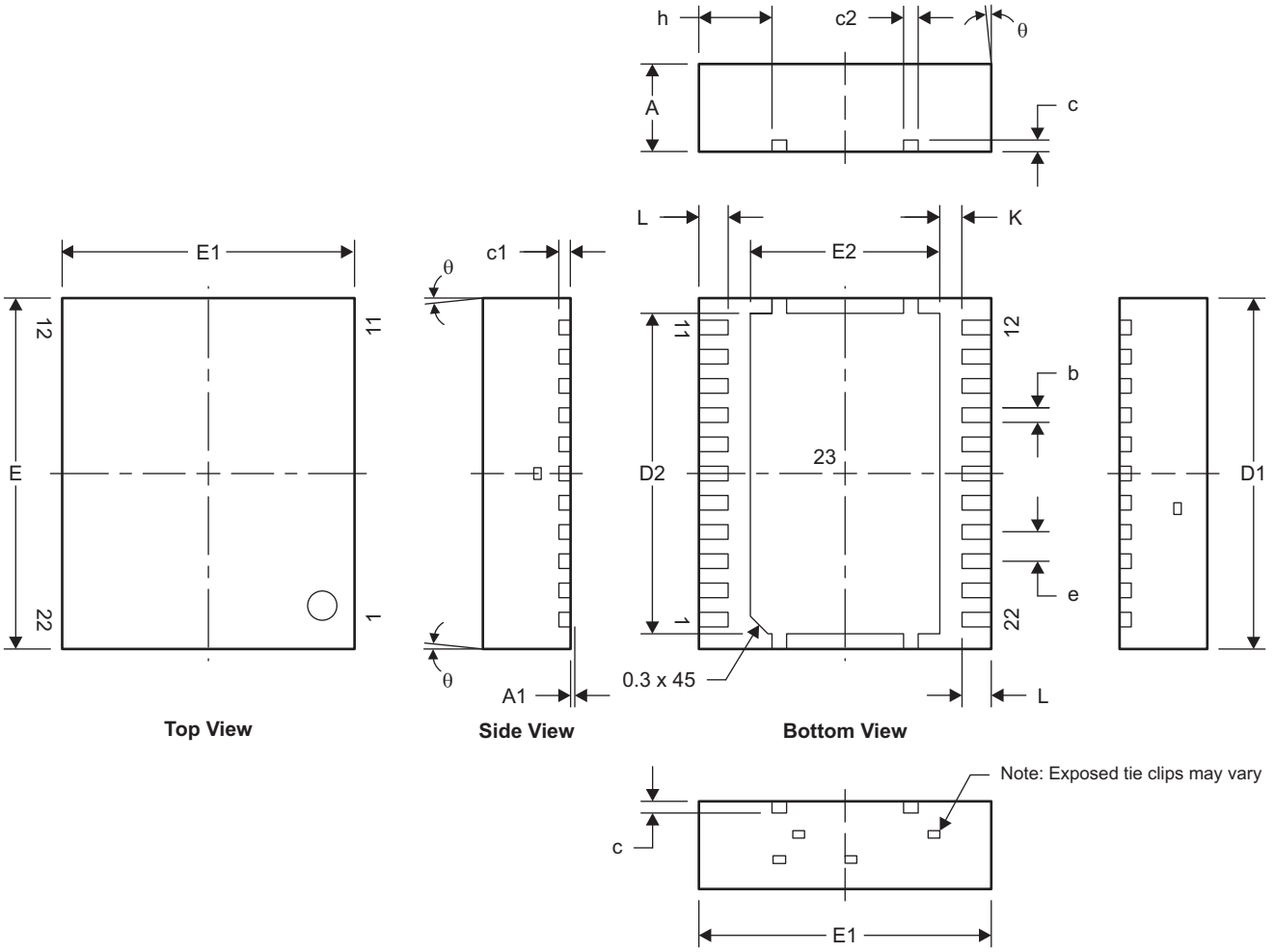


Figure 20. Recommended PCB Layout (Top Down View)

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

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MECHANICAL DATA

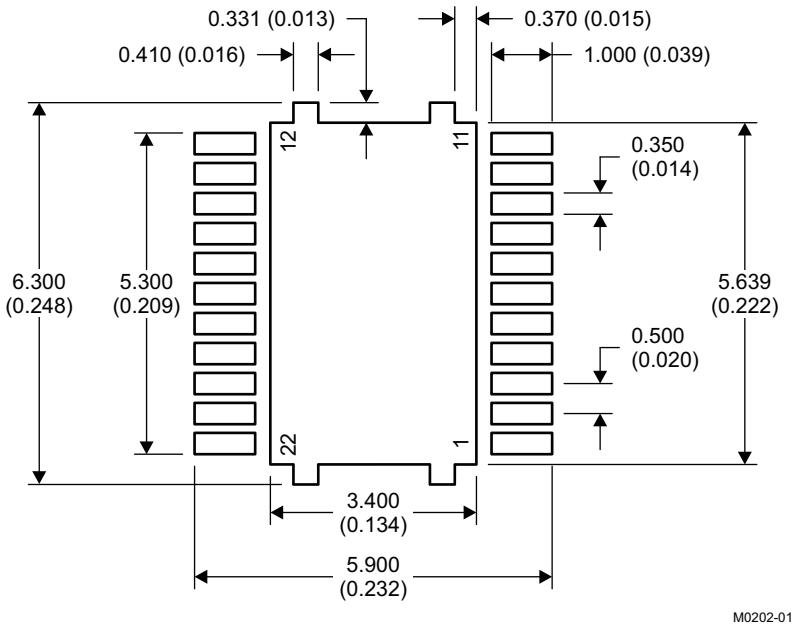


M0201-01

DIM	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.400	1.450	1.500	0.055	0.057	0.059
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.350	0.008	0.010	0.014
c	0.150	0.200	0.250	0.006	0.008	0.010
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.200	0.250	0.300	0.008	0.010	0.012
D1	5.900	6.000	6.100	0.232	0.236	0.240
D2	5.379	5.479	5.579	0.212	0.216	0.220
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.140	3.240	3.340	0.124	0.128	0.132
e		0.500 TYP			0.020 TYP	
h	1.150	1.250	1.350	0.045	0.049	0.053
K		0.380 TYP			0.015 TYP	
L	0.400	0.500	0.600	0.016	0.020	0.024
θ	0.00	—	—	0.00	—	—

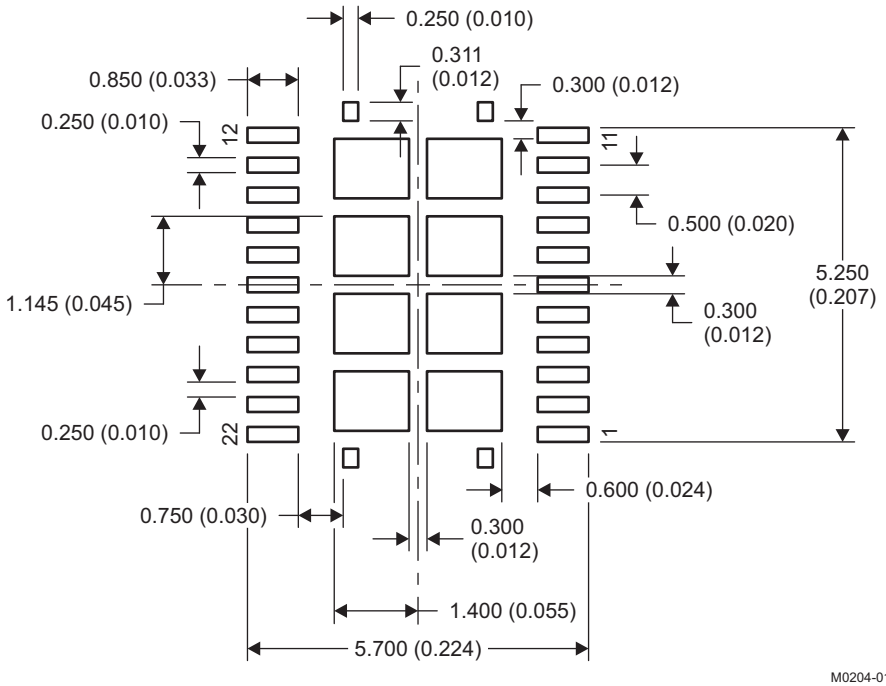
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Land Pattern Recommendation



NOTE: Dimensions are in mm (inches).

Stencil Recommendation



NOTE: Dimensions are in mm (inches).

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD96371Q5M	ACTIVE	LSON-CLIP	DQP	22	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	96371M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

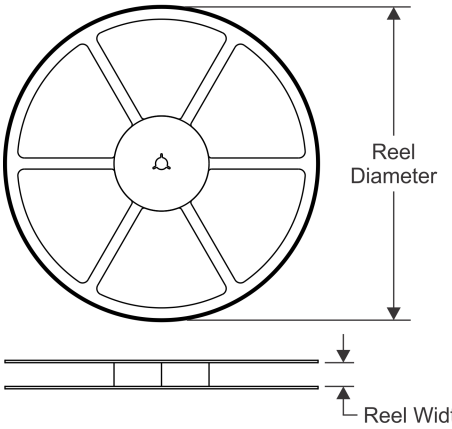
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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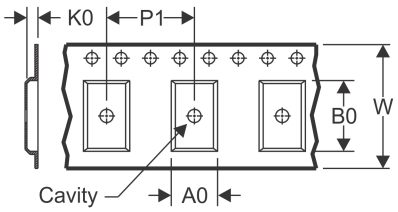
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

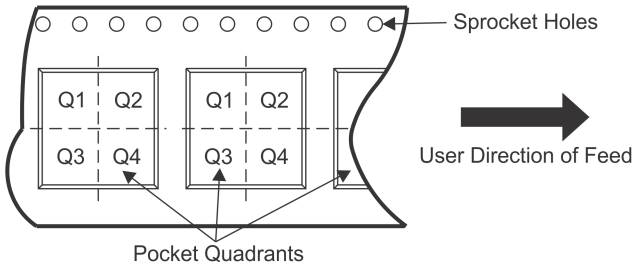


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

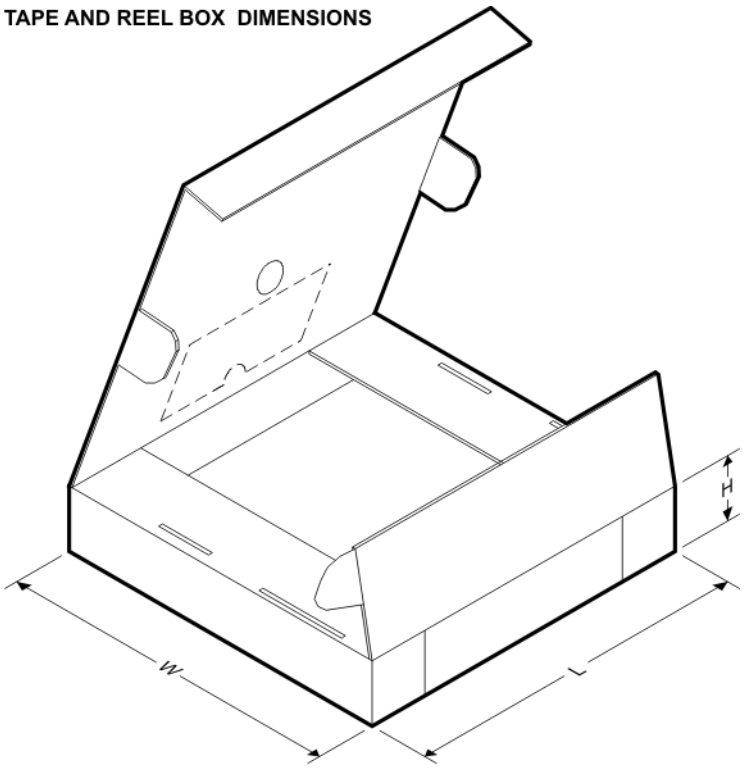
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD96371Q5M	LSON-CLIP	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD96371Q5M	LSON-CLIP	DQP	22	2500	367.0	367.0	35.0

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