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March 2015

# FDMS8050

## N-Channel PowerTrench® MOSFET
### 30 V, 200 A, 0.65 mΩ

## Features

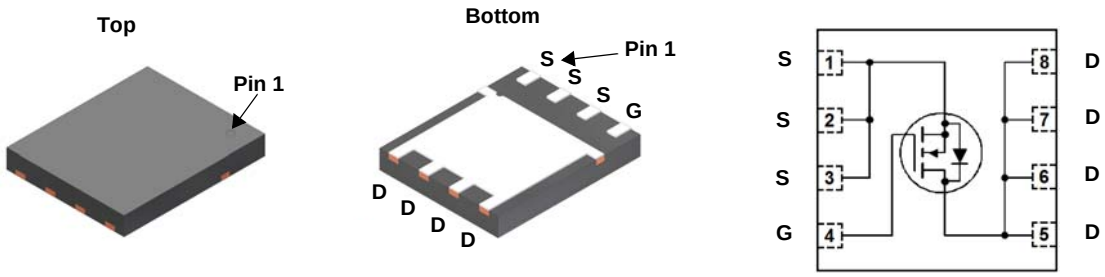
- Max $r_{DS(on)}$ = 0.65 mΩ at $V_{GS}$ = 10 V, $I_D$ = 55 A
- Max $r_{DS(on)}$ = 0.9 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 47 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

## General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge and extremely low $r_{DS(on)}$.

## Applications

- OringFET
- Synchronous Rectifier




Power 56

## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | | (Note 4) | ±20 | V |
| $I_D$ | Drain Current -Continuous | $T_C$ = 25 °C | | 200 | A |
| | -Continuous | $T_A$ = 25 °C | (Note 1a) | 55 | |
| | -Pulsed | | (Note 5) | 400 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 1536 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25 °C | | 156 | W |
| | Power Dissipation | $T_A$ = 25 °C | (Note 1a) | 2.7 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 0.83 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 45 | |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMS8050 | FDMS8050 | Power 56 | 13 ” | 12 mm | 3000 units |

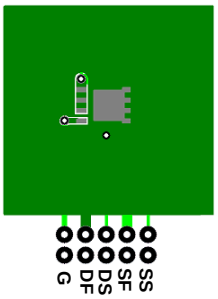
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## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

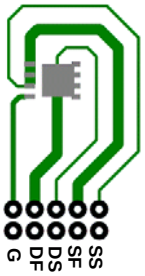
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 750 μA, $V_{GS}$ = 0 V | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 750 μA, referenced to 25 °C | | 20 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 750 μA | 1.0 | 1.8 | 3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 750 μA, referenced to 25 °C | | -6 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 55 A | | 0.5 | 0.65 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 47 A | | 0.7 | 0.9 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 55 A, $T_J$ = 125 °C | | 0.7 | 0.9 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 55 A | | 333 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz | | 16150 | 22610 | pF |
| $C_{oss}$ | Output Capacitance | | | 4455 | 6240 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 220 | 310 | pF |
| $R_g$ | Gate Resistance | | | 1.0 | 3.0 | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 55 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 29 | 47 | ns |
| $t_r$ | Rise Time | | | 22 | 36 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 87 | 139 | ns |
| $t_f$ | Fall Time | | | 16 | 28 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 15 V, $I_D$ = 55 A | | 204 | 285 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V; $V_{DD}$ = 15 V, $I_D$ = 55 A | | 93 | 130 | nC |
| $Q_{gs}$ | Gate to Source Charge | $V_{DD}$ = 15 V, $I_D$ = 55 A | | 41 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 15 V, $I_D$ = 55 A | | 18 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.2 A (Note 2) | | 0.64 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 55 A (Note 2) | | 0.74 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 55 A, di/dt = 100 A/μs | | 77 | 124 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 141 | 226 | nC |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.




a. 45 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper.




b. 115 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. $E_{AS}$ of 1536 mJ is based on starting $T_J$ = 25 °C, L = 3 mH, $I_{AS}$ = 32 A, $V_{DD}$ = 30 V, $V_{GS}$ = 10 V, 100% test at L = 0.3 mH, $I_{AS}$ = 69 A.
4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
5. Pulse Id limited by junction temperature, td ≤ 100 μs. Please refer to SOA curve for more details..

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## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

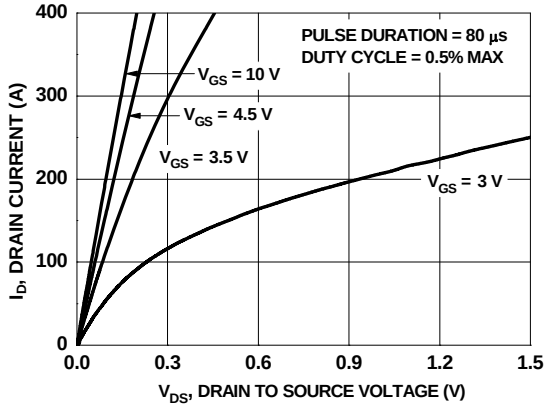



**Figure 1. On-Region Characteristics**

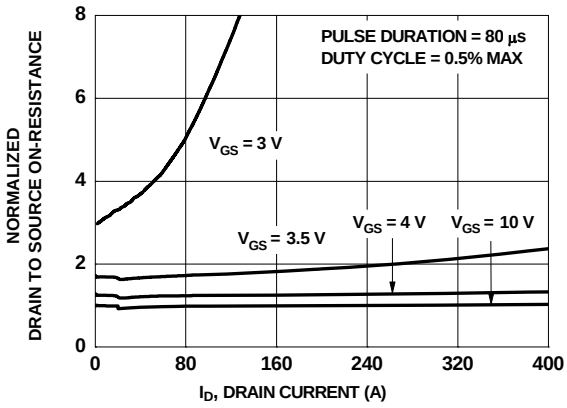



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

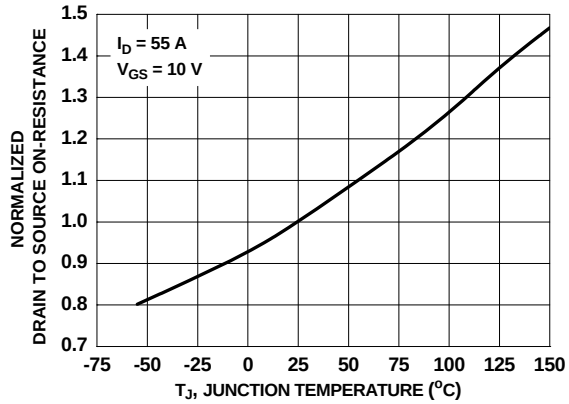



**Figure 3. Normalized On-Resistance vs Junction Temperature**

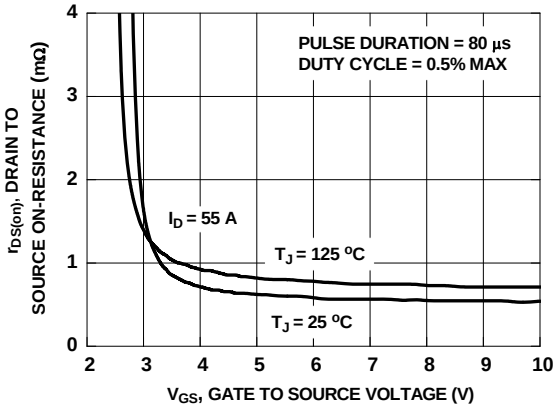



**Figure 4. On-Resistance vs Gate to Source Voltage**

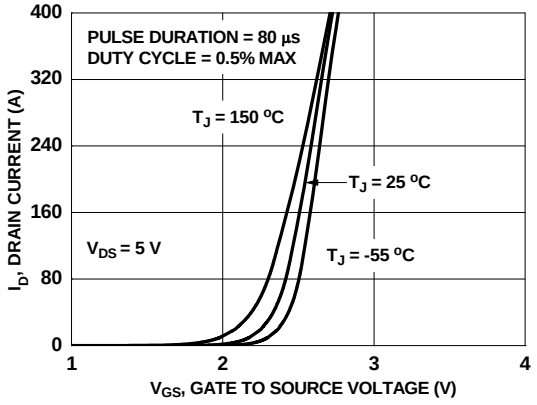



**Figure 5. Transfer Characteristics**

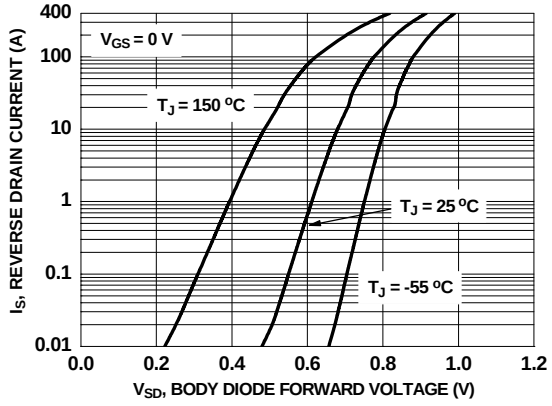



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

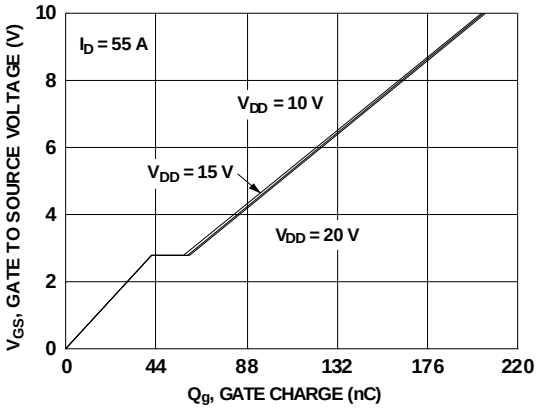



**Figure 7. Gate Charge Characteristics**

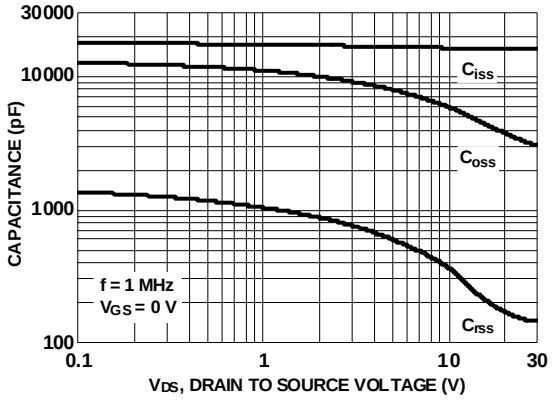



**Figure 8. Capacitance vs Drain to Source Voltage**

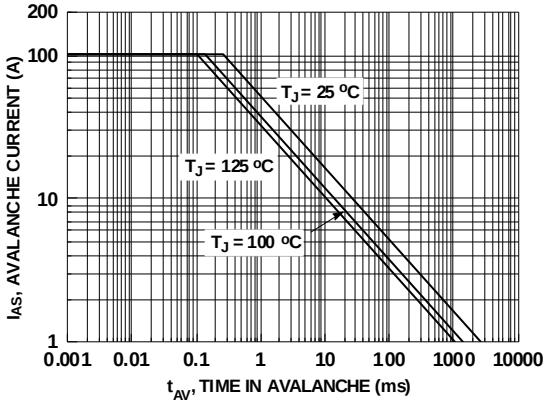



**Figure 9. Unclamped Inductive Switching Capability**

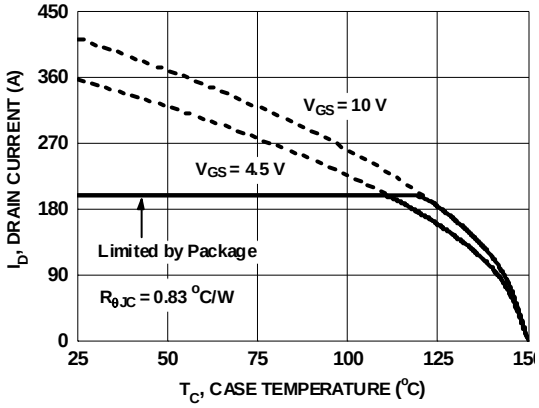



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

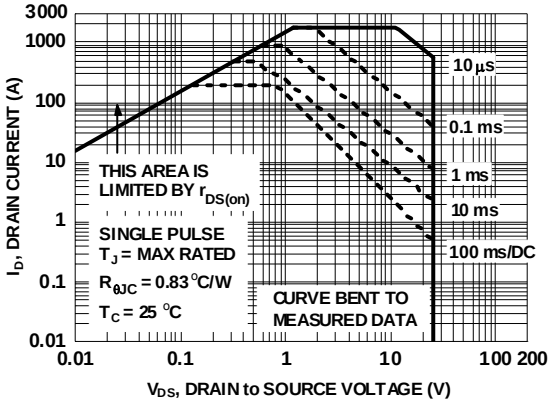



**Figure 11. Forward Bias Safe Operating Area**

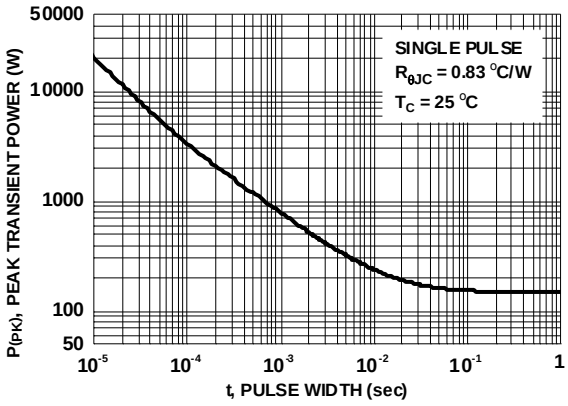



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

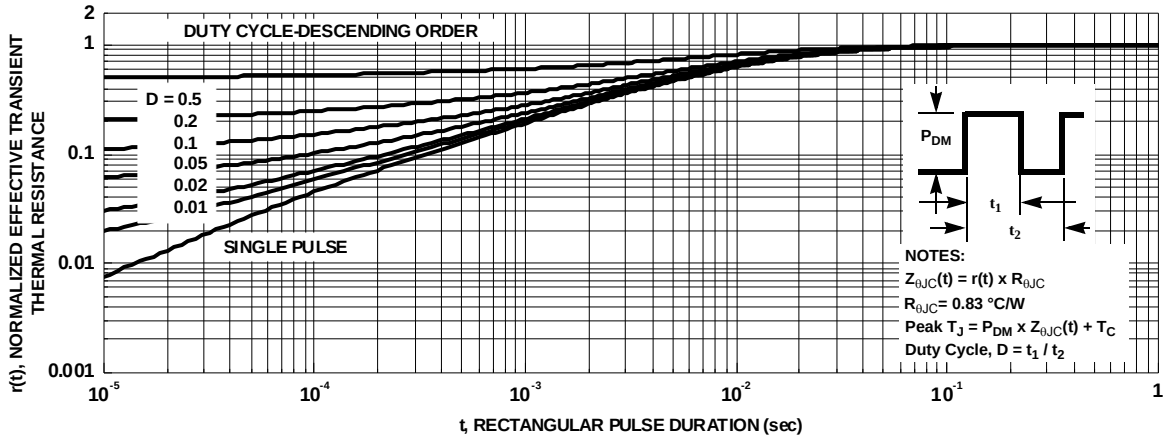
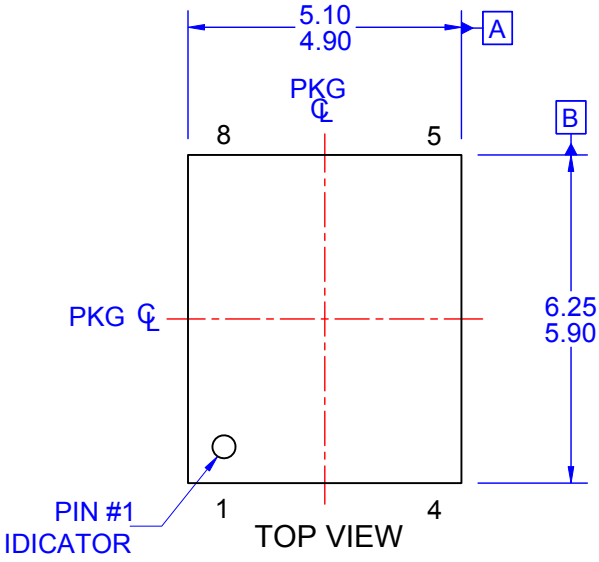
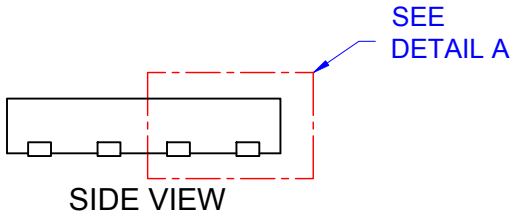
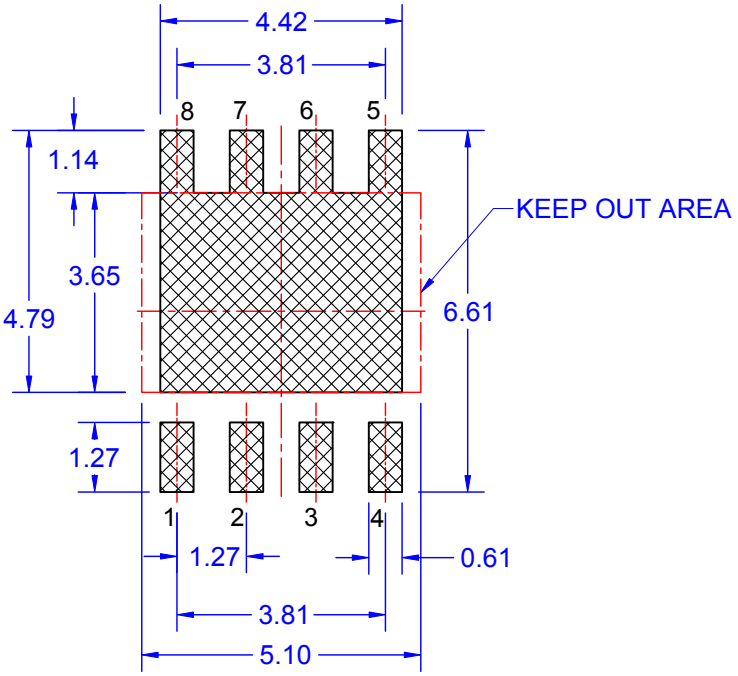
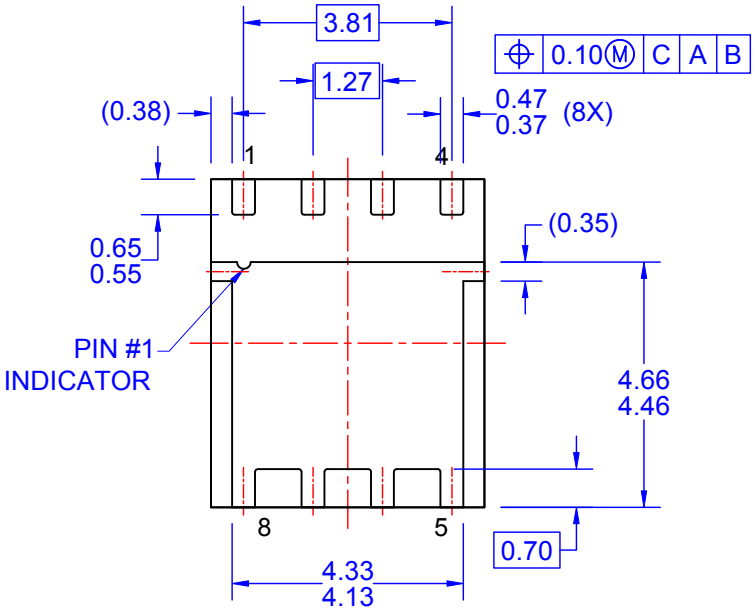



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**




NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,

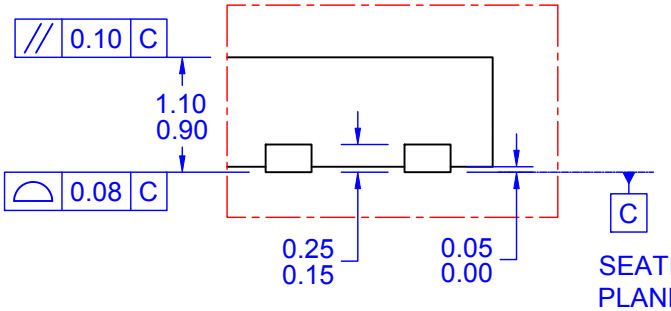
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**DETAIL A**

SCALE: 2:1

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