LM8365EVM User Guide

User's Guide

Literature Number: SNVU493
October 2015

Introduction

The Texas Instruments LM8365EVM evaluation module (EVM) helps designers evaluate the operation and performance of the LM8365 Micropower Undervoltage Supervisor with Programmable Output Delay. For this EVM, the 2.7 V reset threshold LM8365 will be used. The EVM demonstrates proper functionality of the LM8365 via selection of 3 distinct capacitors corresponding to programmable delay times. For more information about the LM8365 functional and electrical characteristics, consult the LM8365 datasheet (SNVS233).

The EVM contains one LM8365 Micropower Undervoltage Supervisor (See Table 1).

Table 1. Device and Package Configurations

REF DES	IC	PACKAGE
U1	LM8365BALMF27/NOPB	SOT-23

1 Features

- INPUT Voltage Range: 1 V to 6 V
- Extremely Low Quiescent Current: 0.65 µA, at VIN = 2.87 V
- Threshold Voltage of 2.7 V
- High Accuracy Threshold Voltage (± 2.5%)
- Active Low, Open Drain Output
- Surface Mount Package (5-Pin SOT-23)
- Programmable Output Delay
  - o 3 capacitor options for programmable delay
- Board Size: 1.50” x 1.15”

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Setup

This section describes the connectors on the EVM as well as how to properly connect, set up, and use the LM8365EVM. Ensure the external power supply is turned off while making connections on the board.

1 Input/Output Connector Description

- TP1 – VIN is the input power supply.
- TP2 – RST is the RESEToutput.
- TP3 – DLY is the positive side of the delay capacitor(s). This can be monitored to observe capacitor behavior during delay charging/discharging.
- TP4 – GND is the ground.

2 Header Description

- J1 is the header that selects the 0.01 µF capacitor for programmable delay.
- J2 is the header that selects the 0.1 µF capacitor for programmable delay.
- J3 is the header that selects the 1 µF capacitor for programmable delay.

3 Board Setup

Before applying power to the LM8365EVM, all external connections should be verified. An external power supply should be turned off and connected with proper polarity to the VIN (TP1) and GND (TP4) connectors. The input voltage range for the EVM is 1 V to 6 V. The RST (TP2) pin can be used to monitor the RESET output of the LM8365 in response to various input voltages. The DLY (TP3) terminal provides a means for observation of the capacitor charging/discharging behavior.

Furthermore, the LM8365EVM allows for programming of the RESET output time delay by selecting from 3 different sized capacitors through the use of headers J1, J2, and J3. These capacitors, labeled C1, C2, and C3 are 0.01 µF, 0.1 µF, and 1 µF respectively. To select a capacitor, the provided jumper should be connected to the respective header. If the jumpers are left unpopulated, the EVM will be programmed with the minimum amount of delay. Multiple capacitors can also be connected in parallel by placing multiple jumpers.

Once all the connections to the LM8365EVM have been verified, power can be applied to VIN, and evaluation can begin.

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Applications

For the following operation examples, we will use an LM8365 with a typical voltage threshold of 2.7 V.

1 RST Response to VIN Undervoltage

In a typical application, the RESET output can order a microprocessor to enter reset when VCC drops below its minimum operating voltage. Jumpers J1, J2, and J3 are left unpopulated resulting in the minimum programmed output delay. As shown in Figure 1, the RST voltage follows VIN as long as the VIN voltage is above the RESET threshold. When VIN falls below this threshold, the RESET pin outputs low. When VIN rises above the threshold, the RST voltage is pulled back up to VIN, corresponding to the RESET pin outputting high. The LM8365 provides proper voltage supervision in critical situations like undervoltage input to a microprocessor.

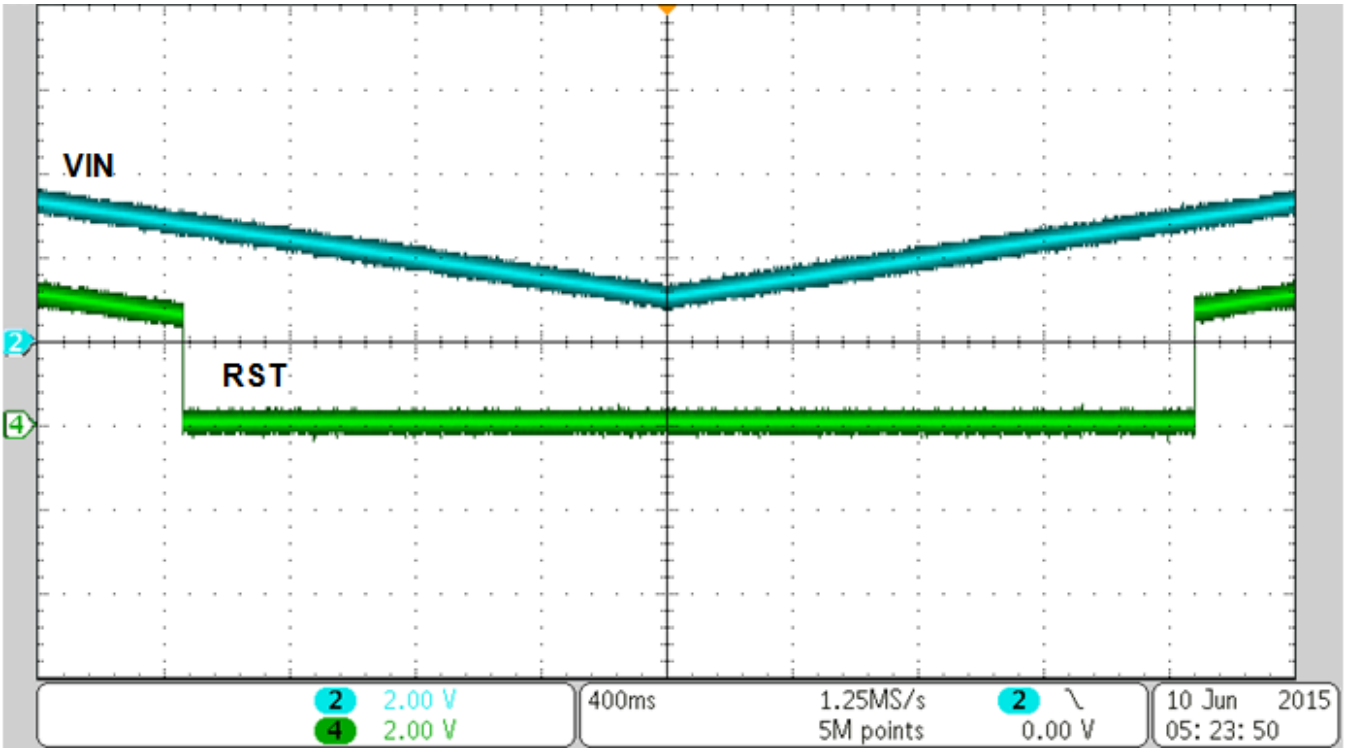


Figure 1. RST Response to Low VIN

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2 RST Hysteresis Behavior

One valuable piece of information to understand is the hysteresis around the RESET threshold. J1, J2, and J3 are unpopulated resulting in the minimum programmed output delay. The RESET pin outputs high only when VIN rises above the RESET threshold plus a certain amount of hysteresis. Figure 2 shows the observed hysteresis, which can eliminate erratic reset responses in certain situations, for example, when the input voltage is hovering very close to the threshold voltage.

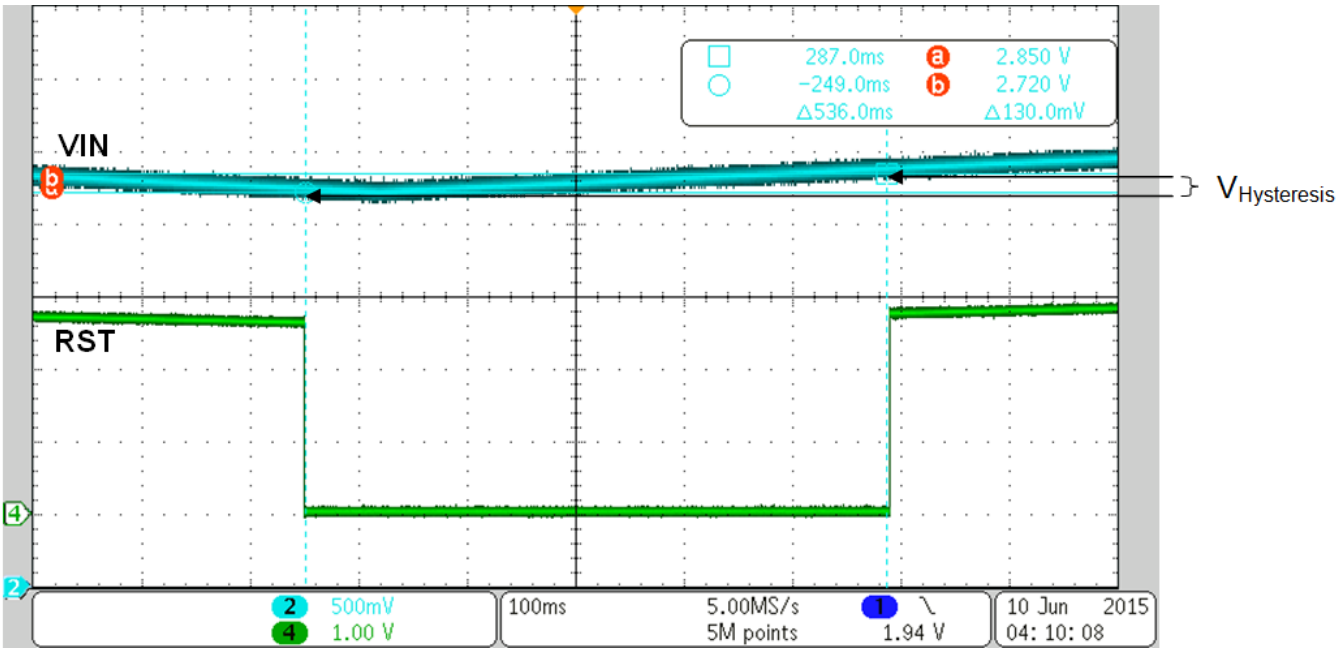


Figure 2. RST Response to Threshold VIN

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3 Programmed Delay with 0.1 µF Capacitor

A typical application usually requires a certain delay before the microprocessor is pulled out of reset once the VCC rises above its minimum operating voltage. This is to allow some time for the VCC to settle to a stable voltage before the microprocessor begins running. Figure 3 shows this delay, which is programmed by populating J2. This corresponds to a CD capacitor of 0.1 µF. In an application, this provides the user confidence that the microprocessor will exit its reset state when its VCC has stabilized above the minimum operating voltage.

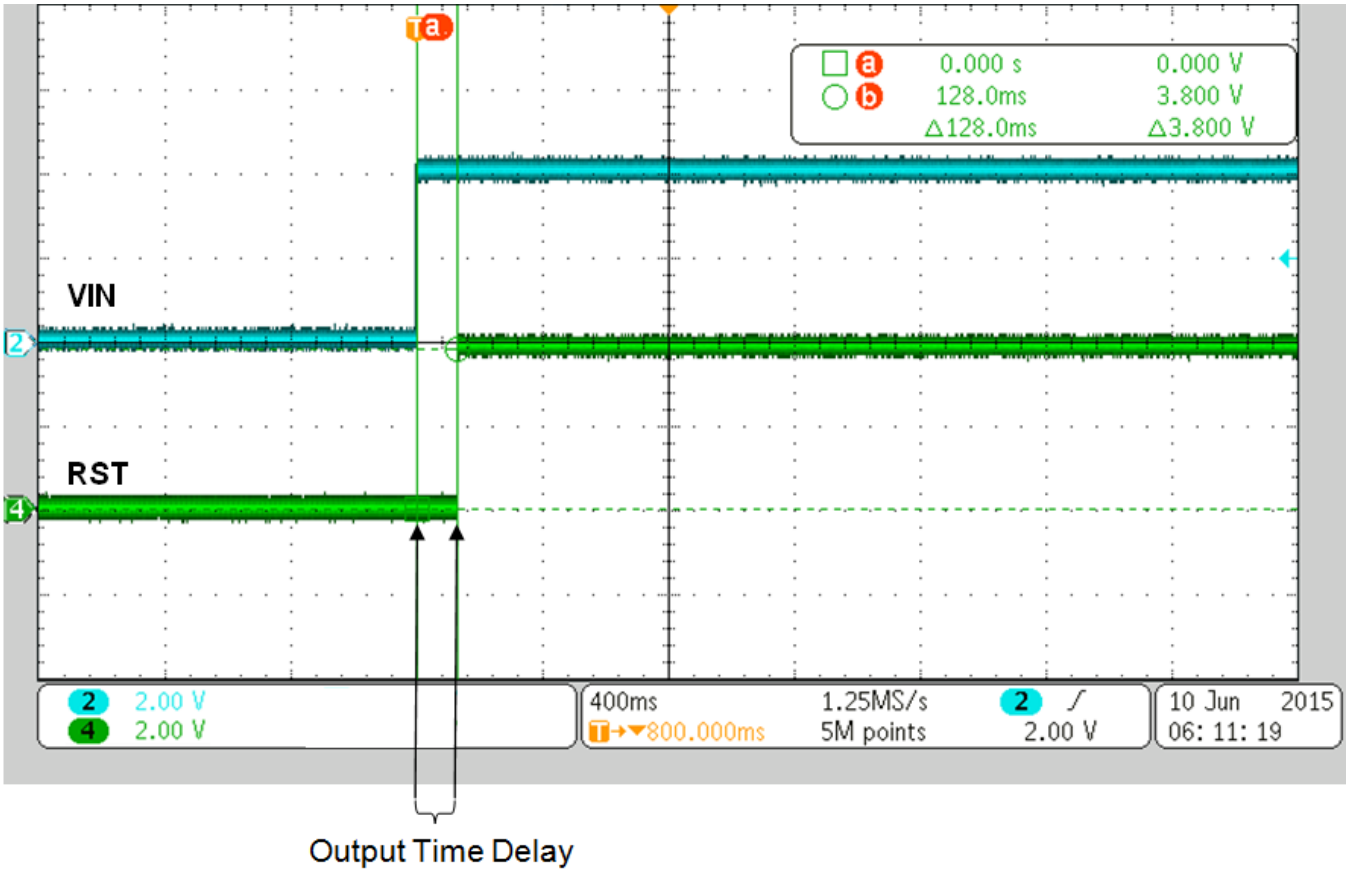


Figure 3. 0.1 µF Capacitor Programmed Delay

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4 Programmed Delay with 1 µF Capacitor

In some supervising applications, a long output delay is necessary. This provides some time for VCC to stabilize above the RESET threshold before the supervised device can exit reset state. Using the exact same setup as in Section 3 Programmed Delay with 0.1 µF Capacitor, we populate J3 instead. This corresponds to a CD capacitor of 1 µF.

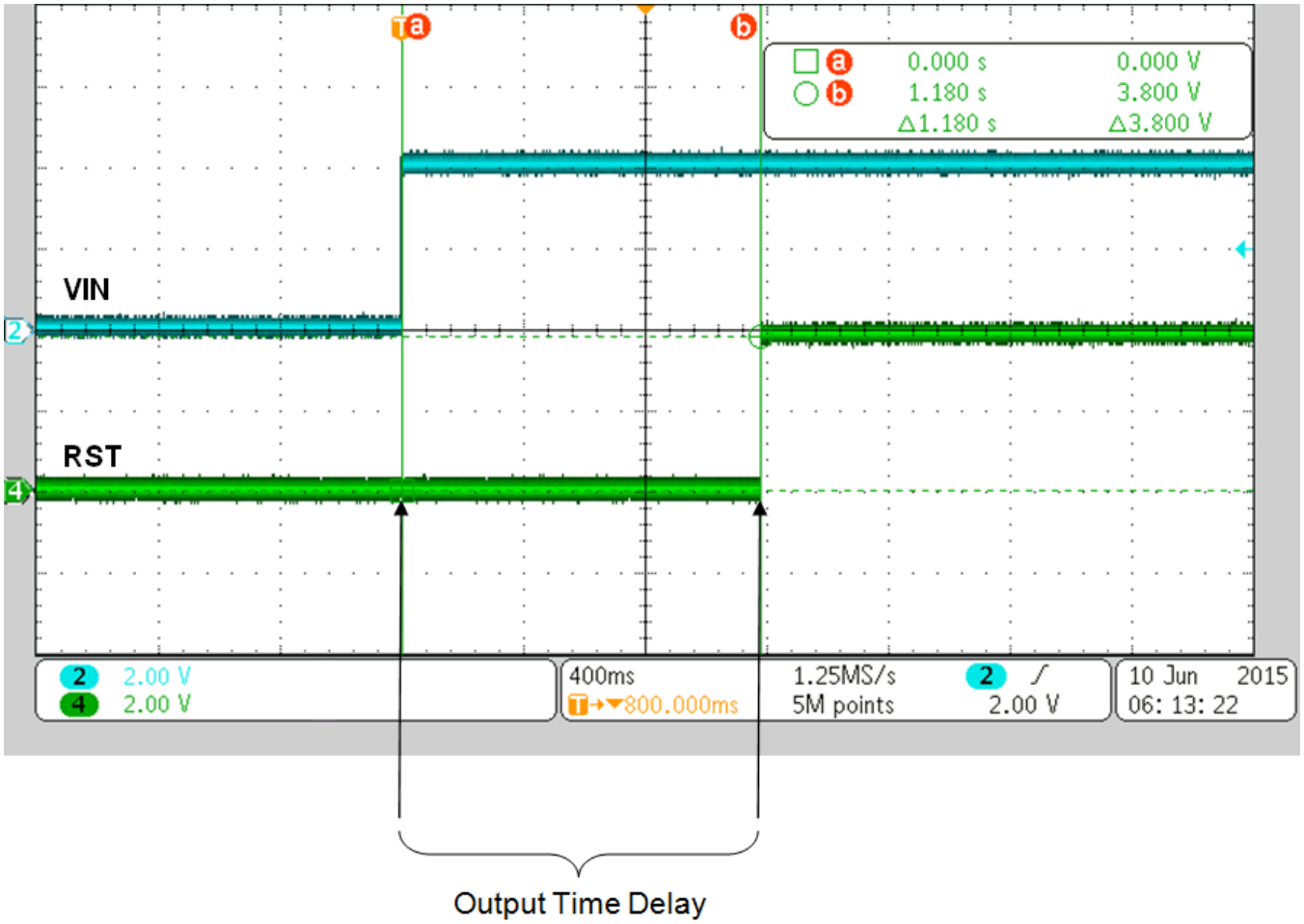


Figure 4. 1 µF Capacitor Programmed Delay

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5 CD Voltage Behavior

Aside from observing the programmed output delay, the LM8365EVM provides the option to observe the behavior of the selected capacitor(s). For this example, we use the same setup as Section 4 Programmed Delay with 1 µF Capacitor. The behavior of the 1 µF CD capacitor is shown in Figure 5.

It should be noted that when the DLY terminal voltage is measured using an oscilloscope probe, the CD capacitor may exhibit some leakage current into the oscilloscope probe. As a result, the RESET pin may output with a slightly longer delay.

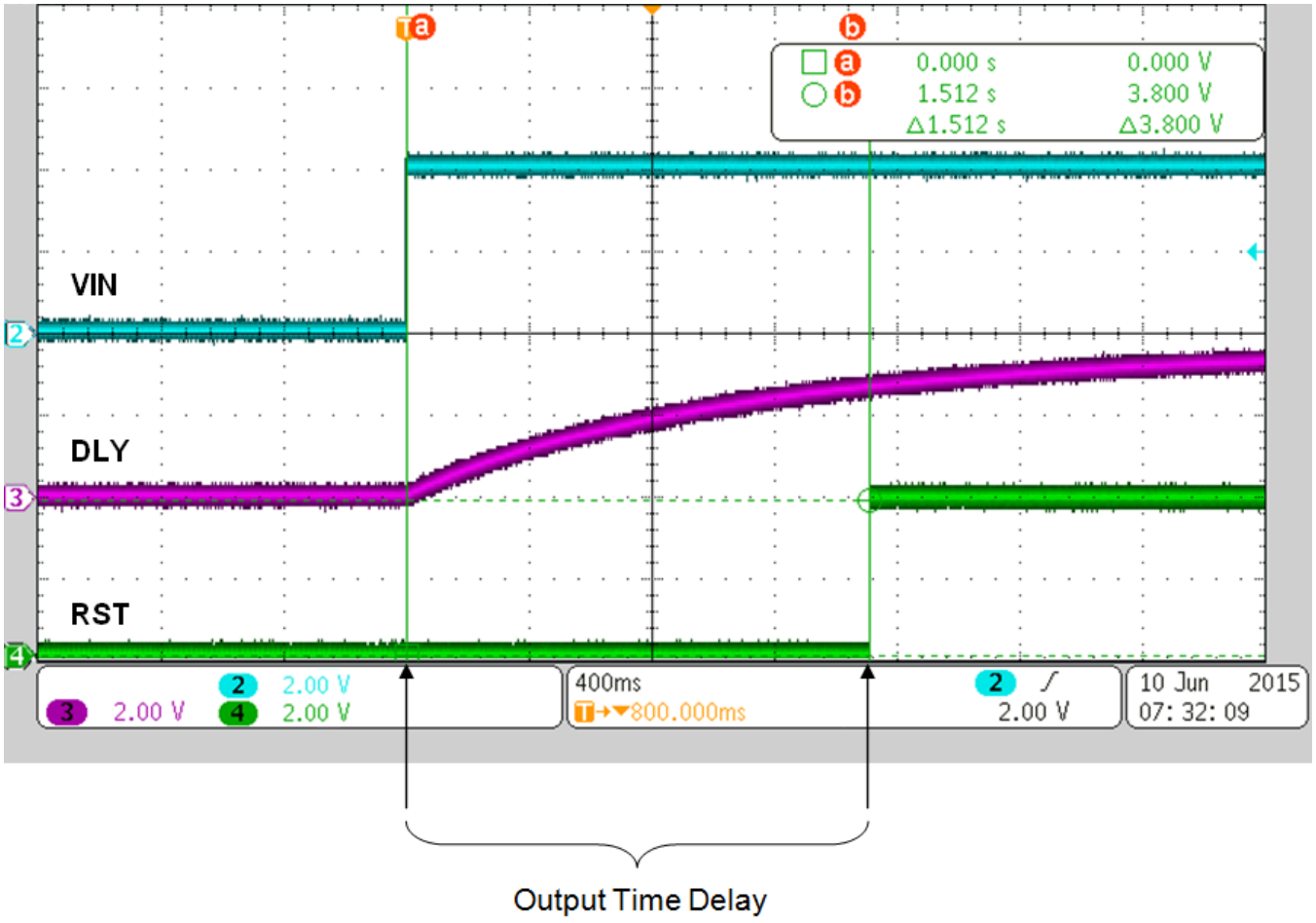


Figure 5. 1 µF Capacitor Delay Behavior

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6 Fast RST Response to Falling VIN

In an application, it is beneficial to have flexibility in time delay for exiting reset state, but when entering reset state we need extremely fast response. For example, if we have a microprocessor running code, it is crucial that this device does not operate below its specified operating voltage. This could potentially lead to disastrous results. Figure 6 shows the reaction time of the RESET output when VIN falls below the RESET threshold.

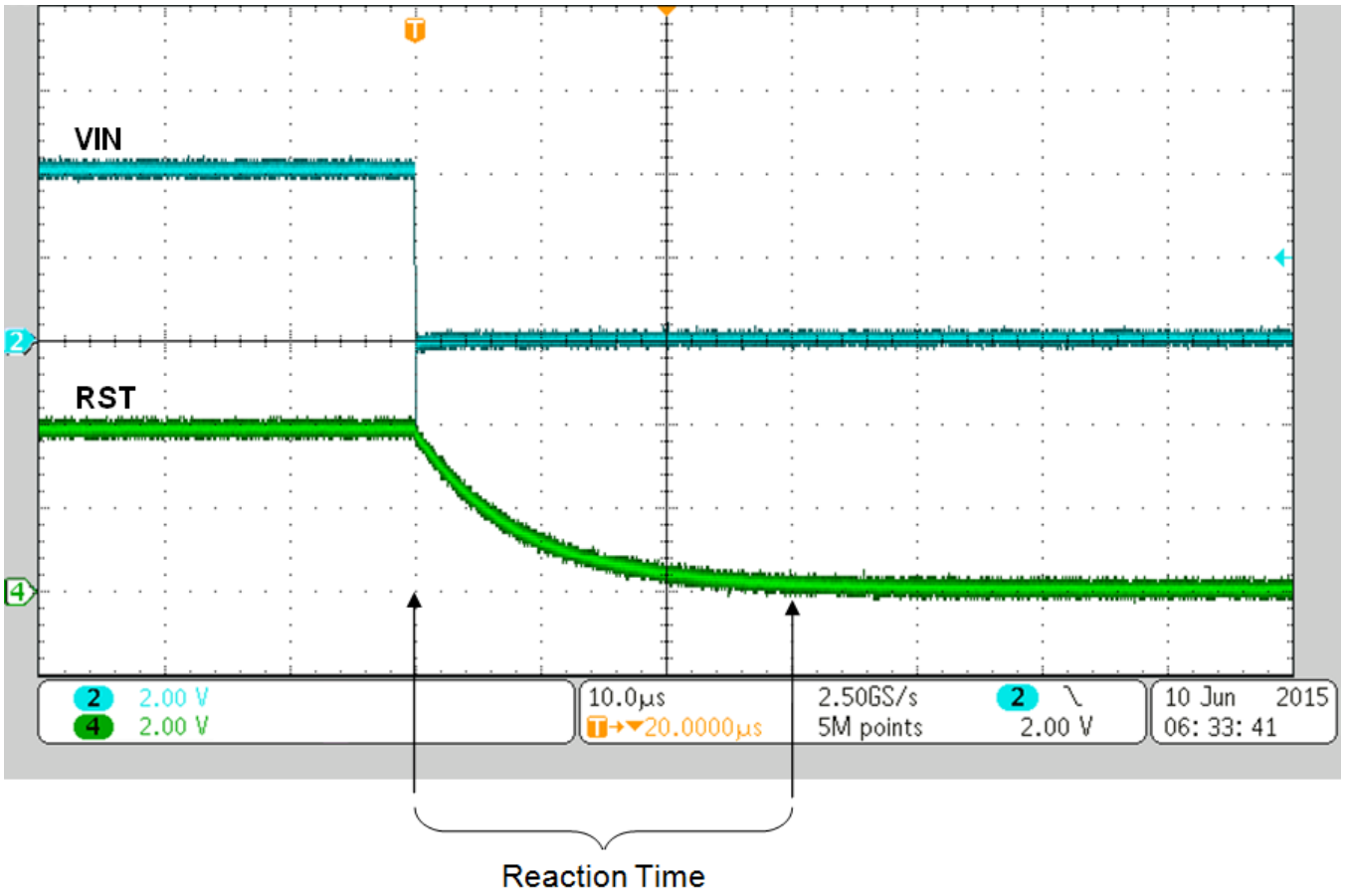


Figure 6. RST Output Low Response

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Board Layout

Figure 7 shows the board layout for the LM8365EVM. Please note that we have provided an unpopulated footprint for C4 which allows room for an input capacitor.

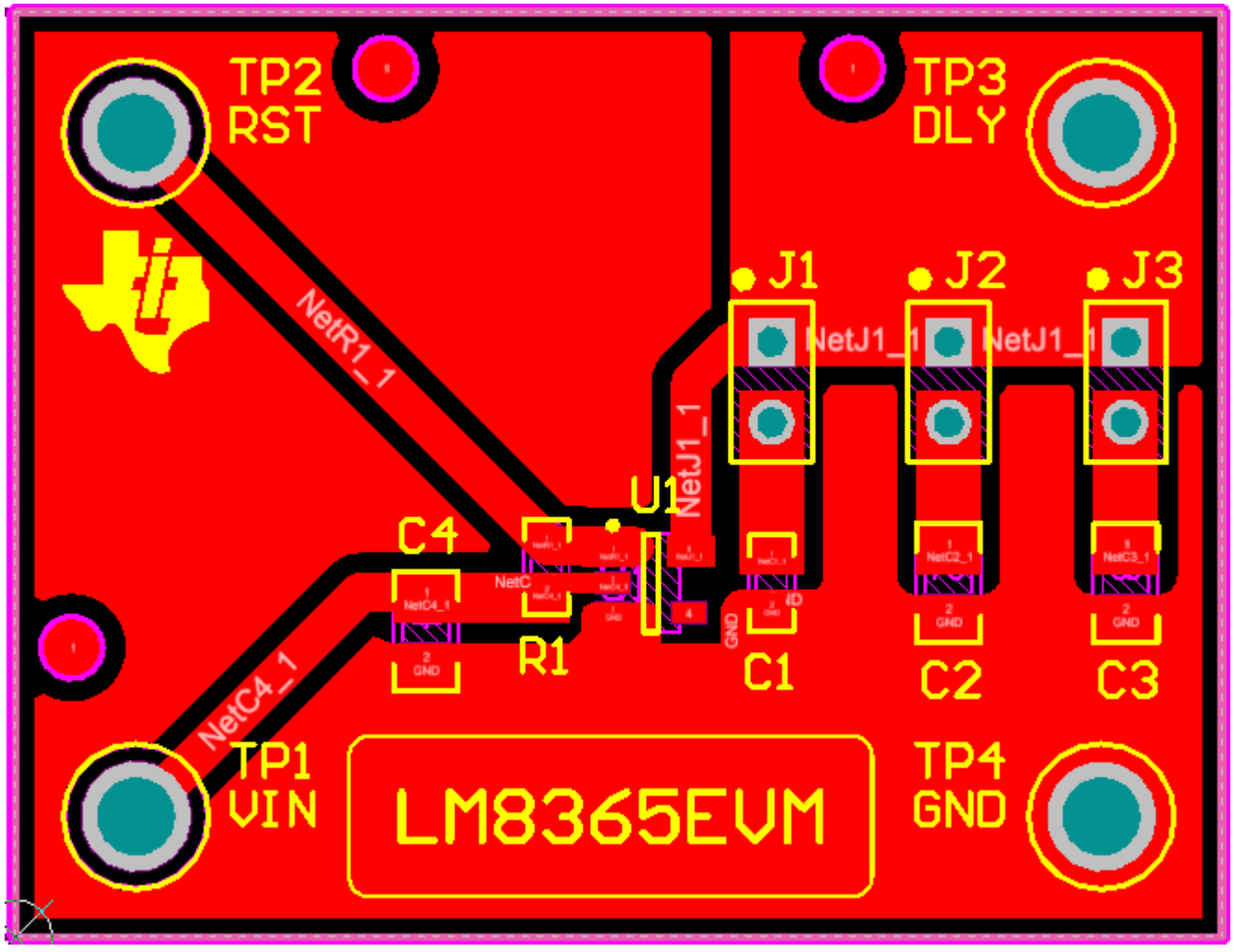


Figure 7. Top Layer Layout

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Schematic

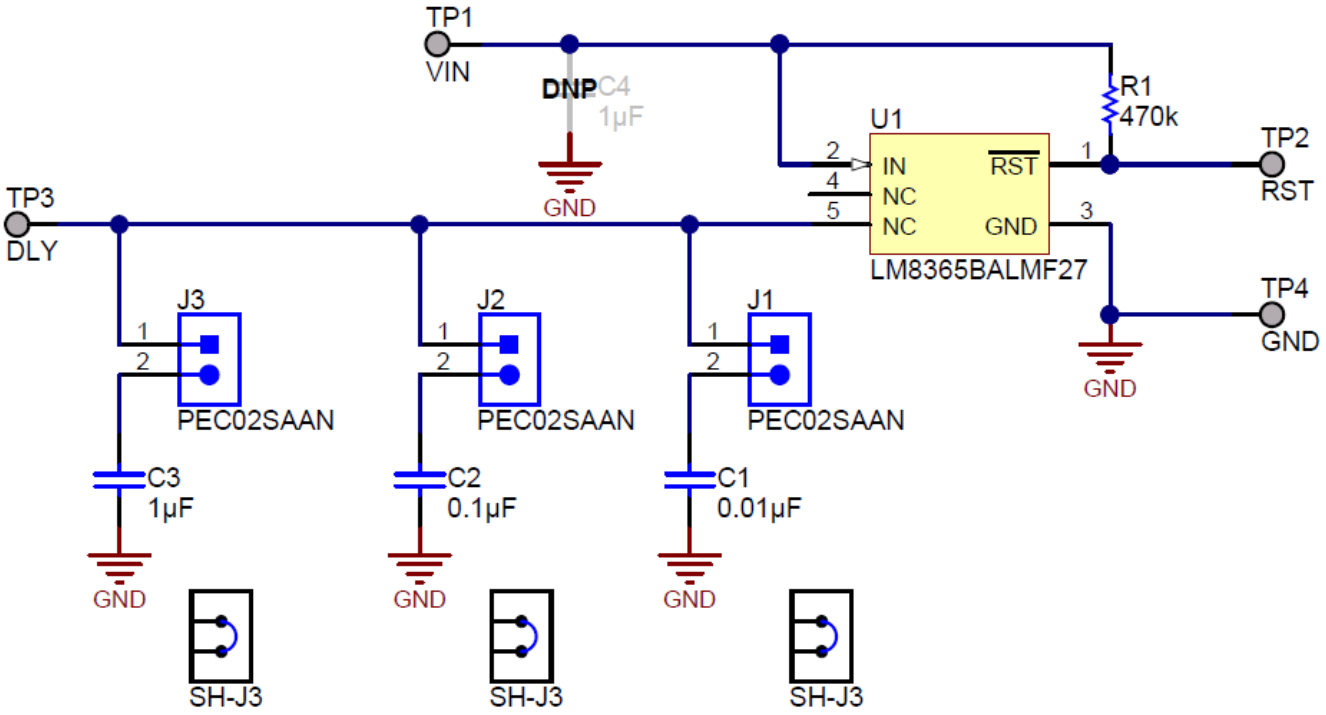


Figure 8. LM8365EVM Schematic

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Bill of Materials

Table 2. LM8365EVM Bill of Materials

COUNT	REF DES	DESCRIPTION	PACKAGE REF	MFR	PART NUMBER
1	PCB	Printed Circuit Board		Any	SV601177
1	C1	CAP, CERM, 0.01µF, 16V, +/- 10%, X7R, 0603	603	MuRata	GRM188R71C103KA01D
1	C2	CAP, CERM, 0.1µF, 16V, +/- 10%, X7R, 0805	805	MuRata	GRM219R71C104KA01D
1	C3	CAP, CERM, 1µF, 16V, +/- 10%, X7R, 0805	805	Kemet	C0805C105K4RACTU
3	J1, J2, J3	Header, 100mil, 2x1, Tin, TH	Header,	Sullins Connector Solutions	PEC02SAAN
			2 PIN, 100mil, Tin		
1	LM8365EVM	Thermal Transfer Printable Labels, 0.650” W x 0.200” H – 10,000 per roll	PCB Label 0.650” H x 0.200” W	Brady	THT-14-423-10
1	R1	RES, 470 k, 5%, 0.1 W, 0603	603	Vishay-Dale	CRCW0603470KJNEA
3	SH-J3	Shunt, 100mil, Gold plated, Black	Shunt	3M	969102-0000-DA
4	TP1, TP2, TP3, TP4	Terminal, Turret, TH, Double	Keystone 1502-2	Keystone	1502-2
1	U1	Micropower Undervoltage Sensing Circuits with Programmable Output Delay, 2.7V Threshold, 5-pin SOT-23	MF05A	Texas Instruments	LM8365BALMF27
0	C4	CAP, CERM, 1µF, 16V, +/- 10%, X7R, 0805	805	Kemet	C0805C105K4RACTU
0	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

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Related Documentation

LM8365 Micropower Undervoltage Sensing Circuits with Programmable Output Delay datasheet (SNVS233).

Revision History

DATE	REVISION	NOTES
October 2015	*	Initial release.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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