UG410: EFP0108 Evaluation Kit User's Guide

The EFP0108 Evaluation Kit is an excellent way to evaluate and characterise the EFP01 Energy Friendly Power Management IC (PMIC) in the Single-Cell Boost configuration.

The EFP01 is an extremely flexible, highly efficient, multi-output power management IC with integrated Coulomb counter for lossless charge measurements. The kit contains an EFP0108 Evaluation Board (BRD8100A), which features an EFP0108 in the Single-Cell Boost configuration. The input and output power rails of the EFP01 are exposed on terminal blocks and test points making it easy to evaluate and characterize the EFP01 with external hardware. The board can be plugged into a computer using the USB Micro-B connector for conveniently controlling the EFP01's register settings and reading back data. The EFP0108 Evaluation Board is supported in Simplicity Studio and the EFP Configuration Tool.



TARGET DEVICE

- EFP0108 multi-output PMIC in Single-Cell Boost configuration

KIT FEATURES

- Wire to board terminal blocks for EFP0108 input and output power connections
- Test points for easy probing
- Host MCU with two push buttons and three LEDs
- Convenient control of the EFP from a computer

SOFTWARE SUPPORT

- Simplicity Studio
- EFP Configuration Tool

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1. Introduction

The EFP0108 Evaluation Kit (OPN: SLEVK1000A) is an excellent starting point to evaluate and characterize the EFP01 Energy Friendly Power Management IC (PMIC) in the Single-Cell Boost configuration. The EFP01 is an extremely flexible, highly efficient, multi-output power management IC with integrated Coulomb counter for lossless charge measurements.

The kit contains an EFP0108 Evaluation Board (BRD8100A), which features an EFP0108 in the Single-Cell Boost configuration. The input and output power rails of the EFP01 are exposed on terminal blocks and test points instead of powering the host MCU, making it easy to evaluate and characterise the EFP01 with external hardware. The board can be plugged into a computer using the USB Micro-B connector for conveniently controlling the EFP01's register settings and reading back data. Writing and reading registers is handled through the host MCU, which is embedded on the board and connected to the digital interface of the EFP01. An on-board SEGGER J-Link debugger provides the host MCU with a virtual COM port and debugging capabilities on the USB connector.

The EFP0108 Evaluation Board is supported in Simplicity Studio and the EFP Configuration Tool.

1.1 Kit Contents

The following items are included in the box:

- 1x EFP0108 Evaluation Board (BRD8100A)
- 1x USB 2.0 AM to Micro BM cable

1.2 Getting Started

Detailed instructions for how to get started with your new EFP0108 Evaluation Kit can be found on the Silicon Labs web pages:

http://www.silabs.com/start-efp

2. Hardware

This section describes the hardware on the EFP0108 Evaluation Board. The main part of the board is the EFP01 with terminal blocks and test points, while the host MCU with peripherals and the on-board debugger is there to provide an easy interface to the registers of the EFP01.

2.1 Block Diagram And Hardware Layout

The block diagram and hardware layout of the EFP0108 Evaluation Kit is illustrated in the two figures below.

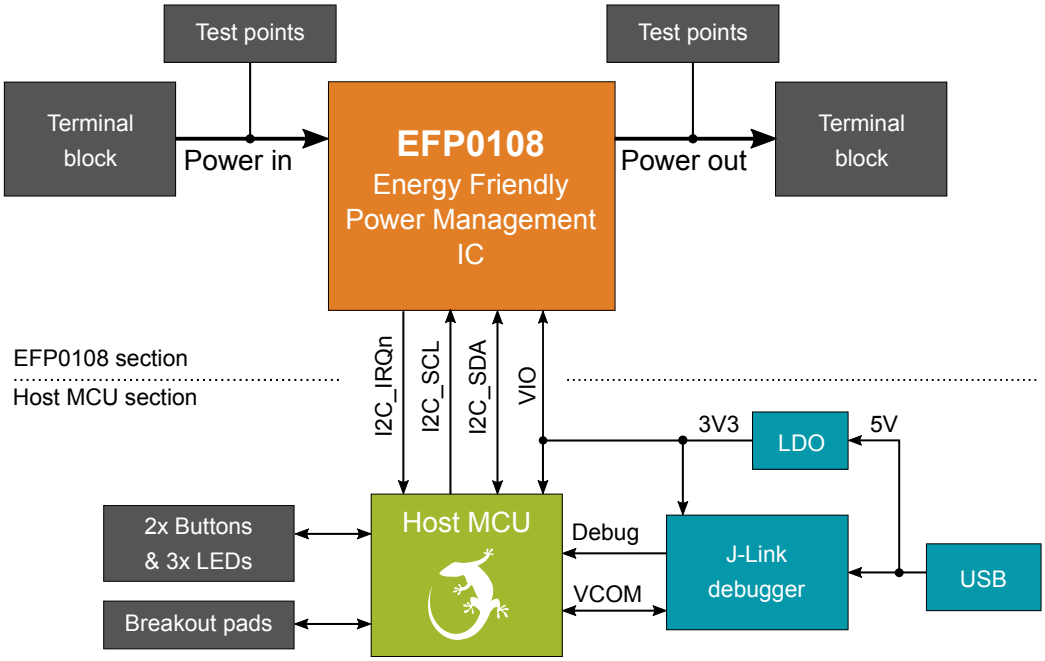


Figure 2.1. Kit Block Diagram

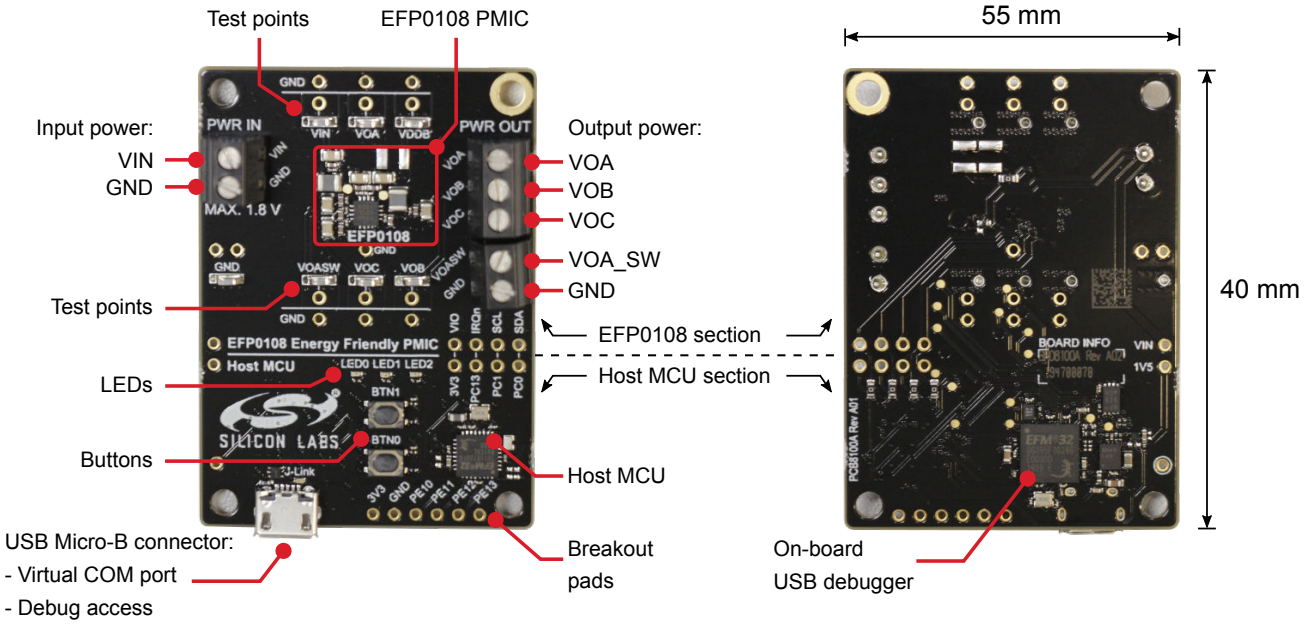


Figure 2.2. EFP0108 Evaluation Kit Hardware Layout

2.2 EFP01

The EFP0108 on the evaluation board is configured in the Single-Cell Boost configuration. It takes an input voltage between 0.8 - 1.8 V (after start-up) and generates four outputs. More information regarding the operating conditions of the device is given in section 2.2.1 Operating Conditions. A simplified block diagram of the EFP0108 power supply connection is shown in the figure below.

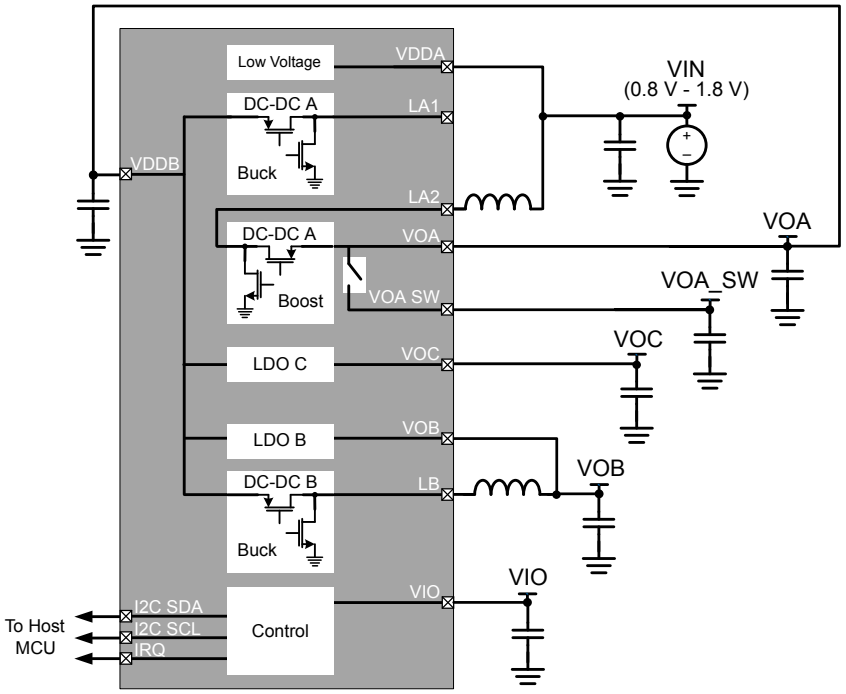


Figure 2.3. Single-Cell Boost Configuration

2.2.1 Operating Conditions

The default operating conditions of the EFP0108 on the board are as specified in the table below. The output voltages can be set to other values by configuring the appropriate registers. Take precautions to not exceed the maximum supported input voltage as this may cause damage to the device.

Table 2.1. Default Operating Conditions

Parameter	Symbol	Voltage (V)	Notes
VIN input voltage range	V_{VIN_START}	0.85 - 1.8 V	Input from external supply at start-up
	V_{VIN}[1]	0.8 - 1.8 V	Input from external supply after start-up
VIO input voltage	V_{VIO}[2]	3.3 V	Supplied by on-board LDO when USB is connected
VOA output voltage	V_{VOA}	1.8	Output to external load
VOB output voltage	V_{VOB}	OFF	Output to external load
VOC output voltage	V_{VOC}	OFF	Output to external load
VOA_SW output voltage	V_{VOA_SW}	OFF	Output to external load

1 Unless otherwise stated, 0.8 - 1.8 V is used throughout this document as the input voltage range of the device.

2 On the EFP0108 Evaluation Board, VIO is generated by an on-board LDO set to 3.3 V. The EFP01 itself supports a wider VIO voltage range.

2.2.2 Overview and Typical Connection

The input and output power rails of the EFP01 are exposed on terminal blocks instead of being used on the board itself. The terminal blocks are of the M2 screw thread type and are suited for wires with a wire gauge of 16-30 AWG. A power supply between 0.8 - 1.8 V should be applied on the "PWR IN" terminal block, while one or several loads can be connected to the "PWR OUT" terminal block.

Power to the VIO terminal must also be applied in addition to power on VIN for proper operation of the EFP01. This is normally done by connecting the EFP0108 Evaluation Board to a power source using the USB Micro-B connector. The 5 volt power net from the USB bus is regulated down to 3.3 V, which is used to power VIO on the EFP01, the host MCU and the on-board debugger. Failure to power VIO may cause improper operation of the EFP01, and the EFP01 may draw several hundred µA of extra current consumption from the VIN terminal. For advanced use-cases it is possible to disconnect VIO and the digital interface of the EFP01 from the rest of the board as described in section 2.2.3 Digital Interface.

The power rails VIN, VOA, VOB, VOC and VOA_SW are routed to test points on the board, which is marked in the silk print on the board with reference to Figure 2.3 Single-Cell Boost Configuration on page 5 and the schematics. In addition to a surface mount test point suitable for miniature probes, clips and hooks, a footprint that fits a standard 2x1, 2.54 mm pitch pin header is also available for each rail. Pad 1 of this footprint is connected to the power rail, while pad 2 is connected to ground. The test points are routed directly to the input/output capacitors of the power rails, and they are primarily intended for low current sensing. The switch nodes of the two DC/DC regulators are also available.

Note: In addition to applying power to the "PWR IN" terminal block, remember to also apply power to the VIO terminal of the EFP01. This is normally done by connecting the USB Micro-B connector on the EFP0108 Evaluation Board to a power source. Also note that all ground connections on the board, including ground on the USB Micro-B connector, are connected together to the same ground plane on the board.

The figure below shows an overview of the power terminal blocks and test points, and how a typical measurement setup on the EFP0108 Evaluation Board looks like.

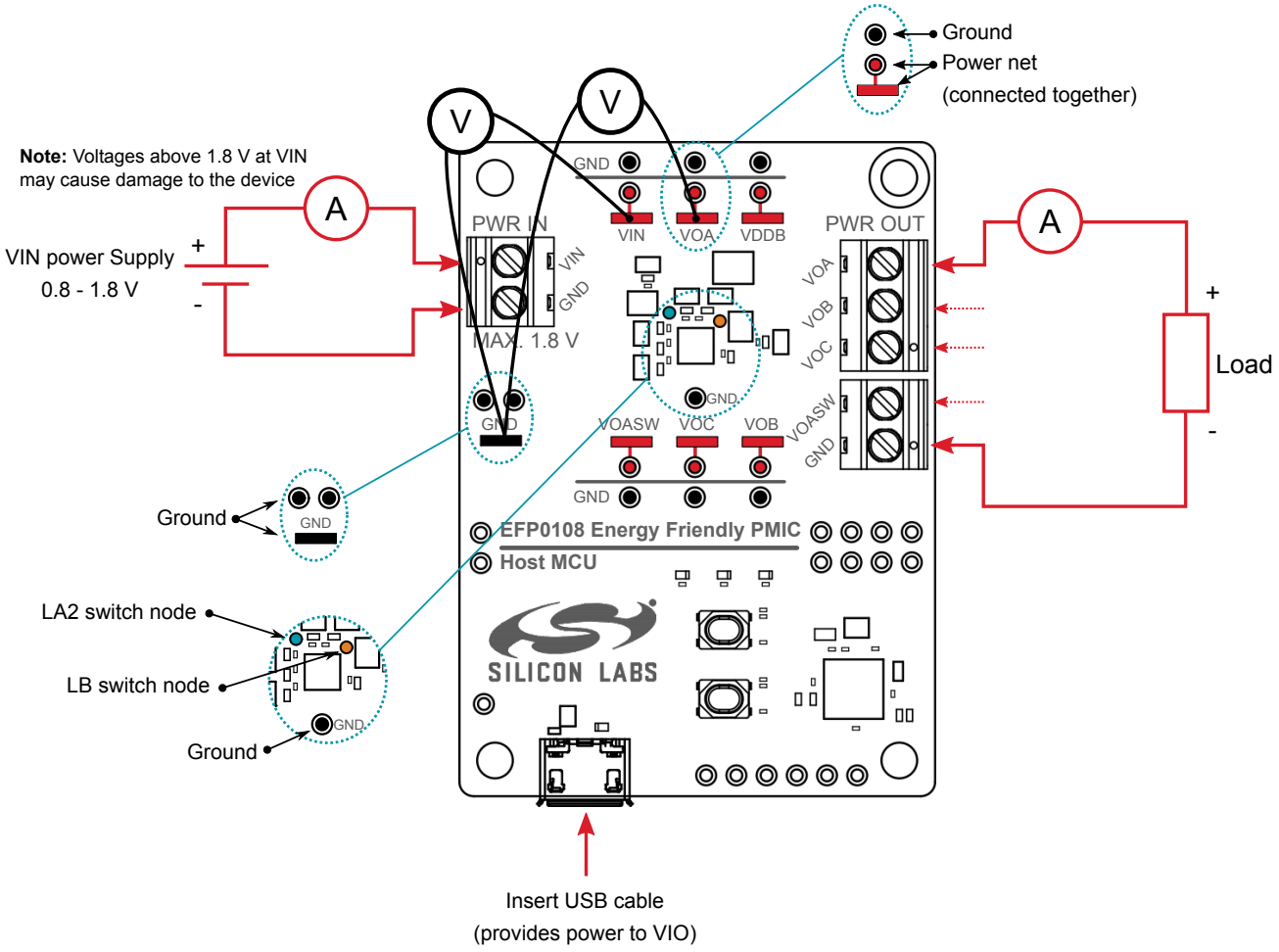


Figure 2.4. Typical Connection

2.2.3 Digital Interface

The EFP01 is connected to the host MCU through two I^2C lines (SCL and SDA), one interrupt line (IRQn), a power rail (VIO) and ground. Except for the ground connection, the EFP can be disconnected from the rest of the board by removing four 0 Ω resistors which are located on the secondary side of the board. The lines are exposed on the footprint for a 2x4, 2.54 mm pitch pin header (P202) as illustrated in the figure below. This header can be used for connecting the EFP01 to an external host or hardware. This is, however, considered an advanced use-case and the user needs to make sure the connection does not violate any absolute maximum ratings of the devices on the board or the external hardware.

Important: If doing any modifications on the board, make sure to not violate any absolute maximum ratings of the devices on the board or the external hardware.

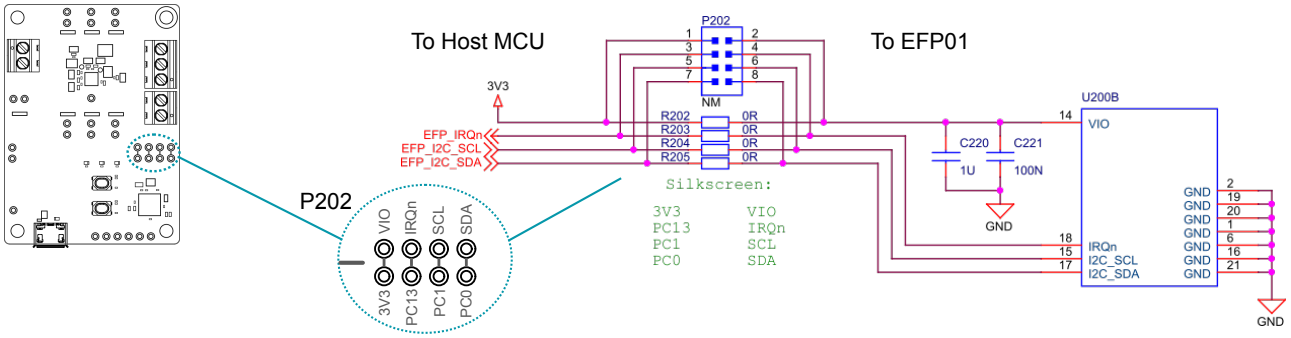


Figure 2.5. Interface Between the EFP Digital Block and the Host MCU

2.2.4 On-Board LDO

An LDO is present on the board that draws current from the USB Micro-B connector and generates 1.5 V. This power rail is not used elsewhere on the board. Applications that only draw a small amount of current, such as testing different register settings with no or high impedance loads, may take advantage of this rail to simplify the hardware setup. This rail is exposed on pad 1 of the footprint (ST208) for a 2x1, 2.54 mm pitch pin header. Pad 1 of this footprint can be shorted to pad 2 in order to connect the 1.5 V rail to the VIN net. Care must be taken to not connect an external power source to the VIN terminal block (P200) when these pads are shorted together.

Important: The intended use-case for the on-board LDO is for high impedance loads and in the absence of a power source on the VIN terminal block. Do not apply a power source on the VIN terminal block (P200) while ST208 is shorted.

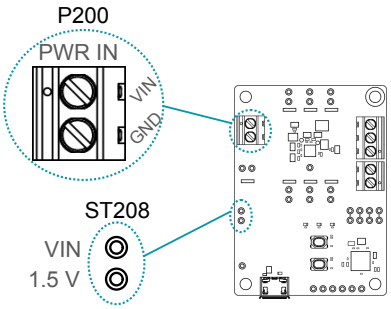


Figure 2.6. Optional On-board LDO Available For Low Current Applications

2.2.5 Design Notes

The printed circuit board (PCB) for this evaluation board has been designed to support both the EFP0108 Evaluation Kit (SLEVK1000A) and the EFP0111 Evaluation Kit (SLEVK100B). The kit has not been designed to optimize the BOM with respect to a given application, and hence, more optimum designs might exist. For guidelines on more optimized BOMs please consult the datasheet.

2.3 Host MCU

2.3.1 EFP01 Interface

The connection between the host MCU and the EFP01 is illustrated below. The connection can be removed with the 0 Ω resistors as described in section 2.2.3 Digital Interface.

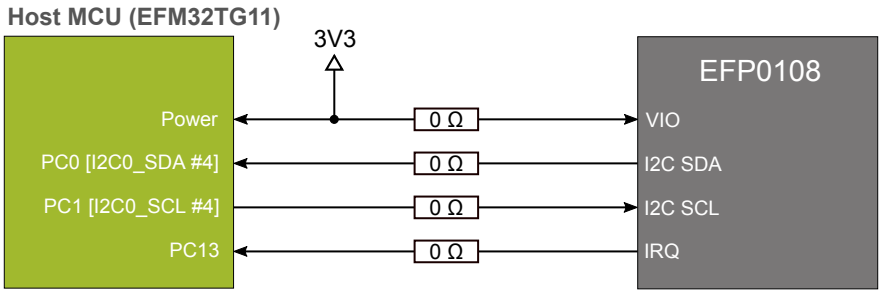


Figure 2.7. Interface Between the Host MCU and the EFP01

2.3.2 Push Buttons and LEDs

The kit has two user push buttons marked BTN0 and BTN1. They are connected directly to the the host MCU (EFM32TG11) and are debounced by RC filters with a time constant of 1 ms. The buttons are connected to pins PB11 and PC14.

The kit also features three user LEDs that is controlled by GPIO pins on the host MCU (EFM32TG11). The LEDs are connected in an active-high configuration. The LEDs are connected to pins PA0, PA1 and PA2.

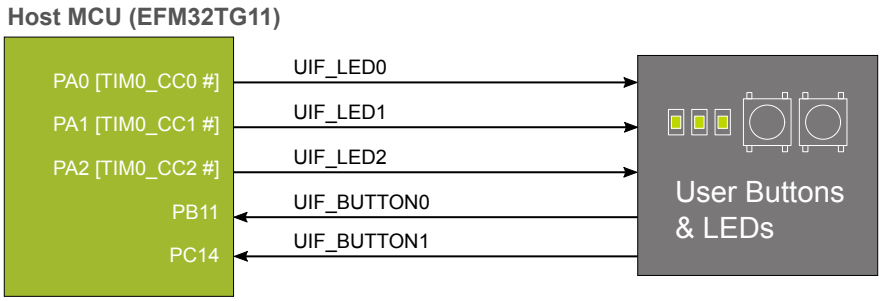


Figure 2.8. Buttons and LEDs

2.3.3 Breakout Pads

The host MCU (EFM32TG11) has four GPIO pins that are not used on the board. These are routed to breakout pads together with the 3V3 rail and ground as illustrated in the figure below.

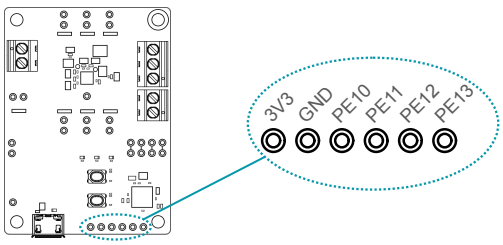


Figure 2.9. Host MCU (EFM32TG11) Breakout Pads

2.4 On-board Debugger

The EFP0108 Evaluation Board contains a microcontroller separate from the host MCU (EFM32TG11) that provides the user with an on-board J-Link debugger through the USB Micro-B debugging port. This microcontroller is referred to as the "on-board debugger", and is not programmable by the user. The debugger allows the user to download code and debug applications running in the host MCU, and it provides a virtual COM port (VCOM) to the host computer that is directly connected to the host MCU's serial port.

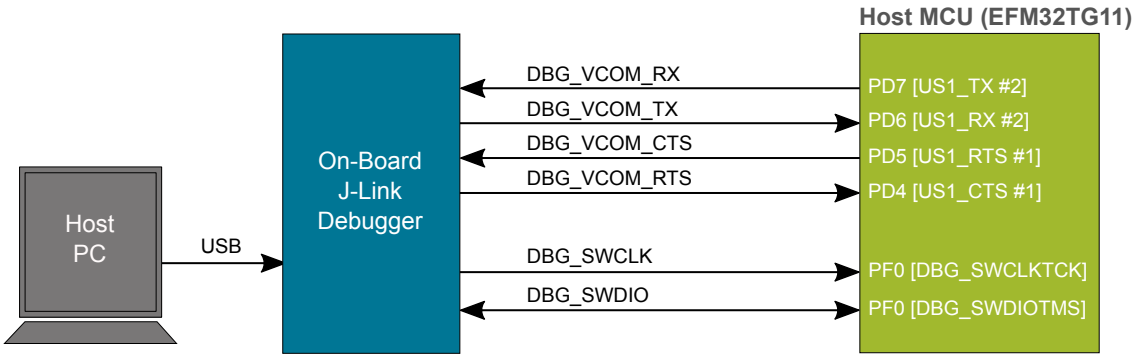


Figure 2.10. On-Board Debugger Connections

2.4.1 Virtual COM Port

The virtual COM port is a connection to a USART of the host MCU, and allows serial data to be sent and received from the device. The on-board debugger presents this as a virtual COM port on the host computer that shows up when the USB cable is inserted.

Data is transferred between the host computer and the debugger through the USB connection, which emulates a serial port using the USB Communication Device Class (CDC). From the debugger, the data is passed on to the host MCU through a physical USART connection.

The serial format is 115200 bps, 8 bits, no parity, and 1 stop bit.

Note: Changing the baud rate for the COM port on the PC side does not influence the USART baud rate between the debugger and the target device.

3. Design Files

Design files are available through Simplicity Studio when the kit documentation package has been installed.

4. Kit Revision History

The kit revision can be found printed on the kit packaging label, as outlined in the figure below.



Figure 4.1. Kit Label

4.1 SLEVK1000A Revision History

Kit Revision	Released	Description
A01	10 January 2020	Updated to BRD8100A Rev. A03.
A00	13 November 2019	Initial release.

5. Document Revision History

Revision 1.1

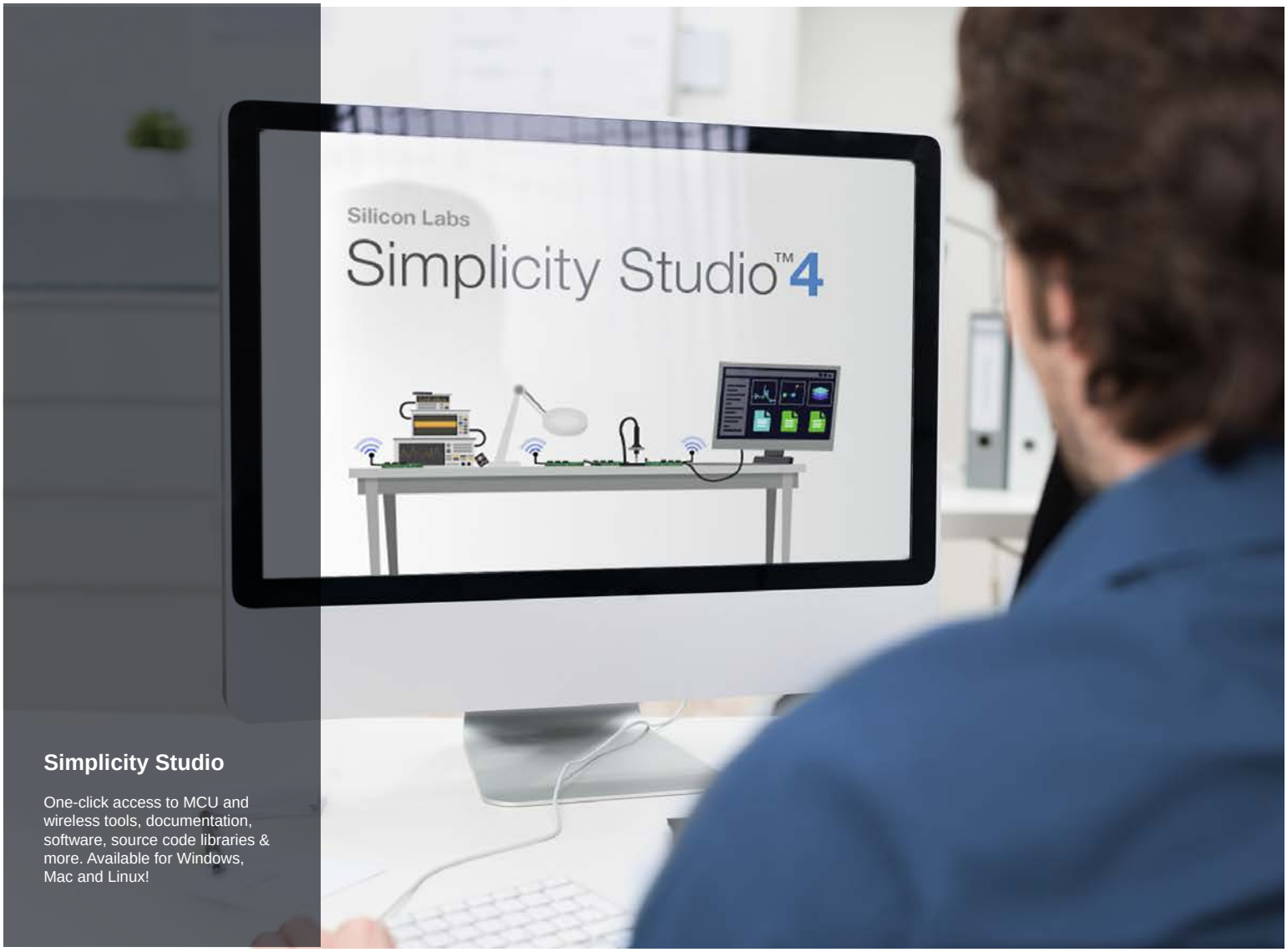
15 January 2020

- Updated kit revision history.

Revision 1.0

20 December 2019

- Initial document release.



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