DSA2311KA2-R0065VAO

Crystal-less™ Configurable Clock Generator for Automotive

General Description

DSA2311KA2-R0065VAO is a crystal-less clock generator that is factory configurable to simultaneously output two separate frequencies from 2.3 to 170MHz.

The clock generator uses proven silicon MEMS technology to provide low jitter and high frequency stability across a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, crystal-less clock generators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of consumer electronics, communications, and storage applications.

DSA2311KA2-R0065VAO has an output enable/disable feature allowing it to disable the outputs when OE is low. The device is available in a space-saving 6-pin 2.5mm x 2.0mm TDFN package that needs only a single external bypass capacitor.

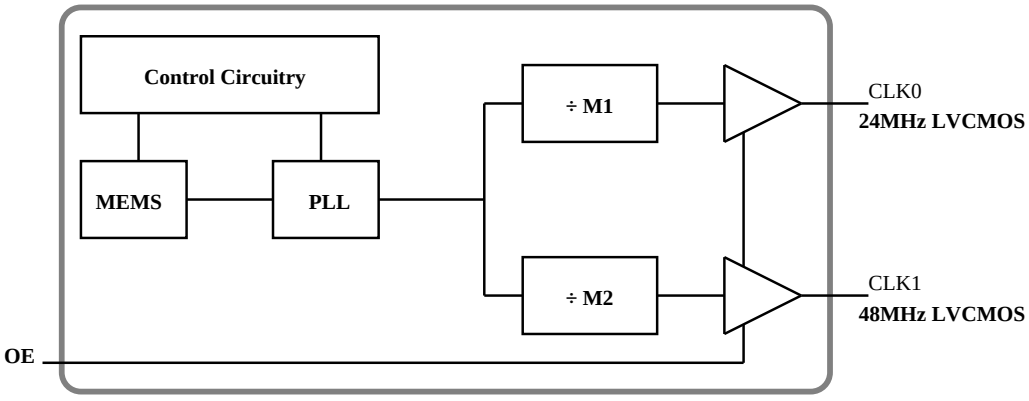
Features

- AEC-Q100 automotive qualified
- Two simultaneous LVCMOS outputs:
  - 24MHz
  - 48MHz
- Low RMS phase jitter: <1ps (typical)
- ±25ppm frequency stability
- -40°C to +125°C (Grade 1) temperature range
- High supply noise rejection: -50dBc
- High shock & vibration immunity
  - Qualified to MIL-STD-883
- High reliability
  - 20x higher MTBF than crystal-based clock generator designs
- Supply range of 2.25 to 3.6V
- 6-pin 2.5mm x 2.0mm TDFN package

Applications

- Automotive Infotainment
- Automotive ADAS
- Automotive Camera Module
- Automotive LIDAR and RADAR

Block Diagram



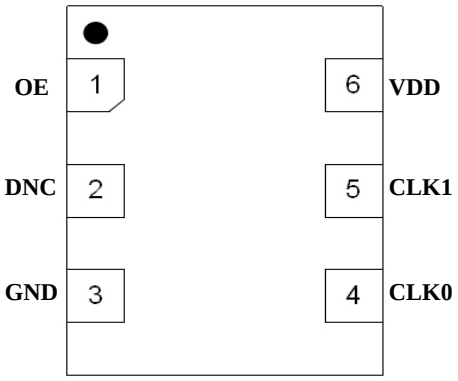
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Ordering Information

Ordering Part Number	Industrial Temperature Range	Shipping	Package
DSA2311KA2-R0065VAO	-40°C to +125°C	Tube	6-pin 2.5mm x 2.0mm TDFN
DSA2311KA2-R0065TVAO	-40°C to +125°C	Tape and Reel	6-pin 2.5mm x 2.0mm TDFN

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



6-pin 2.5mm x 2.0mm TDFN

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I		Active high output enable for CLK0 and CLK1
2	DNC			Leave unconnected or connect to the ground
3	GND	PWR		Power supply ground
4	CLK0	O	LVCMOS	CLK0 output frequency = 24MHz
5	CLK1	O	LVCMOS	CLK1 output frequency = 48MHz
6	VDD	PWR		Power supply

Specifications (Unless specified otherwise: T = 25°C, VDD = 3.3V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage[1]	VDD		2.25		3.6	V
Supply Current[2]	IDD	OE pin low - outputs are disabled		21	23	mA
Frequency Stability[6]	△F	Includes frequency variation due to initial tolerance, temp. and power supply voltage		±25		ppm
Aging	△F	First year (@ 25°C)			±5	ppm
Startup Time[3]	tSU	T = 25°C			5	ms
Input Logic High Input Logic Low	VIH VIL		0.75 x VDD -		- 0.25 x VDD	V
Output Disable Time[4]	tDA				5	ns
Output Enable Time[4]	tEN				20	ns
Pull-Up Resistor[2]		Pull-up exists on pin 1		40		kOhms
Output Logic High Output Logic Low	VOH VOL	I = ±6mA	0.9 x VDD -		- 0.1 x VDD	V
Output Transition Time[4] Rise Time Fall Time	 tR tF	 20% to 80% CL = 15pF		 1.1 1.43	 2 2	ns
Frequency	F0 F1	CLK0 CLK1		24 48		MHz
Output Duty Cycle	SYM		45		55	%
Period Jitter[5]	JPER	CLK0 = CLK1 = 25MHz		3		psRMS
Integrated Phase Noise	JCC	200kHz to 20MHz @ 25MHz 100kHz to 20MHz @ 25MHz 12kHz to 20MHz @ 25MHz		0.3 0.38 1.7	 2	psRMS

Notes:
1. Pin 4 VDD should be filtered with 0.1uF capacitor.
2. Output is enabled if OE pad is high or not connected. Supply current = Disabled Current + ΔIDD from CLK0 + ΔIDD from CLK1. See Current Consumption graph on next page.
3. tSU is time to stable output frequency after VDD is applied and outputs are enabled.
4. See Figure 3 for detail (all based on maximum drive settings).
5. Period Jitter includes crosstalk from adjacent output.
6. For other ppm stabilities, contact the factory at tcg_help@microchip.com.

Absolute Maximum Ratings

Item	Min.	Max.	Units	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	VDD + 0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

Current Consumption

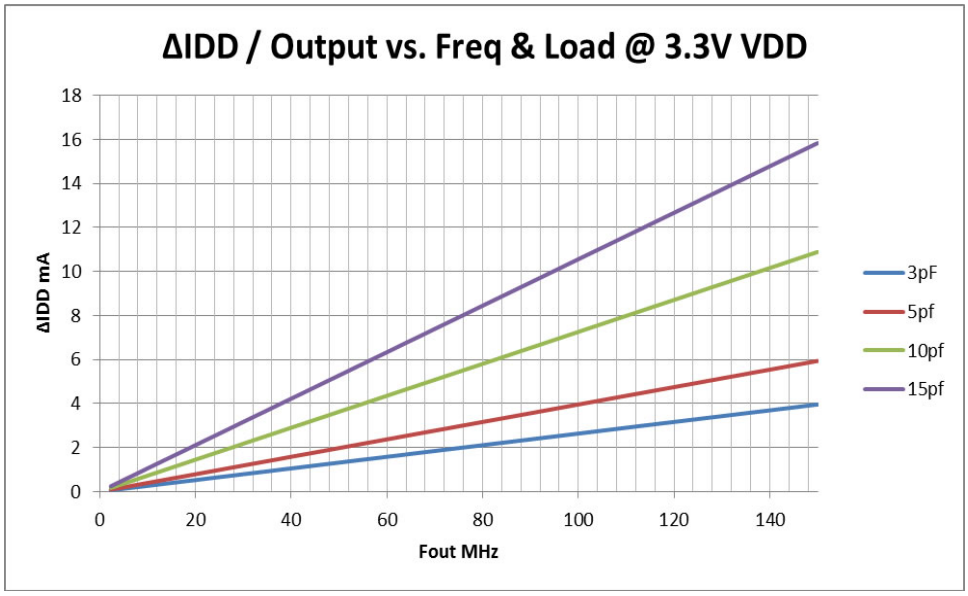


Figure 1. Total Current = Disabled Current + ΔIDD Fout1 + ΔIDD Fout2

Solder Reflow Profile

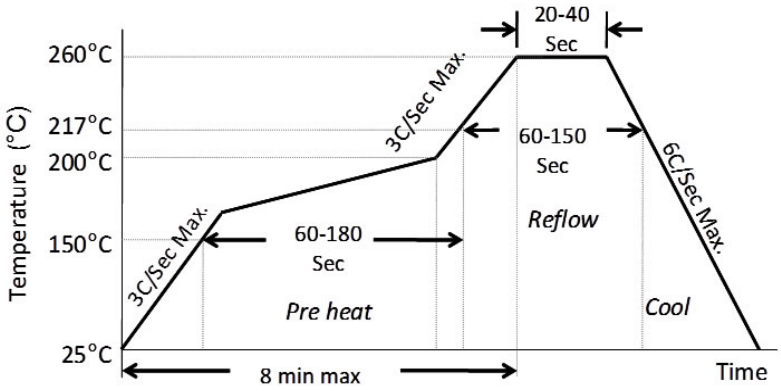


Figure 2. Solder Reflow Profile

6 QFN MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec Max.
Preheat Time 150°C to 200°C	60 - 180 sec
Time maintained above 217°C	60 - 150 sec
Peak Temperature	255 - 260°C
Time within 5°C of actual Peak	20 - 40 sec
Ramp-Down Rate	6°C/sec Max.
Time 25°C to Peak Temperature	8 min Max.

OE Function and Output Waveform

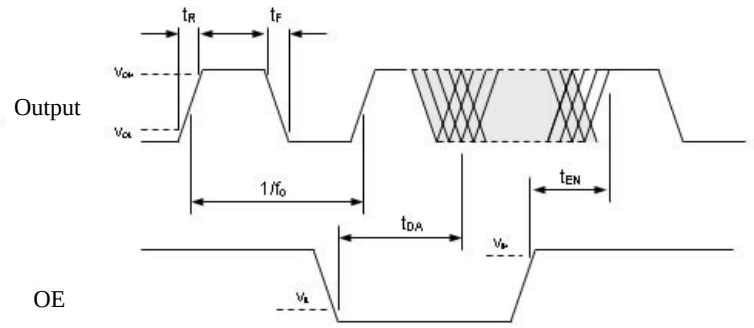
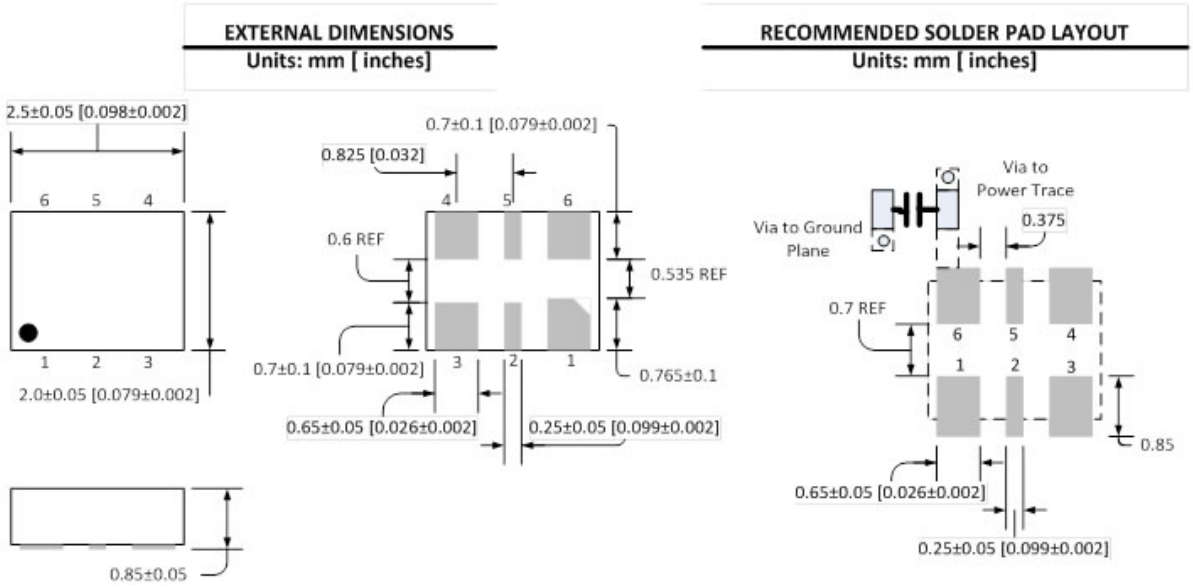


Figure 3. OE Function and Output Waveform

Package Information[7]



6-pin TDFN (2.5mm x 2.0mm)

Note:

7. Package information is correct as of the publication date. For updates and most current information, refer to DSA2311 master data sheet.

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