

## TPS2477x 2.5 to 18-V High Performance Hot Swap

### 1 Features

- 2.5V to 18V Bus Operation (30V abs max)
- Programmable Protection Settings:
  - Current Limit:  $\pm 5\%$  at 10mV
  - Fast Trip:  $\pm 10\%$  at 20mV
- Programmable FET SOA Protection
- Programmable Response Time for Fast Trip
- Dual Timer (Inrush/Fault)
- Analog Current Monitor (1% at 25mV)
- Programmable UV and OV
- Status Flags for Faults and Power Good
- 4mm x 4mm 24-pin QFN
- 70 = Latch, 71 = Retry, 72 = Fast Latch Off

### 2 Applications

- Enterprise Storage
- Enterprise Server
- Networking Cards
- 240 VA Applications

### 3 Description

The TPS2477x is a high performance analog Hot Swap Controller for 2.5 V to 18 V systems. The precise and highly programmable protection settings of the TPS2477x aid the design of high power high availability systems where isolating faults is critical.

Programmable current limit, fast shut down, and fault timer protect the load and supply during fault conditions such as a hot - short. The fast shutdown threshold and response time can be tuned to ensure a fast response to real faults, while avoiding nuisance trips. Programmable Safe Operating Area (SOA) protection and the inrush timer keep the MOSFET safe under all conditions. After asserting power good, TPS2477x acts as a circuit breaker and runs the fault timer during over current events, but doesn't current limit. It shuts down after the fault timer expires. Two independent timers (inrush/fault) allow the user to customize protection based on system requirements.

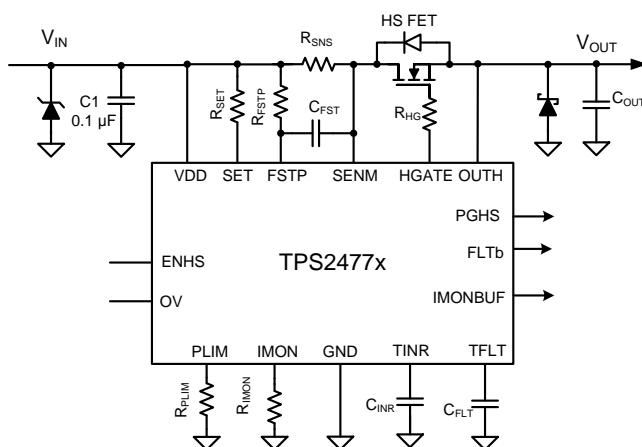
Finally, the flexibility of the TPS2477x aid Hot Swap design for the 240 VA requirement and a design example is shown in the datasheet.

#### Device Information<sup>(1)</sup>

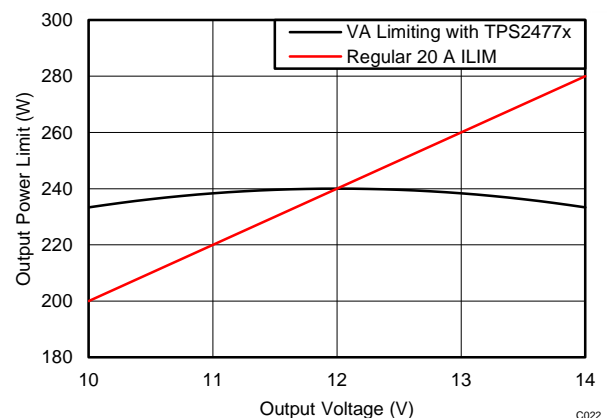
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS24770		
TPS24771	RGE (24)	4.00 mm x 4.00 mm
TPS24772		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



Limiting Output Power to 240VA,  
20 A  $I_{LIM}$  vs TPS2477x Implementation



c022



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	<b>10</b>
<b>2 Applications</b> .....	<b>1</b>	9.3 Feature Description .....	<b>11</b>
<b>3 Description</b> .....	<b>1</b>	9.4 Device Functional Modes .....	<b>16</b>
<b>4 Simplified Schematic</b> .....	<b>1</b>	<b>10 Application and Implementation</b> .....	<b>17</b>
<b>5 Revision History</b> .....	<b>2</b>	10.1 Application Information .....	<b>17</b>
<b>6 Device Comparison Table</b> .....	<b>3</b>	10.2 Typical Application .....	<b>17</b>
<b>7 Pin Configuration and Functions</b> .....	<b>3</b>	<b>11 Power Supply Recommendations</b> .....	<b>40</b>
<b>8 Specifications</b> .....	<b>4</b>	<b>12 Layout</b> .....	<b>40</b>
8.1 Absolute Maximum Ratings .....	<b>4</b>	12.1 Layout Guidelines .....	<b>40</b>
8.2 ESD Ratings .....	<b>4</b>	12.2 Layout Example .....	<b>42</b>
8.3 Recommended Operating Conditions .....	<b>5</b>	<b>13 Device and Documentation Support</b> .....	<b>43</b>
8.4 Thermal Information .....	<b>5</b>	13.1 Related Links .....	<b>43</b>
8.5 Electrical Characteristics .....	<b>5</b>	13.2 Trademarks .....	<b>43</b>
8.6 Timing Requirements .....	<b>7</b>	13.3 Electrostatic Discharge Caution .....	<b>43</b>
8.7 Typical Characteristics .....	<b>8</b>	13.4 Glossary .....	<b>43</b>
<b>9 Detailed Description</b> .....	<b>10</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>43</b>
9.1 Overview .....	<b>10</b>		

## 5 Revision History

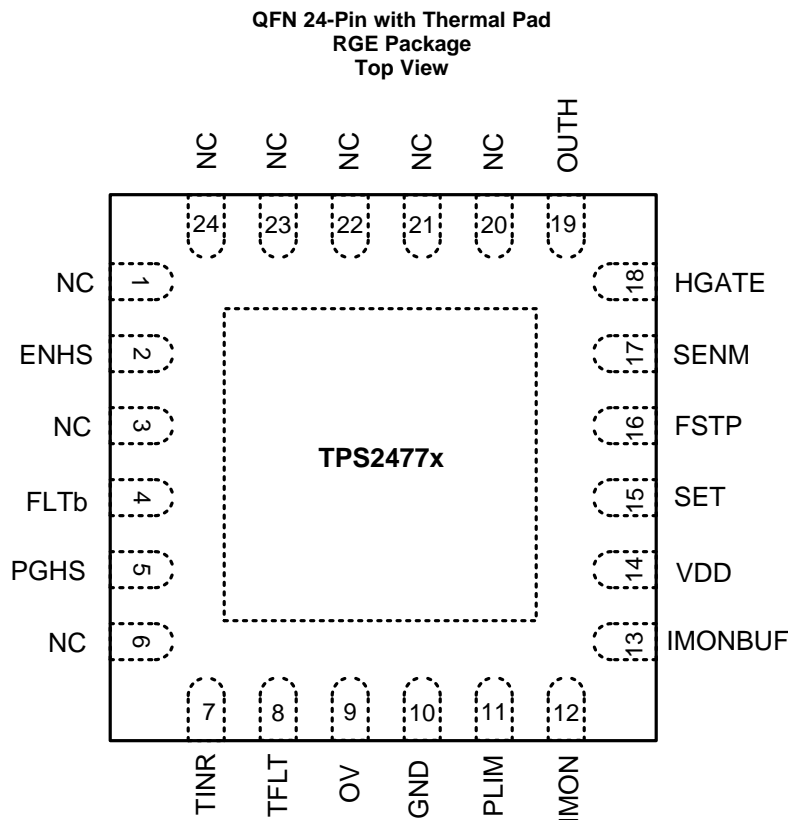
DATE	REVISION	NOTES
March 2015	*	Initial release.

## 6 Device Comparison Table

PART NUMBER <sup>(1)</sup>	LATCH / RETRY OPTION
TPS24770	Latch
TPS24771	Auto – Retry
TPS24772	Fast Latch Off

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## 7 Pin Configuration and Functions



### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
ENHS	2	I	Active-high enable input of Hot Swap. Logic input. Connects to resistor divider.
FLTb	4	O	Active-low, open-drain output indicating various faults.
FSTP	16	I	Fast trip programming set pin for Hot Swap. A resistor is connected from positive terminal of $R_{SNS}$ to FSTP.
GND	10	–	Ground.
HGATE	18	O	Gate driver output for external Hot Swap MOSFET.
IMON	12	I/O	Analog monitor and current limit program point. Connect $R_{IMON}$ to ground.
IMONBUF	13	O	Voltage output proportional to the load current (0V–3.0V).
NC	1, 3, 6, 20–24	NC	No connect. Tie to ground or leave floating.

(1) I = Input; O = Output ; P = Power, NC = No Connect

### Pin Functions (continued)

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
OUTH	19	I	Output voltage sensor for monitoring Hot Swap MOSFET's power. Connects to the source terminal of the Hot Swap N channel MOSFET.
OV	9	I	Overvoltage comparator input. Connects to resistor divider. HGATE is pulled low when OV exceeds the threshold. Connect to ground when not used.
PGHS	5	O	Active-high, open-drain power-good indicator.
PLIM	11	I	Power limit programming pin. A resistor from this pin to GND sets the maximum power dissipation for the Hot Swap FET. Connect a 4.99 kΩ resistor to disable power limit.
SENM	17	I	Current-sensing input for the sense resistor. Directly connects to the negative terminal of the sense resistor.
SET	15	I	Current-limit programming set pin for Hot Swap. A resistor is connected from positive terminal of the sensing resistor.
TFLT	8	I/O	Fault timer, which runs when the device is in regular operation and there is an overcurrent condition.
TINR	7	I/O	Inrush timer, which runs during the inrush operation (start-up) if the part is in current limit or power limit.
VDD	14	P	Power Supply

## 8 Specifications

### 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Input Voltage	VDD, SET, FSTP, SENM, OUTH, ENHS, FLTb, PGHS, OV	-0.3	30	V
	HGATE to OUTH	-0.3	15	V
	SET to VDD	-0.3	0.3	V
	SENM, FSTP to VDD	-0.6	0.3	V
	TINR, TFLT, PLIM, IMON	-0.3	3.6	V
	IMONBUF	-0.3	7	V
Sink Current	FLTb, PGHS		5	mA
Source Current	IMON, IMONBUF		5	mA
Storage temperature, T <sub>stg</sub>		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 8.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> <sup>(1)</sup>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(2)</sup>	±1500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup>	±500

- (1) Electrostatic discharge (ESD) measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.  
 (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VDD, SENM, SET, FSTP	2.5	18	V
	ENHS, FLTb, PGHS, OUTH	0	18	
Sink current	FLTb, PGHS	0	2	mA
Source current	IMON	0	1	mA
External resistance	PLIM	4.99	500	kΩ
	IMON	1	6	kΩ
	FSTP	10	4000	Ω
	SET	10	400	Ω
R <sub>IMON</sub> / R <sub>SET</sub>	w/o R <sub>STBL</sub>	10	70	
	With appropriate R <sub>STBL</sub> <sup>(1)</sup>	3	10	
	with C <sub>HGATE</sub> > 47nF <sup>(2)</sup>	10	200	
External capacitor	TINR, TFLT	1		nF
	HGATE, <sup>(2)</sup>	0	1	μF
	IMON		30	pF
	IMONBUF		100	pF
Operating junction temperature, T <sub>J</sub>		-40	125	°C

(1) Refer to R<sub>STBL</sub> Requirement for R<sub>IMON</sub> / R<sub>SET</sub> < 10 as described in section [Select R<sub>SNS</sub> and V<sub>SNS,CL</sub> Setting](#).

(2) External capacitance tied to HGATE, should be in series with a resistor no less than 1kΩ.

### 8.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		RGE	UNIT
		24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	34.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	38.4	
R <sub>θJB</sub>	Junction-to-board thermal resistance	12.9	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.5	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	12.9	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 8.5 Electrical Characteristics

Unless otherwise noted these limits apply to the following: -40°C < T<sub>J</sub> < 125°C; 2.5V < V<sub>VDD</sub>, V<sub>OUT</sub> < 18V; V<sub>ENHS</sub> = 2 V; V<sub>OV</sub> = 0 V; V<sub>HGATE</sub>, V<sub>PGHS</sub>, V<sub>FLTb</sub>, and V<sub>IMONBUF</sub> are floating; C<sub>INR</sub> = 1nF; C<sub>FLT</sub> = 1nF; R<sub>SET</sub> = 44.2 Ω; R<sub>IMON</sub> = 2.98k Ω; R<sub>FSTP</sub> = 200 Ω; R<sub>PLIM</sub> = 52 kΩ.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
<b>INPUT SUPPLY (VDD)</b>							
V <sub>UVR</sub>	UVLO threshold, rising			2.2	2.32	2.45	V
V <sub>UVhyst</sub>	UVLO hysteresis				0.10		V
I <sub>QON</sub>	Supply current: I <sub>VDD</sub> + I <sub>OUTH</sub>	Device on, V <sub>ENHS</sub> = 2V			2.95	4	mA
<b>Hot Swap FET ENABLE (ENHS)</b>							
V <sub>ENHS</sub>	Threshold voltage, rising			1.3	1.35	1.4	V
V <sub>ENShyst</sub>	Hysteresis				50		mV
I <sub>ENHS</sub>	Input Leakage Current	0 ≤ V <sub>ENHS</sub> ≤ 30V		-1		1	μA
<b>OVER VOLTAGE (OV)</b>							
V <sub>OV</sub>	Threshold voltage, rising			1.3	1.35	1.4	mV
V <sub>OVhyst</sub>	Hysteresis				50		mV
I <sub>OV</sub>	Input leakage current	0 ≤ V <sub>OV</sub> ≤ 30V		-1		1	μA

## Electrical Characteristics (continued)

Unless otherwise noted these limits apply to the following:  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ ;  $2.5\text{V} < V_{\text{VDD}}, V_{\text{OUT}} < 18\text{V}$ ;  $V_{\text{ENHS}} = 2\text{V}$ ;  $V_{\text{OV}} = 0\text{V}$ ;  $V_{\text{HGATE}}, V_{\text{PGHS}}, V_{\text{FLTb}}$ , and  $V_{\text{IMONBUF}}$  are floating;  $C_{\text{INR}} = 1\text{nF}$ ;  $C_{\text{FLT}} = 1\text{nF}$ ;  $R_{\text{SET}} = 44.2\ \Omega$ ;  $R_{\text{IMON}} = 2.98\text{k}\ \Omega$ ;  $R_{\text{FSTP}} = 200\ \Omega$ ;  $R_{\text{PLIM}} = 52\ \text{k}\Omega$ .

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>POWER LIMIT PROGRAMING (PLIM)</b>						
$V_{\text{PLIM,BIAS}}$	Bias voltage	Sourcing 10 $\mu\text{A}$	0.65	0.675	0.7	V
$V_{\text{IMON,PL}}$	Regulated IMON voltage during power limit	$R_{\text{PLIM}} = 52\ \text{k}\Omega$ ; $V_{\text{SENM-OUTH}}=12\text{V}$	114.75	135	155.25	mV
		$R_{\text{PLIM}} = 105\ \text{k}\Omega$ ; $V_{\text{SENM-OUTH}}=12\text{V}$	56.95	67	77.05	
		$R_{\text{PLIM}} = 261\ \text{k}\Omega$ ; $V_{\text{SENM-OUTH}}=12\text{V}$	18.9	27	35.1	
		$R_{\text{PLIM}} = 105\ \text{k}\Omega$ ; $V_{\text{SENM-OUTH}}=2\text{V}$	341.7	402	462.3	
		$R_{\text{PLIM}} = 105\ \text{k}\Omega$ ; $V_{\text{SENM-OUTH}}=18\text{V}$	38.25	45	51.75	
<b>SLOW TRIP THRESHOLD (SET)</b>						
$V_{\text{OS\_SET}}$	Input referred offset ( $V_{\text{SNS}}$ to $V_{\text{IMON}}$ scaling)	$R_{\text{SET}} = 44.2\ \Omega$ ; $R_{\text{IMON}}=3\text{k}\ \Omega$ to $1.2\text{k}\ \Omega$ ( $V_{\text{SNS,CL}}=10\text{mV}$ to $25\text{mV}$ )	-150		150	$\mu\text{V}$
$V_{\text{GE\_SET}}$	Gain error ( $V_{\text{SNS}}$ to $V_{\text{IMON}}$ scaling) <sup>(1)</sup>		-0.4%		0.4%	
<b>FAST TRIP THRESHOLD PROGRAMMING (FSTP)</b>						
$I_{\text{FSTP}}$	FSTP input bias current	$V_{\text{FSTP}}=12\text{V}$	95	100	105	$\mu\text{A}$
$V_{\text{FASTRIP}}$	Fast trip threshold	$R_{\text{FSTP}} = 200\ \Omega$ , $V_{\text{SNS}}$ when $V_{\text{HGATE}} \downarrow$	18	20	22	mV
		$R_{\text{FSTP}} = 1\ \text{k}\Omega$ , $V_{\text{SNS}}$ when $V_{\text{HGATE}} \downarrow$	95	100	105	
		$R_{\text{FSTP}} = 4\ \text{k}\Omega$ , $V_{\text{SNS}}$ when $V_{\text{HGATE}} \downarrow$	380	400	420	
<b>CURRENT SUMMING NODE (IMON)</b>						
$V_{\text{IMON,CL}}$	Slow trip threshold at summing node	$V_{\text{IMON}}\uparrow$ , when $I_{\text{TFLT}}$ starts sourcing	660	675	690	mV
$I_{\text{IMON-LKG}}$	IMON leakage current	$V_{\text{ENHS}} = 0\text{V}$ , $V_{\text{IMON}} = 1.5\text{V}$	-200		200	nA
<b>CURRENT MONITOR (IMONBUF)</b>						
$V_{\text{OS\_IMONBUF}}$	Buffer offset	$V_{\text{IMON}} = 50\text{mV}$ to $675\text{mV}$ , Input referred	-3	0	3	mV
$\text{GAIN}_{\text{IMONBUF}}$	Buffer voltage gain	$\Delta V_{\text{IMONBUF}} / \Delta V_{\text{IMON}}$	2.97	2.99	3.01	V
$\text{BW}_{\text{IMONBUF}}$	Buffer closed loop bandwidth	$C_{\text{IMONBUF}} = 75\text{pF}$		1		MHz
<b>Hot Swap GATE DRIVER (HGATE)</b>						
$V_{\text{HGATE}}$	HGATE output voltage	$5 \leq V_{\text{VDD}} \leq 16\text{V}$ ; measure $V_{\text{HGATE-OUTH}}$	12	13.6	15.5	V
		$2.5\text{V} < V_{\text{VDD}} < 5\text{V}$ ; $16\text{V} < V_{\text{VDD}} < 20\text{V}$ measure $V_{\text{HGATE-OUTH}}$	7	7.95	15	V
$V_{\text{HGATEmax}}$	Clamp voltage	Inject 10 $\mu\text{A}$ into HGATE, measure $V_{\text{(HGATE - OUTH)}}$	12	13.9	15.5	V
$I_{\text{HGATEsrc}}$	Sourcing current	$V_{\text{HGATE-OUTH}} = 2\text{V}-10\text{V}$	44	55	66	$\mu\text{A}$
$I_{\text{HGATEfastSink}}$	Sinking current for fast trip	$V_{\text{HGATE-OUTH}} = 2\text{V}-15\text{V}$ ; $V_{\text{(FSTP - SENM)}} = 20\text{mV}$	0.45	1	1.6	A
$I_{\text{HGATEsustSink}}$	Sustained sinking current	Sustained, $V_{\text{HGATE-OUTH}} = 2\text{V} - 15\text{V}$ ; $V_{\text{ENHS}} = 0$	30	44	60	mA
<b>INRUSH TIMER (TINR)</b>						
$I_{\text{TINRsrc}}$	Sourcing current	$V_{\text{TINR}} = 0\text{V}$ , In power limit or current limit	8	10.25	12.5	$\mu\text{A}$
$I_{\text{TINRsink}}$	Sinking current	$V_{\text{TINR}} = 2\text{V}$ , In regular operation	1.5	2	2.5	$\mu\text{A}$
$V_{\text{TINRup}}$	Upper threshold voltage	Raise $V_{\text{TINR}}$ until HGATE starts sinking	1.3	1.35	1.4	V
$V_{\text{TINRir}}$	Lower threshold voltage	Raise $V_{\text{TINR}}$ to 2V. Reduce $V_{\text{TINR}}$ until $I_{\text{TINR}}$ is sourcing.	0.33	0.35	0.37	v
$R_{\text{TINR}}$	Bleed down resistance	$V_{\text{VDD}} = 0\text{V}$ , $V_{\text{TINR}} = 2\text{V}$	70	104	130	k $\Omega$
$I_{\text{TINR-PD}}$	Pulldown current	$V_{\text{TINR}} = 2\text{V}$ , when $V_{\text{ENHS}} = 0\text{V}$	2	4.2	7	mA
$\text{RETRY}_{\text{CYCLE}}$	Cycle number	# of timer cycles before retry (TPS24771 only)	64	64	64	
$\text{RETRY}_{\text{DUTY}}$	Retry duty cycle	TFLT and TINR connected (TPS24771 only)		0.70%		
		TFLT and TINR not connected (TPS24771 only)		0.35%		
$V_{\text{IMON,TINR}}$	See <a href="#">Using Soft Start - I<sub>HGATE</sub> and TINR Considerations</a>	$R_{\text{PLIM}} = 52\text{k}\Omega$ , $V_{\text{SENM}} = 12\text{V}$ , $V_{\text{OUTH}} = 0\text{V}$ . Raise IMON voltage and record IMON when TINR starts sourcing current.	47.75	90	132.25	mV
$V_{\text{IMON,PL}}$	See <a href="#">Using Soft Start - I<sub>HGATE</sub> and TINR Considerations</a>	$R_{\text{PLIM}} = 52\text{k}\Omega$ , $V_{\text{SENM-OUTH}} = 12\text{V}$ , Raise IMON voltage and record IMON when $I_{\text{HGATE}}$ starts sinking current.	114.75	135	155.25	mV
$\Delta V_{\text{IMON,TINR}}$	See <a href="#">Using Soft Start - I<sub>HGATE</sub> and TINR Considerations</a>	$\Delta V_{\text{IMON,TINR}} = V_{\text{IMON,PL}} - V_{\text{IMON,TINR}}$	23	45	67	mV

(1) Specified by characterization.

## Electrical Characteristics (continued)

Unless otherwise noted these limits apply to the following:  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ ;  $2.5\text{V} < V_{\text{VDD}}, V_{\text{OUT}} < 18\text{V}$ ;  $V_{\text{ENHS}} = 2\text{V}$ ;  $V_{\text{OV}} = 0\text{V}$ ;  $V_{\text{HGATE}}, V_{\text{PGHS}}, V_{\text{FLTB}}$ , and  $V_{\text{IMONBUF}}$  are floating;  $C_{\text{INR}} = 1\text{nF}$ ;  $C_{\text{FLT}} = 1\text{nF}$ ;  $R_{\text{SET}} = 44.2\ \Omega$ ;  $R_{\text{IMON}} = 2.98\text{k}\ \Omega$ ;  $R_{\text{FSTP}} = 200\ \Omega$ ;  $R_{\text{PLIM}} = 52\ \text{k}\Omega$ .

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>FAULT TIMER (TFLT)</b>						
$I_{\text{TFLTsrc}}$	Sourcing current	$V_{\text{TFLT}} = 0\text{V}$ , PGHS is high and in overcurrent	8	10.25	12.5	$\mu\text{A}$
$I_{\text{TFLTsink}}$	Sinking current	$V_{\text{TFLT}} = 2\text{V}$ , Not in overcurrent	1.5	2	2.5	$\mu\text{A}$
$V_{\text{TFLTup}}$	Upper threshold voltage	Raise $V_{\text{TFLT}}$ until HGATE starts sinking	1.3	1.35	1.4	V
$R_{\text{TFLT}}$	Bleed down resistance	$V_{\text{ENHS}} = 0\text{V}$ , $V_{\text{TFLT}} = 2\text{V}$	70	104	130	$\text{k}\Omega$
$I_{\text{TFLT-PD}}$	Pulldown current	$V_{\text{TFLT}} = 2\text{V}$ , when $V_{\text{ENHS}} = 0\text{V}$	2	5.6	7	mA
<b>HOT SWAP OUTPUT (OUTH)</b>						
$I_{\text{OUTH, BIAS}}$	Input bias current	$V_{\text{OUTH}} = 12\text{V}$		30	70	$\mu\text{A}$
<b>FAULT INDICATOR (FLTb)</b>						
$V_{\text{OL\_FLTb}}$	Output low voltage	Sinking 2 mA		0.11	0.25	V
$I_{\text{FLTb}}$	Input leakage current	$V_{\text{FLTb}} = 0\text{V}, 30\text{V}$	-1	0	1	$\mu\text{A}$
$V_{\text{HSFLT\_IMON}}$	$V_{\text{IMON}}$ threshold to detect Hot Swap FET short	$V_{\text{ENHS}} = 0\text{V}$ , Measured $V_{\text{IMON}} \uparrow$ to GND when FLTb $\downarrow$	88	101	115	mV
$V_{\text{HSFL\_hyst}}$	Hysteresis			25		mV
<b>HOT SWAP POWER GOOD OUTPUT (PGHS)</b>						
$V_{\text{PGHStH}}$	PGHS Threshold	Measure $V_{\text{SENEM-OUTH}} \downarrow$ when PGHS $\uparrow$	170	270	375	mV
$V_{\text{PGHShyst}}$	PGHS hysteresis	$V_{\text{SENEM-OUTH}} \uparrow$		80		mV
$V_{\text{OL\_PGHS}}$	PGHS Output low voltage	Sinking 2mA		0.11	0.25	V
$I_{\text{PGHS}}$	PHGS Input leakage current	$V_{\text{PGHS}} = 0\text{V}$ to $30\text{V}$	-1	0	1	$\mu\text{A}$
<b>THERMAL SHUTDOWN (OTSD)</b>						
$T_{\text{OTSD}}$	Thermal shutdown threshold	Temperature rising		140		$^{\circ}\text{C}$
$T_{\text{OTSD,HYST}}$	Hysteresis			10		$^{\circ}\text{C}$

## 8.6 Timing Requirements

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT SUPPLY (VDD)</b>						
$\text{DEGL}_{\text{UVLO}}$	UVLO deglitch	Both rising and falling		14		$\mu\text{s}$
<b>HOT SWAP FET ENABLE (ENHS)</b>						
$\text{DEGL}_{\text{ENHS}}$	Deglitch time	Both rising and falling	2.2	3.8	5.5	$\mu\text{s}$
<b>OVER VOLTAGE (OV)</b>						
$\text{DEGL}_{\text{OV}}$	Deglitch time	Both rising and falling	2.2	3.9	5.7	$\mu\text{s}$
<b>FAST TRIP (FSTP)</b>						
$t_{\text{FastOffDly}}$	Fast turn-off delay	$V_{\text{(FSTP - SENM)}} : -5\text{mV}$ to $5\text{mV}$ , $C_{\text{HGATE}} = 0\ \text{pF}$		600		ns
		$V_{\text{(FSTP - SENM)}} : -20\text{mV}$ to $20\text{mV}$ , $C_{\text{HGATE}} = 0\ \text{pF}$		300		
$t_{\text{FastOffDur}}$	Strong pull down current duration		53	63	73	$\mu\text{s}$
<b>INRUSH TIMER (TINR)</b>						
$N_{\text{RETRY}}$	Number of TINR cycles before retry	TPS24741 only		64		
$\text{RETRY}_{\text{DUTY}}$	Retry duty cycle	$T_{\text{INR}}$ not connected to $T_{\text{FLT}}$		0.35%		
		$T_{\text{INR}}$ connected to $T_{\text{FLT}}$		0.7%		
<b>FAULT INDICATOR (FLTb)</b>						
$t_{\text{FLT\_degl}}$	Fault deglitch	Both rising and falling	2.2	3.9	5.3	ms
<b>HOT SWAP POWER GOOD OUTPUT (PGHS)</b>						
$t_{\text{PGHSdegl}}$	PGHS deglitch time	Rising	0.7	1	1.3	ms
		Falling	7	8	9	

## 8.7 Typical Characteristics

Unless otherwise noted these curves apply to the following:  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ ;  $2.5\text{V} < V_{\text{VDD}}, V_{\text{OUT}} < 18\text{V}$ ;  $V_{\text{ENHS}} = 2\text{V}$ ;  $V_{\text{OV}} = 0\text{V}$ ;  $V_{\text{HGATE}}, V_{\text{PGHS}}, V_{\text{FLTb}}$ , and  $V_{\text{IMONBUF}}$  are floating;  $C_{\text{INR}} = 1\text{nF}$ ;  $C_{\text{FLT}} = 1\text{nF}$ ;  $R_{\text{SET}} = 44.2\ \Omega$ ;  $R_{\text{IMON}} = 2.98\text{k}\ \Omega$ ;  $R_{\text{FSTP}} = 200\ \Omega$ ;  $R_{\text{PLIM}} = 52\ \text{k}\Omega$ .

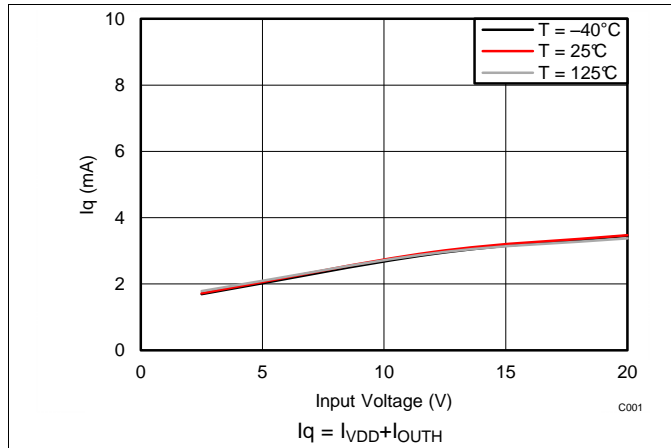


Figure 1.

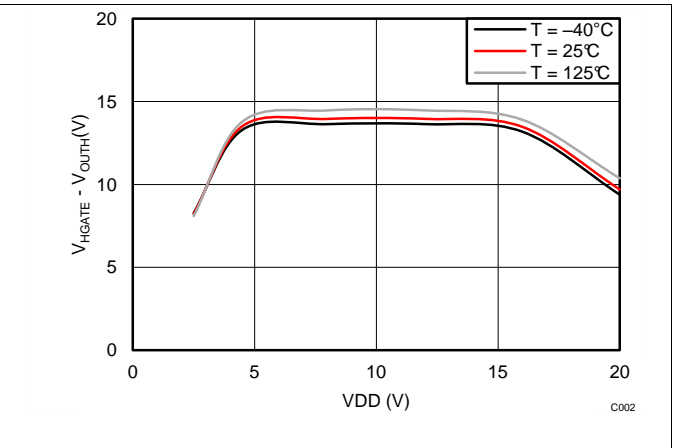


Figure 2.

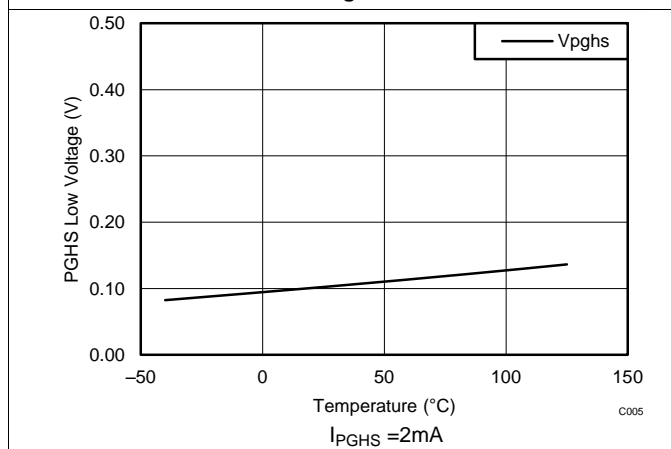


Figure 3.

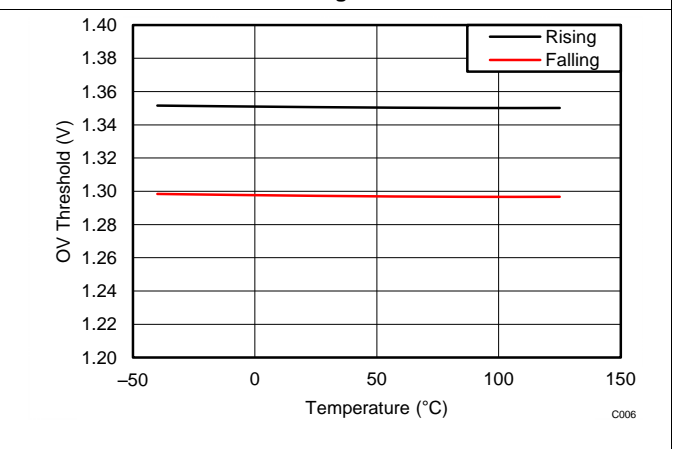


Figure 4.

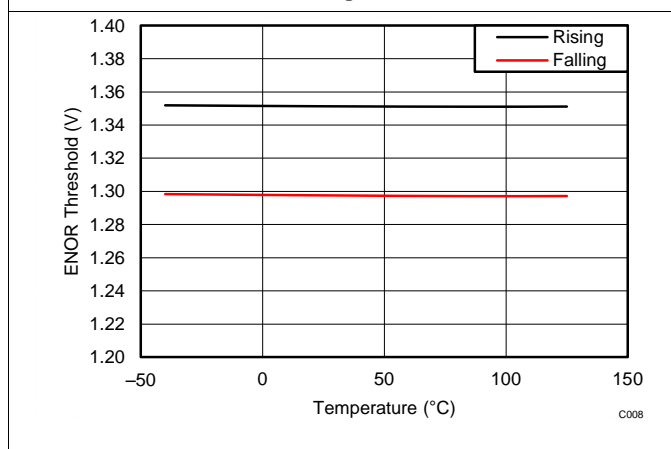


Figure 5.

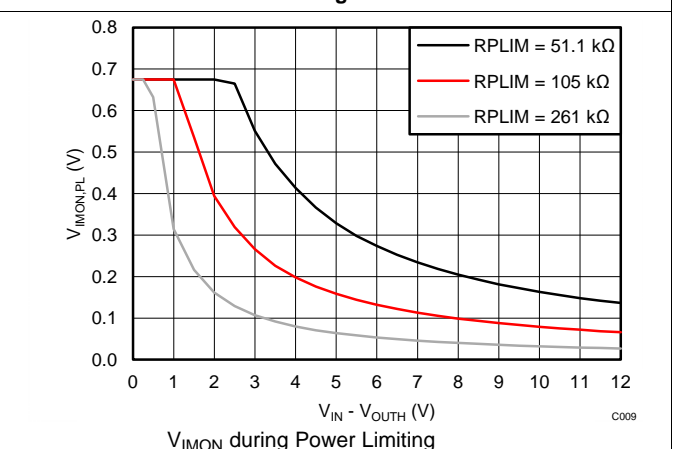


Figure 6.



### Typical Characteristics (continued)

Unless otherwise noted these curves apply to the following:  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ ;  $2.5\text{V} < V_{\text{VDD}}$ ;  $V_{\text{OUT}} < 18\text{V}$ ;  $V_{\text{ENHS}} = 2\text{V}$ ;  $V_{\text{OV}} = 0\text{V}$ ;  $V_{\text{HGATE}}$ ,  $V_{\text{PGHS}}$ ,  $V_{\text{FLTB}}$ , and  $V_{\text{IMONBUF}}$  are floating;  $C_{\text{INR}} = 1\text{nF}$ ;  $C_{\text{FLT}} = 1\text{nF}$ ;  $R_{\text{SET}} = 44.2\ \Omega$ ;  $R_{\text{IMON}} = 2.98\text{k}\ \Omega$ ;  $R_{\text{FSTP}} = 200\ \Omega$ ;  $R_{\text{PLIM}} = 52\ \text{k}\ \Omega$ .

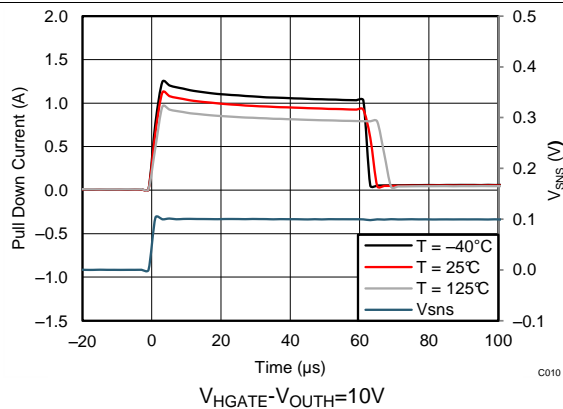


Figure 7.

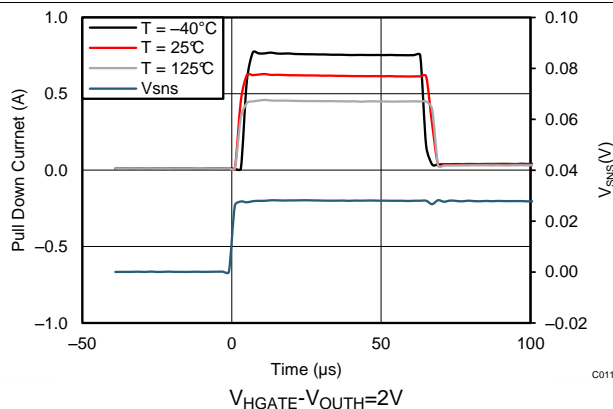


Figure 8.

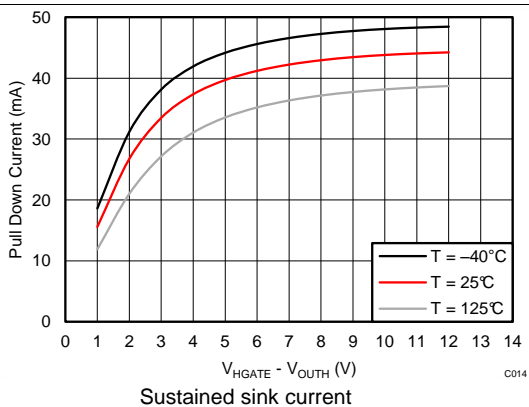


Figure 9.

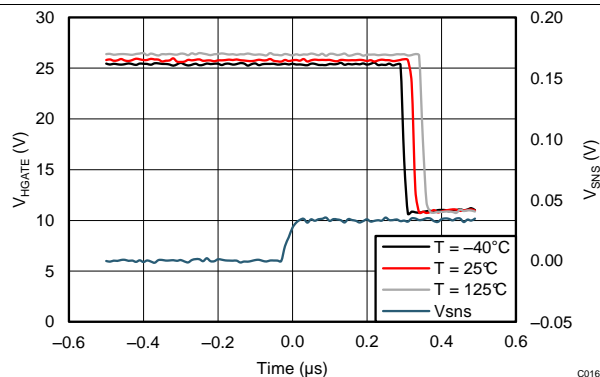


Figure 10.

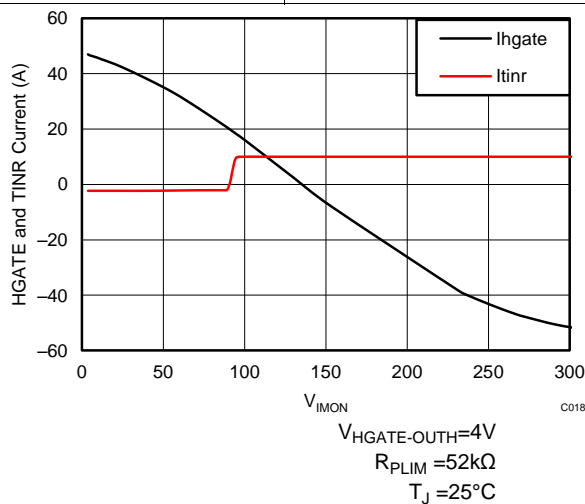


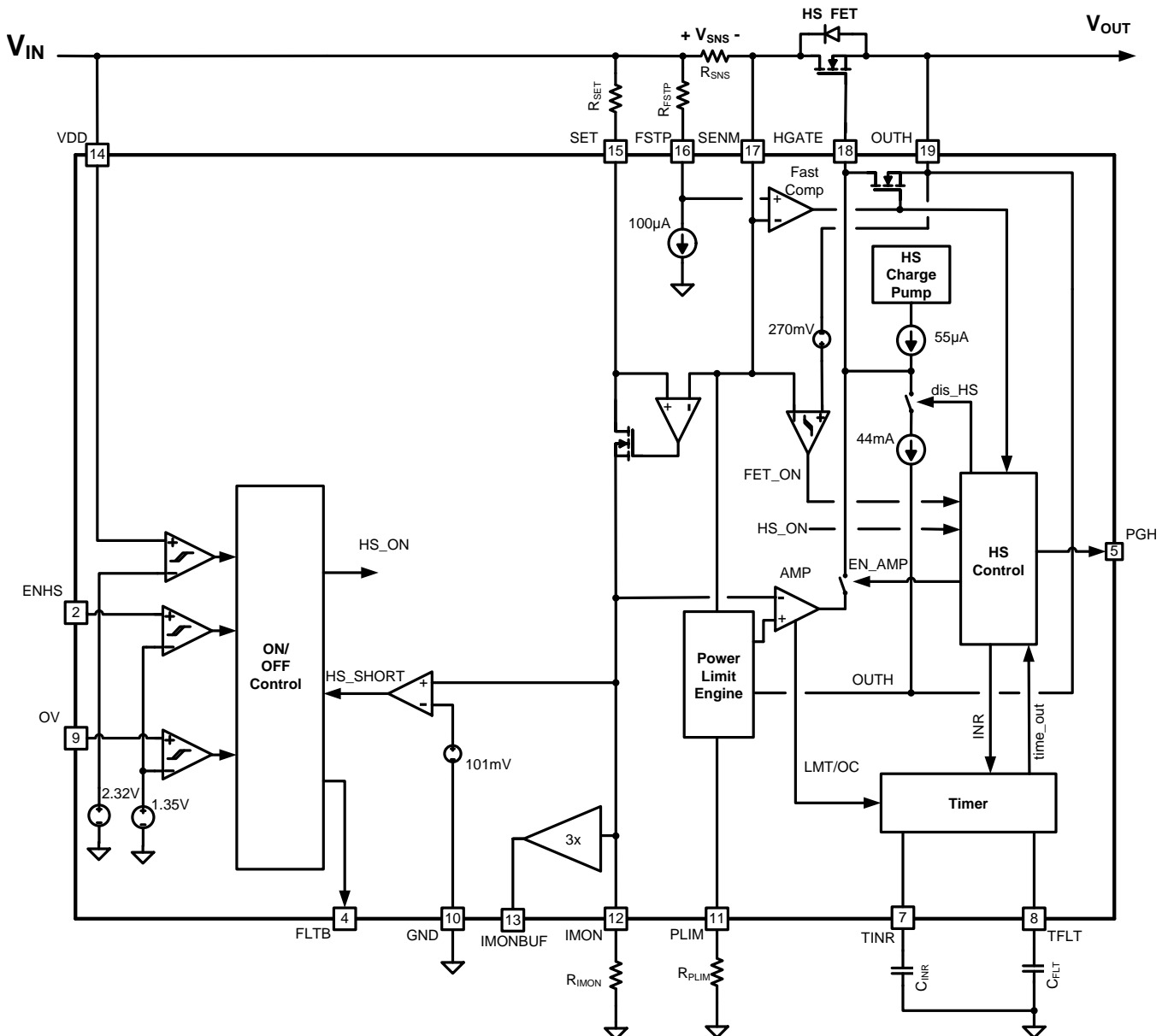
Figure 11.

## 9 Detailed Description

### 9.1 Overview

The TPS2477x Hot Swap features a programmable current limit, power limit, and fast trip threshold. It also has dual timers: one for inrush and one during over current faults. Finally it features an analog current monitor that can be used to provide current information to a microcontroller.

### 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Enable and Over-voltage Protection

The part is enabled when the ENHS pin voltage exceeds 1.35V and is disabled when the pin voltage falls under 1.3V providing 50mV of hysteresis. A resistor divider can be connected to these pins to turn on the TPS2477x at a certain bus voltage. The part will turn off if the OV pin exceeds 1.35V.

### 9.3.2 Current Limit and Power Limit during Start-up

The current limit and power limit of the TPS2477x are programmable to protect the load, power supply, and the Hot Swap MOSFET. During start-up the active control loop will regulate the gate to ensure that the current through the MOSFET and the power dissipation of the MOSFET is below their respective pre-programmed thresholds. The maximum current allowed through the MOSFET ( $I_{LIM}$ ) is determined with the equation below.  $I_{LIM,CL}$  is the programmed current limit,  $P_{LIM}$  is the programmed power limit, and  $V_{DS}$  is the drain to source voltage across the Hot Swap MOSFET.

$$I_{LIM} = \text{MIN} \left( I_{LIM,CL}, \frac{P_{LIM}}{V_{DS}} \right) \quad (1)$$

This results in an IV curve shown in Figure 12.  $I_{LIM,PL}$  denotes the maximum allowed MOSFET current ( $I_{DS}$ ) when the part is in power limit. As  $V_{DS}$  increases,  $I_{LIM,PL}$  decreases and  $I_{LIM,PL,MIN}$  denotes the lowest  $I_{LIM,PL}$ , which occurs at the largest  $V_{DS}$  ( $V_{DS,MAX}$ ). The TPS2477x enforce this by regulating the voltage across  $R_{SNS}$  ( $V_{SNS}$ ).  $V_{SNS,PL}$  denotes  $V_{SNS}$  when power limiting is active. Similarly to  $I_{LIM,PL}$ ,  $V_{SNS,PL}$  decreases as  $V_{DS}$  increases and  $V_{SNS,PL,MIN}$  corresponds to the lowest  $V_{SNS,PL}$ , which occurs at  $V_{DS,MAX}$ .  $V_{SNS,CL}$  is a current limiting sense voltage, which is programmable in the TPS2477x.

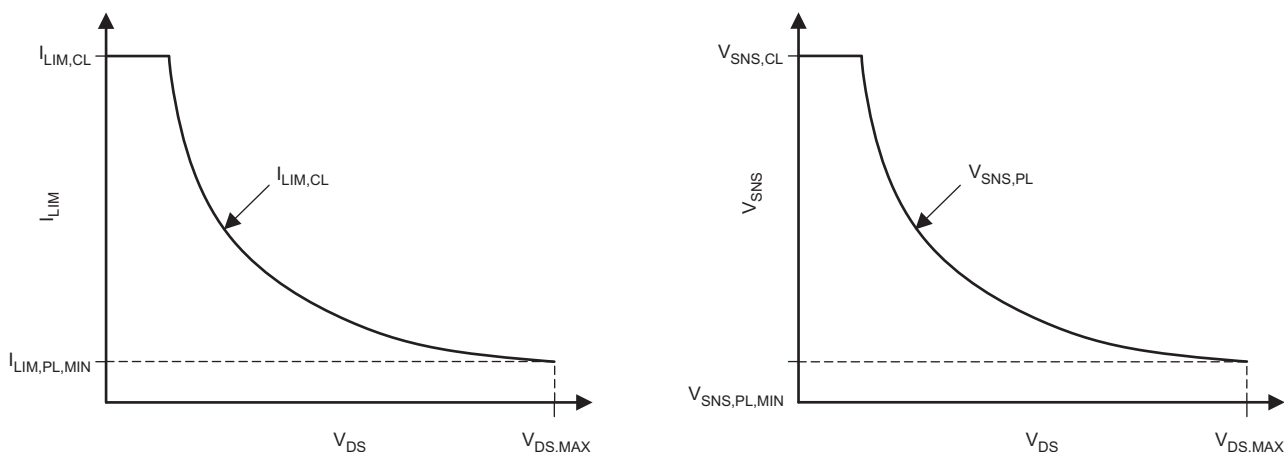


Figure 12. Current vs  $V_{DS}$  and  $V_{SNS}$  vs  $V_{DS}$  Programmed by Power Limit Engine.

The current and power limit can be programmed using the equations below.

$$V_{SNS,CL} = \frac{0.675 \times R_{SET}}{R_{IMON}} \quad (2)$$

$$I_{LIM,CL} = \frac{V_{SNS,CL}}{R_{SNS}} = \frac{0.675 \times R_{SET}}{R_{SNS}} \quad (3)$$

$$P_{LIM} = \frac{84375 \times R_{SET}}{R_{PLIM} \times R_{SNS} \times R_{IMON}} \quad (4)$$

## Feature Description (continued)

Note, that the error is largest at  $V_{SNS,PL,MIN}$  due to offset of the internal amplifier. Also the operation at  $V_{DS,MAX}$  is most critical because it corresponds to the short circuit condition and has the biggest impact on start time. Thus it is critical to consider  $V_{SNS,PL,MIN}$  during design. Equation 5 shows the relationship of  $V_{SNS,PL,MIN}$  as a function of  $P_{LIM}$ ,  $I_{LIM,CL}$ ,  $V_{SNS,CL}$ , and  $V_{DS,MAX}$ . Note that  $I_{LIM,CL}$  and  $V_{DS,MAX}$  are usually determined by the system requirements. The designer will have control over  $P_{LIM}$  and  $V_{SNS,CL}$ . In general, there will be a desire to reduce the power limit to allow for smaller MOSFETs and to reduce the  $V_{SNS,CL}$  to improve efficiency (lower  $R_{SNS}$ ). However, this will also reduce  $V_{SNS,PL,MIN}$  and the designer should ensure that it's above the minimum recommended value of 1.5mV.

$$V_{SNS,PL,MIN} = \frac{P_{LIM} \times V_{SNS,CL}}{V_{DS,MAX} \times I_{LIM,CL}} \quad (5)$$

### 9.3.3 Two Level Protection During Regular Operation

After the TPS2477x has gone through start-up it will no longer actively control the gate. Instead it will run the timer when the current is between the current limit and the fast trip threshold. Once the timer has expired the gate will be pulled down. If the current ever exceeds the fast trip threshold, the gate will be pulled down immediately.

### 9.3.4 Dual Timer (TFLT and TINR)

TPS2477x has two timer pins to allow the user to customize the protection. The TINR pin will source 10.25  $\mu$ A when the device is in start-up mode and is actively regulating the gate to limit the MOSFET power or current. It will sink 2  $\mu$ A otherwise. The TFLT pin will source 10.25  $\mu$ A when the device is in regular operation and the FET current exceeds the current limit. It will sink 2  $\mu$ A otherwise. If either of the timer pins exceeds 1.35, the TPS2477x will time out. The TPS24770 and TPS24772 will latch off. The TPS24771 will go through 64 cycles of TINR and attempt to start-up again.

Since the TINR usually runs when the MOSFET is being stressed, TINR should be sized to maintain the FET within its SOA. In general TFLT runs when the load is drawing more current than expected, which can stress the load and the power supply. Thus TFLT should be programmed to have the right protection settings for the power supply and the load. In some systems the load is allowed to draw current above the current limit for 250ms or 1s. In that case a large TFLT is required, but a short TINR may still be desired to minimize the worst case FET stress. In other applications a long TINR may be required to due to large downstream capacitances, but drawing excessive current from the power supply for more than 5ms is not desired. In that case a short TFLT and a long TINR should be used. Finally, many applications can use the same TINR and TFLT setting, in which case the pins can be tied together and a single capacitor can be used. The two different options are shown in Figure 13.

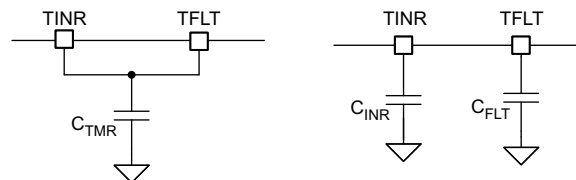


Figure 13. Timer Configurations

If two separate timer capacitors are used their values can be computed with the equations below:

$$C_{INR} = 7.59 \mu\text{F} / \text{s} \times T_{INR} \quad (6)$$

$$C_{FLT} = 7.59 \mu\text{F} / \text{s} \times T_{FLT} \quad (7)$$

If a single capacitor is used  $C_{TMR}$  can be computed with Equation 8.

## Feature Description (continued)

$$C_{TMR} = 6.11 \mu\text{F} / \text{s} \times T_{TMR} \quad (8)$$

### 9.3.5 3 Options for Response to a Fast Trip

The TPS24770, TPS24771, and TPS24772 have different responses to a fast trip event to accommodate different design requirements. When the current exceeds the fast trip threshold, the gate is quickly pulled down to minimize damage that can be caused due to a short circuit. Figure 14 shows the response of the various device options to a hot short on the output. The TPS24770 (latch) will attempt to re-start once after the hot-short is observed and then stay off, the TPS24771 will continuously retry with a duty cycle of ~0.5% (0.7% if  $T_{FLT}$  and  $T_{INR}$  are connected, 0.35% if  $T_{FLT}$  and  $T_{INR}$  are not connected), and the TPS24772 (fast latch off) will shut off and never retry again. In general the TPS24772 will place the least amount of stress on the MOSFET, but is the least likely to recover from a nuisance trip.

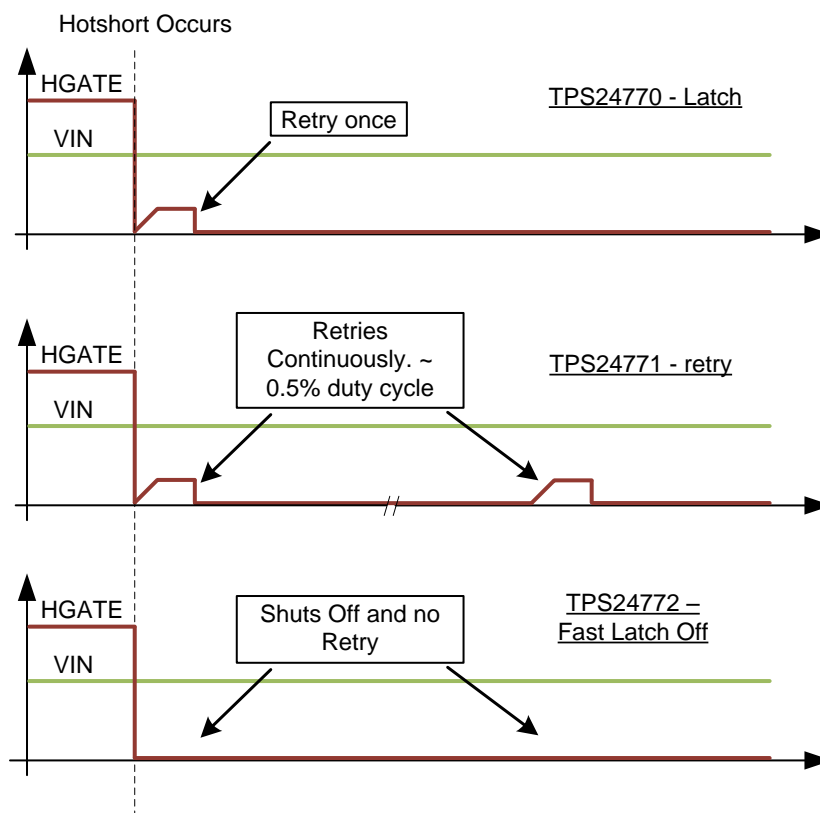


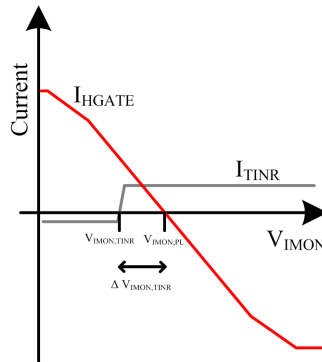
Figure 14. TPS24770/1/2 Response to a Short Circuit

### 9.3.6 Using Soft Start - $I_{HGATE}$ and $T_{INR}$ Considerations

During start-up the TPS2477x regulates the HGATE to keep the FET power dissipation within  $P_{LIM}$ . This is accomplished by an amplifier that monitors the IMON voltage and an internal reference voltage. The TPS2477x will source current into HGATE if  $V_{IMON}$  is lower than the reference voltage and will sink current into HGATE if  $V_{IMON}$  is above the reference voltage. In steady state, the  $V_{IMON}$  will be regulated to the  $V_{IMON,PL}$  point, where  $I_{HGATE}$  equals zero. Note that  $V_{IMON,PL}$  is determined by  $R_{PLIM}$  and  $V_{SENSE} - V_{OUTH}$ .

The same amplifier feeds into the inrush timer circuitry to run the timer when the part is in power limit. The  $V_{IMON}$  threshold at which the timer starts to source current is denoted as  $V_{IMON, T_{INR}}$ . Note that  $V_{IMON, T_{INR}}$  is lower than  $V_{IMON, PL}$  to account for tolerances and ensure that the timer is always active when the device is in power limit. The difference between the two thresholds is defined as  $\Delta V_{IMON, T_{INR}}$ . Refer to Figure 11 for a typical  $I_{HGATE}$  and  $I_{T_{INR}}$  vs  $V_{IMON}$  curve.

## Feature Description (continued)



**Figure 15.  $I_{TINR}$  and  $I_{HGATE}$  vs  $V_{IMON}$  ( $V_{DS} = 12V$ ,  $R_{PLIM} = 52k\Omega$ )**

It is critical to consider  $\Delta V_{IMON, TINR}$  and [Figure 15](#) if a soft start circuit is used. Typically, the soft start is implemented by limiting the gate  $dv/dt$  with a capacitor, which in turn limits the inrush current to the output capacitor. Often times, the inrush current is kept below  $I_{LIM,PL}$  to keep the timer from running. Note that the  $I_{LIM,PL}$  is based on the  $V_{IMON,PL}$  threshold and thus  $T_{INR}$  can be activated even if the inrush current is below  $I_{LIM,PL}$ . To prevent the timer from running unintentionally, the  $P_{LIM}$  should be chosen above  $P_{LIM,MIN,SS}$ , which can be computed as shown below. As an example consider the usage case where the maximum inrush current ( $I_{INR,MAX}$ ) is 2A, the maximum input voltage ( $V_{IN,MAX}$ ) is 13V and  $R_{SET}$ ,  $R_{IMON}$ , and  $R_{SNS}$  are  $100\Omega$ ,  $2.7k\Omega$ , and  $1m\Omega$  respectively. For that case the power limit should be set to at least  $58.3W + P_{LIM}$  tolerance to ensure that the inrush timer doesn't run.

$$\begin{aligned}
 P_{LIM,MIN,SS} &= \left( I_{INR,MAX} + \Delta V_{IMON,TINR,MAX} \times \frac{R_{SET}}{R_{IMON} \times R_{SNS}} \right) \times V_{IN,MAX} \\
 &= \left( 2A + 67mV \times \frac{100\Omega}{2.7k\Omega \times 1m\Omega} \right) \times 13V = 58.3W
 \end{aligned}
 \tag{9}$$

### 9.3.7 Analog Current Monitor

The TPS2477x also features two analog current monitoring outputs: IMON and IMONBUF. Each has their own advantages and disadvantages. The IMON is more accurate, because it doesn't have the error added from the second stage. However it is a high impedance output and leakage current on that node would result in monitoring error. In addition it can only support 30pF of capacitance and its full scale range is 675mV (this is where current limit kicks in). The IMONBUF takes the IMON signal and buffers it 3x. This introduces more error, but the output is low impedance, has a larger full scale range, and can drive up to 100pF of capacitance.

## Feature Description (continued)

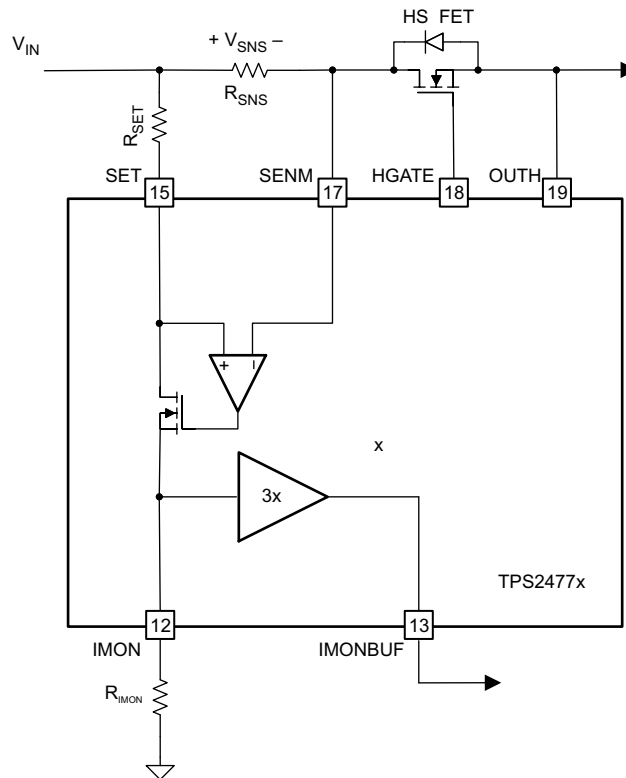


Figure 16. Current Monitoring Circuitry

### 9.3.8 Power Good Flag

The TPS2477x has a power good flag, which should be used to turn on downstream DC/DC converters. This reduces the stress on the Hot Swap MOSFET during start-up. The PGHS pin of the TPS2477x is asserted (with 1 ms deglitch) when both:

- Hot Swap is enabled and
- $V_{DS}$  of Hot Swap MOSFET is below 240 mV.

PGHS is de-asserted (with 8 ms deglitch) when either:

- Hot Swap is disabled.
- $V_{DS}$  of Hot Swap MOSFET is above 310 mV
- In an overcurrent condition that causes the timer to time out and latch off.

### 9.3.9 Fault Reporting

TPS2477x will assert a fault by pulling down on the FLTb pin if any of the following occur:

- Hot Swap MOSFET Shorted Fault ( ENHS = LO, but VIMON > 101 mV)
- Hot Swap timer times out.
- Over Temperature Shut Down (OTSD)

## 9.4 Device Functional Modes

### 9.4.1 Hot Swap Functional Modes

The state machine for the Hot Swap section is shown in Figure 17. After a POR / UVLO event the Hot Swap enters the Inrush up. Once operational the Hot Swap has the following functional modes:

- **Inrush Mode (INR):** In this state the Hot Swap controller is actively regulating the HGATE to meet the current limit and power limit settings. The inrush timer is running if the controller is in power or current limiting. If the inrush timer times out the gate will be pulled down. The TPS24770 and TPS24772 will go to latched mode and TPS24771 will go into retry mode.
- **Regular Operation Mode (REG):** In this mode everything is operating properly so both the timers are discharged and the HGATE is high. If there is an overcurrent condition ( $V_{SNS} > V_{SNS,CL}$ ), the device will go into fault mode. If there is a fast trip condition ( $V_{SNS} > V_{FSTP}$ ), the gate will be pulled down with a 1A / 63  $\mu$ s pulse. The TPS24772 will go to the latched state and the TPS24770 and TPS24771 will go back to inrush for a retry.
- **Fault Mode (FLT):** In this mode the TPS2477x runs the fault timer. Once the timer expires the TPS24770 and TPS24772 will go to latch mode while TPS24771 will go to retry mode. If the overcurrent condition is removed the controller will go back to the regular operation mode.
- **Latched Mode (Latched):** In the latched mode the HGATE is low, the timer is being discharged, and the FLTb is asserted. If there is a rising edge on ENHS the part will discharge the timers and go to the inrush mode.
- **Retry Mode (Retry):** Here the part will charge and discharge the inrush timer 64 times before attempting another retry.

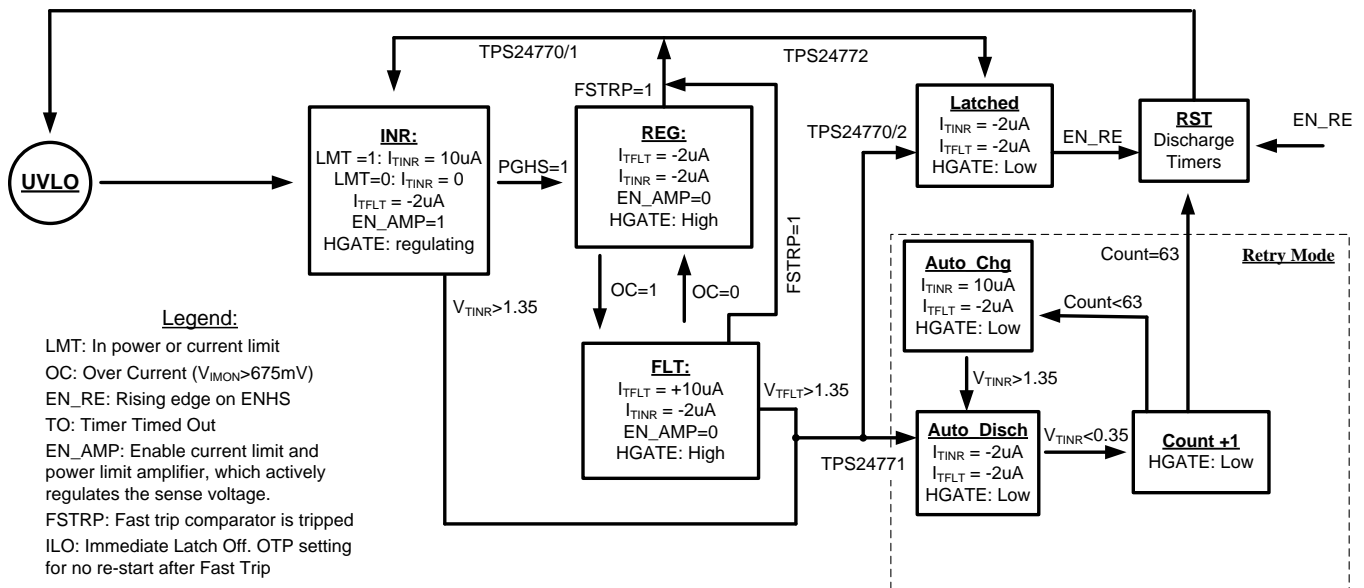


Figure 17. Hot Swap State Machine



## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The TPS2477x is a highly configurable Hot Swap controller that can be fine-tuned for the application requirement. When designing a Hot Swap 3 key scenarios should be considered:

- Start-up.
- Output of a Hot Swap is shorted to ground when the Hot Swap is on. This is often referred to as a “Hot-Short”.
- Powering up a board when the output and ground are shorted. This is usually called a “start into short”.

All of these scenarios place a lot of stress on the Hot Swap MOSFET and special care must be taken when designing the Hot Swap circuit to keep the MOSFET within its Safe Operating Area (SOA). Note that the component selection can often be iteratively and it's recommended to use the publically available excel calculators to crunch the numbers. See the [TPS24770 Design Calculator](#) in the Tools & Software link on the Product folder.

### 10.2 Typical Application

Three application examples are provided. The first one is for a 100A Hot Swap with 5,500  $\mu\text{F}$  of output capacitance that uses standard power limited based start-up. Then there are two examples of designing for the 240 VA design requirement. One uses the CSD16415Q5B, which is an older generation MOFSET with great SOA. The second one uses the CSD17573Q5B, which has lower SOA, but is more cost effective (price vs  $R_{\text{DS(ON)}}$ ).

#### 10.2.1 12 V, 100 A, 5,500 $\mu\text{F}$ Analog Hot Swap Design

The diagram below shows the application schematic for this design example.

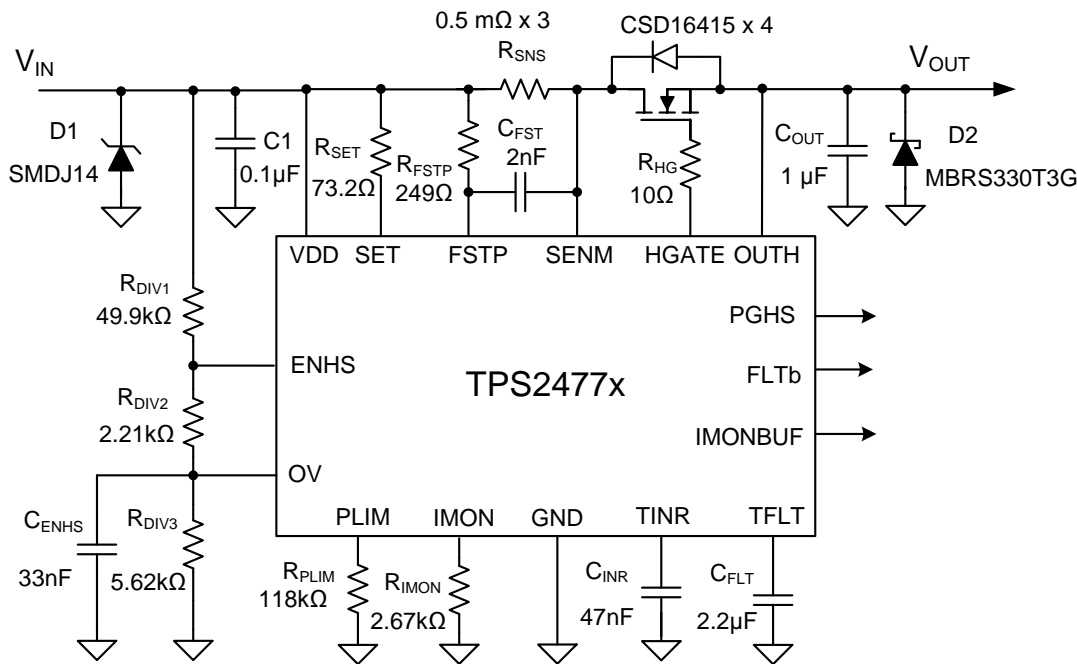


Figure 18. Application Schematic for 100 A Hot Swap

## Typical Application (continued)

### 10.2.2 Design Requirements

Table 1 summarizes the design parameters that must be known before designing a Hot Swap circuit. When charging the output capacitor through the Hot Swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor ( $1/2CV^2$ ). Thus both the input voltage and output capacitance will determine the stress experienced by the MOSFET. The maximum load current will drive the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ( $R_{\theta CA}$ ) will drive the selection of the MOSFET  $R_{DSON}$  and the number of MOSFETs used.  $R_{\theta CA}$  is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Air cooling will also reduce  $R_{\theta CA}$ . It's also important to know if there are any transient load requirements. Finally, whether current monitoring is needed and its accuracy requirement will drive the selection of  $R_{SNS}$ ,  $R_{IMON}$ , and  $R_{SET}$ .

**Table 1. Design Requirements for a 12V, 100A, 5500 $\mu$ F Hot Swap Design**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	11 V – 13 V
Maximum DC load current	100A
Maximum Output Capacitance of the Hot Swap	5500 $\mu$ F
Maximum Ambient Temperature	55°C
MOSFET $R_{\theta CA}$ (function of layout)	50°C/W
Transient load requirement	130A for 250 ms
Pass "Hot-Short" on Output?	Yes
Pass a "Start into short"?	Yes
Is the load off until PG asserted?	Yes
Can a Hot Board be plugged in or Power Cycled?	No
IC used	TPS24772
Analog Current Monitor Used	No

### 10.2.3 Detailed Design Procedure

#### 10.2.3.1 Select $R_{SNS}$ and $V_{SNS,CL}$ Setting

TPS2477x has a programmable  $V_{SNS,CL}$  with a recommended range of 10 mV to 67.5 mV. It can be used with a  $V_{SNS,CL}$  up to 200 mV, but that requires a resistor between SET and SENM to ensure stability of an internal loop. This is shown in Figure 19.  $R_{STBL}$  can be computed using the equation below.

$$R_{STBL} = \frac{R_{IMON} \times R_{SET}}{10 \times R_{SET} - R_{IMON}} \quad (10)$$

For high power applications a lower  $V_{SNS,CL}$  leads to better efficiency so 20 mV is targeted for this design. Targeting a current limit of 110A to allow margin for the load, the sense resistor can be calculated as follows:

$$R_{SNS,CLC} = \frac{V_{SNS,TGT}}{I_{LIM}} = \frac{20 \text{ mV}}{110 \text{ A}} = 0.18 \text{ m}\Omega \quad (11)$$

Since 0.18 m $\Omega$  resistors aren't available, the closest standard resistor should be chosen. To have better efficiency, three 0.5m $\Omega$  resistors are used in parallel. Next the  $V_{SNS,CL}$  should be computed based on the actual  $R_{SNS}$  and then used to compute  $R_{SET}$  and  $R_{IMON}$ .  $R_{SET}$  is chosen to target 250  $\mu$ A of current through SET and IMON pins during current limit.

$$V_{SNS,CL} = I_{LIM} \times R_{SNS} = 110 \text{ A} \times 0.1667 \text{ m}\Omega = 18.37 \text{ mV} \quad (12)$$

$$R_{SET,CLC} = \frac{V_{SNS,CL}}{250 \mu\text{A}} = 73.3 \Omega \quad (13)$$

Chose  $R_{SET}$  to equal 73.2  $\Omega$ , which is the closest available standard resistor. Next obtain the calculated  $R_{IMON}$  ( $R_{IMON,CLC}$ ) as follows:

$$R_{IMON,CLC} = \frac{R_{SET} \times 675 \text{ mV}}{V_{SNS,CL}} = \frac{73.2 \Omega \times 675 \text{ mV}}{18.37 \text{ mV}} = 2.69 \text{ k}\Omega \quad (14)$$

Choose 2.67kΩ resistor for  $R_{IMON}$ , which is the closest available standard resistor. Since accurate current monitoring is not needed a 2512 2 terminal sense resistor can be used.

Finally, compute the actual current limit ( $I_{LIM,CL}$ ) and the analog current monitoring scaling factor  $V_{IMON,GAIN}$  ( $V_{IMON}$  vs  $I_{LOAD}$ )

$$I_{LIM,CL} = \frac{0.675 \text{ V} \times R_{SET}}{R_{IMON} \times R_{SENSE}} = \frac{0.675 \text{ V} \times 73.2 \Omega}{2.67 \text{ k}\Omega \times 0.1667 \text{ m}\Omega} = 111 \text{ A} \quad (15)$$

$$V_{IMON,GAIN} = \frac{R_{IMON} \times R_{SNS}}{R_{SET}} = \frac{0.1667 \text{ m}\Omega \times 2.67 \text{ k}\Omega}{73.2 \Omega} = 6.08 \text{ mV / A} \quad (16)$$

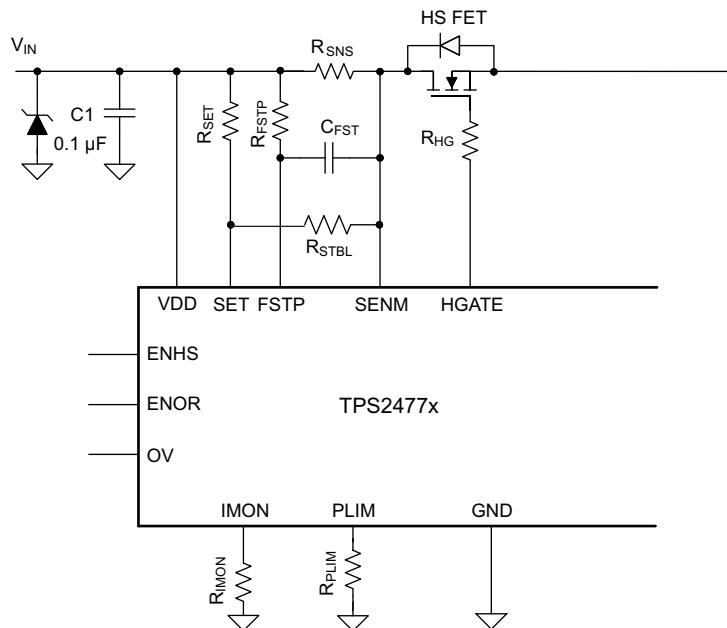


Figure 19. Adding  $R_{STBL}$  for  $V_{SNS,CL} > 67.5\text{mV}$

### 10.2.3.2 Selecting the Fast Trip Threshold and Filtering

The TPS2477x allows the user to program the fast trip threshold. When this threshold is exceeded the gate is quickly pulled down ( $<1\mu\text{s}$ ). In addition  $C_{FSTP}$  can be added to include some filtering into the comparator. The selection of the fast trip threshold and filtering is influenced by the systems environment and requirements. In general, picking a larger threshold and larger filtering time will result in more immunity to nuisance trips, but also a slower response (possibly inadequate) to real fault conditions. It's best to fine tune these threshold after testing the real system. As a starting point it is recommended to set the fast trip threshold at least 1.25x larger than then current limit. For this design example a 150A fast trip threshold along with a 500ns filtering time constant were targeted to ensure that the transient requirement will be passed. The value for  $R_{FSTP}$  and  $C_{FSTP}$  can be computed as shown below:

$$R_{FSTP} = \frac{I_{FSTP} \times R_{SNS}}{100 \mu\text{A}} = \frac{150 \text{ A} \times 0.1667 \text{ m}\Omega}{100 \mu\text{A}} = 250 \Omega \quad (17)$$

$$C_{FSTP} = \frac{t_{FSTP}}{R_{FSTP}} = \frac{500 \text{ ns}}{250 \Omega} = 2 \text{ nF} \quad (18)$$

The next closest standard resistor and capacitor values should be chosen. In this case  $R_{FSTP} = 249\Omega$  and  $C_{FSTP}=2\text{nF}$

### 10.2.3.3 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a Hot Swap design. The device must meet the following requirements:

- The  $V_{DS}$  rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12V systems a 25 V or 30V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- $R_{DS(ON)}$  should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.
- A  $V_{GS}$  rating of +16 V is required, because the TPS2477x can pull up the gate as high as 15.5 V above source.

For this design the CSD16415Q5B was selected for its low  $R_{DS(ON)}$  and superior SOA. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I_{LOAD,MAX}^2 \times \frac{R_{DS(ON)}(T_J)}{n^2} \quad (19)$$

In the equation above n is the number of FETs used in parallel. For this example 4 FETS are used in parallel to prevent over- heating and improve efficiency. Note that the  $R_{DS(ON)}$  is a strong function of junction temperature, which for most MOSFETs will be very close to the case temperature. A few iterations of the above equations may be necessary to converge on the final  $R_{DS(ON)}$  and  $T_{C,MAX}$  value. According to the CSD16415Q5B datasheet, its  $R_{DS(ON)}$  is about 1.3x greater at 100°C compared to room temperature . The equation below uses this  $R_{DS(ON)}$  value to compute the  $T_{C,MAX}$ . Note that the computed  $T_{C,MAX}$  is close to the junction temperature assumed for  $R_{DS(ON)}$ . Thus no further iterations are necessary. For this example an  $R_{\theta CA}$  of 50°C/W was used since there are 4 FETs close together and it's expected that they will heat each other up. It's highly recommended to test the board at full load and double check the thermals with the calculations.

$$T_{C,MAX} = 55^\circ\text{C} + 50^\circ\text{C/W} \times (100\text{A})^2 \times \frac{(1.3 \times 1\text{ m}\Omega)}{4^2} = 95.6^\circ\text{C} \quad (20)$$

### 10.2.3.4 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, at low power limit levels both the  $V_{SNS}$  and  $V_{IMON}$  become very low, which results in more error caused by offsets. It is recommended to keep  $V_{SNS}$  above 1.5mV and  $V_{IMON}$  above 27mV to ensure reasonable accuracy of the power limit engine. Based on these requirements the minimum power limit can be computed as shown below.

$$\begin{aligned} P_{LIM,MIN} &= \frac{V_{IN,MAX}}{R_{SNS}} \times \text{MIN} \left( V_{SNS,MIN}, \frac{V_{IMON,MIN} \times R_{SET}}{R_{IMON}} \right) \\ &= \frac{13\text{ V}}{0.1667\text{ m}\Omega} \times \text{MIN} \left( 1.5\text{ mV}, \frac{27\text{ mV} \times 73.2\ \Omega}{2.67\text{ k}\Omega} \right) = 117\text{ W} \end{aligned} \quad (21)$$

In most applications the power limit can be set to  $P_{LIM,MIN}$  using the equation below. Here  $R_{SNS}$  and  $R_{PWR}$  are in  $\Omega$ s and  $P_{LIM}$  is in Watts.

$$R_{PLIM} = \frac{84375 \times R_{SET}}{R_{SNS} \times R_{IMON} \times P_{LIM}} = \frac{84375 \times 73.2\ \Omega}{0.1.667\text{ m}\Omega \times 2.67\text{ k}\Omega \times 117\text{ W}} = 118.6\text{ k}\Omega \quad (22)$$

The closest available resistor should be selected. In this case it is a 118 k $\Omega$ .

### 10.2.3.5 Set Fault Timer

The inrush timer runs when the Hot Swap is in power limit or current limit, which is the case during start-up. Thus the timer has to be sized large enough to prevent a time-out during start-up. If the part starts directly into current limit ( $I_{LIM} \times V_{DS} < P_{LIM}$ ) the maximum start time can be computed with the equation below:

$$t_{start,max} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM,CL}} \quad (23)$$

For most designs (including this example)  $I_{LIM,CL} \times V_{DS} > P_{LIM}$  so the Hot Swap will start in power limit and transition into current limit. In that case the maximum start time can be computed as follows:

$$t_{start,max} = \frac{C_{OUT}}{2} \times \left[ \frac{V_{IN,MAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM,CL}^2} \right] = \frac{5500 \mu F}{2} \times \left[ \frac{(13 V)^2}{117 W} + \frac{117 W}{(110 A)^2} \right] = 4.0 \text{ ms} \quad (24)$$

Note that the above start-time is based on typical current limit and power limit values. To ensure that the timer never times out during start-up it is recommended to set the fault time ( $T_{INR}$ ) to be  $1.5 \times t_{start,max}$  or 6 ms. This will account for the variation in power limit, timer current, and timer capacitance.

Next the designer should decide if having equal  $T_{INR}$  and  $T_{FLT}$  is acceptable. Note that to pass the load transient the fault timer needs to be longer than 200 ms. If the inrush time is this long, it will place too much stress on the MOSFET during a start into short. For this reason, it's ideal to have two separate timers. To ensure proper start up and to pass the load transient a target inrush time ( $T_{INR,TGT}$ ) of 6 ms and a target fault time ( $T_{FLT,TGT}$ ) of 250ms is used.  $C_{INR,CLC}$  and  $C_{FLT,CLC}$  is computed as follows:

$$C_{INR,CLC} = 7.59 \mu F / s \times T_{INR,TGT} = 7.59 \mu F / s \times 6 \text{ ms} = 45.6 \text{ nF} \quad (25)$$

$$C_{FLT,CLC} = 7.59 \mu F / s \times T_{FLT,TGT} = 7.59 \mu F / s \times 250 \text{ ms} = 1898 \text{ nF} \quad (26)$$

The next largest available  $C_{INR}$  is chosen as 47 nF and the next largest available  $C_{FLT}$  is chosen as 2.2 $\mu$ F

Next, the actual  $T_{INR}$  and  $T_{FLT}$  can be computed as shown below: Once the  $C_{TMR}$  is chosen the actual programmed time out can be computed as follows.

$$T_{TMR} = \frac{C_{INR}}{7.59 \mu F / s} = \frac{47 \text{ nF}}{7.59 \mu F / s} = 6.2 \text{ ms} \quad (27)$$

$$T_{FLT} = \frac{C_{FLT}}{7.59 \mu F / s} = \frac{2.2 \mu F}{7.59 \mu F / s} = 290 \text{ ms} \quad (28)$$

### 10.2.3.6 Check MOSFET SOA

Once the power limit and fault timer are chosen, it's critical to check that the FET will stay within its SOA during all test conditions. For this design example the TPS24772 is used, which does not retry during a hot-short. Thus the worst condition is a start-up into a short circuit. In this case the TPS24772 will start into a power limit and regulate at that point for 6.2 ms ( $T_{INR}$ ). Based on the SOA of the CSD16415Q5B, it can handle 13 V, 15 A for 10 ms and it can handle 13 V, 100 A for 1 ms. The SOA for 6.2 ms can be extrapolated by approximating SOA vs time as a power function as shown below:

$$I_{SOA}(t) = a \times t^m$$

$$m = \frac{\ln(I_{SOA}(t_1) / I_{SOA}(t_2))}{\ln(t_1 / t_2)} = \frac{\ln\left(\frac{100 \text{ A}}{15 \text{ A}}\right)}{\ln\left(\frac{1 \text{ ms}}{10 \text{ ms}}\right)} = -0.82$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{100 \text{ A}}{(1 \text{ ms})^{-0.82}} = 100 \text{ A} \times (\text{ms})^{0.82}$$

$$I_{SOA}(6.2 \text{ ms}) = 100 \text{ A} \times (\text{ms})^{0.82} \times (6.2 \text{ ms})^{-0.82} = 22.4 \text{ A} \quad (29)$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be hotter during a start into a short. It is important to understand the hottest temperature that a MOSFET can be during a start-up ( $T_{C, MAX, START}$ ). If a board has been off for a while and then it's turned on  $T_{A, MAX}$  is a good estimate for  $T_{C, MAX, START}$ . However, if a board is on and then gets power cycled or a hot board is unplugged and plugged back in  $T_{C, MAX}$  should be used for  $T_{C, MAX, START}$ . This will depend on system requirements. For this design example it's assumed that the board can only be plugged in cold and  $T_{A, MAX}$  is used to estimate  $T_{C, MAX, START}$ .

$$I_{SOA} (6.2 \text{ ms}, T_{C, MAX, START}) = I_{SOA} (6.2 \text{ ms}, 25^\circ\text{C}) \times \frac{T_{J, ABSMAX} - T_{A, MAX}}{T_{J, ABSMAX} - 25^\circ\text{C}} = 22.4 \text{ A} \times \frac{150^\circ\text{C} - 55^\circ\text{C}}{150^\circ\text{C} - 25^\circ\text{C}} = 17 \text{ A} \quad (30)$$

Based on this calculation the MOSFET can handle 17 A, 13 V for 6.2 ms at 55°C elevated case temperature, but is only required to handle 9A during a start into short. Thus there is good margin and this will be a robust design. In general, it is recommended that the MOSFET can handle 1.3x more than what is required during a hot-short. This provides margin to cover the variance of the power limit and fault time.

### 10.2.3.7 Choose Under Voltage and Over Voltage Settings

The TPS2477x has comparators with 1.35V threshold on the ENHS, ENOR, and OV pins. A resistor divider can be used to set Undervoltage and Overvoltage thresholds for the bus. For this design example 10V and 14V were chosen as the limits to allow some margin for the 11V to 13V input bus. Once these limits are known,  $R_{DIV2}$  and  $R_{DIV3}$  can be computed using the equations below.  $R_{DIV1}$  was set to 49.9 kΩ, which keeps the power consumption reasonable low without being too susceptible to leakage currents.

$$R_{DIV2,3} = R_{DIV2} + R_{DIV3} = \frac{R_{DIV1} \times 1.35 \text{ V}}{V_{UV} - 1.35 \text{ V}} = \frac{49.9 \text{ k}\Omega \times 1.35 \text{ V}}{10 \text{ V} - 1.35 \text{ V}} = 7.79 \text{ k}\Omega \quad (31)$$

$$R_{DIV3} = \frac{(R_{DIV1} + R_{DIV2,3}) \times 1.35 \text{ V}}{V_{OV}} = \frac{(49.9 \text{ k}\Omega + 7.79 \text{ k}\Omega) \times 1.35 \text{ V}}{14 \text{ V}} = 5.56 \text{ k}\Omega \quad (32)$$

$$R_{DIV2} = R_{DIV2,3} - R_{DIV1} = 7.79 \text{ k}\Omega - 5.56 \text{ k}\Omega = 2.23 \text{ k}\Omega \quad (33)$$

Choose closest available resistors standard 1% resistors:  $R_{DIV2} = 2.21 \text{ k}\Omega$  and  $R_{DIV3} = 5.62 \text{ k}\Omega$ . The actual Under Voltage and Over Voltage settings can be computed for the chosen resistors as follows:

$$V_{UV\_act} = 1.35 \text{ V} \times \frac{R_{DIV1} + R_{DIV2} + R_{DIV3}}{R_{DIV2} + R_{DIV3}} = 1.35 \text{ V} \times \frac{2.21 \text{ k}\Omega + 5.62 \text{ k}\Omega + 49.9 \text{ k}\Omega}{2.21 \text{ k}\Omega + 5.62 \text{ k}\Omega} = 9.95 \text{ V} \quad (34)$$

$$V_{OV\_act} = 1.35 \text{ V} \times \frac{R_{DIV1} + R_{DIV2} + R_{DIV3}}{R_{DIV3}} = 1.35 \text{ V} \times \frac{2.21 \text{ k}\Omega + 5.62 \text{ k}\Omega + 49.9 \text{ k}\Omega}{5.62 \text{ k}\Omega} = 13.87 \text{ V} \quad (35)$$

### 10.2.3.8 Selecting $C_1$ and $C_{OUT}$

It is recommended to add ceramic bypass capacitors to help stabilize the voltages on the input and output. Since  $C_{IN}$  will be charged directly on hot-plug, its value should be kept small. 0.1μF is a good target. Since  $C_{OUT}$  doesn't get charged during hot-plug, a larger value such as 1 μF could be used.

### 10.2.3.9 Adding $C_{ENHS}$

When the ENHS pin is pulled below its threshold and raised back up the IC will reset. Note that during a hot short the input voltage can easily droop below the UV threshold and cycle the ENHS pin. For the TPS24770 and TPS24771 ICs this will not change the behavior. However, when using the TPS24772 the cycling of the ENHS will result in the IC attempting to restart, which is undesired (this is the main reason why someone would use the TPS24772). To avoid this behavior a capacitor should be added to the ENHS to provide filtering. 33 nF was chosen for this example.

### 10.2.3.10 Selecting D1 and D2

During hot plug and hot short events there could be significant transients on the input and output of the Hot Swap that could cause operation outside of the IC specifications. To ensure reliable operation a TVS on the input and a Schottky diode on the output are recommended. In this example a SMDJ14A and MBR330T3G are used.

### 10.2.3.11 Checking Stability

For most applications, the TPS2477x is stable without any additional components. However in some cases additional  $C_{GS,EXT}$  is required as shown in the following figure to help stabilize the current and power limit loop. Typically this is for low current limits and low sense voltages. It is easy to check whether these extra components are needed using the equations below. Note that the transconductance (also referred to as  $g_m$  and  $g_{fs}$ ) of the FET will vary based on the current and thus  $g_m'$  is used in the equations as a normalizing parameter. The CSD16415Q5B has a  $g_m$  of 168 siemens at 40A of  $I_{DS}$ , resulting in  $g_m'$  of 26.56. For this example,  $C_{GS,MIN}$  (per FET) was computed to be 0.25nF, while the  $C_{ISS}$  of the CSD16415Q5B is 3.15nF providing plenty of margin for the design. In general it is recommended to have a 2x margin from the typical  $C_{ISS}$  and  $C_{GS,MIN}$  to account for any variation that the FET would have. If the  $C_{ISS}$  of the MOSFET isn't large enough an external RC should be added as shown in the figure below.

$$C_{GS,MIN} = 6.54 \times 10^{-12} \times g_m' \times \left( \frac{R_{IMON}}{R_{SET}} \right)^{1.5} \times \frac{\sqrt{R_{SNS}}}{\sqrt{n}} \quad (36)$$

$$g_m' = \frac{g_m(I_{DS})}{\sqrt{I_{DS}}} = \frac{168}{\sqrt{40}} = 26.56 \quad (37)$$

$$C_{GS,MIN} = 6.54 \times 10^{-12} \times 26.56 \times \left( \frac{2.67k}{73.2} \right)^{1.5} \times \frac{\sqrt{0.1667m}}{\sqrt{4}} = 0.25nF \quad (38)$$

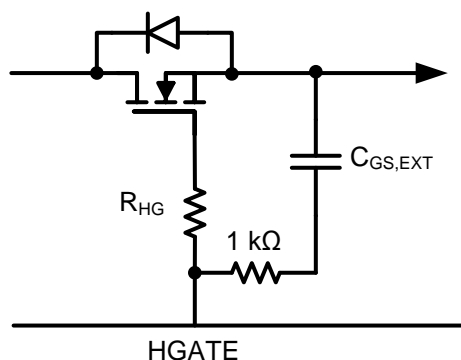


Figure 20. Adding  $C_{GS,EXT}$  to Ensure Stability

### 10.2.3.12 Compute Tolerances

After finishing a design it is often desired to know the variations of each setting. Often times there are multiple error sources and there are two common ways to analyze the circuit. One is worst case, which adds all of the error sources and the other one is root sum square (RSS), which is less conservative. When error sources are independent, using the RSS method provides a more statistically accurate view of the tolerances. This method is used in this section. Note that the error calculations are quite long and tedious and it's recommended to use TI's excel tools, which support both worst case and RSS analysis. For this example the below tolerances are assumed. The following table lists the assumptions for the component tolerances. Note that the sense resistor itself is 1% accurate, but multiple two terminal 2512 resistors are used so additional error is introduced from solder resistance and layout limitations of paralleling resistors. For this example 3% is assumed as the total error of the sensing network.

**Table 2. Component Tolerances**

COMPONENTS	TOLERANCE
R <sub>IMON</sub> and R <sub>SET</sub>	1%
R <sub>SNS</sub> (Including Layout + Soldering)	3%
R <sub>DIV1</sub> , R <sub>DIV2</sub> , R <sub>DIV3</sub> , R <sub>PLIM</sub> , R <sub>FST</sub>	1%
C <sub>INR</sub> , C <sub>FLT</sub>	10%

First, the tolerance of the current monitoring and current limit is computed.

There are 5 error sourcing contributing to the current monitoring accuracy on the IMON pin: tolerance of R<sub>SET</sub> (ER<sub>SET</sub>), tolerance of R<sub>IMON</sub> (ER<sub>IMON</sub>), tolerance of R<sub>SNS</sub> (ER<sub>SNS</sub>), the IC gain error (ER<sub>GAIN</sub>), and the IC offset error (ER<sub>OS</sub>). All of these errors are in % with the exception of the offset error. To get a percent error due to the offset error (ER<sub>OS%</sub>) simply divide the offset by the sense voltage. For the TPS2477x, ER<sub>GAIN</sub> is 0.4%, and ER<sub>OS</sub> is 150 μV.

Based on these values the full scale (I<sub>FS,ERR,IMON</sub>) current monitoring accuracy at the Imon pin can be computed with the following equations.

$$I_{FS,ERR,IMON} = \sqrt{(ER_{SET})^2 + (ER_{SNS})^2 + (ER_{IMON})^2 + (ER_{GAIN})^2 + \left(\frac{ER_{OS}}{R_{SNS} \times I_{LIM}}\right)^2}$$

$$= \sqrt{1\%^2 + 3\%^2 + 1\%^2 + 0.4\%^2 + (150 \mu V / 18.34 mV)^2} = 3.4\% \quad (39)$$

Note that the TPS2477x detects the current limit when the IMON pin exceeds 675 mV. Thus the current limit error I<sub>LIM,ERR</sub> is a combination of the I<sub>FS,ERR,IMON</sub> and the current limit error at the I<sub>MON</sub> pin (I<sub>LIM,ERR,IMON</sub>). The 675 mV threshold varies up to 15 mV so I<sub>LIM,ERR,IMON</sub> is 2.3% and the current limit error can be computed as follows:

$$I_{LIM,ERR} = \sqrt{(I_{FS,ERR,IMON})^2 + (I_{LIM,ERR,IMON})^2} = \sqrt{3.4\%^2 + 2.3\%^2} = 4.1\% \quad (40)$$

Next the power limit error is computed. This error is made up of three sources: the error from external components (ER<sub>COMP</sub>), the error when translating the sense voltage to IMON (I<sub>PL,ERR,IMON</sub>), and the error of the power limit engine at IMON (ER<sub>IMON,PL</sub>). Both ER<sub>SNS</sub> and ER<sub>IMON,PL</sub> are a function of the operating point of the power limit engine. Note that this error is greatest at largest V<sub>DS</sub>, since V<sub>SNS,PL</sub> is smallest (refer to Figure 12). For this example V<sub>DS</sub> is largest when V<sub>IN</sub> = 13 V (maximum V<sub>IN</sub>) and V<sub>OUT</sub> = 0 V and the error is computed at this operating point. The sense voltage (V<sub>SNS</sub>) and the voltage at the IMON pin (V<sub>IMON</sub>) should be computed for this operating point using the equations below:

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} = \frac{117 W \times 0.1667 m\Omega}{13 V} = 1.5 mV \quad (41)$$

$$V_{IMON} = \frac{V_{SNS} \times R_{IMON}}{R_{SET}} = \frac{1.5 mV \times 2670 \Omega}{73.2 \Omega} = 54.7 mV \quad (42)$$

The I<sub>PL,ERR,IMON</sub> can be computed similarly to I<sub>FS,ERR,IMON</sub> using the equation below.

$$I_{PL,ERR,IMON} = \sqrt{(ER_{GAIN})^2 + \left(\frac{ER_{OS}}{V_{SNS}}\right)^2} = \sqrt{(0.4\%)^2 + \left(\frac{150 \mu V}{1.5 mV}\right)^2} = 10\% \quad (43)$$

The tolerance of the power limit engine is specified at three V<sub>IMON</sub> points in the datasheet: 135 mV (±20.3 mV), 67.5 mV (±10.1 mV), and 27 mV (±8.1 mV). To get the % error at the real operating point, the absolute error should be extrapolated and divided by V<sub>IMON</sub> as shown in the equation below. This is graphically depicted in Figure 23.

$$ERR_{IMON,PL} = \frac{8.1 mV + (54.7 mV - 27 mV) \times \frac{10.1 mV - 8.1 mV}{67.5 mV - 27 mV}}{54.7 mV} = 17.3\% \quad (44)$$



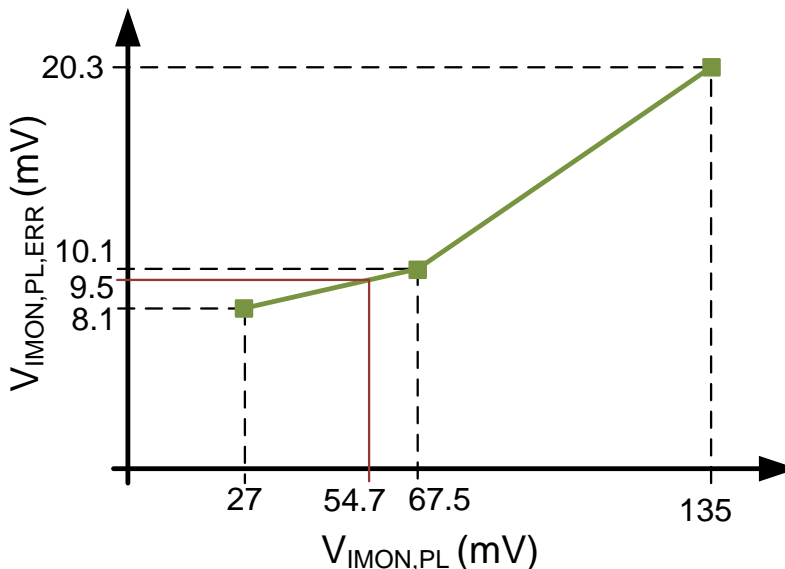


Figure 21. Extrapolating Power Limit Error

Once  $ER_{IMON,PL}$  and  $I_{PL,ERR,IMON}$  are known the total power limit error ( $PL_{ERR,TOT}$ ) can be computed using the equation below. The component error (3.5%) comes from  $R_{SNS}$  (3%),  $R_{PLIM}$  (1%),  $R_{SET}$  (1%), and  $R_{IMON}$  (1%).

$$PL_{ERR,TOT} = \sqrt{(ERR_{IMON,PL})^2 + (I_{PL,ERR,IMON})^2 + (ERR_{COMP})^2}$$

$$= \sqrt{(17.3\%)^2 + (10\%)^2 + (3.5\%)^2} = 20.3\% \quad (45)$$

After computing the fast trip voltage threshold to be 24.9 mV ( $100 \mu A \times 249 \Omega$ ), the fast trip threshold error resulting from the IC ( $FST_{ERR,IC}$ ) can be computed using a similar extrapolation method as used for power limit. The component error of  $R_{SNS}$  and  $R_{FST}$  should be added to obtain the total fast trip error ( $FST_{ERR,TOT}$ ). Both equations are shown below.

$$FST_{ERR,IC} = \frac{2 \text{ mV} + (24.9 \text{ mV} - 20 \text{ mV}) \times \frac{5 \text{ mV} - 2 \text{ mV}}{100 \text{ mV} - 20 \text{ mV}}}{24.9 \text{ mV}} = 8.8\% \quad (46)$$

$$FST_{ERR,TOT} = \sqrt{(8.8\%)^2 + (1\%)^2 + (3\%)^2} = 9.4\% \quad (47)$$

The IC error of the UV / OV threshold is always 3.7% ( $0.05 \text{ V} / 1.35 \text{ V}$ ). Assuming that all resistors have a 1% error the component error is 1.41% (2 resistors). When using the RSS method the total error is 4%. For the timer error, the IC contributes 22% and 10% comes from the component. When using the RSS method the total error becomes 24.2%.

The table below summarizes the final tolerances of the design:

Table 3. Design Tolerances

SETTINGS	ACCURACY
Current Limit	4.1%
Fast Trip	9.4%
Power Limit	20.3%
TFLT, TINR	24.2%
UV/OV	4.0%

## 10.2.4 Application Curves

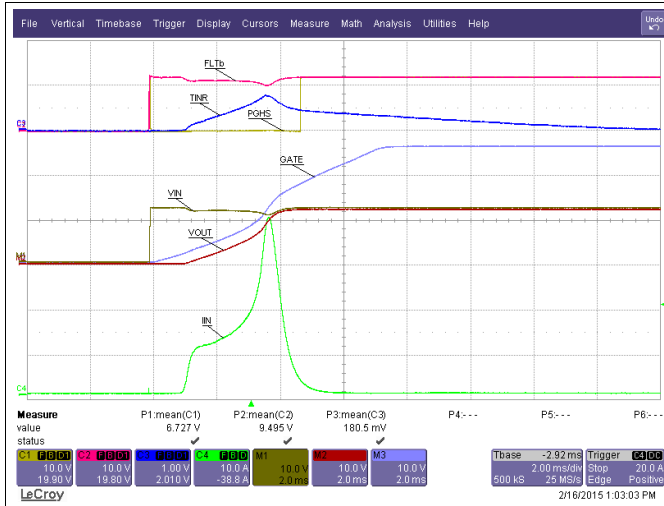


Figure 22. Start up ( $C_{OUT}=5500\mu F$ )

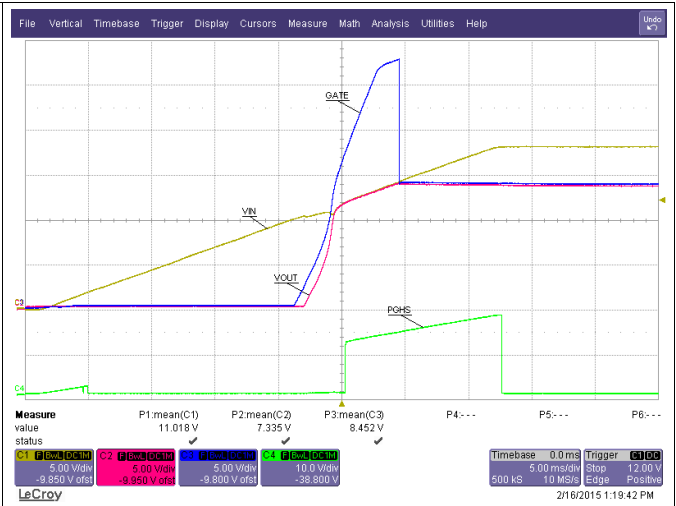


Figure 23. Undervoltage and Overvoltage

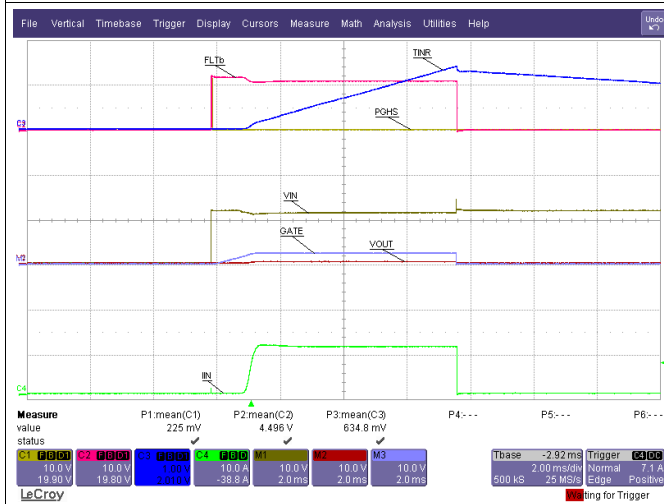


Figure 24. Start Up with Output Shorted to GND

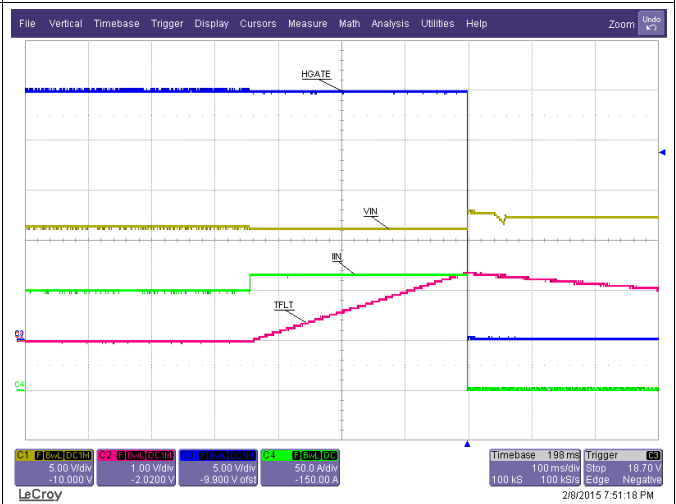


Figure 25. Load Step 100A to 120A

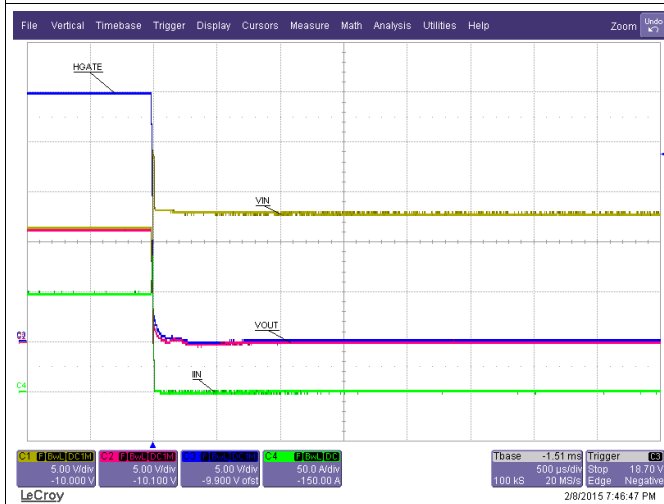


Figure 26. Hot Short on Output with Full Load (zoomed out)

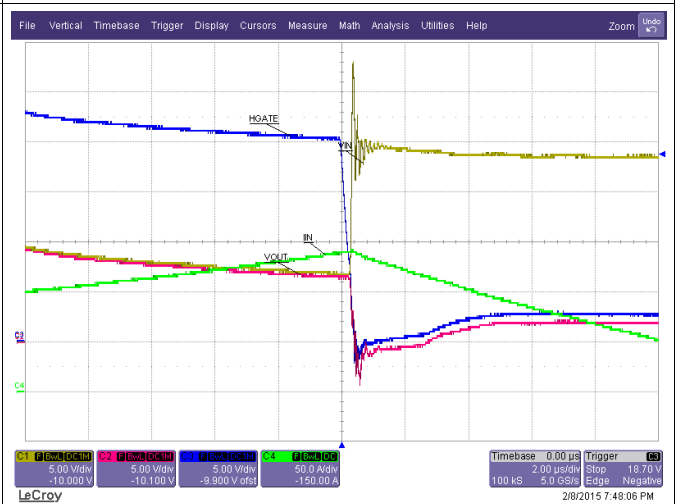


Figure 27. Hot Short on Output with Full Load (zoomed in)

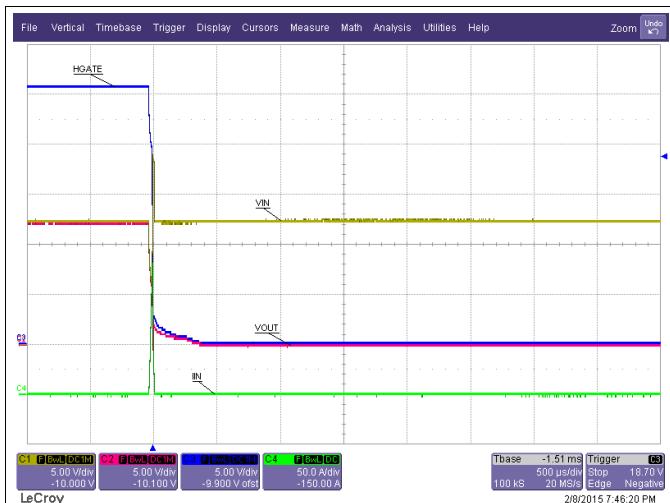


Figure 28. Hot Short on Output with No Load (zoomed out)

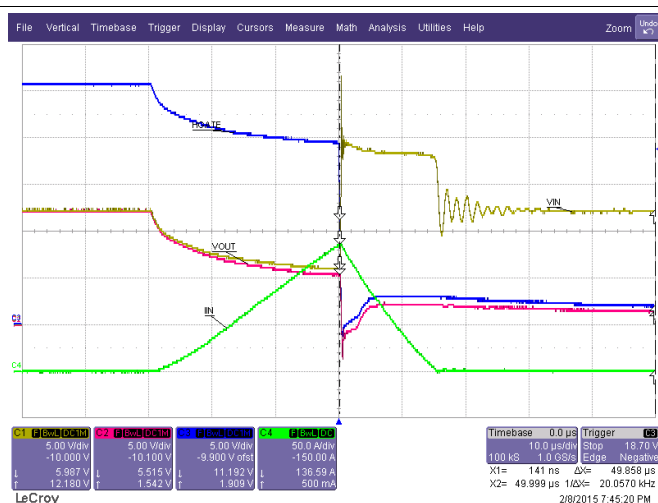


Figure 29. Hot Short on Output with No Load (zoomed in)

### 10.2.5 240 VA Application Using CSD16415Q5B

The diagram below shows the application schematic for this design example. See the [TPS24770 Design Calculator](#) to help with these calculations.

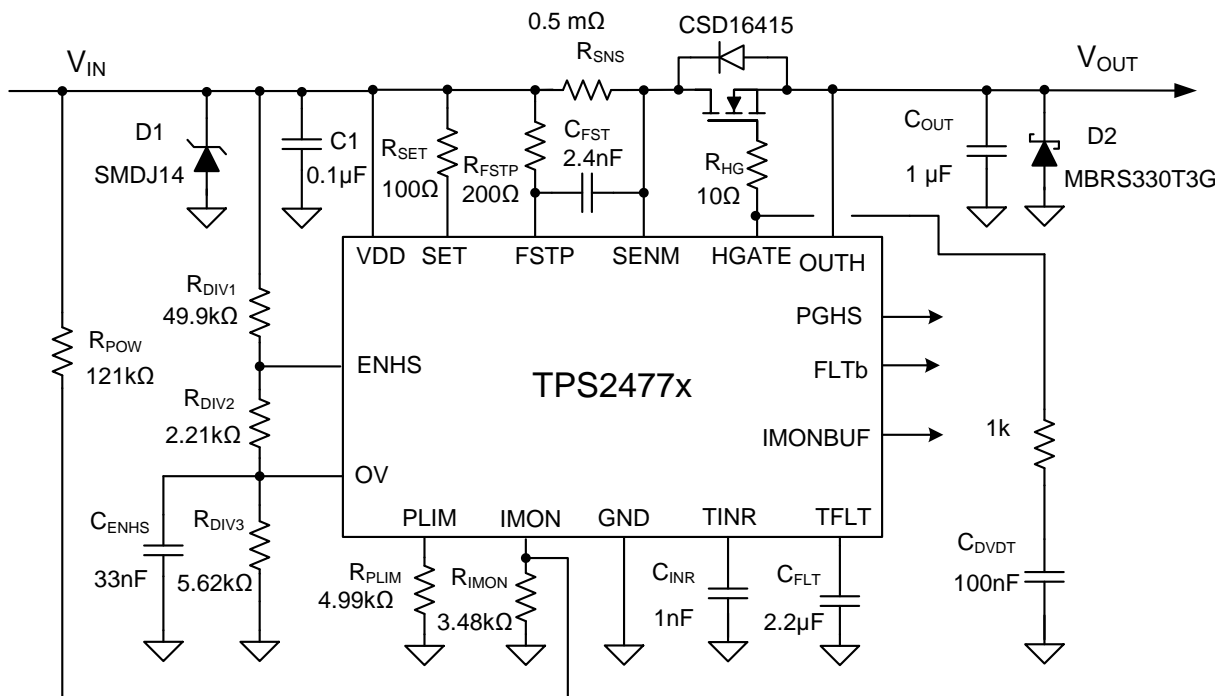


Figure 30. Application Schematic for 240VA Design with CSD16415Q5B

#### 10.2.5.1 Design Requirements

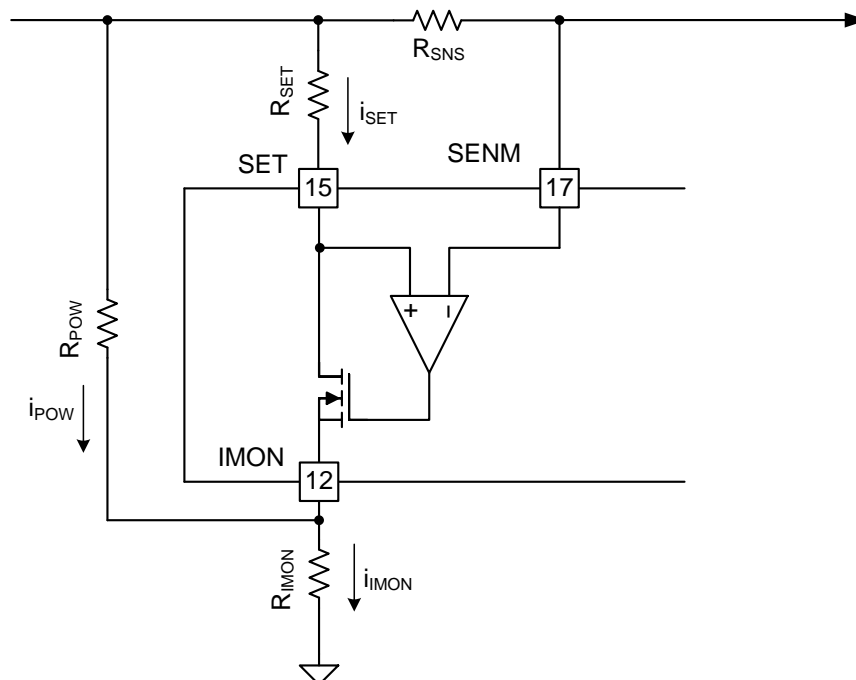
The following table summarizes the requirements for this design. Note that the output power cannot exceed 240W for more than 250 ms.

**Table 4. Design Requirements for a 240 VA Design using CSD16415Q5B**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10.8 V – 13.2V
Output Power Limit (VA limiting)	240 W
Maximum Output Capacitance of the Hot Swap	2500 uF
Maximum Ambient Temperature	55°C
MOSFET $R_{\theta CA}$ (function of layout)	35°C/W
Transient load requirement?	POUT is allowed to surpass 240W for <250 ms
Pass “Hot-Short” on Output?	Yes
Pass a “Start into short”?	Yes
Is the load off until PG asserted?	Yes
IC used	TPS24772
Analog Current Monitor Used	No
MOSFET	CSD16415Q5B
Can a Hot Board be plugged in or Power Cycled?	Yes

### 10.2.5.2 Theory of Operations

Before going into the details of the design it’s important to understand the impact that  $R_{POW}$  has on the circuit. Refer to [Figure 31](#) for this discussion.



**Figure 31. Impact of  $R_{POW}$  Resistor**

Note that the TPS2477x detects overcurrent conditions when  $V_{IMON}$  reaches 675mV, which occurs when there is sufficient current ( $i_{IMON}$ ) flowing through  $R_{IMON}$ . Also note that  $i_{IMON}$  is a sum of  $i_{SET}$  and  $i_{POW}$ . If  $i_{IMON,CL}$ ,  $i_{SET,CL}$ , and  $i_{POW,CL}$  correspond to these same current when  $V_{IMON}$  reaches 675mV and TPS2477x detects current limit, the following equations can be written.

$$i_{IMON,CL} = \frac{675 \text{ mV}}{R_{IMON}}; i_{IMON,CL} = i_{SET,CL} + i_{POW,CL} \quad (48)$$

$$i_{SET,CL} = \frac{675 \text{ mV}}{R_{IMON}} - \frac{V_{IN} - 675 \text{ mV}}{R_{POW}} \quad (49)$$

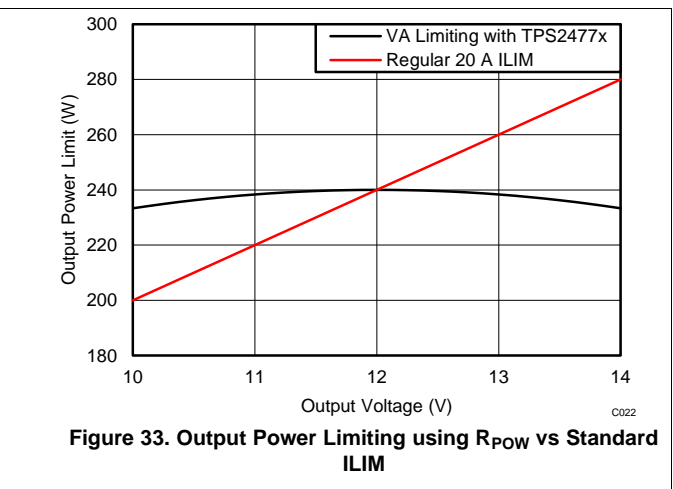
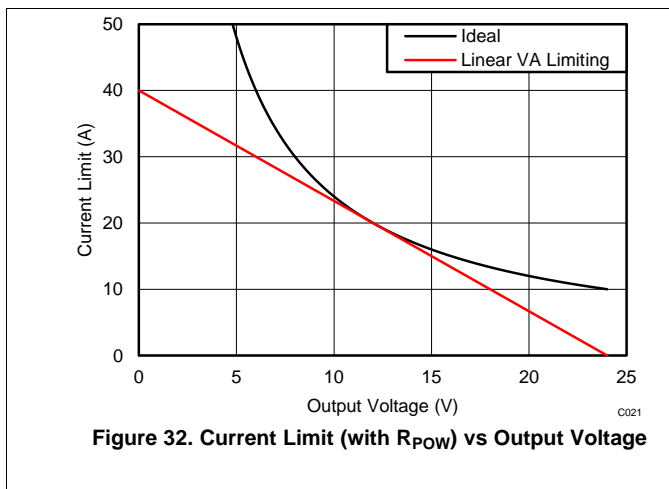
Also note that the amplifier ensures that SET and SENM are equal and thus  $I_{LIM}$  can be derived as follows:

$$i_{IMON,CL} = \frac{675 \text{ mV}}{R_{IMON}}; i_{IMON,CL} = i_{SET,CL} + i_{POW,CL} \quad (50)$$

$$I_{LIM} = i_{SET,CL} \times \frac{R_{SET}}{R_{SNS}} = \frac{R_{SET}}{R_{SNS}} \times \left( \frac{675 \text{ mV}}{R_{IMON}} + \frac{675 \text{ mV}}{R_{POW}} \right) - \frac{V_{IN} \times R_{SET}}{R_{SNS} \times R_{POW}} \quad (51)$$

Examining the equation above, it can be seen that  $I_{LIM}$  reduces as  $V_{IN}$  becomes larger. Note that the ultimate goal is to limit output power. However, when the FET is on,  $V_{IN}$  is very close to  $V_{OUT}$  and they can be assumed to be equal.

The figure below compares the ideal  $I_{LIM}$  vs  $V_{OUT}$  ( $I_{LIM} = 240 \text{ W} / V_{OUT}$ ) profile to that of the  $R_{POW}$  implementation shown here. The error is large when the output voltage is far from 12V, but the performance is quite good near 12V. The next figure shows the effective output power limit for output voltages from 10 V to 14 V. It can be seen that the results are quite good and much better than using a simple 20A current limit, without the  $R_{POW}$  resistor to compensate for  $V_{IN}$  variation.



### 10.2.5.3 Design Procedure

#### 10.2.5.3.1 Select $V_{SNS,CL}$ , $R_{SNS}$ , and $R_{SET}$ Setting

For this example,  $V_{SNS,CL}$  of 10 mV was selected to optimize efficiency. Then  $R_{SNS}$  can be computed to 0.5m $\Omega$ . There is some flexibility in picking the  $R_{SET}$  value. In this case targeting 100  $\mu$ A for  $i_{SET,CL}$ ,  $R_{SET}$  is computed to be 100  $\Omega$  as shown in the following equation.

$$R_{SET} = \frac{V_{SNS,CL}}{i_{SET,CL}} = \frac{10 \text{ mV}}{100 \mu\text{A}} = 100 \Omega \quad (52)$$

#### 10.2.5.3.1.1 Select $R_{POW}$ and $R_{IMON}$

$R_{POW}$  controls the slope of the  $I_{LIM}$  vs  $V_{IN}$  curve and thus the ideal slope should be found first before selecting  $R_{POW}$ . This can be done by taking the derivative of the ideal current limit ( $I_{LIM, IDEAL}$ ) vs  $V_{IN}$  curve and evaluating it at 12V. This is found to be -1.667 A/V as shown in the equations below. Next the derivative of equation 51 is taken to isolate the terms that influence the slope of  $I_{LIM}$  vs  $V_{IN}$  curve. Since  $R_{SET}$  and  $R_{SNS}$  have already been selected,  $R_{POW}$  remains the only parameter that can be varied. Thus,  $R_{POW}$  is computed using the last equation below.

$$\frac{dI_{LIM,IDEAL}}{dV_{IN}} (V_{IN} = 12 \text{ V}) = \frac{-240 \text{ W}}{(12 \text{ V})^2} = -1.667 \text{ A/V} \quad (53)$$

$$\frac{dI_{LIM}}{dV_{IN}} = \frac{-R_{SET}}{R_{SNS} \times R_{POW}} \quad (54)$$

$$R_{POW,CLC} = \frac{\frac{-R_{SET}}{R_{SNS}}}{\frac{dI_{LIM,IDEAL}}{dV_{IN}} (V_{IN} = 12\text{ V})} = \frac{\frac{-100\ \Omega}{0.5\text{m}\ \Omega}}{-1.667\ \frac{A}{V}} = 120\ \text{k}\Omega \quad (55)$$

The closest available standard resistor is chosen for  $R_{POW}$ , which is 121k $\Omega$ .

Next  $R_{IMON}$  should be chosen to ensure that the output power limit is 240 W at 12 V, which is the typical operating point.  $R_{IMON}$  is computed to be 3.49k $\Omega$  and the closest available standard resistor of 3.48 k $\Omega$  is chosen.

$$I_{IMON,CL} = I_{SET,CL} + I_{POW,CL} = 100\ \mu\text{A} + \frac{12\ \text{V} - 0.675\ \text{V}}{121\ \text{k}\Omega} = 193.6\ \mu\text{A} \quad (56)$$

$$R_{IMON} = \frac{V_{IMON,CL}}{I_{IMON,CL}} = \frac{675\ \text{mV}}{193.6\ \mu\text{A}} = 3.49\ \text{k}\Omega \quad (57)$$

#### 10.2.5.3.1.2 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a Hot Swap design. The device must meet the following requirements:

- The  $V_{DS}$  rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12V systems a 25 V or 30V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- $R_{DS(ON)}$  should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.
- A  $V_{GS}$  rating of +16 V is required, because the TPS2477x can pull up the gate as high as 15.5 V above source.

For this design the CSD16415Q5B was selected for its low  $R_{DS(ON)}$  and superior SOA. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I_{LOAD,MAX}^2 \times \frac{R_{DS(ON)}(T_J)}{n^2} \quad (58)$$

In the equation above  $n$  is the number of FETs used in parallel. Note that the  $R_{DS(ON)}$  is a strong function of junction temperature, which for most MOSFETs will be very close to the case temperature. A few iterations of the above equations may be necessary to converge on the final  $R_{DS(ON)}$  and  $T_{C,MAX}$  value. According to the CSD16415Q5B datasheet, its  $R_{DS(ON)}$  is about 1.2 x greater at 75°C compared to room temperature. The equation below uses this  $R_{DS(ON)}$  value to compute the  $T_{C,MAX}$ . Note that the computed  $T_{C,MAX}$  is close to the junction temperature assumed for  $R_{DS(ON)}$ . Thus no further iterations are necessary.

$$T_{C,MAX} = 55^\circ\text{C} + 35^\circ\frac{\text{C}}{\text{W}} \times (20\text{A})^2 \times (1.2 \times 1\ \text{m}\Omega) = 72^\circ\text{C} \quad (59)$$

#### 10.2.5.3.1.3 Keeping MOSFET within SOA During Normal Start-up

Next, the designer must ensure that the MOSFET will stay within SOA during start-up and a start-up into short. Note that the TPS24772 (fast latch off) is used for this design so the MOSFET stress during a hot short is minimal.

Since  $R_{POW}$  biases the  $I_{MON}$  pin, it interferes with FET power limiting and it's recommended to disable FET power limiting it by selecting a 4.99k $\Omega$  resistor for  $R_{POW}$ .

The inrush current can be limited by adding a capacitor from HGATE to GND ( $C_{DVDT}$ ) as shown in the application diagram. This capacitor limits the slew rate of HGATE at start-up, which will in turn limit the slew rate of  $V_{OUT}$ . Assuming that the load is off until PGHS is asserted, all of the inrush current would be going into  $C_{OUT}$  and be inversely proportional to the slew rate of  $V_{OUT}$ . Refer to the application plots for a start-up waveform. In addition, a 1k $\Omega$  resistor is placed in series with  $C_{DVDT}$  to ensure that  $C_{DVDT}$  doesn't slow down the short circuit response of the Hot Swap.

For this example, a 100 nF capacitor was used for  $C_{DVDT}$ . This results in an inrush current ( $I_{INR}$ ) of 1.375A, total inrush time ( $t_{INR}$ ) of 24.5, and peak FET power dissipation ( $P_{FET,PEAK}$ ) of 18.7W as shown in equations below. This assumes maximum input voltage of 13.2 V

$$I_{INR} = \frac{I_{HGATE} \times C_{OUT}}{C_{DVDT}} = \frac{55 \mu A \times 2500 \mu F}{100 \text{ nF}} = 1.375 \text{ A} \quad (60)$$

$$t_{INR} = \frac{V_{IN,MAX} \times C_{DVDT}}{I_{HGATE}} = \frac{13.2 \text{ V} \times 100 \text{ nF}}{55 \mu A} = 24.5 \text{ ms} \quad (61)$$

$$P_{INR,MAX} = V_{IN,MAX} \times I_{INR} = 13.2 \text{ V} \times 1.375 \text{ A} = 18.2 \text{ W} \quad (62)$$

Next, it's important to check that the MOSFET can handle this stress level. Note that the power dissipation of the MOSFET will start at  $P_{INR,MAX}$  and will reduce to zero as the  $V_{DS}$  drop across the MOSFET reduces. The effective stress on the MOSFET can be approximated to be  $P_{INR,MAX}$  for  $t_{INR}/2$ , which is the equivalent amount of energy. For this example, the FET stress is 18.7W for 12.3 ms. Looking at the SOA curve of the CSD16415Q5B, at  $V_{DS}$  of 13.2 V it can handle ~15A for 10ms or ~4A for 100ms. Using the same method as the previous design example, it can be computed that the MOSFET can handle 13.4A for 12.3 ms when  $V_{DS}=13.2$  V.

The SOA of a MOSFET is specified at a case temperature of 25°C, while the real case temperature can be hotter during a start into a short. It is important to understand the hottest temperature that a MOSFET can be during a start-up ( $T_{C,MAX,START}$ ). If a board has been off for a while and then it's turned on,  $T_{A,MAX}$  is a good estimate for  $T_{C,MAX,START}$ . However, if a board is on and then gets power cycled or gets unplugged and plugged back in,  $T_{C,MAX}$  should be used for  $T_{C,MAX,START}$ . This will depend on system requirements. For this design example, it is assumed that a hot board can be power cycled or hot plugged and thus  $T_{C,MAX}$  is used to estimate  $T_{C,MAX,START}$ .

$$\begin{aligned} I_{SOA}(12.3 \text{ ms}, T_{C,MAX,START}) &= I_{SOA}(12.3 \text{ ms}, 25^\circ\text{C}) \times \frac{T_{J,ABS,MAX} - T_{C,MAX,START}}{T_{J,ABS,MAX} - 25^\circ\text{C}} \\ &= 13.4 \text{ A} \times \frac{150^\circ\text{C} - 72^\circ\text{C}}{150^\circ\text{C} - 25^\circ\text{C}} = 8.4 \text{ A} \end{aligned} \quad (63)$$

Based on this calculation the MOSFET can handle 8.4 A, 13.2 V for 12.3 ms at 72°C elevated case temperature, but is only required to handle 1.375 A. Thus there is good margin and this will be a robust design. In general a 1.3x margin is recommended to cover for variations.

Next, the start into short case is considered. Since the MOSFET power limit is disabled, the current through the MOSFET will reach 20A before the part starts to regulate and runs the inrush timer. In order to minimize FET stress, a short inrush timer is chosen (1nF of  $C_{INR}$ ). Unfortunately, when a very short timer is used and there is a dv/dt capacitor, the FET stress cannot be simply estimated by  $T_{INR}$ . In the following figure, it is clear that the FET has both voltage and significant current across it for longer than just  $T_{INR}$ . This occurs because  $T_{INR}$  is only activated when  $I_{IN}$  reaches the current limit threshold, which doesn't happen immediately due to the slow dv/dt on the gate and the limited transconductance of the FET.

The current is not a square pulse, which makes it hard to compare the FET stress to the SOA curves. Thus the stress shown in the following figure needs to be converted to an equivalent square pulse. For this example, the equivalent pulse was assumed to be 20 A for 1ms. The MOSFET can handle 100A, 13.2 V for 1ms, which can be derated to 62 A when accounting for elevated case temperature. This provides plenty of margin and ensures a robust design.

$$I_{SOA}(1\text{ ms}, T_{C,MAX,START}) = I_{SOA}(1\text{ ms}, 72^{\circ}\text{C}) \times \frac{T_{J,ABSMAX} - T_{C,MAX,START}}{T_{J,ABSMAX} - 25^{\circ}\text{C}}$$

$$= 100\text{ A} \times \frac{150^{\circ}\text{C} - 72^{\circ}\text{C}}{150^{\circ}\text{C} - 25^{\circ}\text{C}} = 62\text{ A} \quad (64)$$

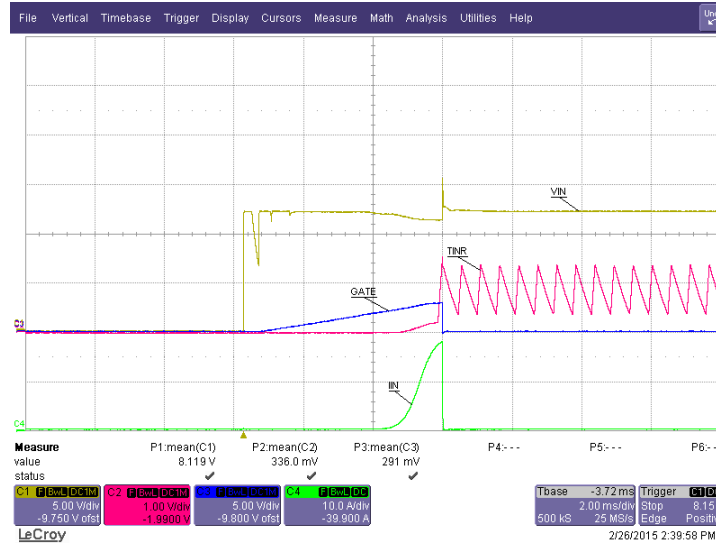


Figure 34. Start-up Into Short

#### 10.2.5.3.1.4 Choose Fault Timer

To pass the load transient, a target fault time ( $T_{FLT,TGT}$ ) of 250ms is used.  $C_{FLT,CLC}$  is computed as follows:

$$C_{FLT,CLC} = 7.59\ \mu\text{F} / \text{s} \times T_{FLT,TGT} = 7.59\ \mu\text{F} / \text{s} \times 250\ \text{ms} = 1898\ \text{nF} \quad (65)$$

The next largest available  $C_{FLT}$  is chosen as 2.2 $\mu\text{F}$ , which results in a TFLT of 290ms as shown below.

$$T_{FLT} = \frac{C_{FLT}}{7.59\ \mu\text{F} / \text{s}} = \frac{2.2\ \mu\text{F}}{7.59\ \mu\text{F} / \text{s}} = 290\ \text{ms} \quad (66)$$

#### 10.2.5.3.1.5 Choose Under Voltage and Over Voltage Settings

For this design example 10V and 14V were chosen as the limits to allow some margin for the 10.8V to 13.2V input bus. These are identical to the previous design example. See [Choose Under Voltage and Over Voltage Settings](#) section for programming these thresholds.

#### 10.2.5.3.1.6 Selecting $C_{IN}$ and $C_{OUT}$

It is recommended to add ceramic bypass capacitors to help stabilize the voltages on the input and output. Since  $C_{IN}$  will be charged directly on hot-plug, it's value should be kept small. 0.1 $\mu\text{F}$  is a good target. Since  $C_{OUT}$  doesn't get charged during hot-plug, a larger value such as 1  $\mu\text{F}$  could be used.

#### 10.2.5.3.1.7 Selecting D1 and D2

During hot plug and hot short events there could be significant transients on the input and output of the Hot Swap that could cause operation outside of the IC specifications. To ensure reliable operation a TVS on the input and a Schottkey diode on the output are recommended. In this example a SMDJ14A and MBR330T3G are used.



### 10.2.5.3.1.8 Adding $C_{ENHS}$

When the ENHS pulled below its threshold and raised back up the IC will reset. Note that during a hot short the input voltage can easily droop below the UV threshold and cycle the ENHS pin. For the TPS24770 and TPS24771 ICs this will not change the behavior. However, when using the TPS24772 the cycling of the ENHS will result in the IC attempting to restart, which is undesired (this is the main reason why someone would use the TPS24772). To avoid this behavior a capacitor should be added to the ENHS to provide filtering. 33 nF was chosen for this example.

### 10.2.5.3.1.9 Stability Considerations

Since there is a 100nF  $C_{DVRT}$  attached to HGATE, this significantly increases the effective capacitance of HGATE and guarantees stability for this application.

### 10.2.5.4 Application Curves

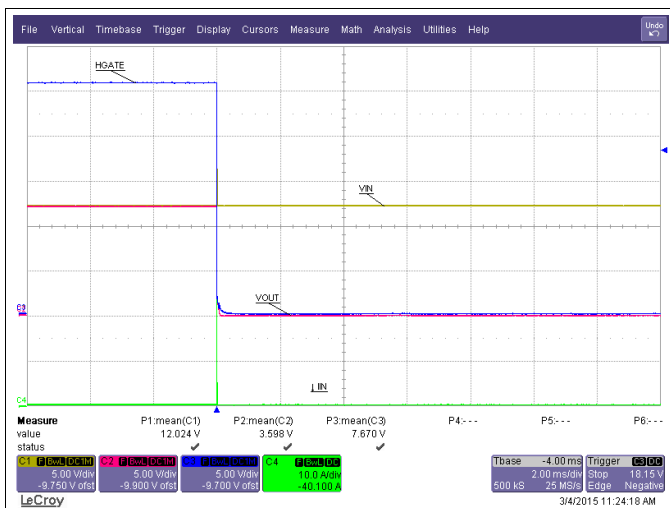


Figure 35. No Load then Hot Short (Zoomed Out)

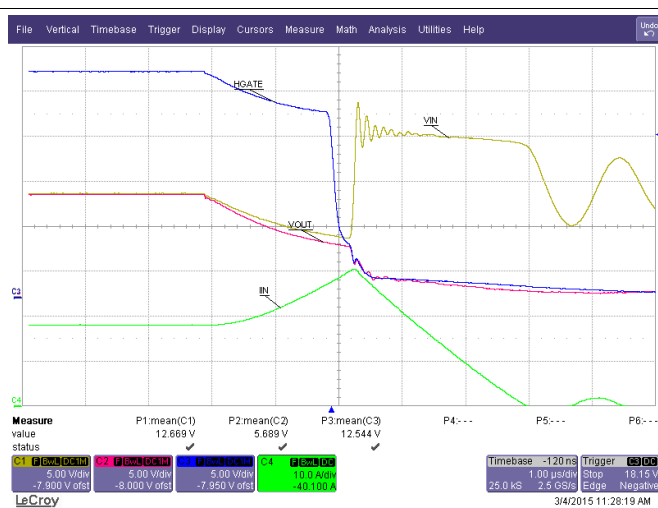


Figure 36. Full Load then Hot Short (Zoomed In)

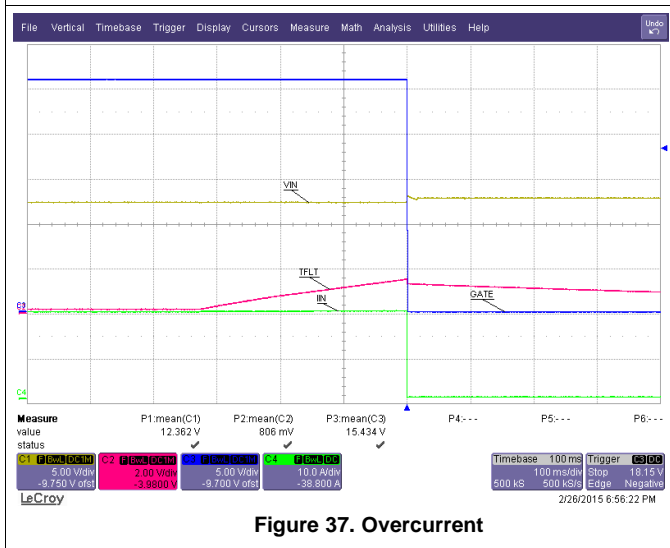


Figure 37. Overcurrent

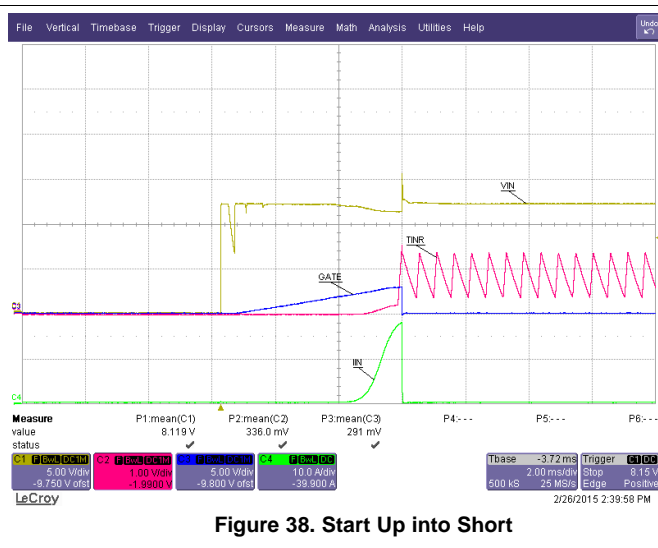
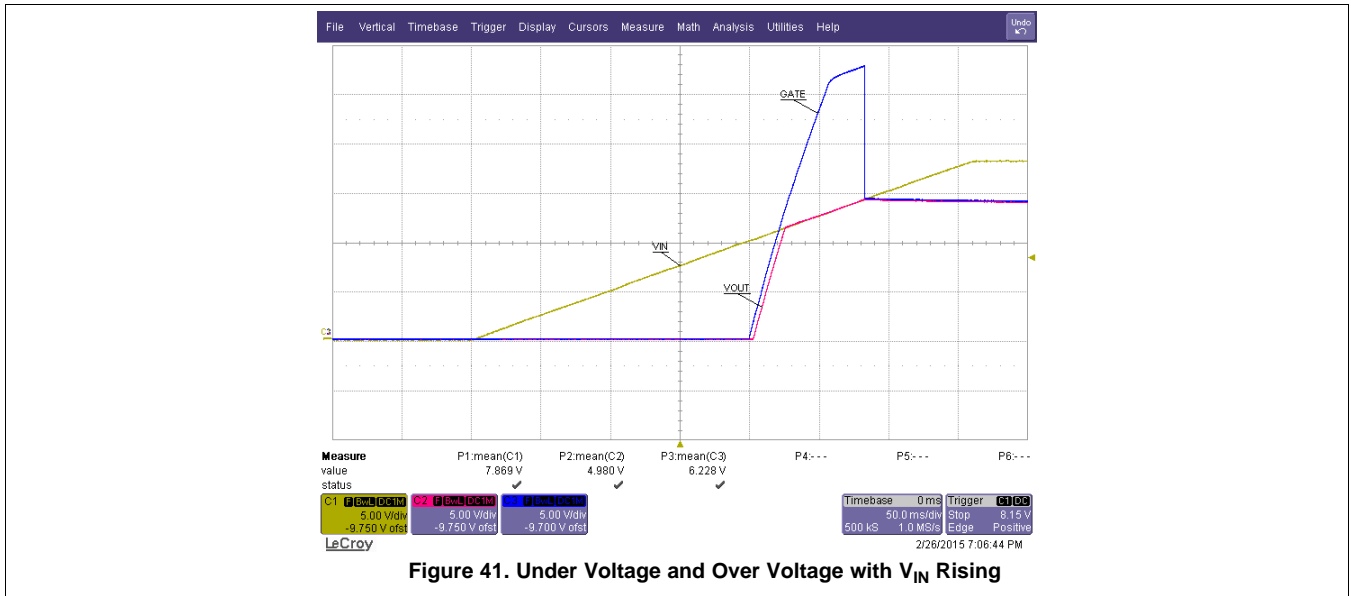
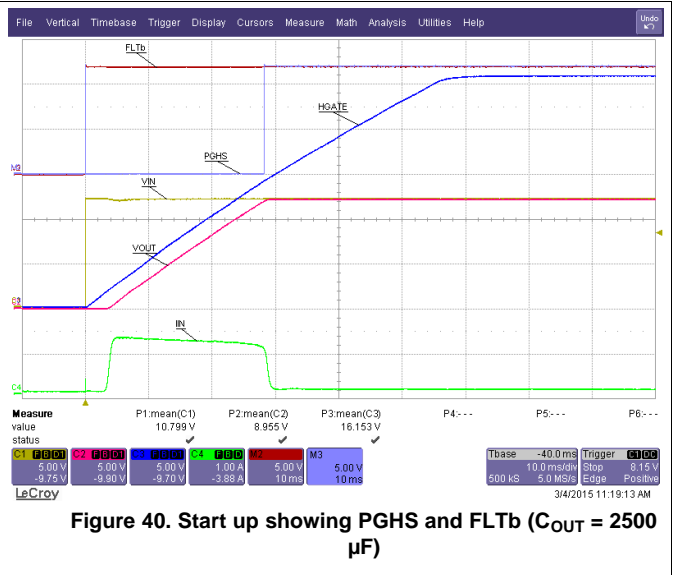
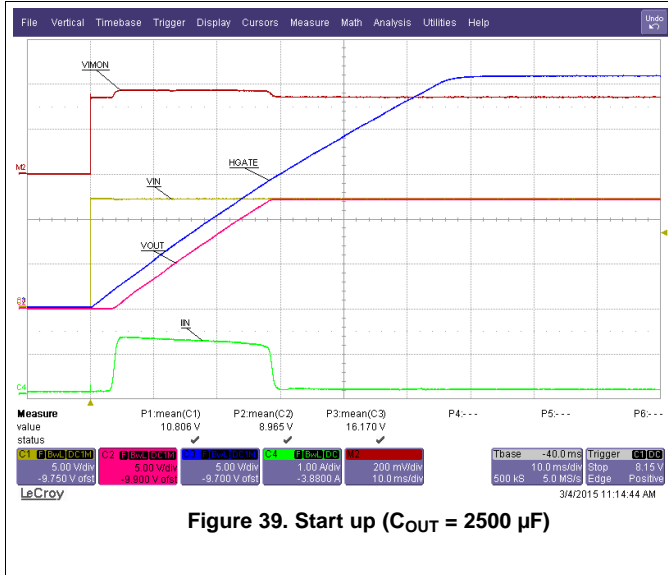


Figure 38. Start Up into Short



### 10.2.6 240 VA Application Using CSD17573Q5B

This design example has identical requirements to the previous one, but the CSD17573Q5B is used instead of the CSD16415Q5B. The CSD17573Q5B is cheaper and offers better  $R_{DS(ON)}$ , but its SOA is not as good. Thus it was necessary to add  $Q_2$  and  $R_{SET2}$  to reduce the stress during a start up into a short circuit. Given that  $Q_2$  is a small signal PFET that is cheap, the overall BOM cost of this solution should be cheaper than the previous one. See the [TPS24770 Design Calculator](#) to help with these calculations.

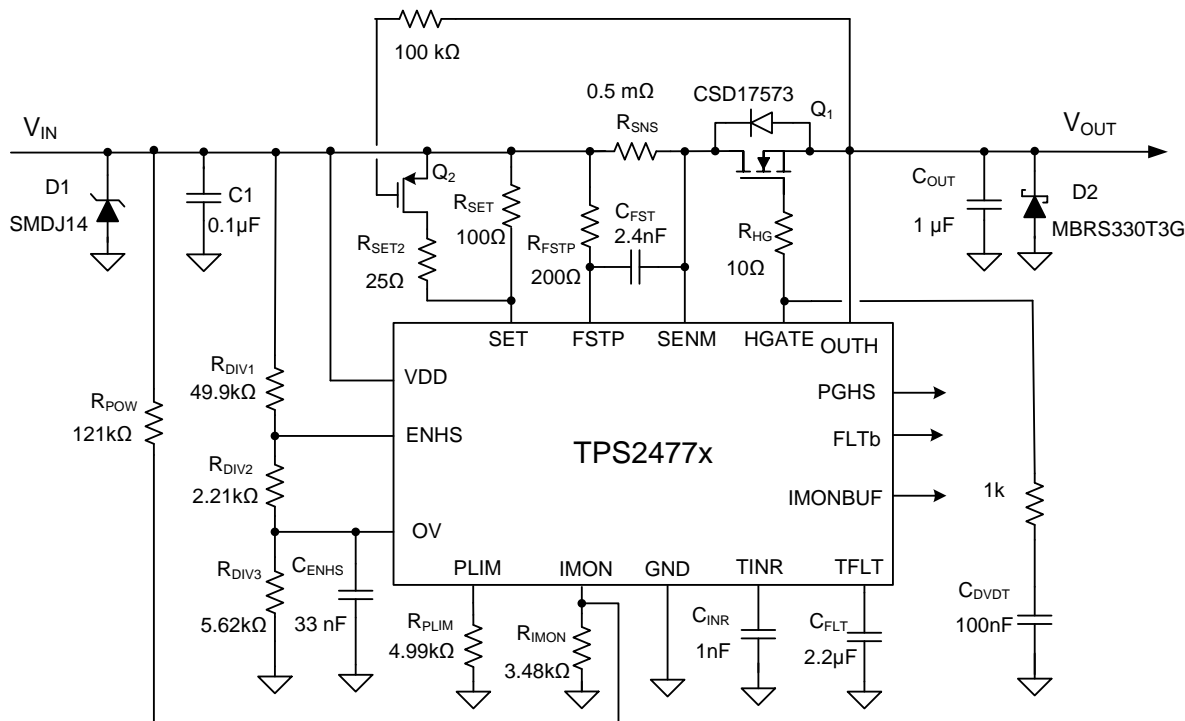


Figure 42. 240 VA Design Using CSD17573Q5B

### 10.2.6.1 Design Requirements

The following table summarizes the requirements for this design.

**Table 5. Design Requirements for the 240 VA Design Using CSD17573Q5B**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10.8 V – 13.2 V
Output Power Limit (VA limiting)	240 W
Maximum Output Capacitance of the Hot Swap	2500 $\mu$ F
Maximum Ambient Temperature	55°C
MOSFET $R_{\theta CA}$ (function of layout)	35°C/W
Transient load requirement?	POUT is allowed to surpass 240W for <250 ms
Pass “Hot-Short” on Output?	Yes
Pass a “Start into short”?	Yes
Is the load off until PG is asserted?	Yes
IC used	TPS24772
Analog Current Monitor Used	No
MOSFET	CSD17573Q5B
Can a Hot Board be plugged in or Power Cycled?	Yes

#### 10.2.6.1.1 Choosing $C_1$ , $C_{OUT}$ , $C_{FLT}$ , $C_{ENHS}$ , $D_1$ , $D_2$ , $R_{SET}$ , $R_{POW}$ , $R_{IMON}$ , $R_{SNS}$ , $C_{DVDT}$ , $R_{PLIM}$ , and UV/OV Thresholds

These components and settings are chosen in the same fashion as the previous design example. See [240 VA Application Using CSD16415Q5B](#).

#### 10.2.6.1.2 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a Hot Swap design. The device must meet the following requirements:

- The  $V_{DS}$  rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12V systems a 25 V or 30V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- $R_{DSON}$  should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.
- A  $V_{GS}$  rating of +16 V is required, because the TPS2477x can pull up the gate as high as 15.5 V above source.

For this design the CSD17573Q5B was selected for its low  $R_{DSON}$  and great cost point. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I_{LOAD,MAX}^2 \times \frac{R_{DSON}(T_J)}{n^2} \quad (67)$$

In the equation above n is the number of FETs used in parallel. Note that the  $R_{DSON}$  is a strong function of junction temperature, which for most MOSFETS will be very close to the case temperature. A few iterations of the above equations may be necessary to converge on the final  $R_{DSON}$  and  $T_{C,MAX}$  value. According to the CSD17573Q5B datasheet, its  $R_{DSON}$  is about 1.2 x greater at 65°C compared to room temperature. The equation below uses this  $R_{DSON}$  value to compute the  $T_{C,MAX}$ . Note that the computed  $T_{C,MAX}$  is close to the junction temperature assumed for  $R_{DSON}$ . Thus no further iterations are necessary.

$$T_{C,MAX} = 55^\circ\text{C} + 35^\circ\frac{\text{C}}{\text{W}} \times (20 \text{ A})^2 \times (1.2 \times 0.84 \text{ m}\Omega) = 69^\circ\text{C} \quad (68)$$

### 10.2.6.1.3 Keeping the MOSFET within SOA

As in the previous example, it is important to ensure that the MOSFET stays within its SOA during both regular start-up and start-up into short.

First consider the regular start-up. The same  $C_{D\text{VDT}}$  is used as the last example so the FET is required to handle 18.2W (or 1.38A and 13.2V) for 12.3 ms. Based on the SOA curve of the CSD17573Q55B, at  $V_{\text{DS}}$  of 13.2 V it can handle 4.5 A for 10 ms or 2 A for 100 ms. Using the same method as the previous design example, it can be inferred that the MOSFET can handle 4.2 A for 12.3 ms when  $V_{\text{DS}}=13.2$  V.

The SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be hotter during a start into a short. It is important to understand the hottest temperature that a MOSFET can be during a start-up ( $T_{\text{C, MAX, START}}$ ). If a board has been off for a while and then it's turned on  $T_{\text{A, MAX}}$  is a good estimate for  $T_{\text{C, MAX, START}}$ . However, if a board is on and then gets power cycled  $T_{\text{C, MAX}}$  should be used for  $T_{\text{C, MAX, START}}$ . This will depend on system requirements. For this design example, it's assumed that a hot board can be power cycled or hot plugged and  $T_{\text{C, MAX}}$  is used to estimate  $T_{\text{C, MAX, START}}$ .

$$\begin{aligned} I_{\text{SOA}}(12.3 \text{ ms}, T_{\text{C, MAX, START}}) &= I_{\text{SOA}}(12.3 \text{ ms}, 25^\circ\text{C}) \times \frac{T_{\text{J, ABSMAX}} - T_{\text{C, MAX, START}}}{T_{\text{J, ABSMAX}} - 25^\circ\text{C}} \\ &= 4.2 \text{ A} \times \frac{150^\circ\text{C} - 69^\circ\text{C}}{150^\circ\text{C} - 25^\circ\text{C}} = 2.7 \text{ A} \end{aligned} \quad (69)$$

Based on this calculation the MOSFET can handle 2.7 A, 13.2 V for 12.3 ms at 69°C elevated case temperature, but is only required to handle 1.38 A. Thus there is sufficient margin to make this a robust design. Again a 1.3x margin is recommended to cover for variations.

Next, consider the start into short condition. Similar to the previous design the MOSFET would need to handle 20A and 13.2 V for ~1ms. Checking the SOA curve of the CSD17573Q5B, it can only handle 10A and 13.2 V for 1ms, so it's SOA is clearly not sufficient.

This is where  $Q_2$  and  $R_{\text{SET2}}$  come in. They serve to reduce the current limit during starting up ( $I_{\text{LIM, START}}$ ) while the  $V_{\text{DS}}$  of the Hot Swap MOSFET is above  $V_{\text{T}}$  of  $Q_2$  (1V to 2V). The ratio of  $I_{\text{LIM}}$  to  $I_{\text{LIM, START}}$ , denoted as  $I_{\text{RATIO}}$ , is a function of  $R_{\text{SET}}$  and  $R_{\text{SET2}}$  as shown below. For this example a ratio of 0.2 ( $I_{\text{LIM, START}}=4\text{A}$ ) was targeted to reduce MOSFET stress, keep the current limit above  $I_{\text{INR}}$ , and ensure sufficient signal on  $V_{\text{SNS}}$  to keep the error reasonable. Once  $I_{\text{RATIO}}$  is chosen,  $R_{\text{SET2}}$  is computed to be 25  $\Omega$  as shown below.

$$I_{\text{RATIO}} = \frac{I_{\text{LIM, START}}}{I_{\text{LIM}}} = \frac{R_{\text{SET}} / R_{\text{SET2}}}{R_{\text{SET}}} \quad (70)$$

$$R_{\text{SET2}} = R_{\text{SET}} \times \frac{I_{\text{RATIO}}}{1 - I_{\text{RATIO}}} = 100 \Omega \times \frac{0.2}{1 - 0.2} = 25 \Omega \quad (71)$$

The start-up into short (with  $R_{\text{SET2}}$  and  $Q_2$ ) is shown in [Figure 43](#) below. The equivalent power pulse is now 4A for ~0.5ms. The MOSFET can handle 10A, 13.2 V for 1ms, which can be derated to 6.5 A when accounting for elevated case temperature. Since the MOSFET is only required to handle 4A for 0.5ms there is plenty of margin in the design.

$$\begin{aligned} I_{\text{SOA}}(1 \text{ ms}, T_{\text{C, MAX, START}}) &= I_{\text{SOA}}(1 \text{ ms}, 25^\circ\text{C}) \times \frac{T_{\text{J, ABSMAX}} - T_{\text{C, MAX, START}}}{T_{\text{J, ABSMAX}} - 25^\circ\text{C}} \\ &= 10 \text{ A} \times \frac{150^\circ\text{C} - 69^\circ\text{C}}{150^\circ\text{C} - 25^\circ\text{C}} = 6.5 \text{ A} \end{aligned} \quad (72)$$

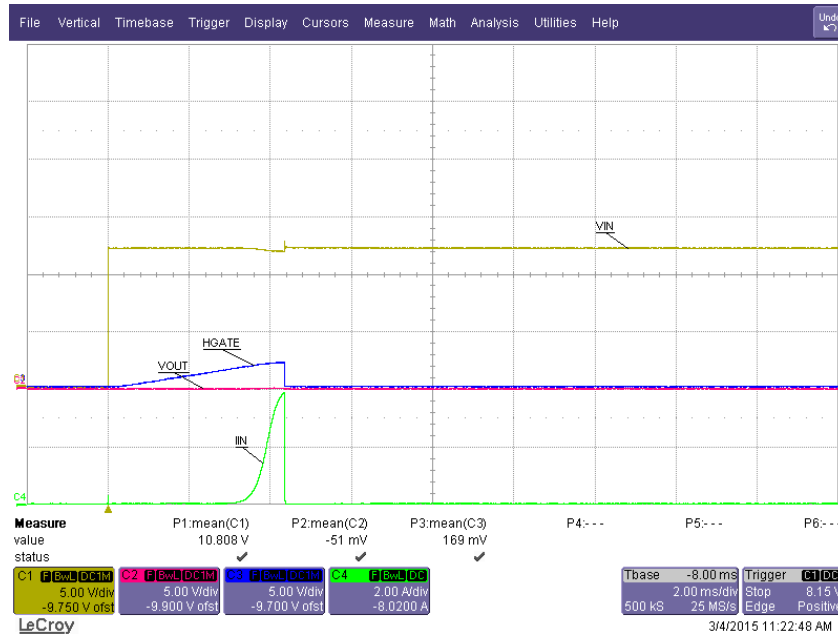


Figure 43. Start-up Into Short (with  $R_{SET}$  and  $Q_2$ )

### 10.2.6.2 Q2 Selection

There is a lot of flexibility when selecting  $Q_2$ . Any PMOS with a  $\pm 20V$   $V_{GS}$  rating and  $20V$  of  $V_{DS}$  rating is sufficient. For this example IRLML5203PbF was used. Note that the  $100k$  series resistor along with the  $C_{ISS}$  of  $Q_2$  ( $\sim 500pF$ ) for a filter with a  $50 \mu s$  time constant. This protects  $Q_2$  in case there is high frequency ringing on  $V_{IN}$  that causes  $V_{IN} - V_{OUT}$  to exceed  $20V$ . This will usually happen during hot-plug or hot-short.

### 10.2.6.3 Application Curves

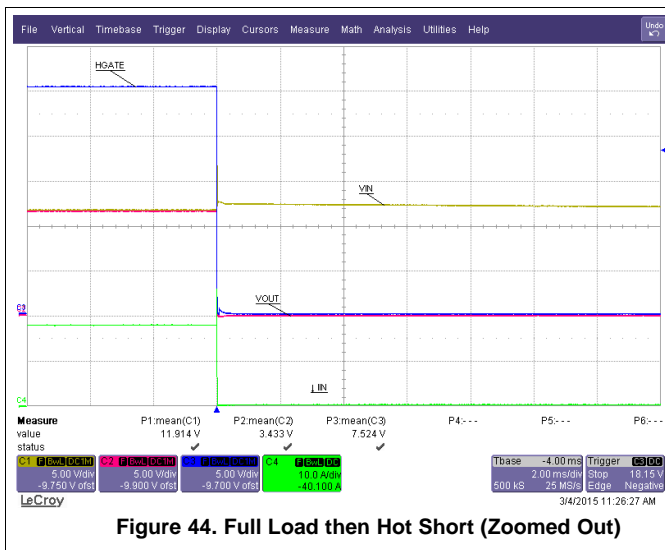


Figure 44. Full Load then Hot Short (Zoomed Out)

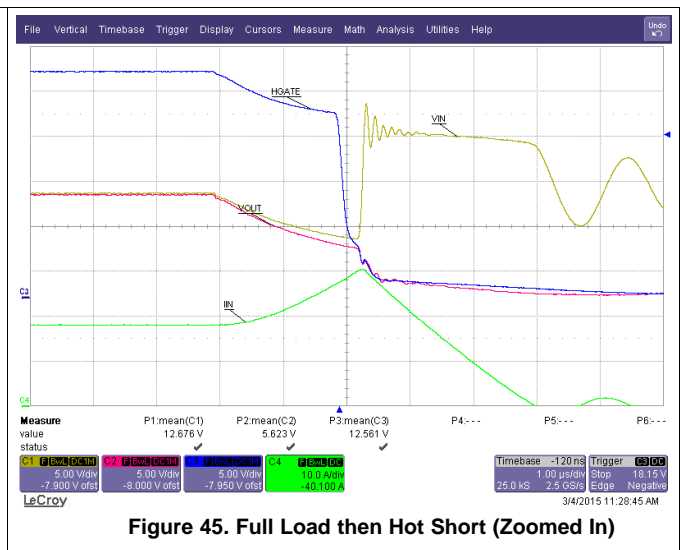


Figure 45. Full Load then Hot Short (Zoomed In)

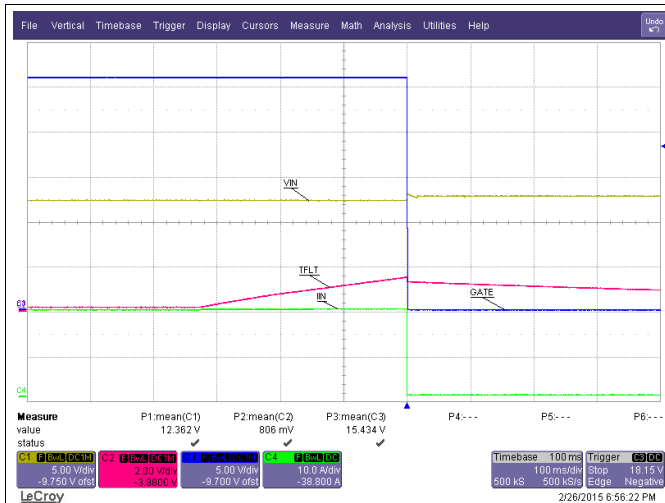


Figure 46. Over Current

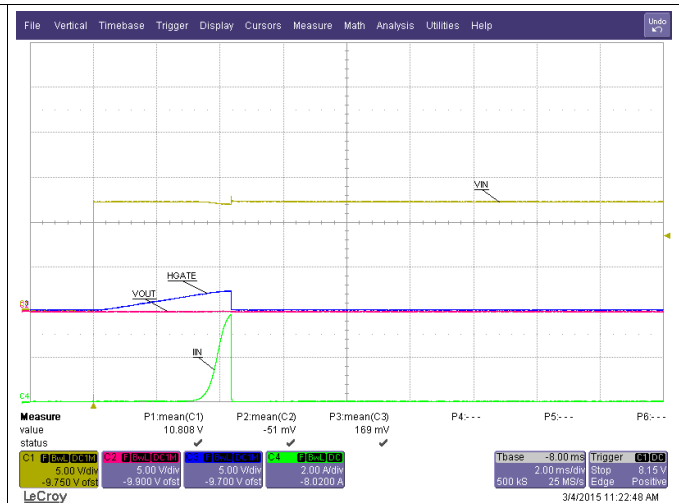


Figure 47. Start Up Into Short

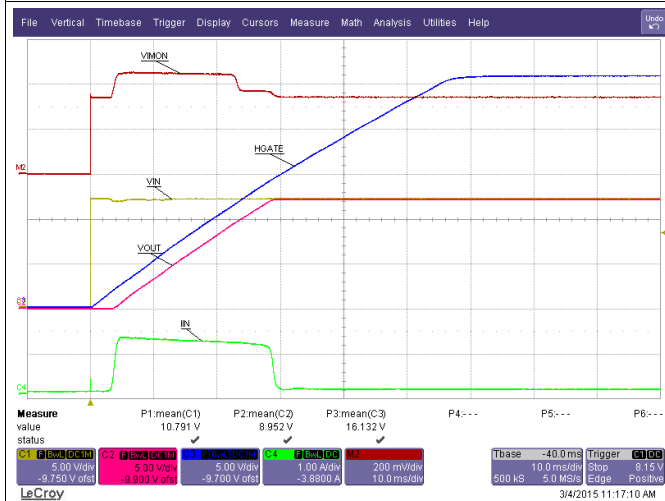


Figure 48. Start up ( $C_{OUT} = 2500 \mu F$ )

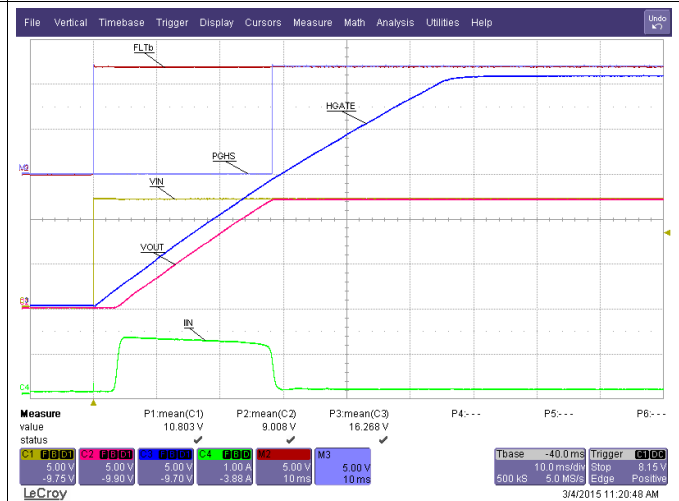


Figure 49. Start up showing PGHS and FLTB ( $C_{OUT} = 2500 \mu F$ )

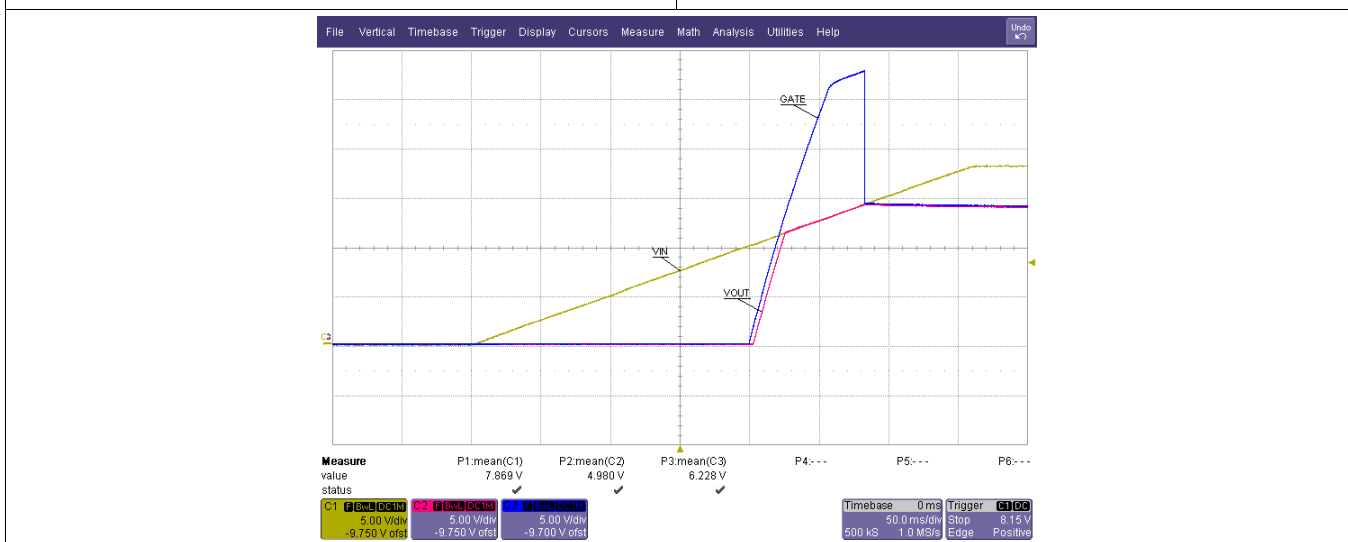


Figure 50.

## 11 Power Supply Recommendations

In general, operation is best when the input supply isn't noisy and doesn't have significant transients. For noisier environments filtering on input, output, and fast trip should be adjusted to avoid nuisance trips.

## 12 Layout

### 12.1 Layout Guidelines

When doing the layout of the TPS2477x the following are considered best practice.

- Ensure proper Kelvin Sense of  $R_{SNS}$ .
- Keep the filtering capacitor  $C_{FSTP}$  as close to the IC as possible.
- Place a Schottky diode and a ceramic bypass capacitor close to the source of the Hot Swap MOSFET
- Do not connect VDD to the Kelvin Sense trace for SET and FSTP
- Note that special care must be taken when placing the bypass capacitor for the VDD pin. During Hot Shorts, there is a very large  $dv/dt$  on input voltage during the MOSFET turn off. If the bypass capacitor is placed right next to the pin and the trace from  $R_{SNS}$  to the pin is long, an LC filter is formed. As a result a large differential voltage can develop between VDD and SENM if there is a large transient on  $V_{in}$ . This could result in a violation of the abs max rating from VDD to SENM. To avoid this, place the bypass capacitor close to  $R_{SNS}$  instead of the VDD pin.

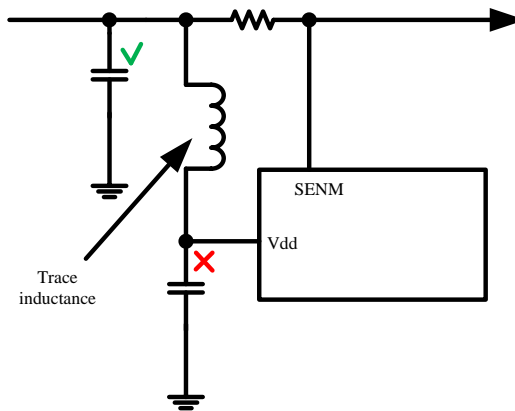


Figure 51. Layout Don't

- When using parallel resistors the layout becomes even more critical. Due to PCB parasitics, the current through each  $R_{SNS}$  may be different, which results in different sense voltages across the two resistors. It's important to average these in order to get a proper current measurement. This can be accomplished by forming a resistor divider with the traces. As long as  $Dis1 = Dis2$ , the final  $V_{SNS}$  will be an average of the drop across the two resistors.



Layout Guidelines (continued)

# Power Flow

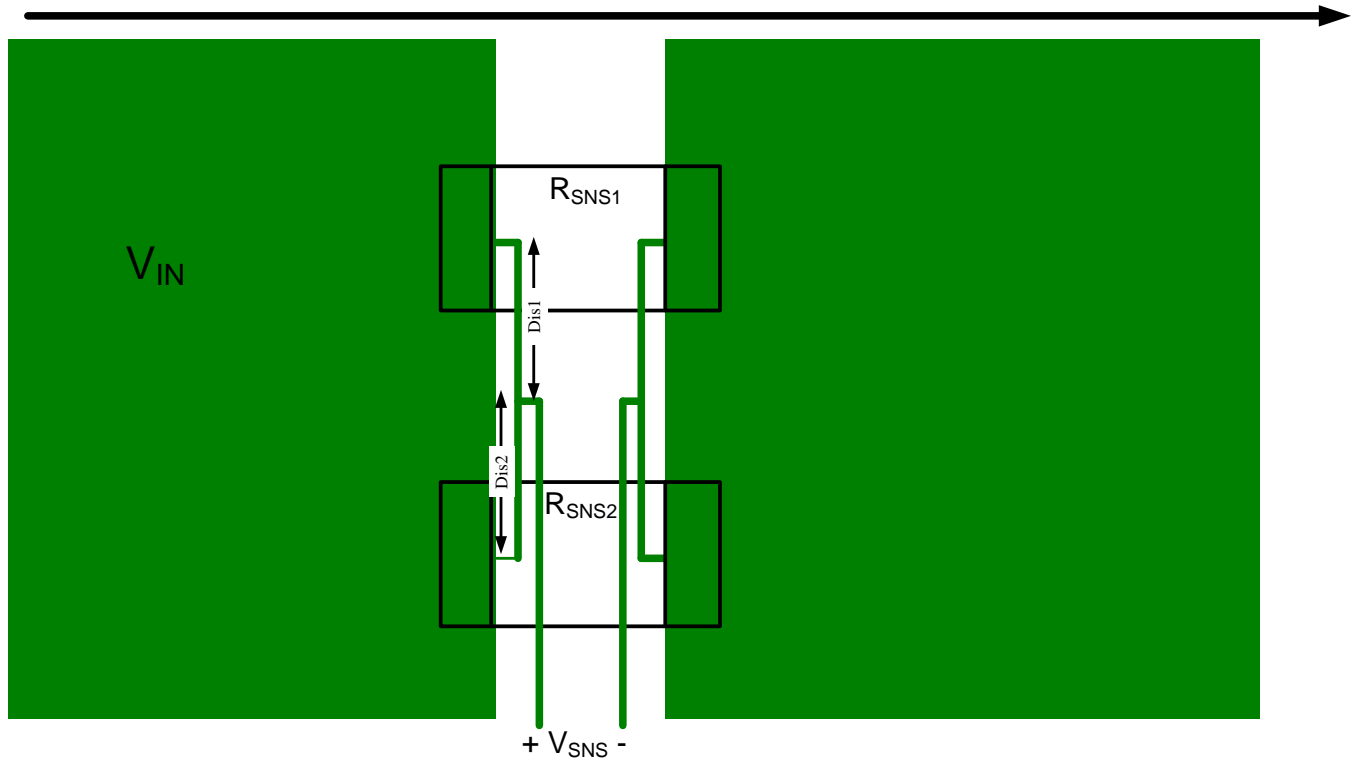
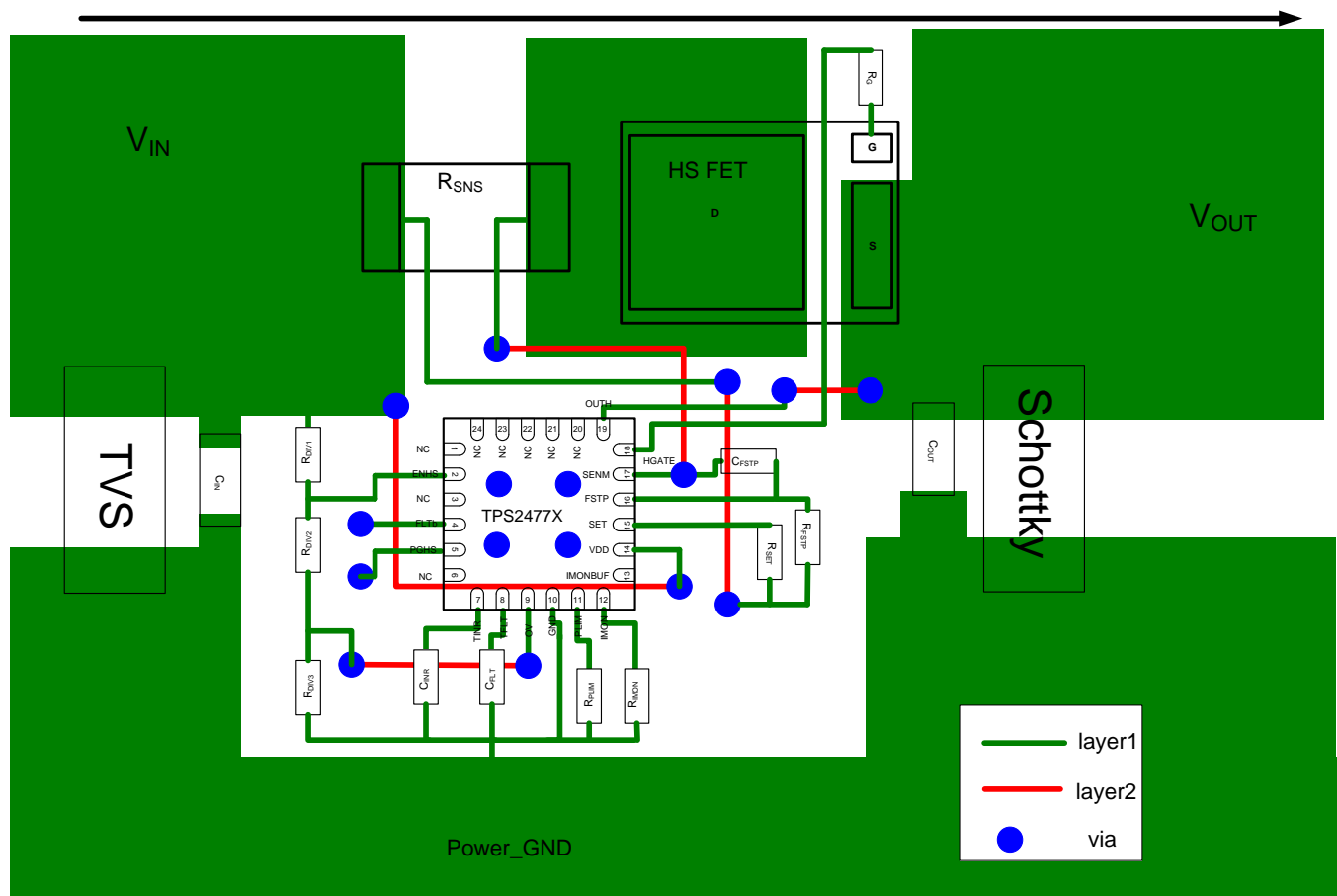


Figure 52. Sense Layout with 2  $R_{SNS}$

## 12.2 Layout Example

### Power Flow



## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 6. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS24770	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS24771	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS24772	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS24770RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24770	<a href="#">Samples</a>
TPS24770RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24770	<a href="#">Samples</a>
TPS24771RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24771	<a href="#">Samples</a>
TPS24771RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24771	<a href="#">Samples</a>
TPS24772RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24772	<a href="#">Samples</a>
TPS24772RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24772	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS24770RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24770RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24771RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24771RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24772RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24772RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS24770RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS24770RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS24771RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS24771RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS24772RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS24772RGET	VQFN	RGE	24	250	210.0	185.0	35.0

**RGE 24**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H





4219013/A 05/2017

NOTES:

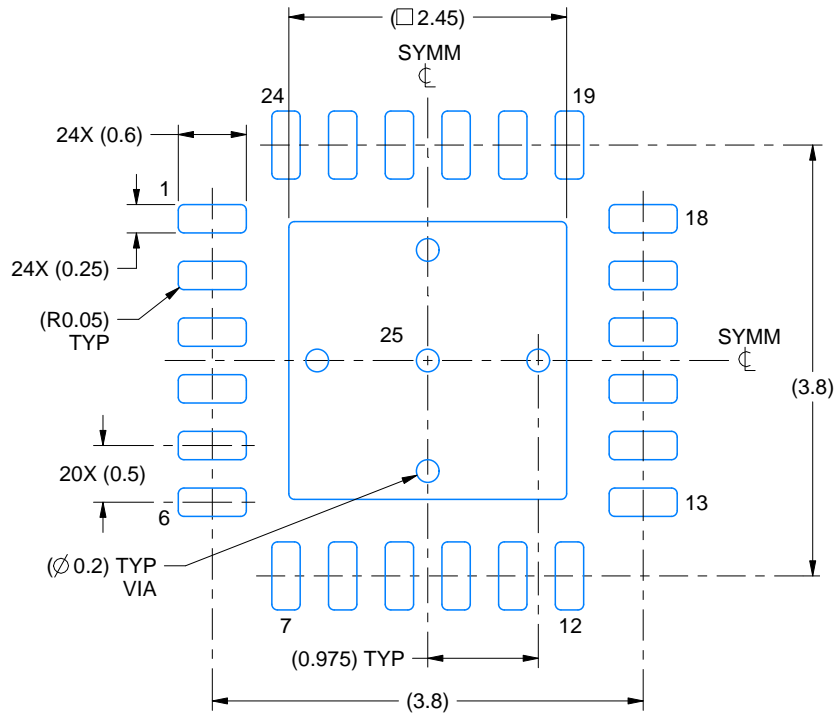
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25  
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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