AN-1411 LM3075 Evaluation Board

1 Introduction

The LM3075 is a current mode synchronous buck controller. Use of synchronous rectification and pulse-skipping operation at light load achieves high efficiency over a wide load range. Current mode control assures excellent line and load regulation and a wide loop bandwidth for fast response to load transients. It is achieved by sensing across the high side NFET, eliminating the need for a sense resistor. The switching frequency is selectable to 200 kHz or 300 kHz. Protection Features include over-voltage protection (OVP), under-voltage protection (UVP), thermal protection, and positive and negative peak current limiting.

This evaluation board generates 5V at 5A from a wide input voltage range of 8V to 25V utilizing the LM3075. The switching frequency is set at 300 kHz. This document contains the demo board schematic, Bill of Materials, circuit design description, and PCB layout guide. Performance data and typical waveforms are also provided.

For detailed information about the LM3075, please see *LM3075 High Efficiency, Synchronous Current Mode Buck Controller* (SNVS398).

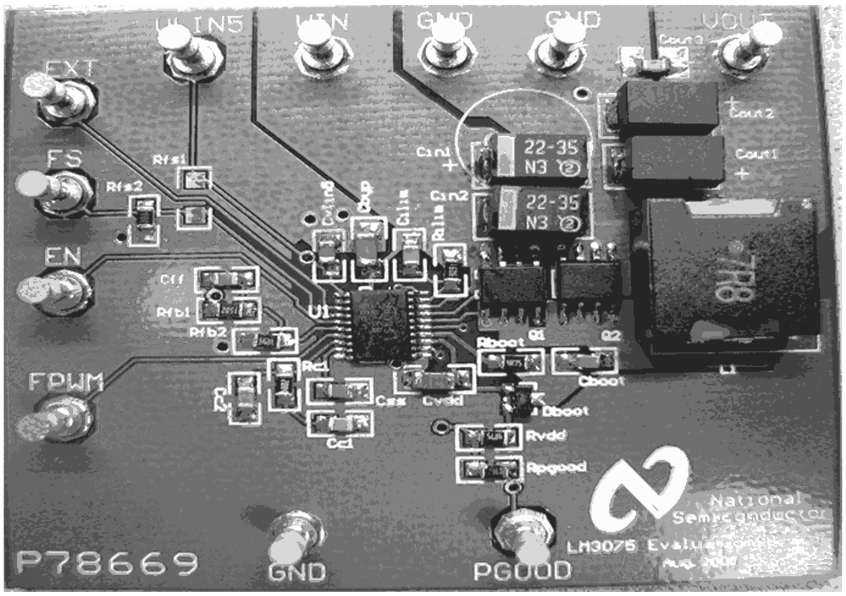


Figure 1. LM3075 Evaluation Board Top View

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2 Electrical Specifications

Description		Min	Typical	Max	Unit
Input Voltage	V_{IN}	8	-	25	V
Output Current	I_{OUT}	0	-	5	A
Output Voltage	VOUT	4.80	5	5.20	V
Ripple and Noise	Irr(peak-peak)	-	-	50	mV
Load Transient					
Load Step			5A		
Voltage Deviation		-7%		+7%	%
Current Limit	I_{LIM}	6	6.5	7	A
Startup					
Overshoot				5.25	V
Undershoot		4.75			V
Switching Frequency	fsw		300		kHz

3 Evaluation Board Setup

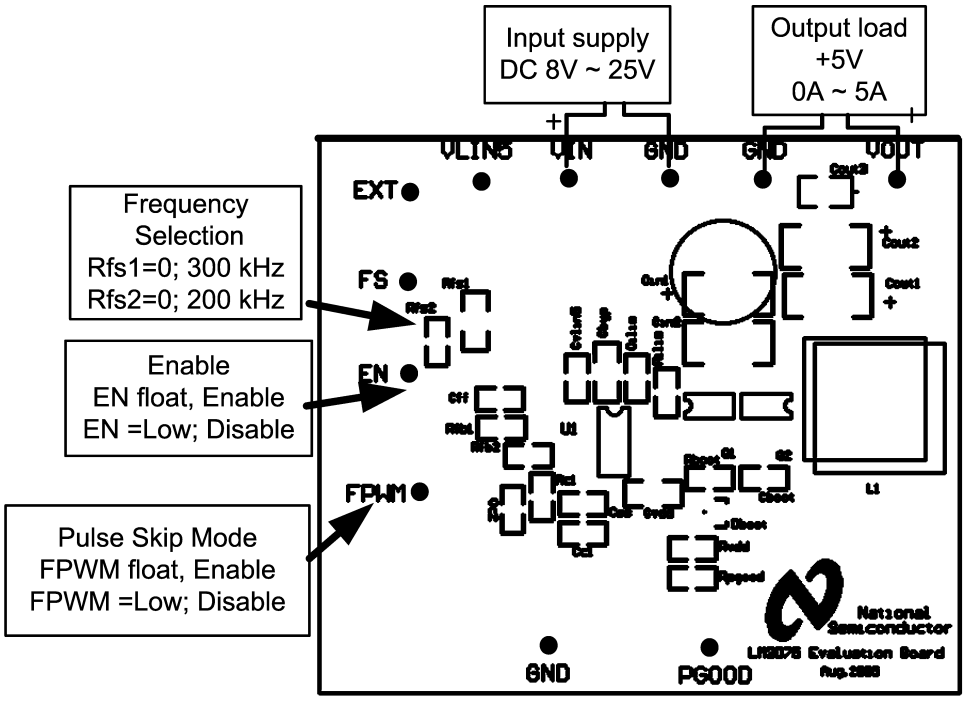


Figure 2. LM3075 Evaluation Board Setup

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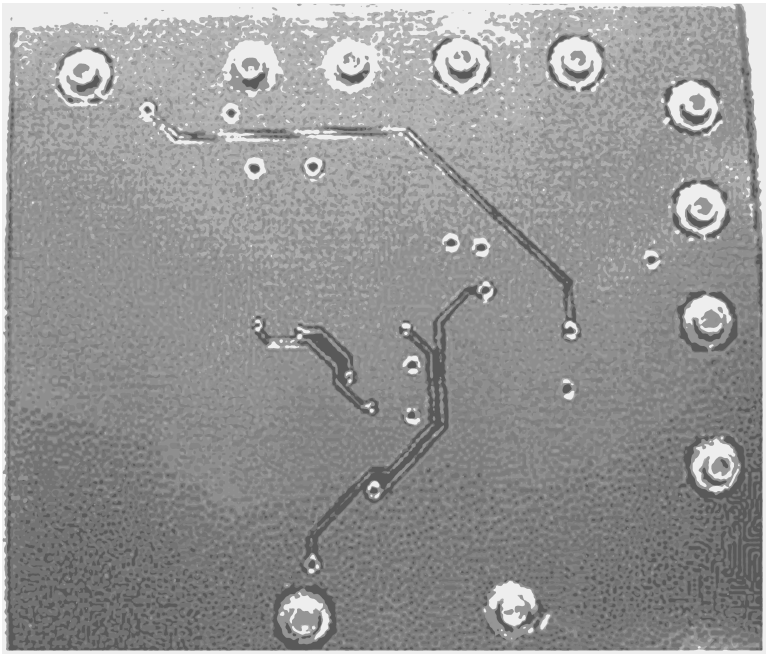


Figure 3. LM3075 Evaluation Board Bottom View

4 Quick Setup Table

Item	Description	Notes
1	DC Input Voltage range	8V ~ 25V
2	DC load current	0A ~ 5A, +5V
3	EN Float , Enable default EN = GND, Disable	
4	FPWM FPWM float, skip mode available default FPWM = GND, skip mode disable	
5	Frequency selection Rfs1 = 0, Rfs2 = open, the switching frequency is 300 kHz Rfs2 = open, Rfs2 = 0, FS connects to GND, the switching frequency is 200 kHz at typical	

In this design, the Vlin5 is chosen to drive the bootstrap circuit. The inductor and capacitor were chosen for operation at a 300 kHz switching frequency. Connecting the FS pin to Vlin5 through the zero ohm resistor Rfs1 sets the switching frequency to 300kHz. Grounding the FS pin (open Rfs1 and set Rfs2 to 0 Ohms) programs the regulator to 200 kHz. This evaluation board leaves options for input capacitors Cin1/Cin2, inductor L1, and output capacitors Cout1/Cout2. It provides the flexibility to evaluate the LM3075 in several different configurations.

5 Component Selection

Detailed design procedures can be found in the LM3075 datasheet (SNVS398). In this document, we will give brief instructions on the circuit design and describe the procedures used in testing the board.

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5.1 Output Capacitor (Cout1, Cout2) and Inductor (L1)

The first priority in component selection is given to the output capacitors as there is often less flexibility in this choice than in other parameters. These capacitors must meet requirements for output voltage rating, high ripple current rating, low ESR and surface mount design. Sanyo POSCAPs and Panasonic SP-CAPs are good choices. Here we selected the SP-CAP UE series. The typical ESR is 12 mΩ and the ripple current rating is 3.3A at 100 KHz/ 20°C. The allowable steady-state ripple voltage is 50 mV peak to peak maximum. In order to ensure reasonable design margins 40 mV is used. The allowed output voltage excursion during a load transient is:

$$\Delta V_{TRANS} = (7\% - 4\%) \times 5V - \frac{40\ mV}{2} = 130\ mV \quad (1)$$

The maximum allowed total combined ESR is:

$$R_{ESR(MAX)} = \frac{130mV}{5A} = 26\ m\Omega \quad (2)$$

The minimum inductance value is determined as follows:

$$L_{MIN} = \frac{25V - 5.0V}{300\,kHz \times 25V} \times \frac{5.0V \times 12\ m\Omega}{40\ mV} = 4\ \mu H \quad (3)$$

A 7.8 µH inductor from TDK (RLF12545-7R8N5R4) is chosen. The RMS current rating is 5.4A that should prove adequate. The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest input and output voltages and load transient requirements should be considered.

The inductor ripple current can be determined as follows:

$$\Delta I_L = \frac{25V - 5.0V}{300\ kHz \times 7.8\ \mu H} \times \frac{5.0V}{25V} = 1.7A \quad (4)$$

Given a maximum load current of 5A, the ripple content is 1.7A / 5A = 34%. In general, the ripple current is designed to be between 20% and 40% of the full load output current although less than 50% is fine. Larger ripple current causes excessive losses in the inductor, higher RMS switch currents and overall lower efficiency. On the plus side, transient response will generally be better with higher ripple current.

The corresponding minimum capacitance is calculated as follows:

$$C_{OUT} = \frac{5.6\ \mu H \times \left[130\,mV - \sqrt{(160\ mV)^2 - (5A \times 12\,m\Omega)^2}\right]}{5 \times (12\,m\Omega)^2} = 114\ \mu F. \quad (5)$$

The output capacitance should be chosen to be slightly larger than the calculated value as capacitance and ESR vary somewhat with temperature. Here we would likely be fine choosing 180µF.

5.2 Input Capacitor (Cin1, Cin2)

The input capacitor is selected to handle both the maximum ripple RMS current at highest ambient temperature as well as the maximum input voltage 25V. The maximum total input ripple RMS current for duty cycles under 50% is:

$$I_{in_rms} = 5A \sqrt{0.42 \times (1 - 0.42)} = 2.46A \quad (6)$$

Choose input capacitors that can handle 2.46A RMS of ripple current at the highest expected ambient temperature. Actually, there are several types of capacitor to choose from. The OS-CON series from Sanyo and TR3 series from Vishay are good choices with low ESR, high ripple current rating and small size. In this design, we selected the Vishay TR3 series 22 µF 35V.

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5.3 MOSFET (Q1, Q2)

In this design, VLIN5 is chosen to drive the bootstrap circuit. The top FET starts to turn on when the input voltage exceeds the threshold voltage of the UVLO, which has a minimum threshold of 3.8V. In this case VLIN5 will be approximately 3.8V when the LM3975's UVLO clears. Thus the bias voltage to the top FET driver is about 3V after the bootstrap diode. So the gate threshold voltage of the top FET should be less than 3V (maximum).

Vishay's Si4840 is chosen for Q1 and Q2. The Si4840 has a maximum Rds(on) of 12 mΩ at VGS = 4.5V. The maximum gate threshold voltage is 3V. The total gate charge is 28 nC at maximum. Some FETs have on-resistance specified at 2.7V and would be potentially good choices as well, though slightly more expensive than the 4.5V specified parts.

5.4 Output Voltage Setting (Rfb1, Rfb2)

The output voltage is set by the ratio of Rfb1 and Rfb2. The resistor values can be determined by the following equation:

$$Rfb2 = \frac{Rfb1}{\left(\frac{V_{OUT}}{V_{FB}} - 1\right)} \tag{7}$$

Where VFB is the typical value of feedback pin voltage and VOUT is the nominal output voltage. Although increasing the value of Rfb1 and Rfb2 increases efficiency, this also decreases accuracy due to bias currents at the VFB input. Therefore, a maximum value is recommended for Rfb2 of about 15 kΩ . Rfb1 is simply calculated as 5 kΩ using the above equation.

5.5 Current Limit Setting (RLIM)

With an external resistor connected between the ILIM pin and the CSH pin the LM3075's internal 10µA current sink on the ILIM pin produces a voltage across the resistor to serve as the reference voltage for current limit. Adding a 10 nF capacitor across this resistor filters unwanted noise that could improperly trip the current limit comparator.

The current limit resistor, RLIM, is calculated as follows:

$$R_{LIM} = \frac{\left(6.5A + \frac{1}{2} \times 2A\right) \times 12\ m\Omega}{10\ \mu A} \tag{8}$$

5.6 Switching Noise Reduction (Rboot)

Rboot is added in series with the CBOOT pin to slow down the gate drive (HDRV) rise time. A slower drain current transition time will reduce shoot through currents and ringing on the switch node caused by parasitic inductance in the power path. Usually a 3.3 to 5.1 ohm resistor is sufficient to suppress excessive noise. It is important to note that the addition of these resistors does increase the power loss in the system and thus decrease the efficiency. It is therefore important to choose the size of the resistor carefully since the top FET switching losses will increase with higher resistance values.

5.7 Soft Start (Css, Cff)

Capacitor Cff is used to add a little phase lead into the feedback loop. Add this cap if excessive overshoot is observed during start up or an improvement in transient response is required.

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6 PCB Layout Guide

The layout should begin with the placement of power path components such as Cin1, Cin2, Q1, Q2, L1, Cout1, Cout2 and current sense resistor. The input capacitor Cout1 and Cout2 should always be placed as close as possible to the current sense resistor or the drain of the top FET. The power MOSFETs, Q1and Q2, should be located close to the inductor, L1. The source of Q2 should be as close as possible to the ground of input capacitor. This helps to keep large pulse currents out of the ground plane. The decoupling capacitor Cout3 should be located close to the output terminal. The objective is to minimize the loop area of power path, and minimize the stray inductance.

The controller should be close to Q1 and Q2 in order to keep the gate drive paths as short as possible. The control circuits should be placed in the quiet area out of the power path loop. AGND and PGND should be directly connected with a wide trace. Connect PGND to the main ground plane with a via close to the pin. The bootstrap circuit Dboot and Cboot should be located adjacent to the SW and Cboot pins. All of the power source pins Vin, Vlin5 and Vdd should be well bypassed, respectively by Cbyp, Clin5 and Cvdd.

In this design, the current limit is configured to sense the Vds of top switching FET, Q1. This configuration has the advantages of saving PCB area while lowering power loss and cost. However, the connection approach from CSH / CSL to the Drain/Source of the FETs needs to be thought out carefully. Poor layout will result in unwanted noise spikes at the source node of switching FET Q1. In general, the connection should be immediately adjacent to the Drain and Source pins respectively. The two traces should be placed in parallel.

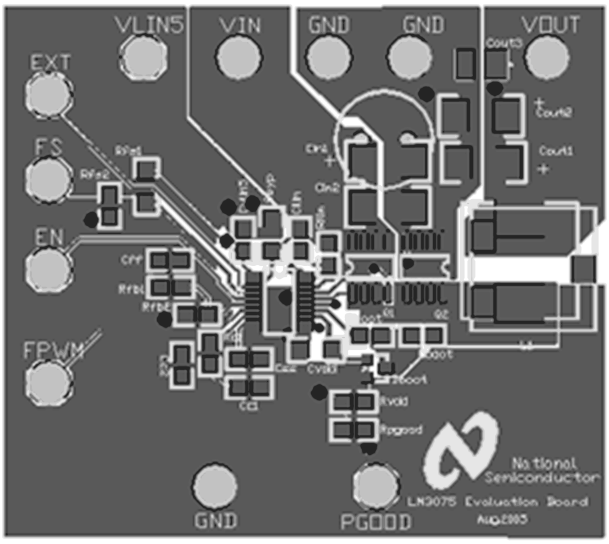


Figure 4. LM3075 Evaluation Board Top Layer Layout

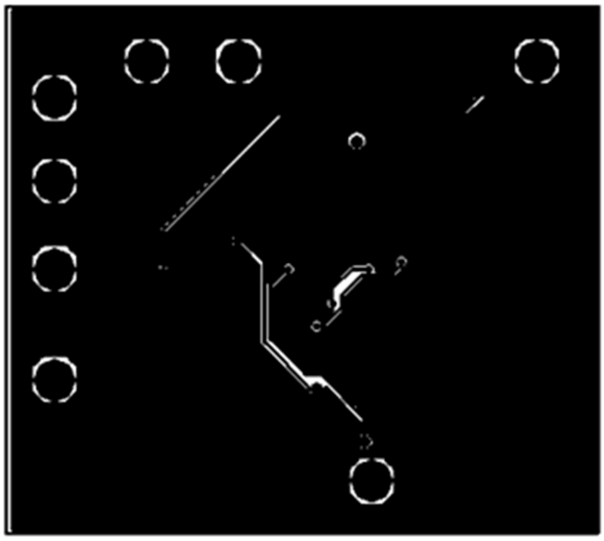


Figure 5. LM3075 Evaluation Board Bottom Layer Layout

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7 Evaluation Board Schematic

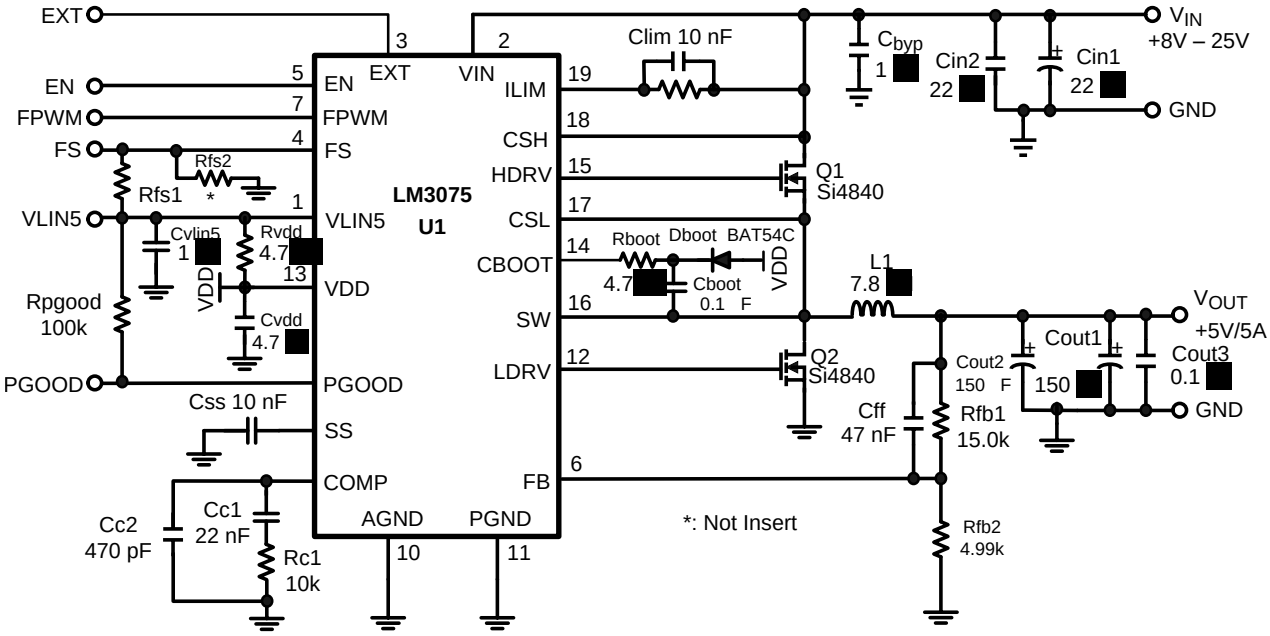


Figure 6. LM3075 Evaluation Board Schematic

8 Bill of Materials

Table 1. Bill of Materials

Designation	Description	Size	Manufacture Part #	Vendor
Cbyp	Cap Ceramic X7R 1µF 50V	1206	C3216X7R1H105K	TDK
Cin1, Cin2	Cap Tantalum 22µF 35V	2815	293D226X0035E2T	Vishay
Cin2	Cap Tantalum 22µF 35V	2815	293D226X0035E2T	Vishay
Cilim	Cap MLCC 10nF 25V X7R	0805	VJ0805Y103KXX	Vishay
Cboot	Cap MLCC 0.1µF 25V X7R	0805	VJ0805Y104KXX	Vishay
Cc2	Cap MLCC 470pF 25V X7R	0805	VJ0805Y471KXX	Vishay
Cc1	Cap MLCC 22nF 25V X7R	0805	VJ0805Y223KXX	Vishay
Css	Cap MLCC 10nF 25V X7R	0805	VJ0805Y103KXX	Vishay
Cvdd	Cap MLCC 4.7µF 10V X7R	1206	C3216X7R1C475K	TDK
Cvlin5	Cap MLCC 1µF 10V X7R	0805	VJ0805Y105KXQ	Vishay
Cout3	Cap MLCC 0.1µF 25V X7R	0805	VJ0805Y104KXX	Vishay
Cout1	Cap POSCAP 150µF 6.3V	D2E	6TPE150MI	Sanyo
Cout2	Cap POSCAP 150µF 6.3V	D2E	6TPE150MI	Sanyo
Cff	Cap MLCC 0.047µF 25V X7R	0805	VJ0805Y473KXX	Vishay
Rilim	Resistor Chip 9.09kΩ J	0805	CRCW08059091J	Vishay
Rfb2	Resistor Chip 4.99kΩ F	0805	CRCCW08054991F	Vishay
Rfb1	Resistor Chip 15.0kΩ F	0805	CRCW08051502F	Vishay
Rboot	Resistor Chip 1Ω J	0805	CRCW08051R00J	Vishay
Rc1	Resistor Chip 10kΩ J	0805	CRCW0805103J	Vishay
Rvdd	Resistor Chip 4.7Ω J	0805	CRCW08054R7J	Vishay
Rpgood	Resistor Chip 100kΩ J	0805	CRCW0805105J	Vishay
Rfs1	Resistor Chip 0 J	1206	CRCW12060R0J	Vishay

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Table 1. Bill of Materials (continued)

Designation	Description	Size	Manufacture Part #	Vendor
Q1	FET N 40V 12A	SO-8	Si4840	Vishay
Q2	FET N 40V 12A	SO-8	Si4840	Vishay
L1	Inductor 7.8µH 5.4A	12.5x12.5x6	RLF12545-7R8N5R4PF	TDK
Dboot	Diode Shottky 30V 0.5A	SOT-23	BAT54C	Vishay
U1	IC LM3075	TSSOP-20	LM3075	Texas Instruments
PCB	LM3075 Demoboard		Aug-05	Texas Instruments

9 Typical Performance and Waveforms

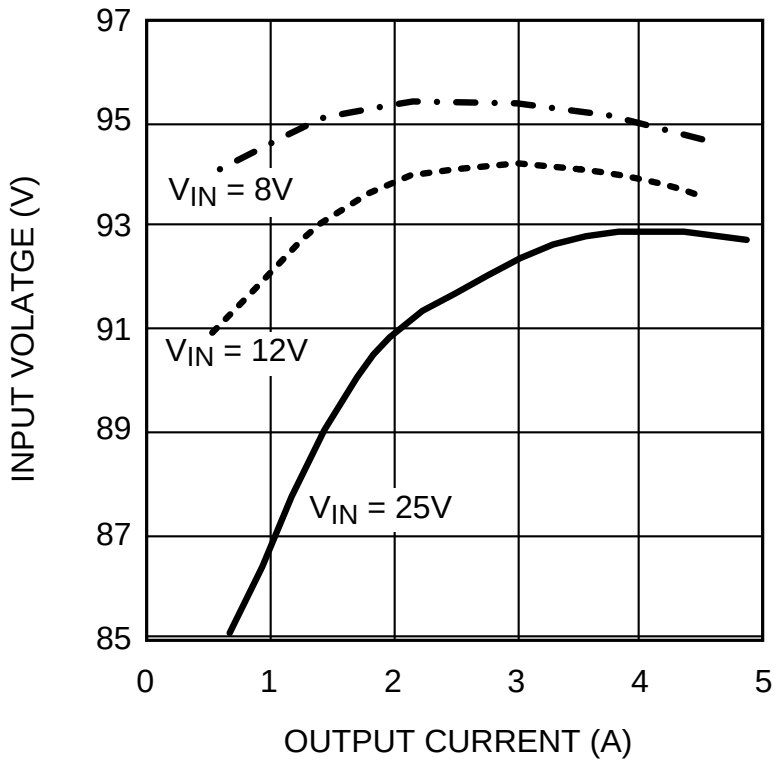


Figure 7. Efficiency

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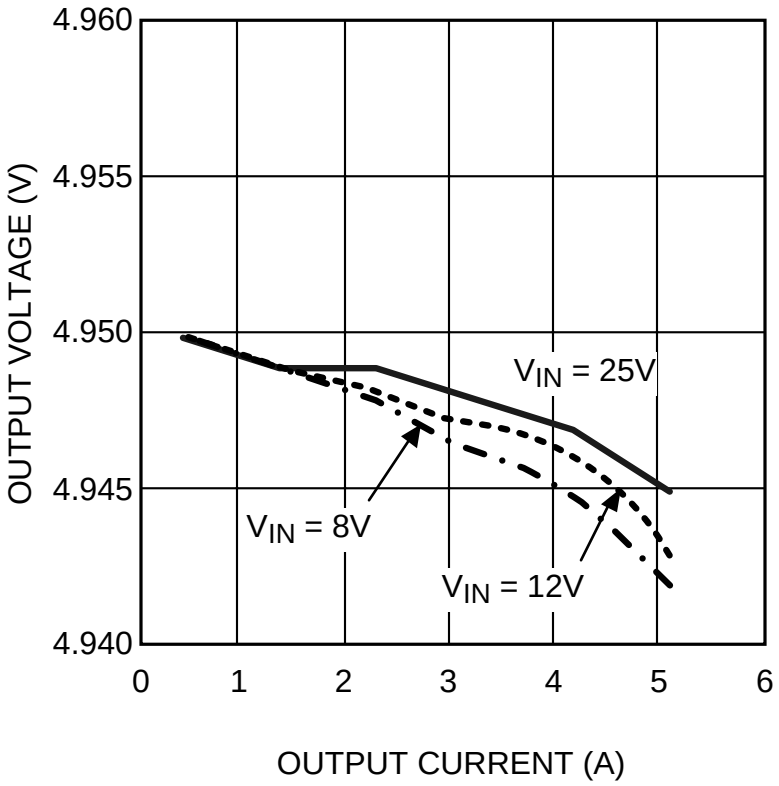


Figure 8. Output Regulation

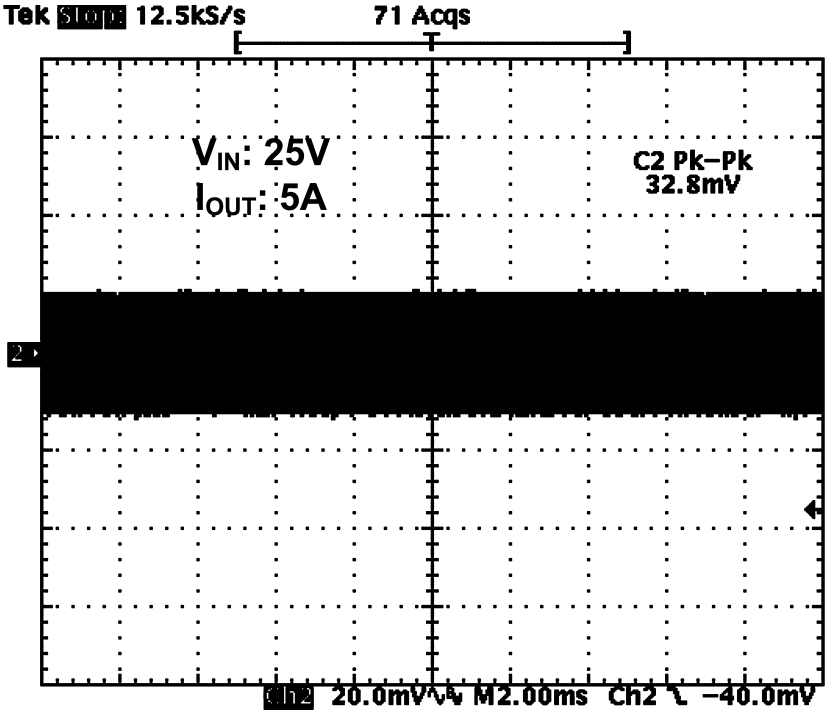


Figure 9. Ripple and Noise

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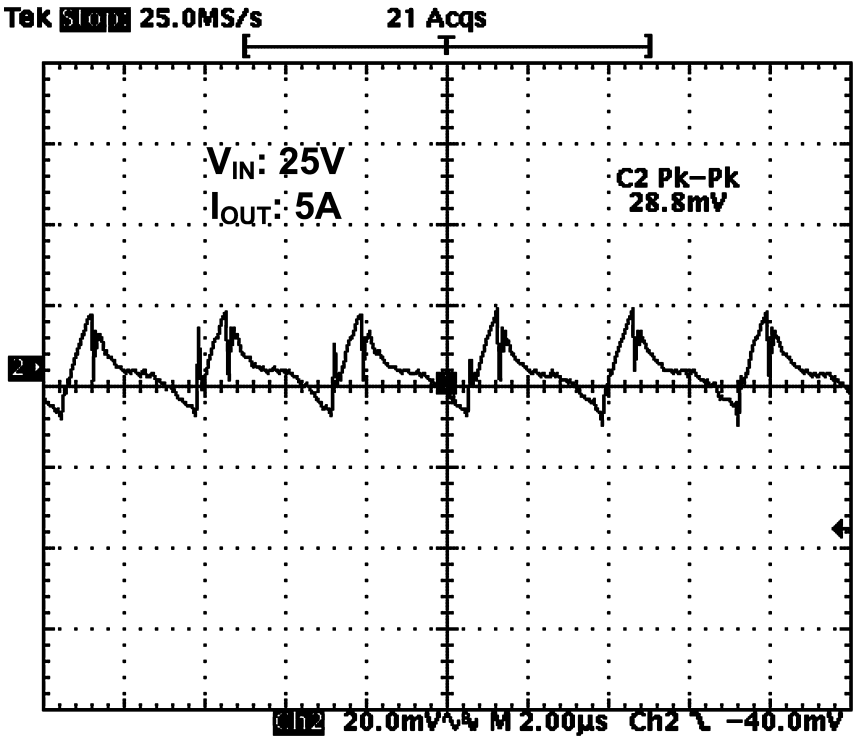


Figure 10. Ripple and Noise

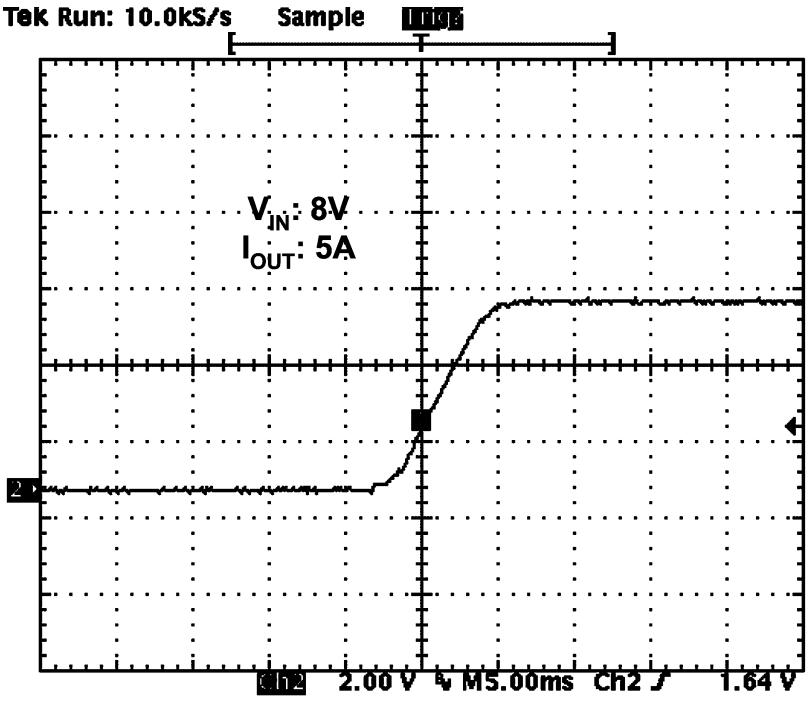


Figure 11. Startup

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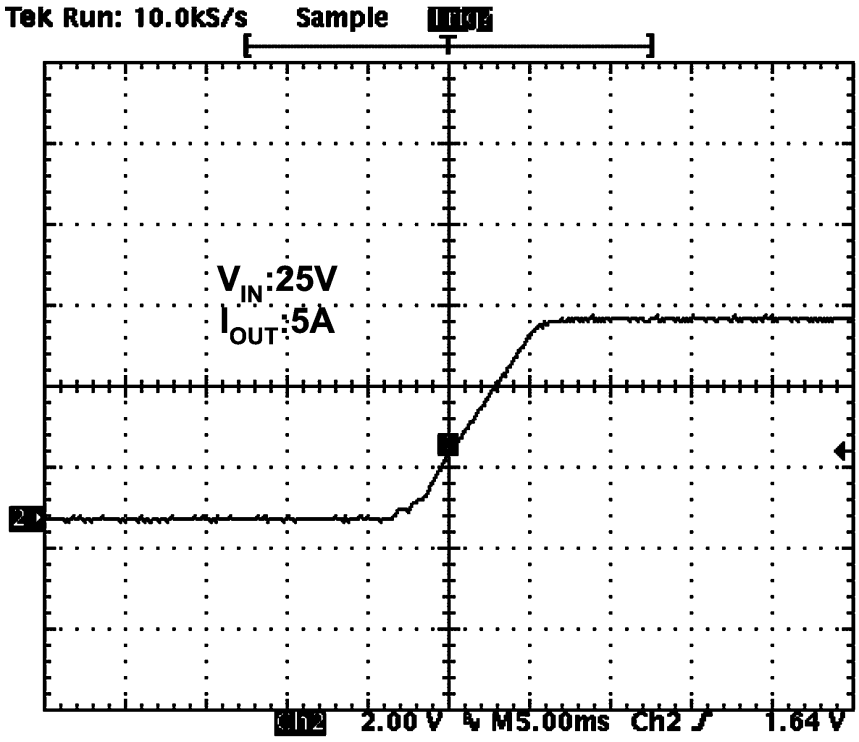


Figure 12. Startup

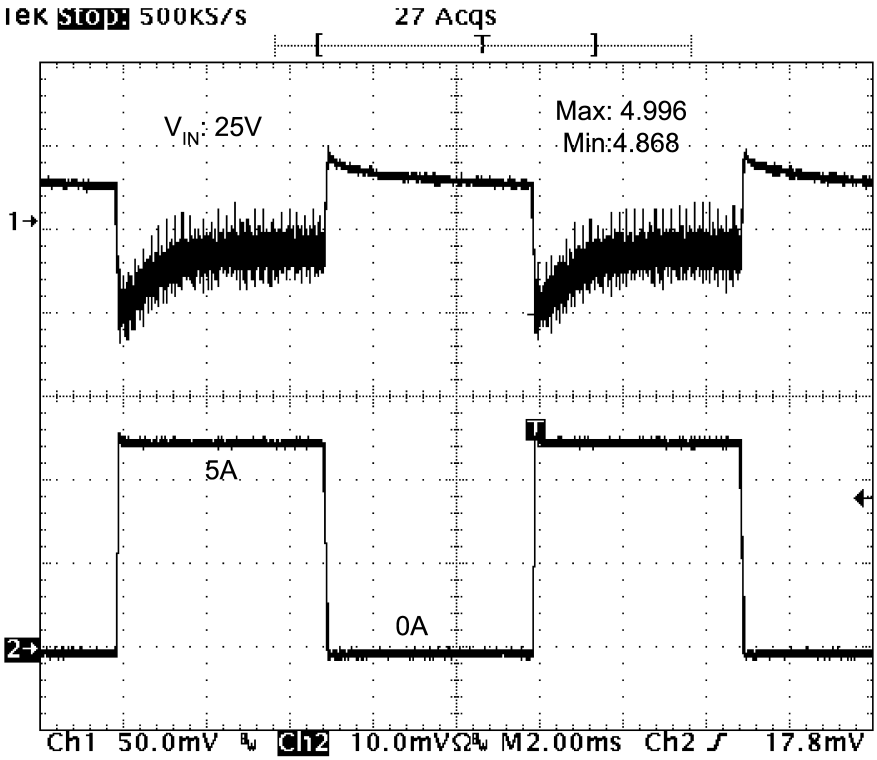


Figure 13. Load Transient Response

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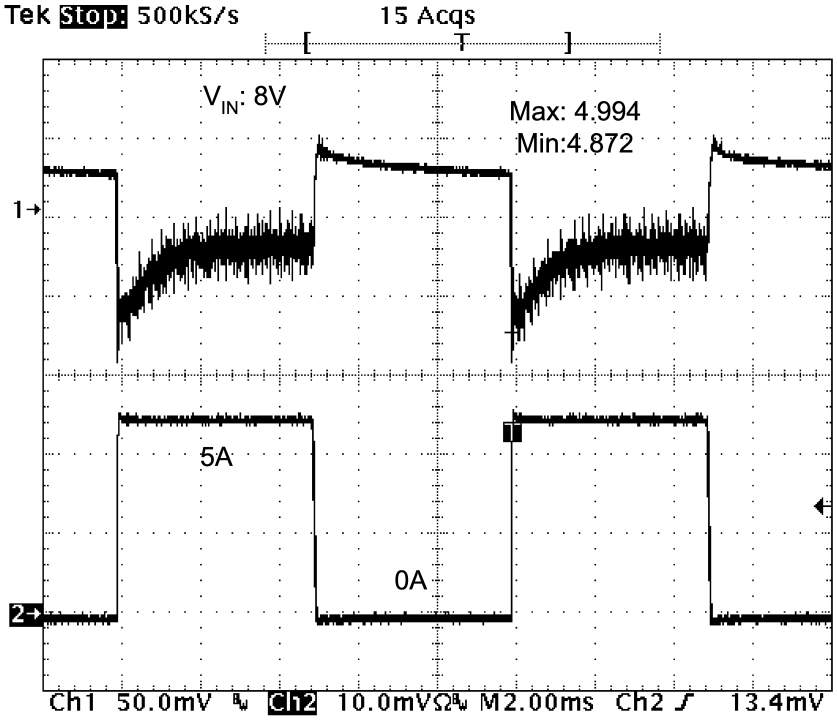


Figure 14. Load Transient Response

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