Dual 5 A, 20 V Synchronous Step-Down Regulator with Integrated High-Side MOSFET

Data Sheet **ADP2325**

FEATURES

- Input voltage: 4.5 V to 20 V
- ±1% output accuracy
- Integrated 48 mΩ typical high-side MOSFET
- Flexible output configuration
  - Dual output: 5 A/5 A
  - Parallel single output: 10 A
- Programmable switching frequency: 250 kHz to 1.2 MHz
- External synchronization input with programmable phase shift or internal clock output
- Selectable PWM or PFM mode operation
- Adjustable current limit for small inductors
- External compensation and soft start
- Startup into precharged output
- Supported by ADIsimPower™ design tool

APPLICATIONS

- Communications infrastructure
- Networking and servers
- Industrial and instrumentation
- Healthcare and medical
- Intermediate power rail conversion

TYPICAL APPLICATION CIRCUIT

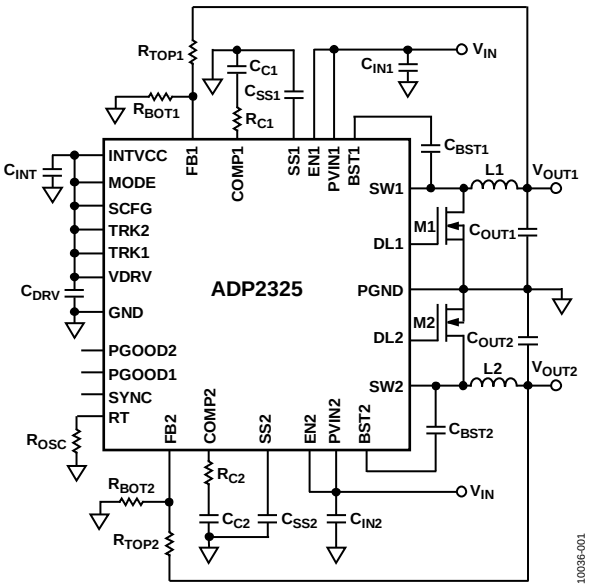

Figure 1.

GENERAL DESCRIPTION

The ADP2325 is a full featured, dual output, step-down dc-to-dc regulator based on a current mode architecture. The ADP2325 integrates two high-side power MOSFETs and two low-side drivers for the external N-channel MOSFETs. The two pulse-width modulation (PWM) channels can be configured to deliver dual 5 A outputs or a parallel-to-single 10 A output. The regulator operates from input voltages of 4.5 V to 20 V, and the output voltage can be as low as 0.6 V.

The switching frequency can be programmed from 250 kHz to 1.2 MHz, or it can be synchronized to an external clock to minimize interference in multirail applications. The dual PWM channels run 180° out of phase, thereby reducing input current ripple as well as reducing the size of the input capacitor.

The bidirectional synchronization pin can be programmed at a 60°, 90°, or 120° phase shift to provide for a stackable, multiphase power solution.

The ADP2325 can be configured to operate in pulse frequency modulation (PFM) mode at a light load for higher efficiency or in forced PWM mode for noise sensitive applications. External compensation and soft start provide design flexibility.

Independent enable inputs and power-good outputs provide reliable power sequencing. To enhance system reliability, the device includes undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection, and thermal shutdown.

The ADP2325 operates over the −40°C to +125°C junction temperature range and is available in a 32-lead LFCSP_WQ package.

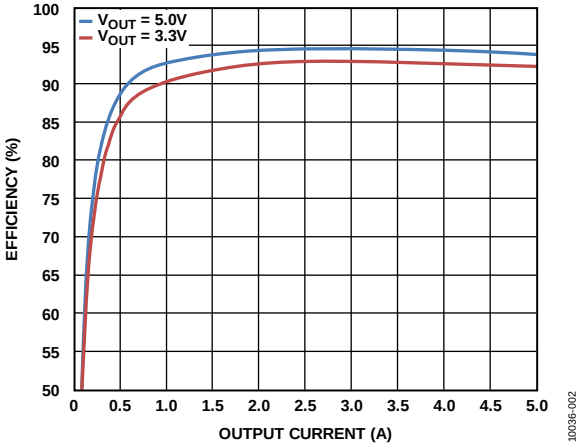

Figure 2. Efficiency vs. Output Current at V_{IN} = 12 V, f_{SW} = 600 kHz

Rev. A

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REVISION HISTORY

7/12—Rev. 0 to Rev. A

Added ADIsimPower Design Tool Section ... 20
Changes to Ordering Guide ... 32

2/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

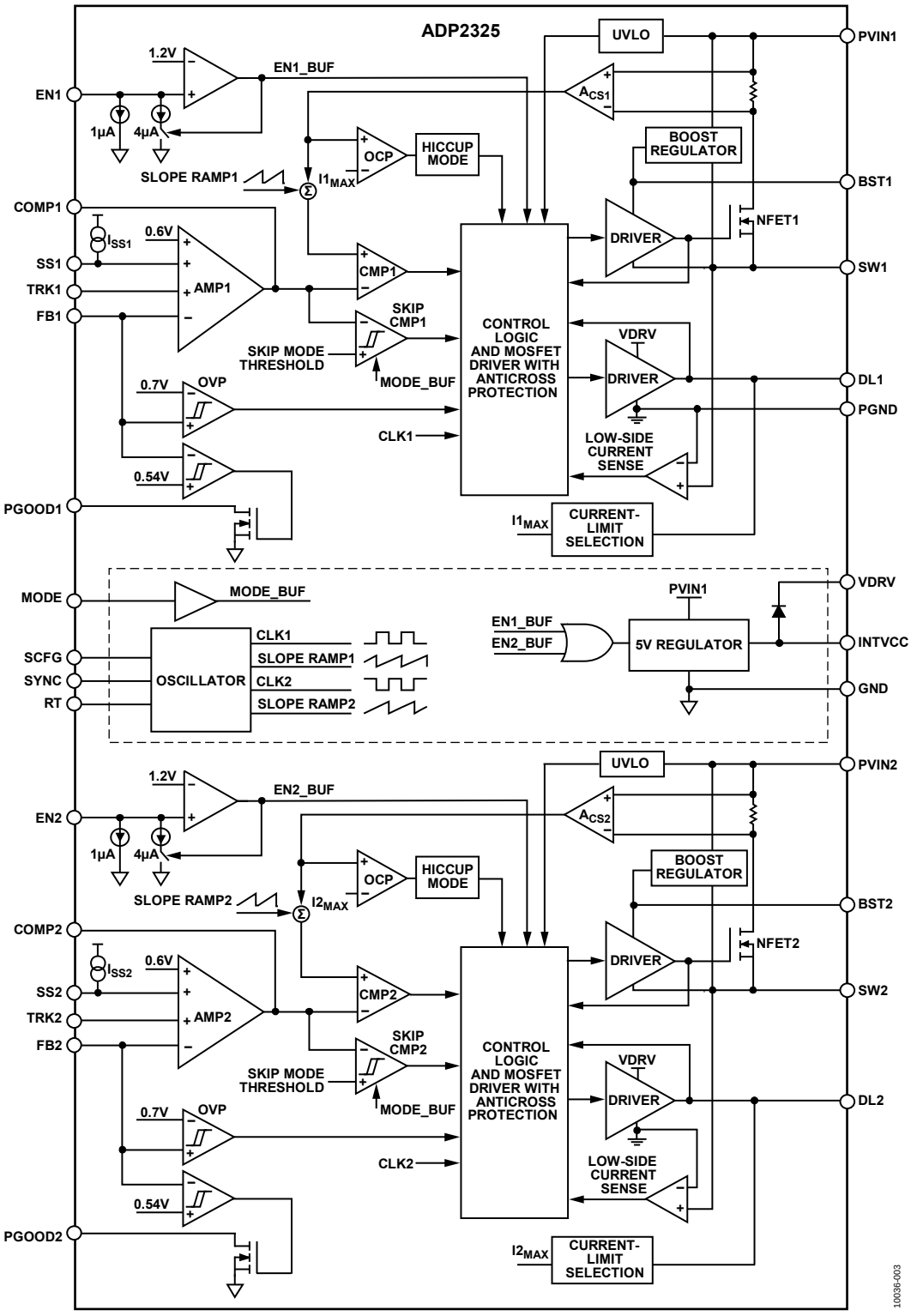

Figure 3.

SPECIFICATIONS

PVIN1 = PVIN2 = 12 V at T_J = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INPUT (PVINx PINS)						
Power Input Voltage Range	V_{PVIN}		4.5		20	V
Quiescent Current (PVIN1 + PVIN2)	I_Q	MODE = GND, no switching		3	5	mA
Shutdown Current (PVIN1 + PVIN2)	I_{SHDN}	EN1 = EN2 = GND		30	40	µA
PVINx Undervoltage Lockout Threshold	UVLO					
PVINx Rising				4.2	4.4	V
PVINx Falling			3.5	3.7		V
FEEDBACK (FBx PINS)						
FBx Regulation Voltage[1]	V_{FB}	PVINx = 4.5 V to 20 V	0.594	0.6	0.606	V
FBx Bias Current	I_{FB}			0.01	0.1	µA
ERROR AMPLIFIER (COMPx PINS)						
Transconductance	g_m		370	500	630	µS
Error Amplifier Source Current	I_{SOURCE}		40	65	90	µA
Error Amplifier Sink Current	I_{SINK}		45	65	85	µA
INTERNAL REGULATOR (INTVCC PIN)						
INTVCC Voltage			4.75	5	5.25	V
Dropout Voltage		I_{INTVCC} = 30 mA		300		mV
Regulator Current Limit			80	100	120	mA
SWITCH NODE (SWx PINS)						
High-Side On Resistance[2]		V_{BST} to V_{SW} = 5 V		48	80	mΩ
High-Side Peak Current Limit		R_{ILIM} = floating, V_{BST} to V_{SW} = 5 V	6.4	8	9.6	A
		R_{ILIM} = 47 kΩ, V_{BST} to V_{SW} = 5 V	3.4	4.8	6.2	A
Low-Side Negative Current-Limit Threshold Voltage[3]				50		mV
SWx Minimum On Time[3]	t_{MIN_ON}			130		ns
SWx Minimum Off Time[3]	t_{MIN_OFF}			150		ns
LOW-SIDE DRIVER (DLx PINS)						
Rising Time[3]	t_R	C_{DL} = 2.2 nF, see Figure 23		20		ns
Falling Time[3]	t_F	C_{DL} = 2.2 nF, see Figure 26		10		ns
Sourcing Resistor				4	6	Ω
Sinking Resistor				1.4	3	Ω
OSCILLATOR (RT PIN)						
PWM Switching Frequency	f_{SW}	R_{OSC} = 100 kΩ	510	600	690	kHz
PWM Frequency Range			250		1200	kHz
SYNCHRONIZATION (SYNC PIN)						
SYNC Input		SYNC configured as input				
Synchronization Range			300		1200	kHz
Minimum On Pulse Width			100			ns
Minimum Off Pulse Width			100			ns
High Threshold			1.3			V
Low Threshold					0.4	V
SYNC Output		SYNC configured as output				
Frequency on SYNC Pin	f_{CLKOUT}			f_{SW}		kHz
Positive Pulse Time			100			ns
SOFT START (SSx PINS)						
SSx Pin Source Current	I_{SS}		2.5	3.5	4.5	µA

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TRACKING INPUT (TRKx PINS)						
TRKx Input Voltage Range			0		600	mV
TRKx-to-FBx Offset Voltage		TRKx = 0 mV to 500 mV	−12		+12	mV
TRKx Input Bias Current					100	nA
POWER GOOD (PGOODx PINS)						
Power-Good Rising Threshold			87	90	93	%
Power-Good Hysteresis				5		%
Power-Good Deglitch Time		From FBx to PGOODx		16		Clock cycles
PGOODx Leakage Current		V_{PGOOD} = 5 V		0.1	1	µA
PGOODx Output Low Voltage		I_{PGOOD} = 1 mA		50	100	mV
ENABLE (ENx PINS)						
ENx Rising Threshold				1.2	1.28	V
ENx Falling Threshold			1.02	1.1		V
ENx Source Current		EN voltage below falling threshold		5		µA
		EN voltage above rising threshold		1		µA
MODE (MODE PIN)						
Input High Voltage			1.3			V
Input Low Voltage					0.4	V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis				15		°C

[1] Tested in a feedback loop that adjusts V_{FB} to achieve a specified voltage on the COMPx pin.
[2] Pin-to-pin measurements.
[3] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN1, PVIN2, EN1, EN2	−0.3 V to +22 V
SW1, SW2	−1 V to +22 V
BST1, BST2	V_{SW} + 6 V
FB1, FB2, SS1, SS2, COMP1, COMP2, PGOOD1, PGOOD2, TRK1, TRK2, SCFG, SYNC, RT, MODE	−0.3 V to +6 V
INTVCC, VDRV, DL1, DL2	−0.3 V to +6 V
PGND to GND	−0.3 V to +0.3 V
Temperature Range	
Operating (Junction)	−40°C to +125°C
Storage	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Boundary Condition

θ_{JA} is measured using natural convection on a JEDEC 4-layer board, and the exposed pad is soldered to the printed circuit board (PCB) with thermal vias.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
32-Lead LFCSP_WQ	32.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

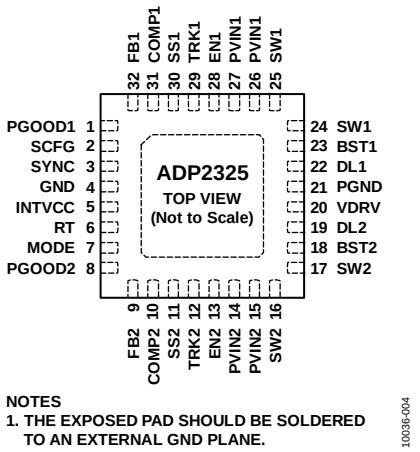

Figure 4. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PGOOD1	Power-Good Output (Open Drain) for Channel 1. A pull-up resistor of 10 kΩ to 100 kΩ is recommended.
2	SCFG	Synchronization Configuration Input. The SCFG pin configures the SYNC pin as an input or an output. Connect SCFG to INTVCC to configure SYNC as an output. Connecting a pull-down resistor to GND configures SYNC as an input with various phase shift degrees.
3	SYNC	Synchronization. This pin can be configured as an input or an output. When configured as an output, it provides a clock at the switching frequency. When configured as an input, this pin accepts an external clock to which the regulators are synchronized. The phase shift is configured by SCFG. Note that when SYNC is configured as an input, the PFM mode is disabled and the device works in continuous conduction mode (CCM) only.
4	GND	Analog Ground. Connect to the ground plane.
5	INTVCC	Internal 5 V Regulator Output. The IC control circuits are powered from this voltage. Place a 1 µF ceramic capacitor between INTVCC and GND.
6	RT	Connect a resistor between RT and GND to program the switching frequency from 250 kHz to 1.2 MHz.
7	MODE	Mode Selection. When this pin is connected to INTVCC, the PFM mode is disabled and the regulator works only in CCM. When this pin is connected to ground, the PFM mode is enabled. If the low-side device is a diode, the MODE pin must be connected to ground.
8	PGOOD2	Power-Good Output (Open Drain) for Channel 2. A pull-up resistor of 10 kΩ to 100 kΩ is recommended.
9	FB2	Feedback Voltage Sense Input for Channel 2. Connect FB2 to a resistor divider from the Channel 2 output voltage, V_{OUT2}. Connect FB2 to INTVCC for parallel applications.
10	COMP2	Error Amplifier Output for Channel 2. Connect an RC network from COMP2 to GND. Connect COMP1 and COMP2 together for parallel applications.
11	SS2	Soft Start Control for Channel 2. To program the soft start time, connect a capacitor from SS2 to GND. For parallel applications, SS2 remains open.
12	TRK2	Tracking Input for Channel 2. To track a master voltage, connect this pin to a resistor divider from the master voltage. If the tracking function is not used, connect TRK2 to INTVCC.
13	EN2	Enable Pin for Channel 2. An external resistor divider can be used to set the turn-on threshold. When not using the enable pin, connect EN2 to PVIN2.
14, 15	PVIN2	Power Input for Channel 2. Connect PVIN2 to the input power source, and connect a bypass capacitor between PVIN2 and ground.
16, 17	SW2	Switch Node for Channel 2.
18	BST2	Supply Rail for the Gate Drive of Channel 2. Place a 0.1 µF capacitor between SW2 and BST2.
19	DL2	Low-Side Gate Driver Output for Channel 2. Connect a resistor between DL2 and PGND to program the current-limit threshold of Channel 2.
20	VDRV	Low-Side Driver Supply Input. Connect VDRV to INTVCC. Place a 1 µF ceramic capacitor between the VDRV pin and PGND.
21	PGND	Driver Power Ground. Connect to the source of the synchronous N-channel MOSFET.
22	DL1	Low-Side Gate Driver Output for Channel 1. Connect a resistor between DL1 and PGND to program the current-limit threshold of Channel 1.
23	BST1	Supply Rail for the Gate Drive of Channel 1. Place a 0.1 µF capacitor between SW1 and BST1.

Pin No.	Mnemonic	Description
24, 25	SW1	Switch Node for Channel 1.
26, 27	PVIN1	Power Input for Channel 1. These pins are the power inputs for Channel 1 and provide power for the internal regulator. Connect to the input power source and connect a bypass capacitor between PVIN1 and ground.
28	EN1	Enable Pin for Channel 1. An external resistor divider can be used to set the turn-on threshold. When not using the enable pin, connect EN1 to PVIN1.
29	TRK1	Tracking Input for Channel 1. To track a master voltage, connect this pin to a resistor divider from the master voltage. If the tracking function is not used, connect TRK1 to INTVCC.
30	SS1	Soft Start Control for Channel 1. To program the soft start time, connect a capacitor from SS1 to GND.
31	COMP1	Error Amplifier Output for Channel 1. Connect an RC network from COMP1 to GND. Connect COMP1 and COMP2 together for parallel applications.
32	FB1	Feedback Voltage Sense Input for Channel 1. Connect FB1 to a resistor divider from the Channel 1 output voltage, V_{OUT1}.
N/A[1]	EP	Exposed Pad. Solder the exposed pad to an external GND plane.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 2.2 µH, C_{OUT} = 2 × 100 µF, f_{SW} = 600 kHz, unless otherwise noted.

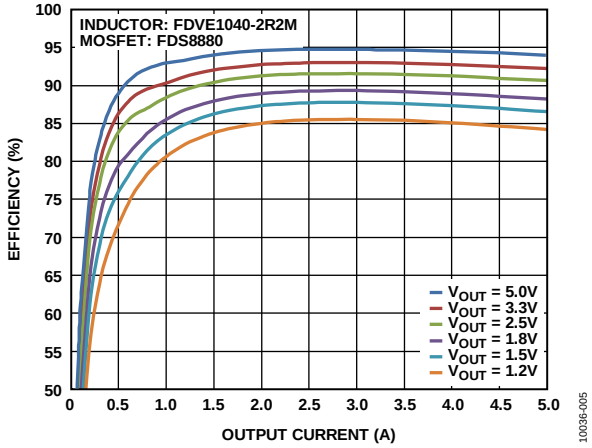

Figure 5. Efficiency at V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM

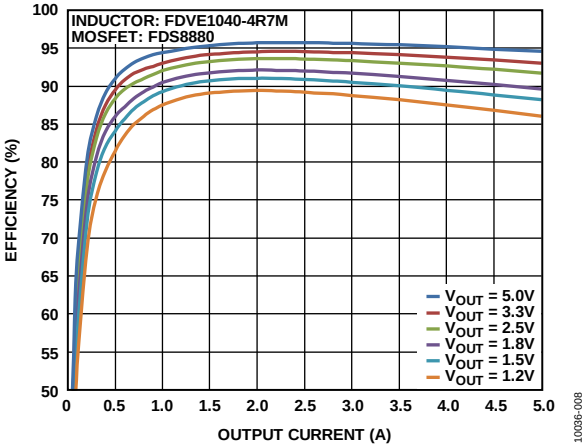

Figure 8. Efficiency at V_{IN} = 12 V, f_{SW} = 300 kHz, FPWM

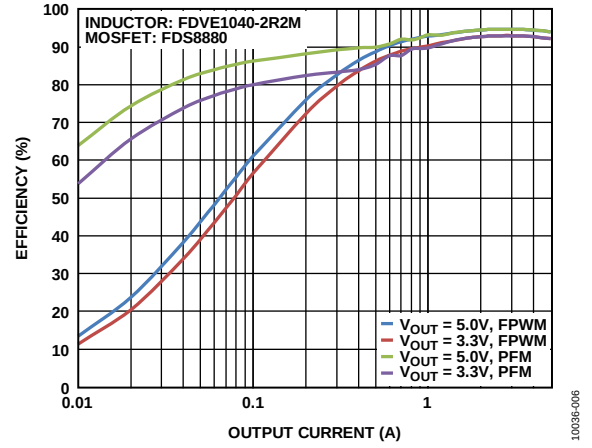

Figure 6. Efficiency at V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and PFM

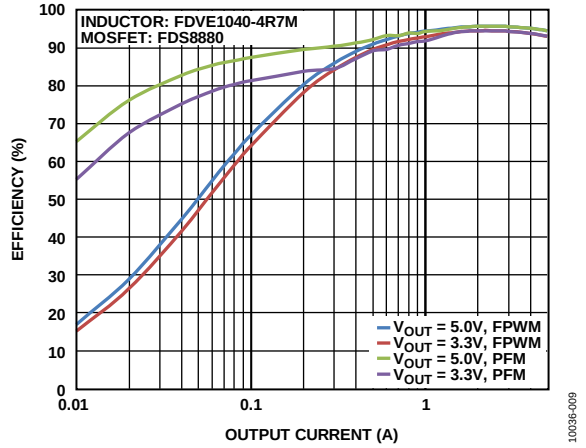

Figure 9. Efficiency at V_{IN} = 12 V, f_{SW} = 300 kHz, FPWM and PFM

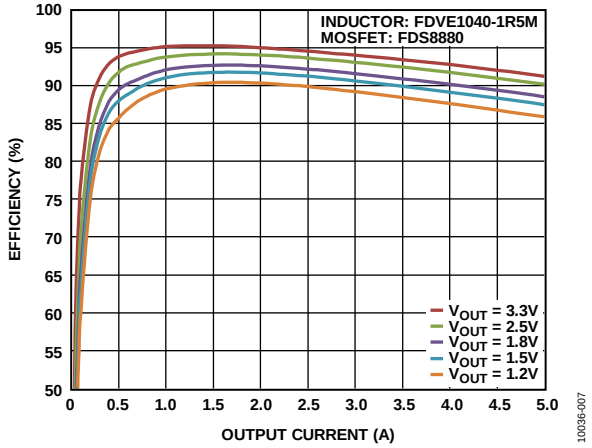

Figure 7. Efficiency at V_{IN} = 5 V, f_{SW} = 600 kHz, FPWM

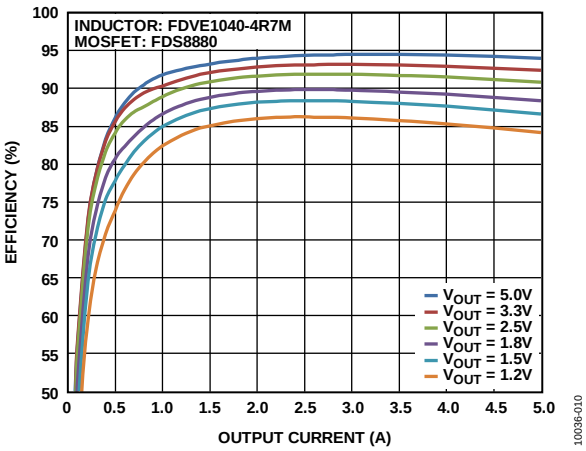

Figure 10. Efficiency at V_{IN} = 18 V, f_{SW} = 300 kHz, FPWM

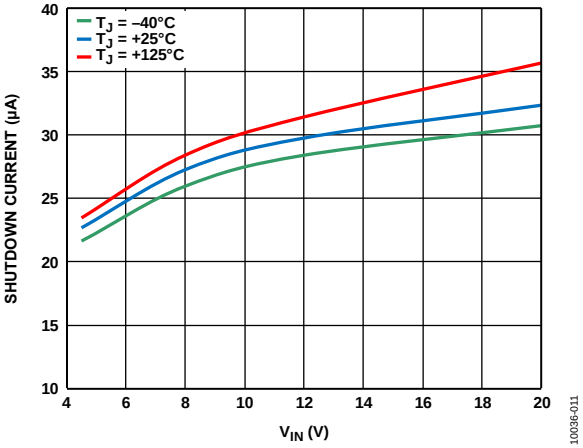

Figure 11. Shutdown Current vs. V_{IN}

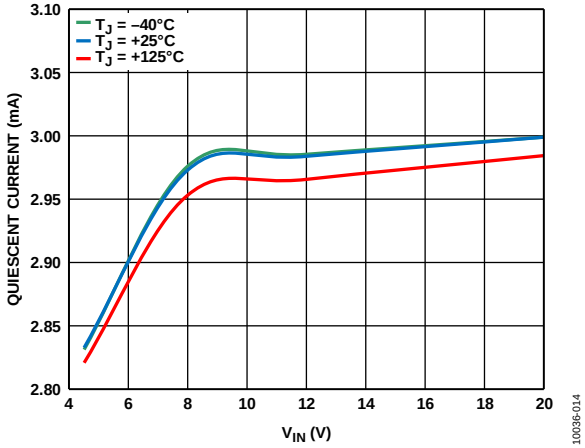

Figure 14. Quiescent Current vs. V_{IN}

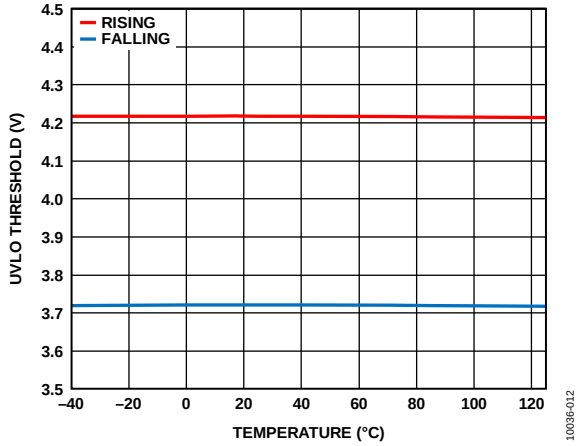

Figure 12. UVLO Threshold vs. Temperature

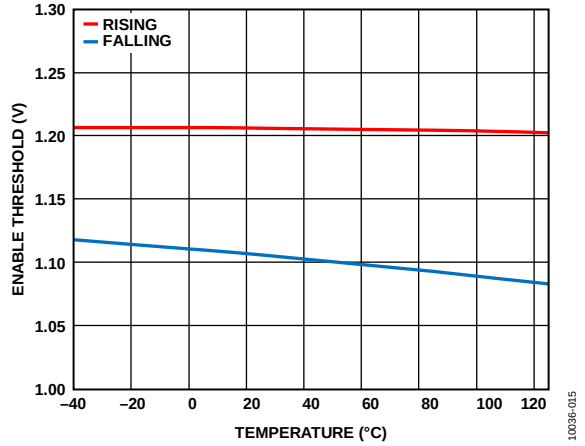

Figure 15. EN Threshold vs. Temperature

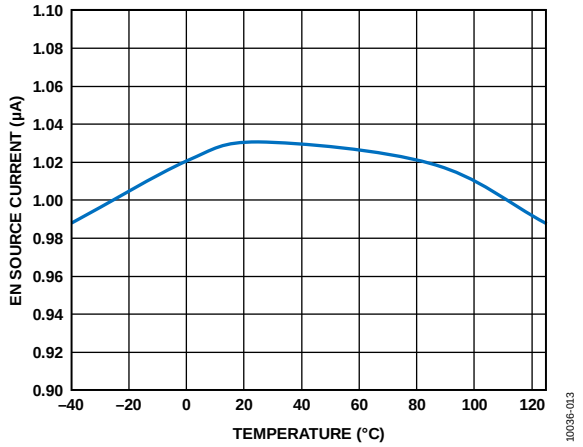

Figure 13. EN Source Current vs. Temperature at V_{EN} = 1.5 V

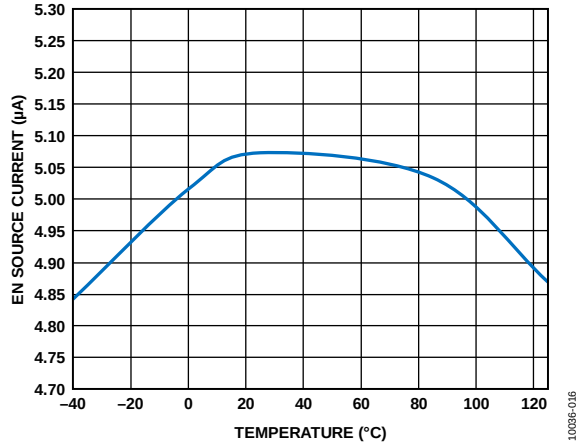

Figure 16. EN Source Current vs. Temperature at V_{EN} = 1 V

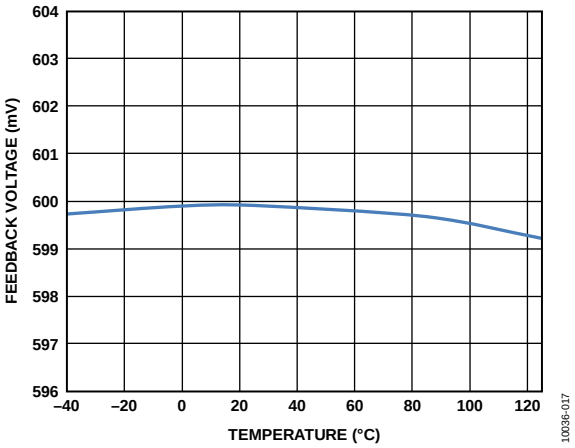

Figure 17. Feedback Voltage vs. Temperature

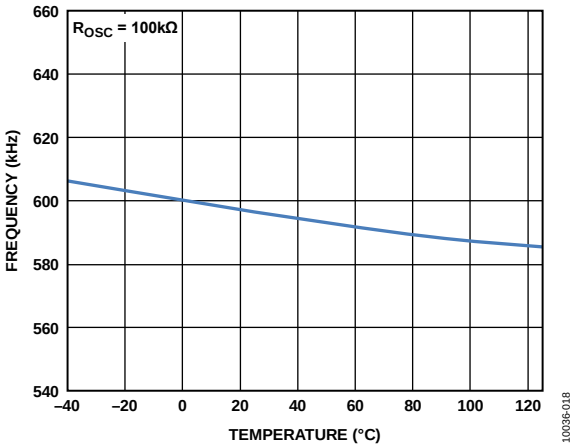

Figure 18. Frequency vs. Temperature

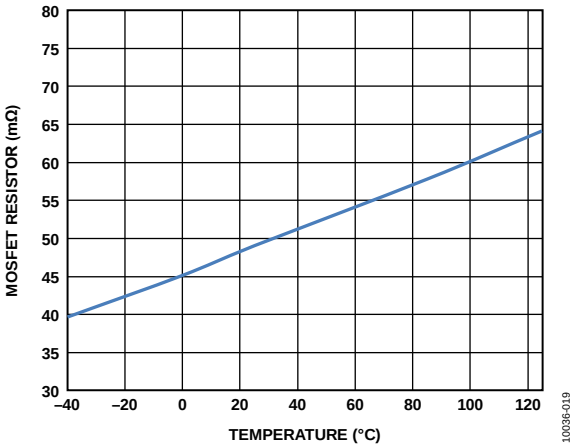

Figure 19. MOSFET R_{DSON} vs. Temperature

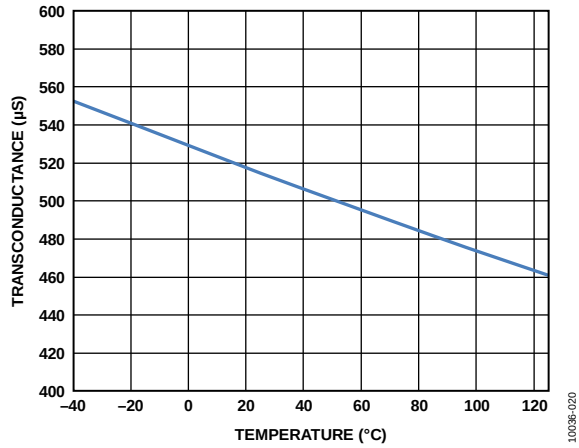

Figure 20. Transconductance (g_m) vs. Temperature

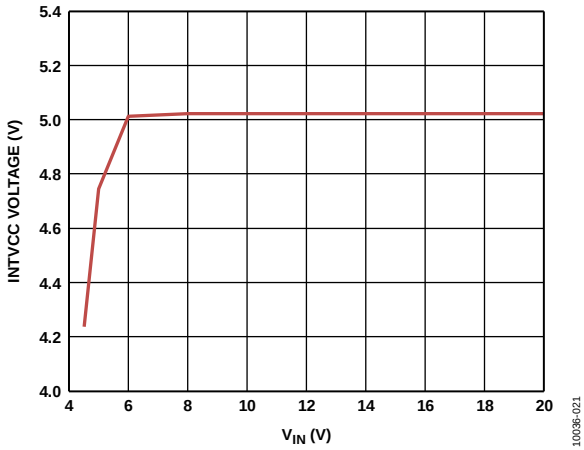

Figure 21. INTVCC Voltage vs. V_{IN}

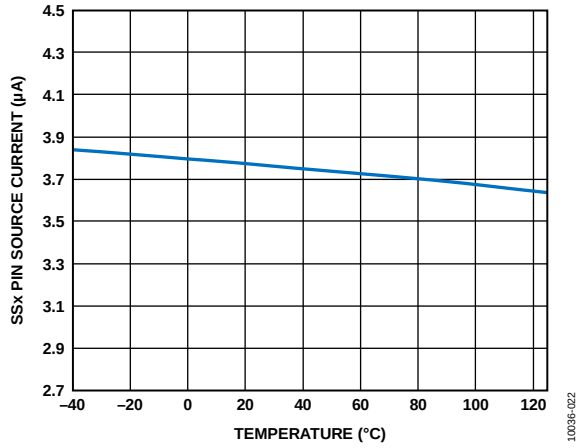

Figure 22. SSx Pin Source Current vs. Temperature

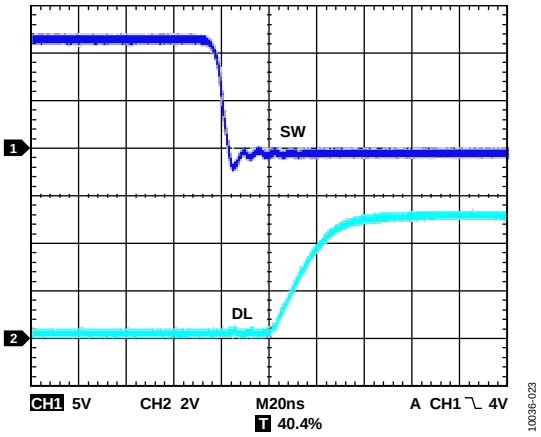

Figure 23. Low-Side Driver Rising Edge Waveform, C_{DL} = 2.2 nF

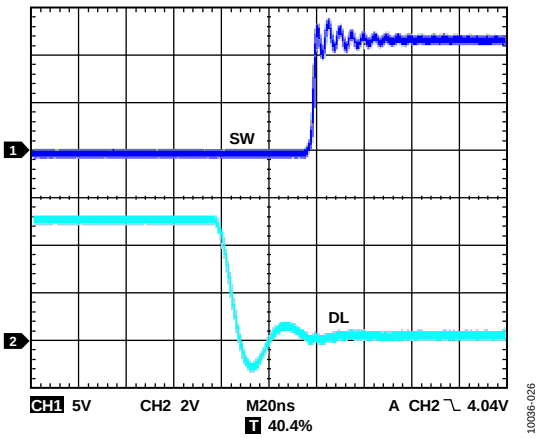

Figure 26. Low-Side Driver Falling Edge Waveform, C_{DL} = 2.2 nF

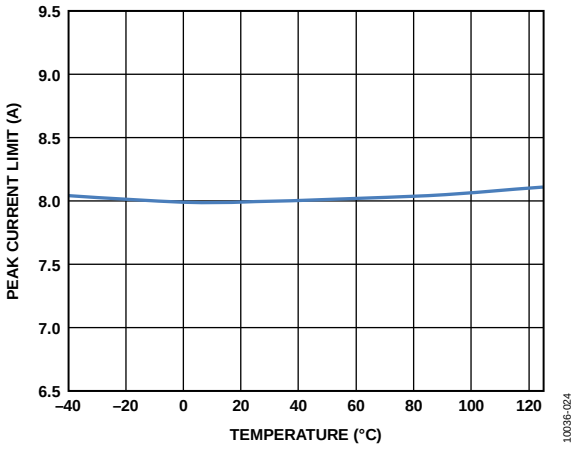

Figure 24. Peak Current-Limit Threshold vs. Temperature, R_{ILIM} = Floating

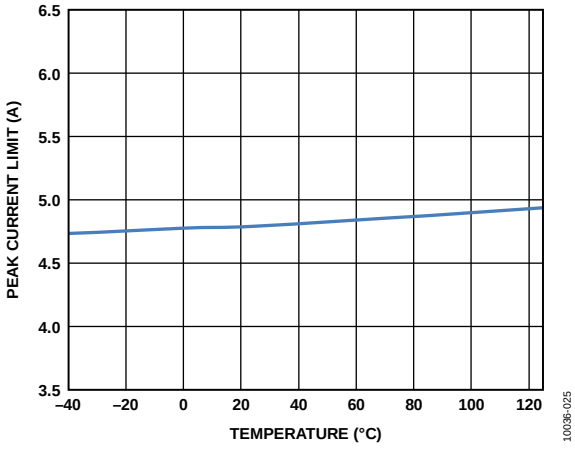

Figure 27. Peak Current-Limit Threshold vs. Temperature, R_{ILIM} = 47 kΩ

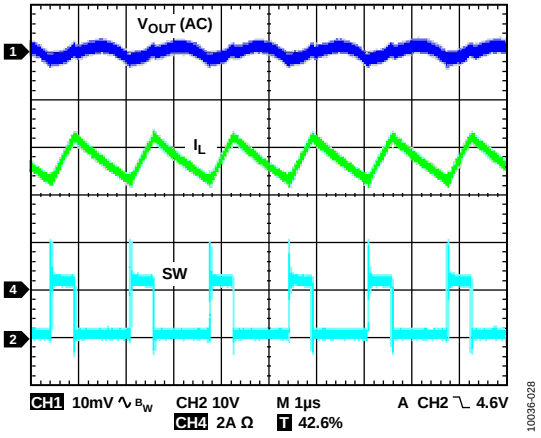

Figure 25. Continuous Conduction Mode (CCM)

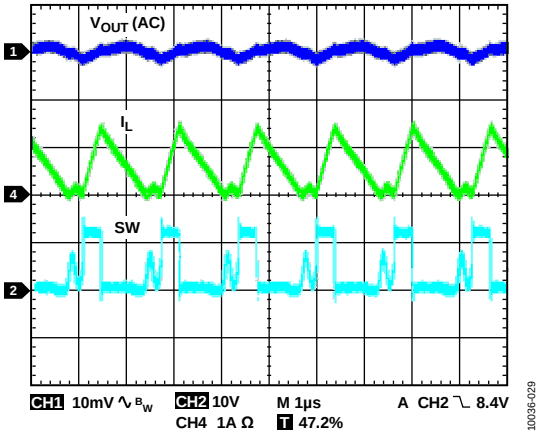

Figure 28. Discontinuous Conduction Mode (DCM)

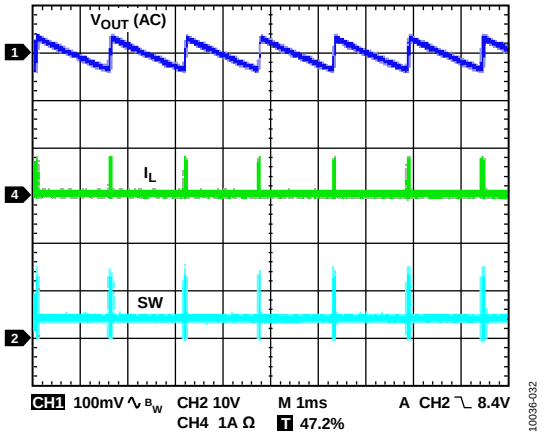

Figure 29. Power Saving Mode

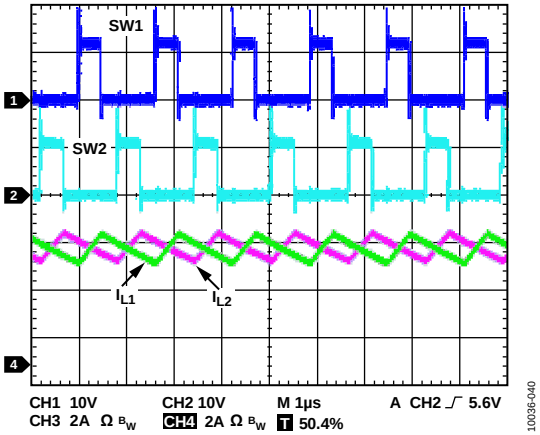

Figure 32. Dual Phase, Single Output, V_{OUT} = 3.3 V, I_{OUT} = 10 A

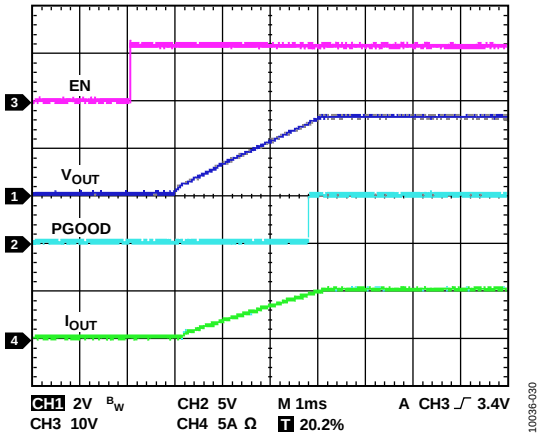

Figure 30. Soft Start with Full Load

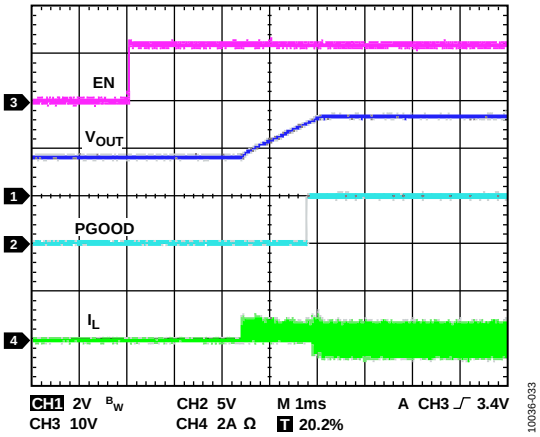

Figure 33. Soft Start with Precharged Output

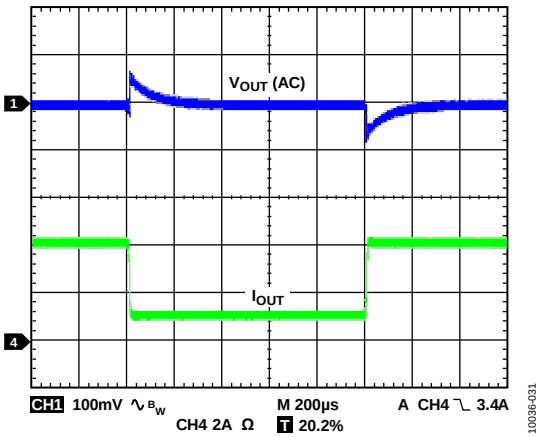

Figure 31. Load Transient Response, 1 A to 4 A

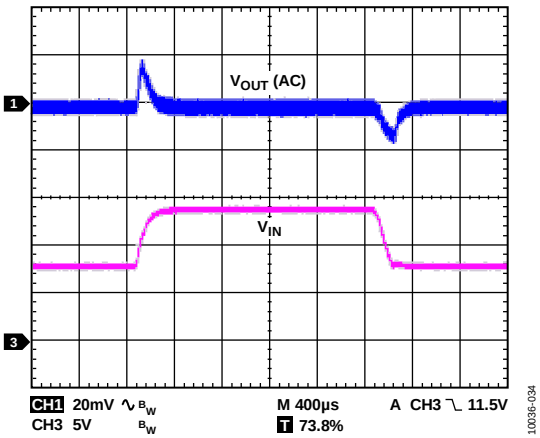

Figure 34. Line Transient Response, V_{IN} from 8 V to 14 V, I_{OUT} = 5 A

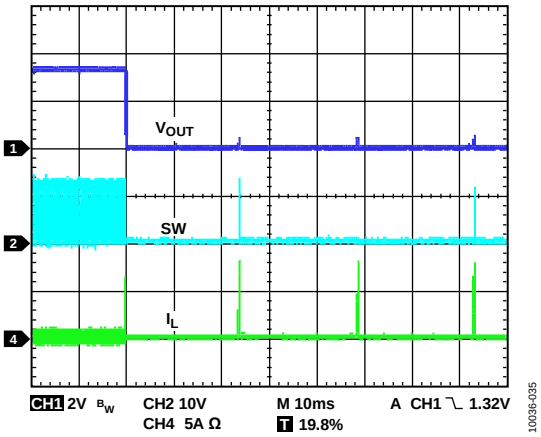

Figure 35. Output Short

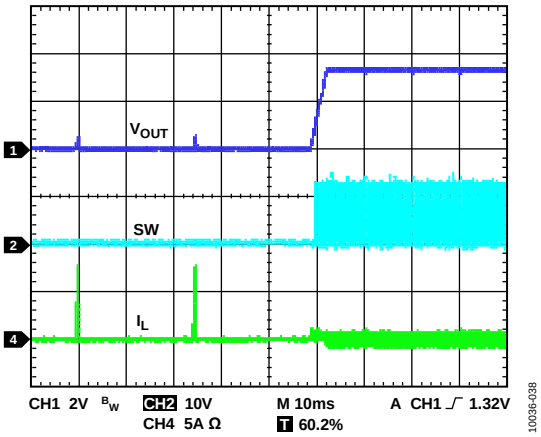

Figure 38. Output Short Recovery

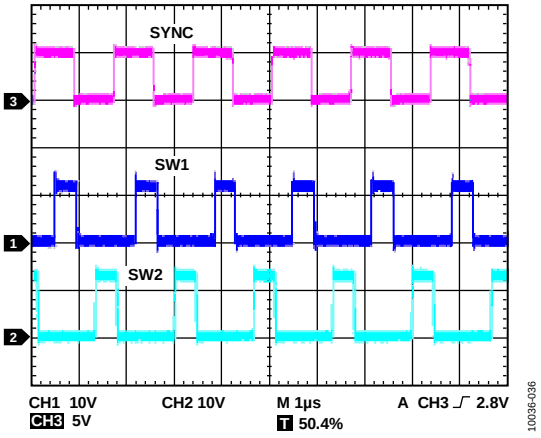

Figure 36. External Synchronization with 60° Phase Shift

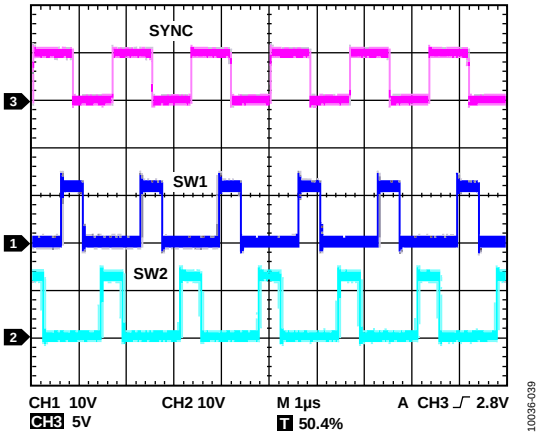

Figure 39. External Synchronization with 90° Phase Shift

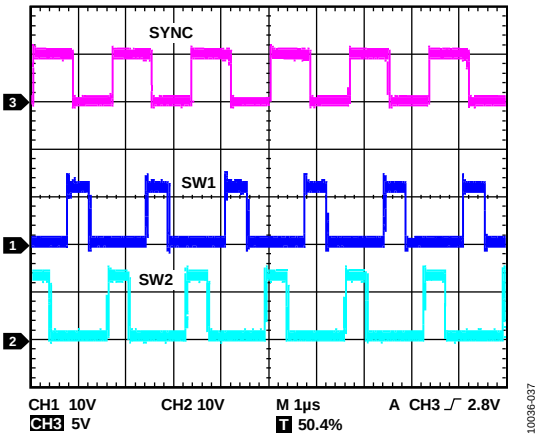

Figure 37. External Synchronization with 120° Phase Shift

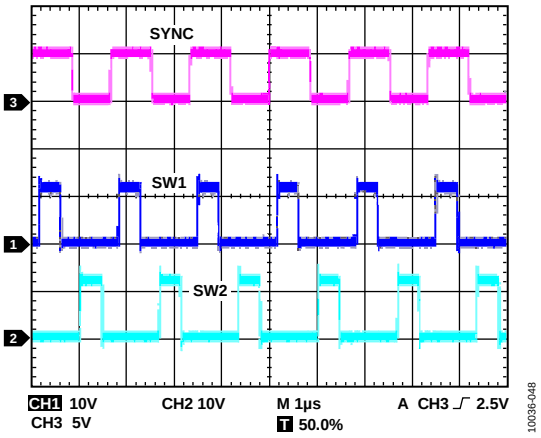

Figure 40. SYNC Pin Configured as Output

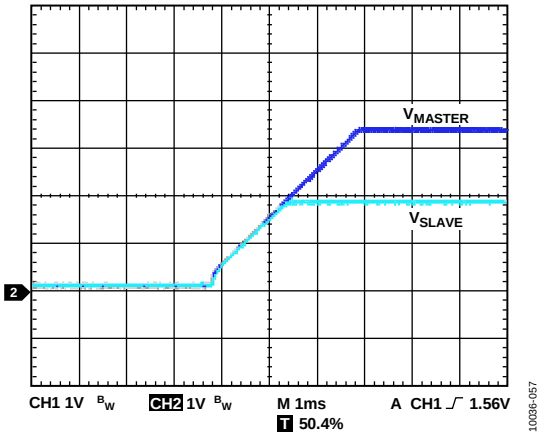

Figure 41. Coincident Tracking

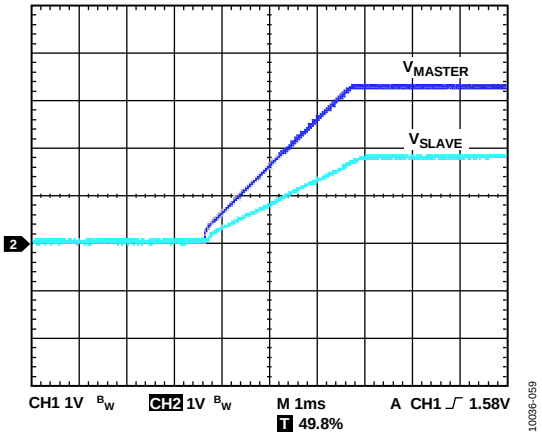

Figure 43. Ratiometric Tracking

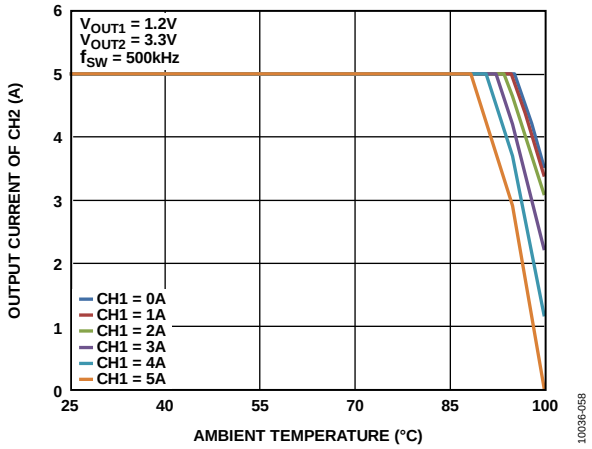

Figure 42. Thermal Derating Performance at 110°C Case Temperature Based on ADP2325-EVALZ Board

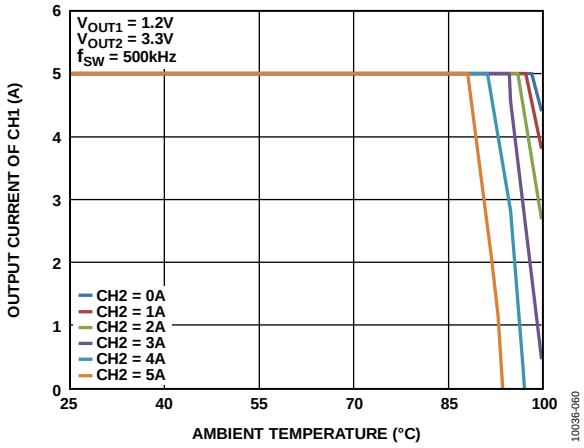

Figure 44. Thermal Derating Performance at 110°C Case Temperature Based on ADP2325-EVALZ Board

THEORY OF OPERATION

The ADP2325 is a full featured, dual output, step-down dc-to-dc regulator based on a current mode architecture. It integrates two high-side power MOSFETs and two low-side drivers for external MOSFETs. The ADP2325 is designed for high performance applications that require high efficiency and design flexibility.

The ADP2325 can operate with an input voltage from 4.5 V to 20 V and can regulate the output voltage to as low as 0.6 V. Additional features for flexible design include programmable switching frequency, programmable soft start, external compensation, independent enable inputs, and power-good outputs.

CONTROL SCHEME

The ADP2325 uses a fixed frequency, current mode PWM control architecture during medium to full loads, but shifts to a power save mode (PFM) at light loads when the PFM mode is enabled. The power save mode reduces switching losses and boosts efficiency under light loads.

When operating in the fixed frequency PWM mode, the duty cycle of the integrated N-channel MOSFET (referred to interchangeably as NFET or MOSFET) is adjusted, this, in turn, regulates the output voltage. When the device operates in power save mode, the switching frequency is adjusted to regulate the output voltage.

PWM MODE

In PWM mode, the ADP2325 operates at a fixed frequency set by an external resistor. At the start of each oscillator cycle, the high-side NFET turns on, placing a positive voltage across the inductor. The inductor current increases until the current sense signal crosses the peak inductor current threshold, turning off the high-side NFET and turning on the low-side NFET (diode). This places a negative voltage across the inductor, causing a reduction in the inductor current. The low-side NFET (diode) stays on for the remainder of the cycle or until the inductor current reaches zero.

PFM MODE

To enable the PFM mode, pull the MODE pin to ground. When the COMPx voltage is below the PFM threshold voltage, the device enters the PFM mode.

When the device enters the PFM mode, it monitors the FBx voltage to regulate the output voltage. Because the high-side and low-side NFETs are turned off, the load current discharges the output capacitor causing the output voltage to drop. When the FBx voltage drops below 0.605 V, the device starts switching and the output voltage increases as the output capacitor is charged by the inductor current. When the FBx voltage exceeds 0.62 V, the device turns off both the high-side and low-side NFETs until the FBx voltage drops to 0.605 V. In the PFM mode, the output voltage ripple is larger than the ripple in the PWM mode.

PRECISION ENABLE/SHUTDOWN

The ADP2325 has two independent enable pins (EN1 and EN2), one for each channel. The ENx pin has an internal pull-down current source of 5 µA to provide a default turn-off whenever an ENx pin is open.

When the voltage on the EN1 or EN2 pin exceeds 1.2 V (typical), Channel 1 (per the EN1 pin) or Channel 2 (per the EN2 pin) is enabled and the internal pull-down current source at the EN1 or EN2 pin is reduced to 1 µA, which allows the user to program the UVLO lockout of the input voltage.

When the voltage on the EN1 or EN2 pin drops below 1.1 V (typical), Channel 1 or Channel 2 turns off. When EN1 and EN2 are both below 1.1 V, all of the internal circuits turn off and the device enters the shutdown mode.

SEPARATE INPUT VOLTAGES

The ADP2325 supports two separate input voltages. This means that the PVIN1 and PVIN2 voltages can be connected to two different supply voltages. In these types of applications, because the PVIN1 voltage provides the power supply for the internal regulator and control circuitry, the PVIN1 voltage must be above the UVLO voltage before the PVIN2 voltage begins to rise.

This feature allows for a cascading supply operation, as shown in Figure 45 where PVIN2 is sourced from the Channel 1 output. In this configuration, the Channel 1 output voltage needs to be high enough to maintain Channel 2 in regulation, and the Channel 1 output voltage must be higher than the input voltage UVLO threshold.

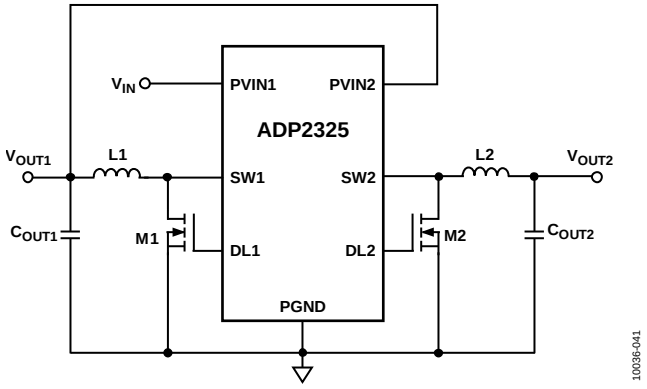

Figure 45. Cascading Supply Operation

INTERNAL REGULATOR (INTVCC)

The internal regulator provides a stable voltage supply for the internal control circuits and a bias voltage for the low-side gate drivers. It is recommended that a 1 µF ceramic capacitor be placed between INTVCC and GND. The internal regulator also includes a current-limit circuit for protection.

The internal regulator is active when either of the channels is enabled. The PVIN1 pin provides power for the internal regulator, which is used by both channels.

BOOTSTRAP CIRCUITRY

The ADP2325 integrates the boot regulators to provide the gate drive voltage for the high-side NFETs. The regulators generate 5 V bootstrap voltages between the BSTx and the SWx pins.

It is recommended that an X7R or X5R, 0.1 µF ceramic capacitor be placed between the BSTx and the SWx pins.

LOW-SIDE DRIVER

The DLx pin provides the gate drive for the low-side N-channel MOSFET. Internal circuitry monitors the gate driver signal to ensure break-before-make switching to prevent crossconduction.

The VDRV pin provides the power supply to the low-side drivers. It is limited to a 5.5 V maximum input; placing a 1 µF ceramic capacitor close to this pin is recommended.

OSCILLATOR

A resistor from RT to GND programs the switching frequency according to the following equation:

$$f_{SW}\,[\text{kHz}] = \frac{60{,}000}{R_{OSC}[\text{k}\Omega]}$$

A 200 kΩ resistor sets the frequency to 300 kHz, and a 100 kΩ resistor sets the frequency to 600 kHz. Figure 46 shows the typical relationship between f_{SW} and R_{OSC}.

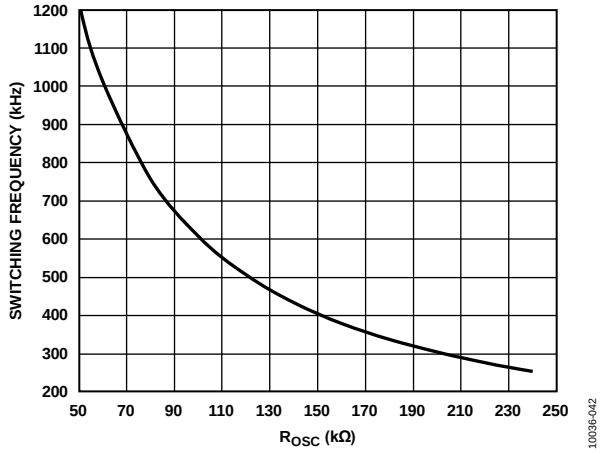

Figure 46. f_{SW} vs. R_{OSC}

SYNCHRONIZATION

The SYNC pin can be configured as an input or an output by setting the SCFG pin, as shown in Table 5.

Table 5. SCFG Configuration

SCFG	SYNC	Phase Shift
INTVCC	Output	0°
GND	Input	90°
180 kΩ to GND	Input	120°
100 kΩ to GND	Input	60°

When the SYNC pin is configured as an output, it generates a clock with a frequency that is equal to the internal switching frequency.

When the SYNC pin is configured as an input, the ADP2325 synchronizes to the external clock that is applied to the SYNC pin, and the internal clock must be programmed lower than the external clock. The phase shift can be programmed by the SCFG pin.

When working in synchronization mode, the ADP2325 disables the PFM mode and works only in the CCM mode.

SOFT START

Use the SSx pins to program the soft start time. Place a capacitor between SSx and GND; an internal current charges this capacitor to establish the soft start ramp. The soft start time can be calculated using the following equation:

$$t_{SS} = \frac{0.6\ \text{V} \times C_{SS}}{I_{SS}}$$

where:
C_{SS} is the soft start capacitance.
I_{SS} is the soft start pull-up current (3.5 µA).

If the output voltage is precharged prior to power-up, the ADP2325 prevents the low-side MOSFET from turning on until the soft start voltage exceeds the voltage on the FBx pin.

During soft start, the ADP2325 uses frequency foldback to prevent output current runaway. The switching frequency is reduced according to the voltage present at the FBx pin, which allows more time for the inductor to discharge. The correlation between the switching frequency and the FBx pin voltage is listed in Table 6.

Table 6. FBx Pin Voltage and Switching Frequency

FBx Pin Voltage	Switching Frequency
$V_{FB} \geq 0.4$ V	f_{SW}
0.4 V > $V_{FB} \geq 0.2$ V	1/2 f_{SW}
$V_{FB} < 0.2$ V	1/4 f_{SW}

PEAK CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2325 uses a peak current-limit protection circuit to prevent current runaway. Place a resistor between DLx and PGND to program the peak current-limit value, as listed in Table 7. The programmable peak current-limit threshold feature allows for the use of a small size inductor for low current applications.

Table 7. Peak Current-Limit Threshold Setting

R_{ILIM}	Peak Current-Limit Threshold
Floating	8 A
47 kΩ	4.8 A

The ADP2325 uses hiccup mode for overcurrent protection. When the peak inductor current reaches the current-limit threshold, the high-side MOSFET turns off and the low-side driver turns on until the next cycle while the overcurrent counter is incremented.

If the overcurrent counter reaches 10, or if the FBx pin voltage falls to 0.2 V after the soft start, the device enters hiccup mode. During this mode, the high-side MOSFET and low-side driver are both turned off. The device remains in this mode for seven soft start cycles and then attempts to restart from soft start. If the current-limit fault is cleared, the device resumes normal operation; otherwise, it reenters hiccup mode.

The ADP2325 provides a negative current limit. When the low-side FET voltage exceeds the negative current-limit threshold voltage (50 mV typical), the low-side FET turns off immediately for the remainder of this cycle. Both the high-side and low-side FETs turn off until the next cycle.

In some cases, the input voltage (PVIN) ramp rate is too slow or the output capacitor is too large to support the set regulation voltage during the soft start, causing the device to enter the hiccup mode. To prevent such cases, use a resistor divider at the ENx pin to program the UVLO of the input voltage or use a longer soft start time.

VOLTAGE TRACKING

The ADP2325 has a tracking input, TRKx, that allows the output voltage to track an external (master) voltage. Voltage tracking allows power sequencing applicable for FPGAs, DSPs, and ASICs, which may require a power sequence between the core and the I/O voltages.

The internal error amplifier includes three positive inputs: the internal reference voltage, the soft start voltage, and the tracking input voltage. The error amplifier regulates the feedback voltage to the lowest of the three voltages. To track a master voltage, connect the TRKx pin to a resistor divider from the master voltage, as shown in Figure 47.

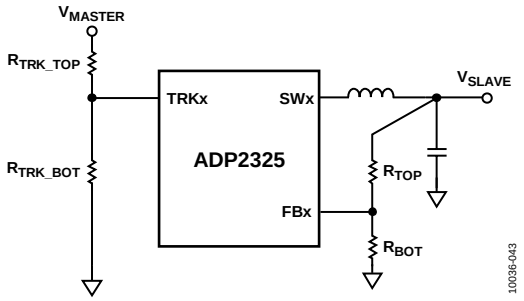

Figure 47. Voltage Tracking

Coincident Tracking

A common application is coincident tracking, which is shown in Figure 48. Coincident tracking limits the slave output voltage to be the same as the master voltage until it reaches regulation. To enable coincident tracking, set $R_{TRK_TOP} = R_{TOP}$ and $R_{TRK_BOT} = R_{BOT}$.

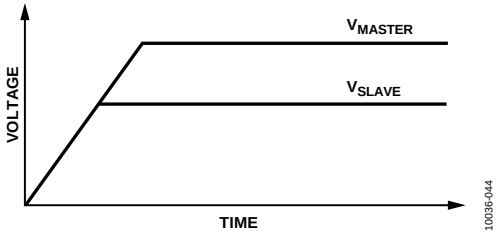

Figure 48. Coincident Tracking

Ratiometric Tracking

In ratiometric tracking, the slave output voltage is limited to a fraction of the master voltage. In this application, the slave and master voltages reach their final values at the same time (see Figure 49).

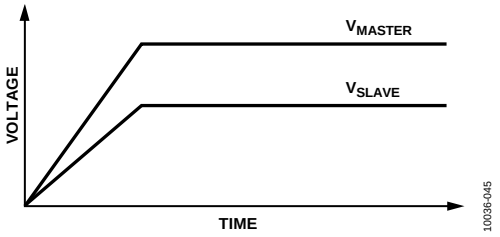

Figure 49. Ratiometric Tracking

The ratio of the slave output voltage to the master voltage is a function of the two dividers, as follows:

$$\frac{V_{SLAVE}}{V_{MASTER}} = \frac{1+\frac{R_{TOP}}{R_{BOT}}}{1+\frac{R_{TRK_TOP}}{R_{TRK_BOT}}}$$

The final TRKx pin voltage must be higher than 0.54 V. If the tracking function is not used, connect the TRKx pin to INTVCC.

PARALLEL OPERATION

The ADP2325 supports a 2-phase parallel operation to provide a single output of 10 A. To configure the ADP2325 as a 2-phase single output

1. Connect the FB2 pin to INTVCC, thereby disabling the Channel 2 error amplifier.
2. Connect COMP1 to COMP2 and connect EN1 to EN2.
3. Use SS1 to set the soft start time and keep SS2 open.

During parallel operation, the voltages of PVIN1 and PVIN2 should be the same.

POWER GOOD

The power-good (PGOODx) pin is an active high, open-drain output that indicates whether the regulator output voltage is within regulation. Logic high indicates that the voltage at the FBx pin (and, therefore, the output voltage) is above 90% of the reference voltage. Logic low indicates that the voltage at the FBx pin (and, therefore, the output voltage) is below 85% of the reference voltage. There is a 16-cycle deglitch time between FBx and PGOODx.

OVERVOLTAGE PROTECTION

The ADP2325 provides an OVP feature to protect the system against an output shorting to a higher voltage supply or for when a strong load transient occurs. If the feedback voltage increases to 0.7 V, the internal high-side MOSFET and low-side driver turn off until the voltage at the FBx pin is reduced to 0.63 V, at which time the ADP2325 resumes normal operation.

UNDERVOLTAGE LOCKOUT

The UVLO threshold is 4.2 V with 0.5 V hysteresis to prevent power-on glitches on the device. When the PVIN1 or PVIN2 voltage rises above 4.2 V, Channel 1 or Channel 2 is enabled and the soft start period initiates. When either PVIN1 or PVIN2 drops below 3.7 V, it turns off Channel 1 or Channel 2, respectively.

THERMAL SHUTDOWN

In the event that the ADP2325 junction temperature exceeds 150°C, the thermal shutdown circuit turns off the regulator. A 15°C hysteresis is included so that the ADP2325 does not recover from thermal shutdown until the on-chip temperature drops below 135°C. Upon recovery, soft start initiates prior to normal operation.

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP2325 is supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

INPUT CAPACITOR SELECTION

The input decoupling capacitor attenuates high frequency noise on the input and acts as an energy reservoir. This capacitor should be a ceramic capacitor in the range of 10 µF to 47 µF and must be placed close to the PVINx pin. The loop composed of this input capacitor, high-side NFET, and low-side NFET must be kept as small as possible. The voltage rating of the input capacitor must be greater than the maximum input voltage. Ensure that the rms current rating of the input capacitor is larger than that expressed in following equation:

$$I_{C_{IN-rms}} = I_{OUT} \times \sqrt{D \times (1-D)}$$

OUTPUT VOLTAGE SETTING

The output voltage of the ADP2325 can be set by an external resistor divider using the following equation:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

To limit output voltage accuracy degradation due to FBx pin bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that R_{BOT} is less than 30 kΩ. Table 8 provides the recommended resistor divider for various output voltage options.

Table 8. Resistor Divider for Various Output Voltages

V_{OUT} (V)	R_{TOP}, ±1% (kΩ)	R_{BOT}, ±1% (kΩ)
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	47.5	15
3.3	10	2.21
5.0	22	3

VOLTAGE CONVERSION LIMITATIONS

The minimum output voltage for a given input voltage and switching frequency is limited by the minimum on time. The minimum on time of the ADP2325 is typically 130 ns. The minimum output voltage in CCM mode at a given input voltage and frequency can be calculated using the following equation:

$$V_{OUT_MIN} = V_{IN} \times t_{MIN_ON} \times f_{SW} - (R_{DSON1} - R_{DSON2}) \times I_{OUT_MIN} \times t_{MIN_ON} \times f_{SW} - (R_{DSON2} + R_L) \times I_{OUT_MIN}$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
I_{OUT_MIN} is the minimum output current.
f_{SW} is the switching frequency.
R_{DSON1} is the high-side MOSFET on resistance.
R_{DSON2} is the low-side MOSFET on resistance.
R_L is the series resistance of the output inductor.

The maximum output voltage for a given input voltage and switching frequency is also limited by the minimum off time and the maximum duty cycle. The minimum off time is typically 150 ns and the maximum duty is typically 90% in the ADP2325.

The maximum output voltage that is limited by the minimum off time at a given input voltage and frequency can be calculated using the following equation:

$$V_{OUT_MAX} = V_{IN} \times (1 - t_{MIN_OFF} \times f_{SW}) - (R_{DSON1} - R_{DSON2}) \times I_{OUT_MAX} \times (1 - t_{MIN_OFF} \times f_{SW}) - (R_{DSON2} + R_L) \times I_{OUT_MAX}$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

The maximum output voltage that is limited by the maximum duty cycle at a given input voltage can be calculated using the following equation:

$$V_{OUT_MAX} = D_{MAX} \times V_{IN}$$

where D_{MAX} is the maximum duty cycle.

As the previous equations demonstrate, reducing the switching frequency alleviates the minimum on time and minimum off time limitation.

CURRENT-LIMIT SETTING

The ADP2325 has two selectable current-limit thresholds. Make sure that the selected current-limit value is larger than the peak current of the inductor, I_{PEAK}.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor provides faster transient response but degrades efficiency due to larger inductor ripple current, whereas a large inductor value provides smaller ripple current and better efficiency but results in a slower transient response. Thus, there is a trade-off between the transient response and efficiency. As a guideline, the inductor ripple current, ΔI_L, is typically set to one-third of the maximum load current. The inductor value can be calculated by using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
ΔI_L is the inductor ripple current.
f_{SW} is the switching frequency.
D is the duty cycle.

$$D = \frac{V_{OUT}}{V_{IN}}$$

The ADP2325 uses adaptive slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

For a duty cycle that is larger than 50%, the minimum inductor value is determined by the following equation:

$$\frac{V_{OUT} \times (1 - D)}{2 \times f_{SW}}$$

The inductor peak current is calculated by

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be larger than the peak inductor current. For the ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor should be higher than the current-limit threshold of the switch to prevent the inductor from entering saturation.

The rms current of the inductor can be calculated by

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI.

Table 9. Recommended Inductors

Vendor	Part No.	Value (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (mΩ)
Sumida	CDRH105RNP-0R8N	0.8	13.5	9.5	4.3
	CDRH105RNP-1R5N	1.5	10.5	8.3	5.8
	CDRH105RNP-2R2N	2.2	9.25	7.5	7.2
	CDRH105RNP-3R3N	3.3	7.8	6.5	10.4
	CDRH105RNP-4R7N	4.7	6.4	6.1	12.3
	CDRH105RNP-6R8N	6.8	5.4	5.4	18
Coilcraft	MSS1048-152NL	1.5	10.5	10.8	5.1
	MSS1048-222NL	2.2	8.4	9.78	7.2
	MSS1048-332NL	3.3	7.38	7.22	10.1
	MSS1048-472NL	4.7	6.46	6.9	11.4
	MSS1048-682NL	6.8	5.94	6.01	15.4
Wurth Elektronik	7447797110	1.1	16	7.6	14
	7447797180	1.8	13.3	7.3	16
	7447797300	3.0	10.5	7.0	18
	7447797470	4.7	8.0	5.8	27
	7447797620	6.2	7.5	5.5	30

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the regulator. For example, during load step transient on the output, when the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current, which causes an undershoot of the output voltage. Use the following equation to calculate the output capacitance that is required to meet the voltage droop requirement:

$$C_{OUT_UV} = \frac{K_{UV} \times {\Delta I_{STEP}}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT_UV}}$$

where:
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.
K_{UV} is a factor, typically setting K_{UV} = 2.

Another example is when a load is suddenly removed from the output and the energy stored in the inductor rushes into the output capacitor, which causes the output to overshoot. The output capacitance required to meet the overshoot requirement can be calculated using the following equation:

$$C_{OUT_OV} = \frac{K_{OV} \times {\Delta I_{STEP}}^2 \times L}{(V_{OUT} + \Delta V_{OUT_OV})^2 - {V_{OUT}}^2}$$

where:
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.
K_{OV} is a factor, typically setting K_{OV} = 2.

The output ripple is determined by the ESR of the output capacitor and its capacitance value. Use the following equation to select a capacitor that can meet the output ripple requirements:

$$C_{OUT_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT_RIPPLE}}{\Delta I_L}$$

where:
ΔV_{OUT_RIPPLE} is the allowable output voltage ripple.
R_{ESR} is the equivalent series resistance of the output capacitor.

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple performance.

The selected output capacitor voltage rating must be greater than the output voltage. The minimum rms current rating of the output capacitor is determined by the following equation:

$$I_{C_{OUT}_rms} = \frac{\Delta I_L}{\sqrt{12}}$$

LOW-SIDE POWER DEVICE SELECTION

The ADP2325 has integrated low-side MOSFET drivers, which can drive the low-side N-channel MOSFETs (NFETs). The selection of the low-side N-channel MOSFET affects the dc-to-dc regulator performance.

The selected MOSFET must meet the following requirements:

- Drain source voltage (V_{DS}) must be higher than $1.2 \times V_{IN}$.
- Drain current (I_D) must be greater than $1.2 \times I_{LIMIT_MAX}$, where I_{LIMIT_MAX} is the selected maximum current-limit threshold.

The ADP2325 low-side gate drive voltage is 5 V. Make sure that the selected MOSFET can be fully turned on at 5 V.

Total gate charge (Qg at 5 V) must be less than 50 nC. Lower Qg characteristics constitute higher efficiency.

When the high-side MOSFET is turned off, the low-side MOSFET carries the inductor current. For low duty cycle applications, the low-side MOSFET carries the current for most of the period. To achieve higher efficiency, it is important to select a low on-resistance MOSFET. The power conduction loss for the low-side MOSFET can be calculated by

$$P_{FET_LOW} = I_{OUT}^2 \times R_{DSON} \times (1 - D)$$

where R_{DSON} is the on resistance of the low-side MOSFET.

Make sure that the MOSFET can handle the thermal dissipation due to the power loss.

In some cases, efficiency is not critical for the system; therefore, the diode can be selected as the low-side power device. The average current of the diode can be calculated by

$$I_{DIODE\,(AVG)} = (1 - D) \times I_{OUT}$$

The reverse breakdown voltage rating of the diode must be greater than the input voltage with an appropriate margin to allow for ringing, which may be present at the SWx node. A Schottky diode is recommended because it has a low forward voltage drop and a fast switching speed.

If a diode is used for the low-side device, the ADP2325 must enable the PFM mode by connecting the MODE pin to ground.

Table 10. Recommended MOSFETs

Vendor	Part No.	V_{DS}	I_D	R_{DSON}	Qg
Fairchild	FDS8880	30 V	10.7 A	12 mΩ	12 nC
Fairchild	FDMS7578	25 V	14 A	8 mΩ	8 nC
Fairchild	FDS6898A	20 V	9.4 A	14 mΩ	16 nC
Vishay	Si4804CDY	30 V	7.9 A	27 mΩ	7 nC
Vishay	SiA430DJ	20 V	10.8 A	18.5 mΩ	5.3 nC
AOS	AON7402	30 V	39 A	15 mΩ	7.1 nC
AOS	AO4884L	40 V	10 A	16 mΩ	13.6 nC

PROGRAMMING THE UVLO INPUT

The precision enable input can be used to program the UVLO threshold and hysteresis of the input voltage, as shown in Figure 50.

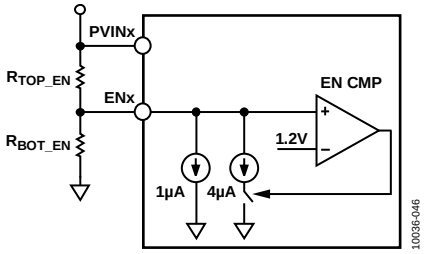

Figure 50. Programming the UVLO Input

Use the following equation to calculate R_{TOP_EN} and R_{BOT_EN}:

$$R_{TOP_EN} = \frac{1.1\,\text{V} \times V_{IN_RISING} - 1.2\,\text{V} \times V_{IN_FALLING}}{1.1\,\text{V} \times 5\,\mu\text{A} - 1.2\,\text{V} \times 1\,\mu\text{A}}$$

$$R_{BOT_EN} = \frac{1.2\,\text{V} \times R_{TOP_EN}}{V_{IN_RISING} - R_{TOP_EN} \times 5\,\mu\text{A} - 1.2\,\text{V}}$$

where:
V_{IN_RISING} is the V_{IN} rising threshold.
$V_{IN_FALLING}$ is the V_{IN} falling threshold.

COMPENSATION COMPONENTS DESIGN

In peak current mode control, the power stage can be simplified to a voltage controlled current source supplying current to the output capacitor and load resistor. It is composed of one domain pole and a zero contributed by the output capacitor ESR. The control-to-output transfer function is shown in the following equations:

$$G_{VD}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_Z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_P}\right)}$$

$$f_Z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_P = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:

A_{VI} = 8.33 A/V.

R is the load resistance.

C_{OUT} is the output capacitance.

R_{ESR} is the equivalent series resistance of the output capacitor.

The ADP2325 uses a transconductance amplifier for the error amplifier to compensate the system. Figure 51 shows the simplified peak current mode control small signal circuit.

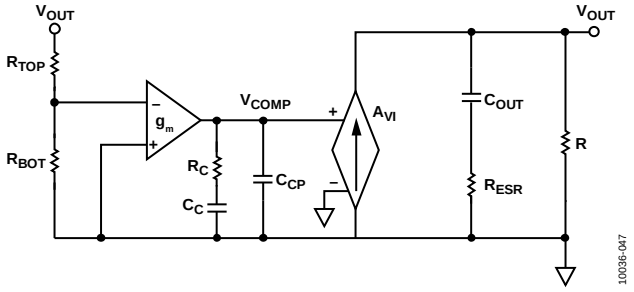

Figure 51. Simplified Peak Current Mode Control Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero, and the optional C_{CP} and R_C contribute an optional pole.

The closed-loop transfer equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s\right)} \times G_{VD}(s)$$

The following design guidelines show how to select the compensation components, R_C, C_C, and C_{CP}, for ceramic output capacitor applications.

4. Determine the cross frequency (f_C). Generally, the f_C is between $f_{SW}/12$ and $f_{SW}/6$.
5. R_C can be calculated by using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.6\,\text{V} \times g_m \times A_{VI}}$$

6. Place the compensation zero at the domain pole (f_P). C_C can be determined by

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

7. C_{CP} is optional. It can be used to cancel the zero caused by the ESR of the output capacitor.

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

The ADP2325 has an internal 10 pF capacitor at the COMPx pin; therefore, if C_{CP} is smaller than 10 pF, no external capacitor is required.

DESIGN EXAMPLE

This section describes the design procedure and component selection for the example application shown in Figure 54, and Table 11 provides a list of the required settings.

Table 11. Dual Step-Down DC-to-DC Regulator Requirements

Parameter	Specification
Channel 1	
Input Voltage	V_{IN1} = 12.0 V ± 10%
Output Voltage	V_{OUT1} = 1.2 V
Output Current	I_{OUT1} = 5 A
Output Voltage Ripple	ΔV_{OUT1_RIPPLE} = 12 mV
Load Transient	±5%, 1 A to 4 A, 1 A/µs
Channel 2	
Input Voltage	V_{IN2} = 12.0 V ± 10%
Output Voltage	V_{OUT2} = 3.3 V
Output Current	I_{OUT2} = 5 A
Output Voltage Ripple	ΔV_{OUT2_RIPPLE} = 33 mV
Load Transient	±5%, 1 A to 4 A, 1 A/µs
Switching Frequency	f_{SW} = 500 kHz

OUTPUT VOLTAGE SETTING

Choose a 10 kΩ top feedback resistor (R_{TOP}); calculate the bottom feedback resistor using the following equation:

$$R_{BOT} = R_{TOP} \times \left(\frac{0.6}{V_{OUT} - 0.6} \right)$$

To set the output voltage to 1.2 V, the resistor values are R_{TOP1} = 10 kΩ and R_{BOT1} = 10 kΩ. To set the output voltage to 3.3 V, the resistors values are R_{TOP2} = 10 kΩ and R_{BOT2} = 2.21 kΩ.

CURRENT-LIMIT SETTING

For 5 A output current operation, the typical peak current limit is 8 A. In this case, no R_{ILIM} is required.

FREQUENCY SETTING

To set the switching frequency to 500 kHz, use the following equation to calculate the resistor value, R_{OSC}:

$$R_{OSC}(\text{k}\Omega) = \frac{60{,}000}{f_{SW}(\text{kHz})}$$

Therefore, R_{OSC} =120 kΩ.

INDUCTOR SELECTION

The peak-to-peak inductor ripple current, ΔI_L, is set to 30% of the maximum output current. Use the following equation to estimate the value of the inductor:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

For V_{OUT1} = 1.2 V, Inductor L1 = 1.4 µH, and for V_{OUT2} = 3.3 V, Inductor L2 = 3.2 µH.

Select the standard inductor value of 1.5 µH and 3.3 µH for the 1.2 V and 3.3 V rails.

Calculate the peak-to-peak inductor ripple current as follows:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

For V_{OUT1} = 1.2 V, ΔI_{L1} = 1.44 A. For V_{OUT2} = 3.3 V, ΔI_{L2} = 1.45 A.

Find the peak inductor current using the following equation:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

For the 1.2 V rail, the peak inductor current is 5.73 A, and for the 3.3 V rail, the peak inductor current is 5.73 A.

The rms current through the inductor can be estimated by

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

The rms current of the inductor for both the 1.2 V and 3.3 V rails is approximately 5.02 A.

For the 1.2 V rail, select an inductor with a minimum rms current rating of 5.01 A and a minimum saturation current rating of 5.73 A. For the 3.3 V rail, select an inductor with a minimum rms current rating of 5.02 A and a minimum saturation current rating of 5.73 A.

Based on these requirements, for the 1.2 V rail, select a 1.5 µH inductor, such as the Sumida CDRH105RNP-1R5N, with a DCR = 5.8 mΩ; for the 3.3 V rail, select a 3.3 µH inductor, such as the Sumida CDRH105RNP-3R3N, with a DCR = 10.4 mΩ.

OUTPUT CAPACITOR SELECTION

The output capacitor is required to meet the output voltage ripple and load transient requirements. To meet the output voltage ripple requirement, use the following equation to calculate the capacitance and ESR:

$$C_{OUT_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT_RIPPLE}}{I_L}$$

For V_{OUT1} = 1.2 V, $C_{OUT_RIPPLE1}$ = 30 µF and R_{ESR1} = 8.3 mΩ. For V_{OUT2} = 3.3 V, $C_{OUT_RIPPLE2}$ = 11 µF and R_{ESR2} = 23 mΩ.

To meet the ±5% overshoot and undershoot requirement, use the following equation to calculate the capacitance:

$$C_{OUT_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{\left(V_{OUT} + \Delta V_{OUT_OV}\right)^2 - V_{OUT}{}^2}$$

$$C_{OUT_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times \left(V_{IN} - V_{OUT}\right) \times \Delta V_{OUT_UV}}$$

For estimation purposes, use $K_{OV} = K_{UV} = 2$. For $V_{OUT1} = 1.2$ V, use $C_{OUT_OV1} = 188$ µF and $C_{OUT_UV1} = 21$ µF. For $V_{OUT2} = 3.3$ V, use $C_{OUT_OV2} = 55$ µF and $C_{OUT_UV2} = 21$ µF.

For the 1.2 V rail, ESR of the output capacitor must be smaller than 8.3 mΩ, and the output capacitance must be larger than 188 µF. It is recommend that three 100 µF, X5R, 6.3 V ceramic capacitors be used, such as the GRM32ER60J107ME20 from Murata, with an ESR = 2 mΩ.

For the 3.3 V rail, the ESR of the output capacitor must be smaller than 23 mΩ, and the output capacitance must be larger than 55 µF. It is recommended that two 47 µF, X5R, 6.3 V ceramic capacitors be used, such as the Murata GRM32ER60J476ME20, with an ESR = 2 mΩ.

LOW-SIDE MOSFET SELECTION

A low R_{DSON} N-channel MOSFET is selected for high efficiency solutions. The MOSFET breakdown voltage must be greater than 1.2 V × V_{IN}, and the drain current must be greater than 1.2 V × I_{LIMIT}.

It is recommended that a 30 V, N-channel MOSFET be used, such as the FDS8880 from Fairchild. The R_{DSON} of the FDS8880 at a 4.5 V driver voltage is 12 mΩ, and the total gate charge is 12 nC.

COMPENSATION COMPONENTS

For better load transient and stability performance, set the cross frequency, f_C, to $f_{SW}/10$. In this case, f_{SW} runs at 500 kHz; therefore, the f_C is set to 50 kHz.

For the 1.2 V rail, the 100 µF ceramic output capacitor has a derated value of 64 µF.

$$R_{C1} = \frac{2 \times \pi \times 1.2\,\text{V} \times 3 \times 64\,\mu\text{F} \times 50\,\text{kHz}}{0.6\,\text{V} \times 500\,\mu\text{S} \times 8.33\,\text{A/V}} = 28.9\,\text{k}\Omega$$

$$C_{C1} = \frac{\left(0.24\,\Omega + 0.001\,\Omega\right) \times 3 \times 64\,\mu\text{F}}{28.9\,\text{k}\Omega} = 1598\,\text{pF}$$

$$C_{CP1} = \frac{0.001\,\Omega \times 3 \times 64\,\mu\text{F}}{28.9\,\text{k}\Omega} = 6.6\,\text{pF}$$

By choosing standard components where $R_{C1} = 28$ kΩ and $C_{C1} = 1500$ pF, no C_{CP1} is needed.

Figure 52 shows the 1.2 V rail bode plot at 5 A. The cross frequency is 42 kHz and the phase margin is 50°.

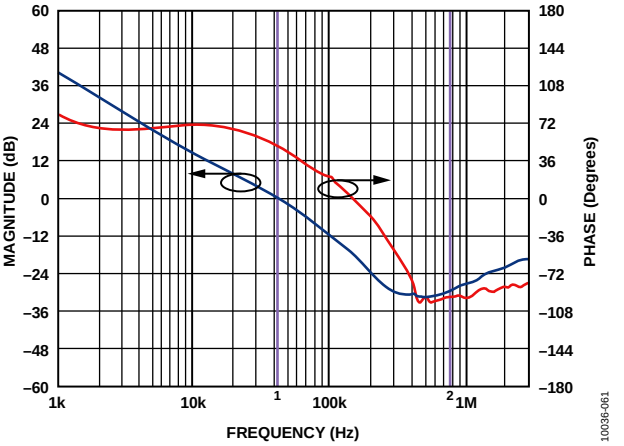

Figure 52. Bode Plot for 1.2 V Rail

For the 3.3 V rail, the 47 µF ceramic output capacitor has a derated value of 32 µF.

$$R_{C2} = \frac{2 \times \pi \times 3.3\,\text{V} \times 2 \times 32\,\mu\text{F} \times 50\,\text{kHz}}{0.6\,\text{V} \times 500\,\mu\text{S} \times 8.33\,\text{A/V}} = 26.5\,\text{k}\Omega$$

$$C_{C2} = \frac{\left(0.66\,\Omega + 0.001\,\Omega\right) \times 2 \times 32\,\mu\text{F}}{26.5\,\text{k}\Omega} = 1594\,\text{pF}$$

$$C_{CP2} = \frac{0.001\,\Omega \times 2 \times 32\,\mu\text{F}}{26.5\,\text{k}\Omega} = 2.4\,\text{pF}$$

By using standard component values of $R_{C2} = 27$ kΩ and $C_{C2} = 1500$ pF, no C_{CP2} is needed.

Figure 53 shows the 3.3 V rail bode plot at 5 A. The cross frequency is 55 kHz and phase margin is 67°.

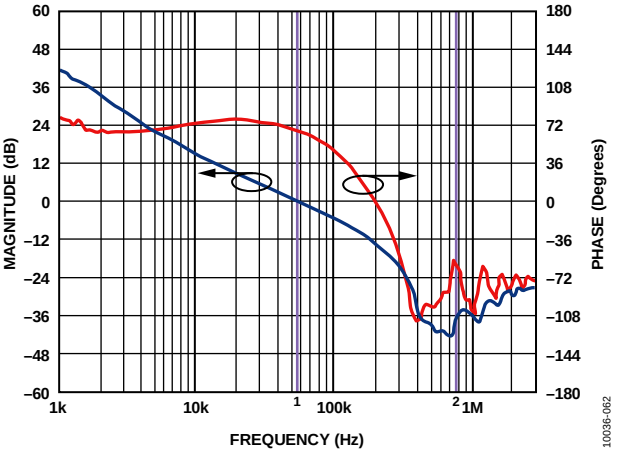

Figure 53. Bode Plot for 3.3 V Rail

SOFT START TIME PROGRAMMING

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting inrush current. The soft start time is set to 3 ms.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{0.6\ \text{V}} = \frac{3.5\ \mu\text{A} \times 3\ \text{ms}}{0.6\ \text{V}} = 17.5\ \text{nF}$$

Choose a standard component value of $C_{SS1} = C_{SS2} = 22$ nF.

INPUT CAPACITOR SELECTION

A minimum 10 µF ceramic capacitor is required, placed near the PVINx pin. In this application, one X5R ceramic capacitor of 10 µF and 25 V is recommended.

EXTERNAL COMPONENTS RECOMMENDATIONS

Table 12. Recommended External Components for Typical Applications with 5 A Output Current

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)[1]	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)	C_{CP} (pF)
300	12	1	2.2	2 × 330	10	15	47	2700	56
	12	1.2	2.2	2 × 330	10	10	59	2700	56
	12	1.5	3.3	2 × 330	15	10	75	2700	47
	12	1.8	3.3	330	20	10	43	2700	68
	12	2.5	4.7	330	47.5	15	62	2700	56
	12	3.3	4.7	2 × 100	10	2.21	33	2700	3.3
	12	5	6.8	100 + 47	22	3	36	2700	3.3
	5	1	1.5	2 × 330	10	15	49	2700	68
	5	1.2	2.2	2 × 330	10	10	59	2700	56
	5	1.5	2.2	330	15	10	37	2700	82
	5	1.8	2.2	330	20	10	43	2700	68
	5	2.5	2.2	2 × 100	47.5	15	22	2700	4.7
	5	3.3	2.2	100	10	2.21	15	2700	4.7
600	12	1.5	1.5	330	15	10	75	1500	47
	12	1.8	1.5	3 × 100	20	10	53	1500	2.2
	12	2.5	2.2	2 × 100	47.5	15	47	1500	2.2
	12	3.3	2.2	100 + 47	10	2.21	47	1500	2.2
	12	5	3.3	100	22	3	47	1500	2.2
	5	1	1	330	10	15	49	1500	68
	5	1.2	1	330	10	10	59	1500	56
	5	1.5	1	2 × 100	15	10	27	1500	4.7
	5	1.8	1.5	2 × 100	20	10	33	1500	3.3
	5	2.5	1.5	100 + 47	47.5	15	33	1500	2.2
	5	3.3	1.5	100	10	2.21	30	1500	4.7
1000	12	1.8	1	2 × 100	20	10	56	820	2.2
	12	2.5	1	100	47.5	15	39	820	2.2
	12	3.3	1.5	100	10	2.21	53	820	2.2
	12	5	2	47	22	3	39	820	2.2
	5	1	0.56	3 × 100	10	15	47	820	2.2
	5	1.2	0.56	2 × 100	10	10	37	820	6.8
	5	1.5	0.68	2 × 100	15	10	47	820	4.7
	5	1.8	0.8	100 + 47	20	10	43	820	4.7
	5	2.5	0.8	100	47.5	15	43	820	4.7
	5	3.3	0.8	47	10	2.21	27	820	2.2

[1] 330 µF: 6.3 V, Sanyo 6TPD330M; 100 µF: 6.3 V, X5R, Murata GRM32ER60J107ME20; 47 µF: 6.3 V, X5R, Murata GRM32ER60J476ME20.

TYPICAL APPLICATION CIRCUITS

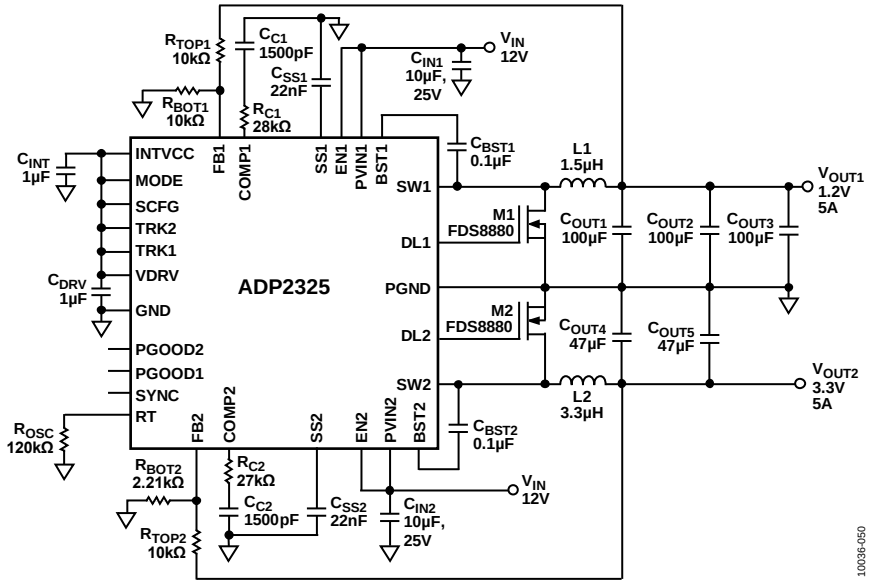

Figure 54. Using an External MOSFET Application, $V_{IN1} = V_{IN2} = 12$ V, $V_{OUT1} = 1.2$ V, $I_{OUT1} = 5$ A, $V_{OUT2} = 3.3$ V, $I_{OUT2} = 5$ A, $f_{SW} = 500$ kHz

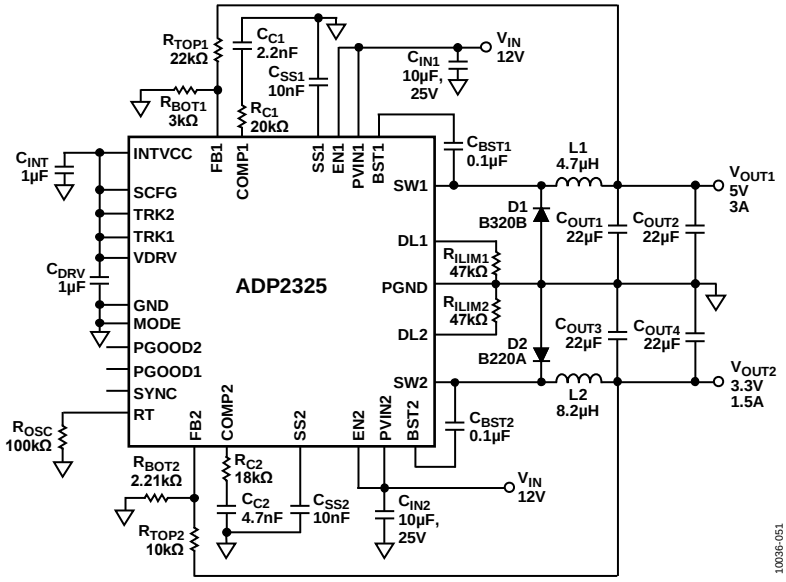

Figure 55. Using an External Diode Application, $V_{IN1} = V_{IN2} = 12$ V, $V_{OUT1} = 5$ V, $I_{OUT1} = 3$ A, $V_{OUT2} = 3.3$ V, $I_{OUT2} = 1.5$ A, $f_{SW} = 600$ kHz

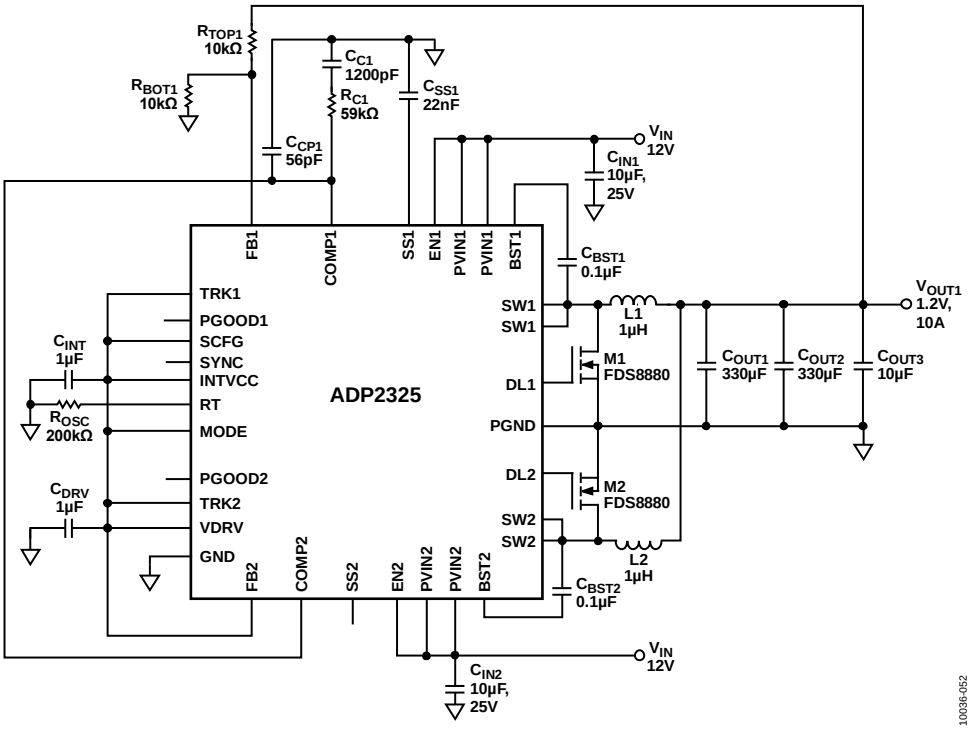

Figure 56. Parallel Single Output Application, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 10 A, f_{SW} = 300 kHz

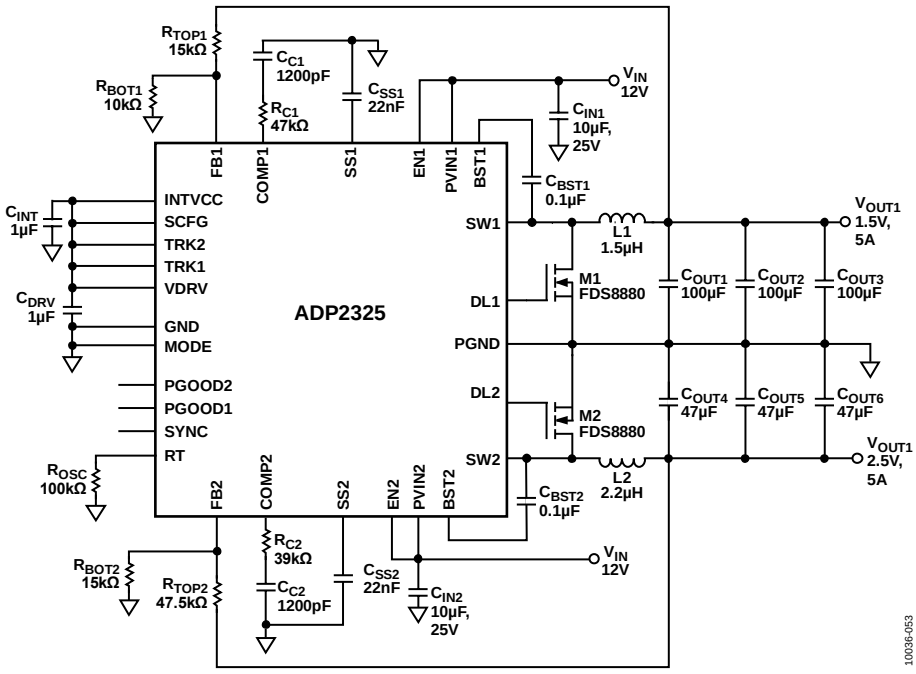

Figure 57. Enable PFM Mode with the MODE Pin Pulled to GND, V_{IN1} = V_{IN2} = 12 V, V_{OUT1} = 1.5 V, I_{OUT1} = 5 A, V_{OUT2} = 2.5 V, I_{OUT2} = 5 A, f_{SW} = 600 kHz

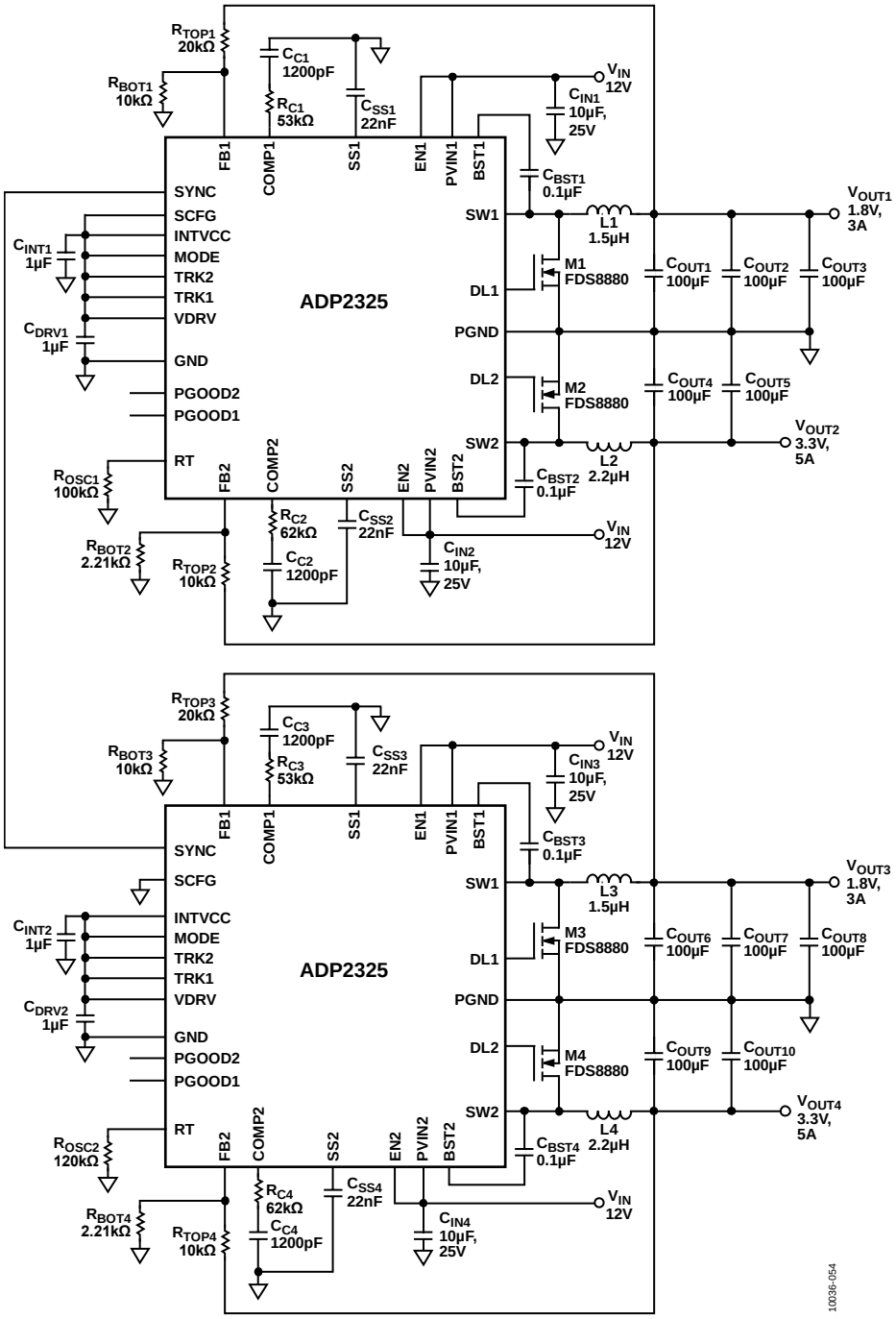

Figure 58. Synchronization with 90° Phase Shift Between Each Channel

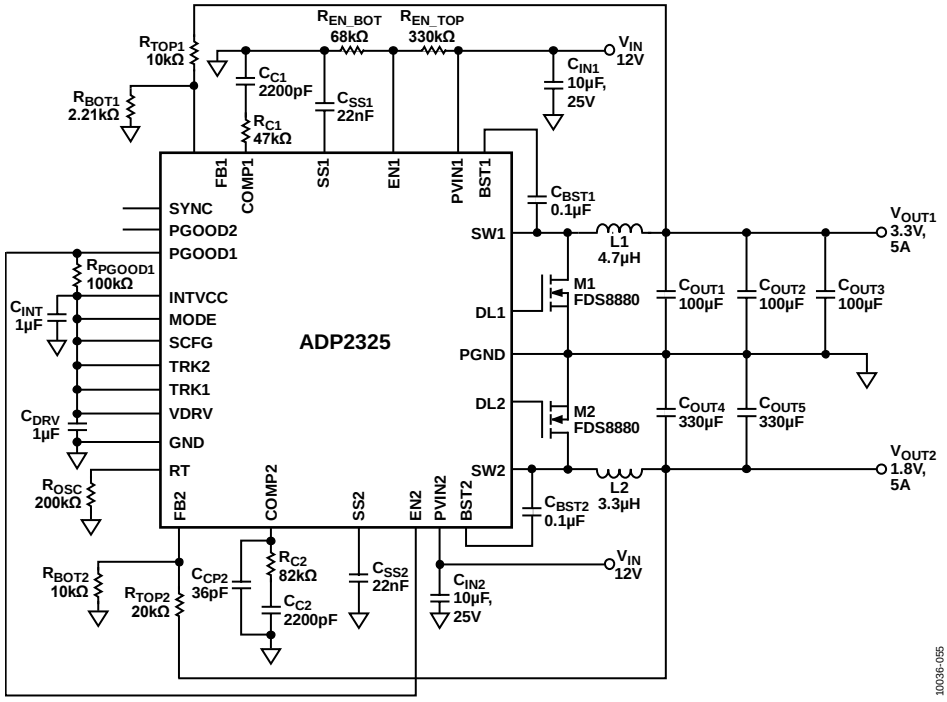

Figure 59. Programmable V_{IN_RISING} = 8.7 V, $V_{IN_FALLING}$ = 6.7 V, 3.3 V Startup Prior to 1.8 V, $V_{IN1} = V_{IN2}$ = 12 V, V_{OUT1} = 3.3 V, I_{OUT1} = 5 A, V_{OUT2} = 1.8 V, I_{OUT2} = 5 A, f_{SW} = 300 kHz

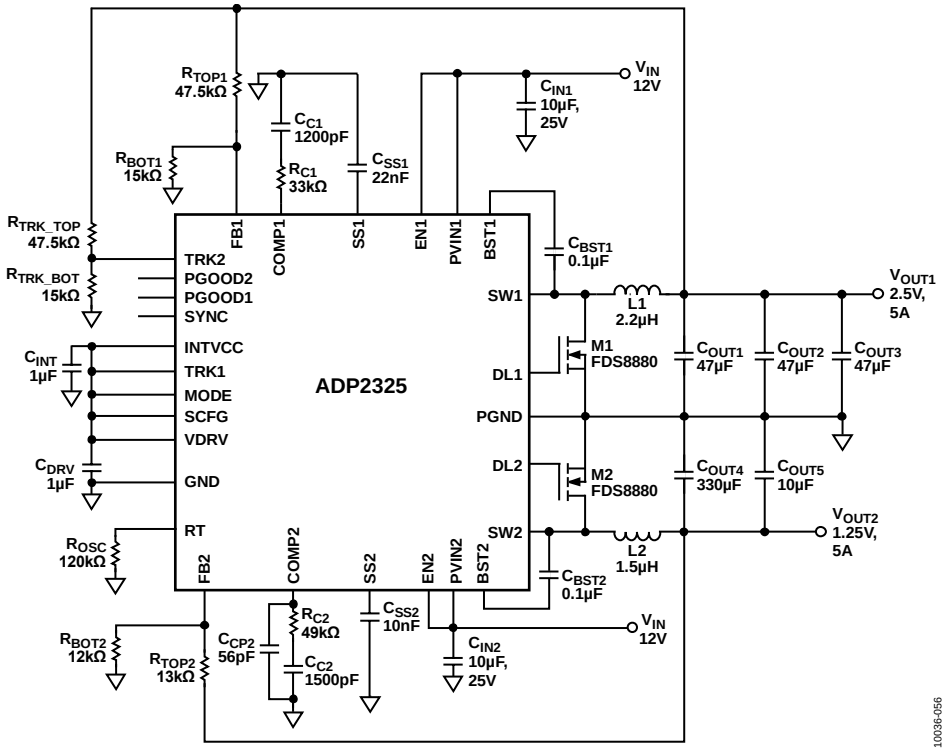

Figure 60. Channel 2 Tracking with Channel 1
$V_{IN1} = V_{IN2}$ = 12 V, V_{OUT1} = 2.5 V, I_{OUT1} = 5 A, V_{OUT2} = 1.25 V, I_{OUT2} = 5 A, f_{SW} = 500 kHz

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

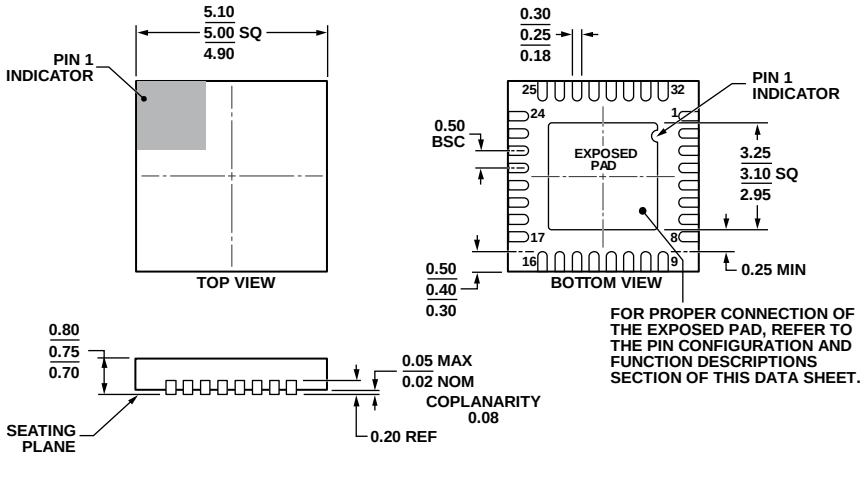

Figure 61. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage	Package Description	Package Option
ADP2325ACPZ-R7	−40°C to +125°C	Adjustable	32-Lead LFCSP_WQ	CP-32-7
ADP2325-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.

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