TPS57112EVM User's Guide

The TPS57112-Q1 DC-DC converter is designed to provide up to 2-A output from an input voltage source of 2.95 V to 6 V. Table 1 lists the rated input voltage and output current range for the evaluation module (EVM). This evaluation module is designed to demonstrate the small printed-circuit-board (PCB) areas that can be achieved when designing with the TPS57112-Q1 regulator. The switching frequency is externally set at a nominal 2000 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS57112-Q1 device to achieve high efficiencies and to maintain a low junction temperature at high output currents. The compensation components are external to the integrated circuit (IC) and have been selected to optimize the transient performance of the device. An external divider allows for an adjustable output voltage. Additionally, the TPS57112-Q1 device provides adjustable slow-start and undervoltage lockout inputs. The absolute-maximum input voltage is 7 V for the TPS57112EVM.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output current Range
TPS57112EVM	V_{IN} = 3 V to 6 V	0 A to 2 A

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1 Performance-Specification Summary

Table 2 lists a summary of the TPS57112EVM performance specifications. Specifications are given for an input voltage of V_{IN} = 5 V and an output voltage of 1.2 V, unless otherwise specified. The TPS57112EVM is designed and tested for V_{IN} = 3 V to 6 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS57112EVM Performance-Specification Summary

SPECIFICATION	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IN} operating voltage range			3	5	6	V
V_{IN} start voltage				2.84		V
V_{IN} stop voltage				2.68		V
Output voltage set point				1.2		V
Output current range	V_{IN} = 3 V to 6 V		0		2	A
Line regulation	I_O = 1 A, V_{IN} = 3 V to 6 V			±0.25%		
Load regulation	V_{IN} = 3.3 V, I_O = 0 A to 2 A			±0.3%		
Load transient response	I_O = 500 mA to 1.5 A	Voltage change		–30		mV
		Recovery time		80		µs
	I_O = 1.5 A to 500 mA	Voltage change		30		mV
		Recovery time		80		µs
Loop bandwidth	V_{IN} = 5 V, I_O = 1 A			88		kHz
Phase margin	V_{IN} = 5 V, I_O = 1 A			42		°
Output ripple voltage	I_O = 2 A			5		mV_{pp}
Output rise time				4		ms
Operating frequency				2000		kHz
Maximum efficiency	V_{IN} = 3.3 V, I_O = 1.8 A			86%		

1.1 Modifications

This EVM is designed to provide access to the features of the TPS57112-Q1 device. Some modifications can be made to the module.

1.1.1 Output Voltage Set-Point

The voltage dividers R_5 and R_7 set the output voltage. To change the output voltage of the EVM, changing the value of resistor R_5 is necessary. Changing the value of R_5 changes the output voltage above 0.8 V. The value of R_5 for a specific output voltage is calculated using Equation 1.

$$R_5 = 80.6\ k\Omega \times \frac{V_{OUT} - V_{REF}}{V_{REF}} \quad (1)$$

Table 3 lists the R_5 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 75 ns, and the maximum duty cycle is less than 92%. The values given in Table 3 are standard values and are not the exact value calculated using Equation 1.

Table 3. Common Output-Voltage Options

Output Voltage (V)	R_5 Value (kΩ)
1	20
1.2	40.2
1.5	71.5
1.8	100
2.5	174
3.3	249

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1.1.2 Slow-Start Time

The slow-start time is adjusted by changing the value of C_{15}. Equation 2 calculates the required value of C_{15} for a desired slow-start time.

$$C_{15}\,(nF) = \frac{T_{SS}\,(ms) \times I_{SS}\,(\mu A)}{V_{REF}\,(V)} \quad (2)$$

where

- I_{SS} = 2 µA

C_{15} is set to 0.01 µF on the EVM for a default slow-start time of 4 ms.

1.1.3 Adjustable Undervoltage Lockout

The undervoltage lockout (UVLO) is adjusted externally using R_3 and R_4. The EVM is set for a start voltage of 2.84 V and a stop voltage of 2.68 V using R_3 = 25.5 kΩ and R_2 = 20 kΩ. Use Equation 3 and Equation 4 along with notes included in the TPS57112-Q1 data sheet (SLVSAL8) to calculate required resistor values for different start and stop voltages.

$$R_3 = \frac{0.944 \times V_{START} - V_{STOP}}{1.71 \times 10^{-6}} \quad (3)$$

$$R_4 = \frac{1.18 \times R_3}{V_{STOP} - 1.18 + R_3 \times 3.5 \times 10^{-6}} \quad (4)$$

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS57112EVM evaluation module. Test results typical of this evaluation module are also included. This section covers efficiency, output voltage regulation, load transients, loop response, output ripple, and startup.

2.1 Input and Output Connections

The TPS57112EVM is provided with input and output connectors and test points as shown in Table 4. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load-current capability must be at least 2 A to use the full capability of this EVM. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP3 monitors the output voltage with TP4 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range)
J2	V_{OUT}, 1.2 V at 2 A maximum
JP1	2-pin header for enable. Connect EN to ground to disable, open to enable
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	V_{OUT} test point at V_{OUT} connector
TP4	GND test point at V_{OUT}
TP5	Test point between voltage divider network and output. Used for loop response measurements
TP6	COMP test point

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2.2 Efficiency

Figure 1 shows the efficiency for the TPS57112EVM at two different input voltages and at an ambient temperature of 25°C.

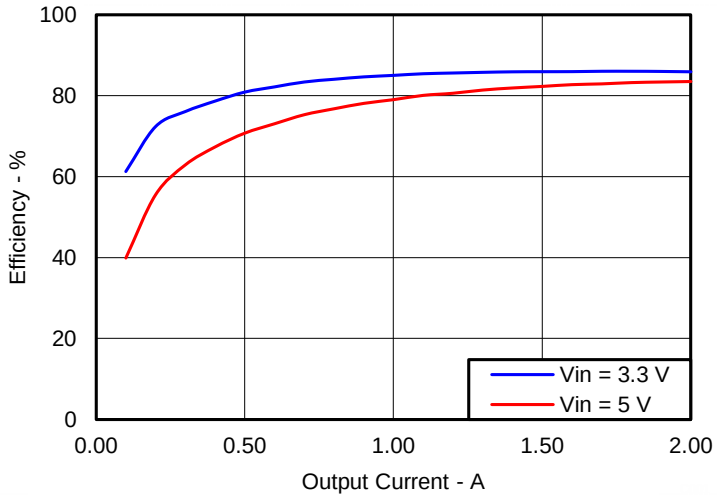


Figure 1. TPS57112EVM Efficiency

2.3 Output-Voltage Load Regulation

Figure 2 shows the load regulation for the TPS57112EVM at two different input voltages.

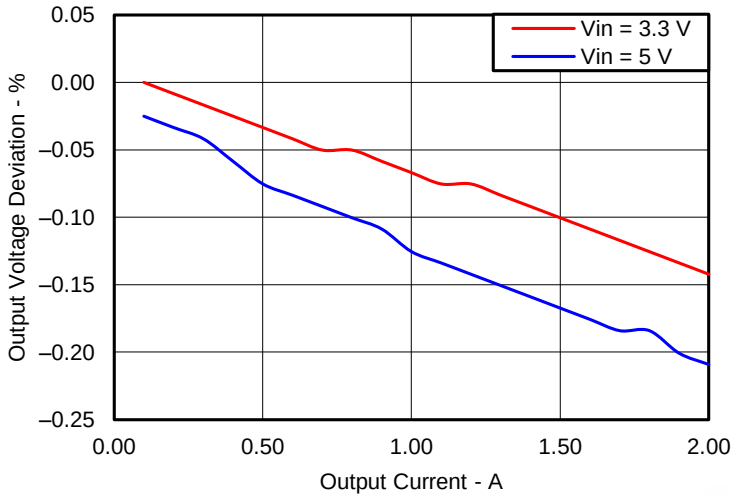


Figure 2. TPS57112EVM Load Regulation

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2.4 Output-Voltage Line Regulation

Figure 3 shows the line regulation for the TPS57112Q1EVM at room temperature and I_{LOAD} = 1 A.

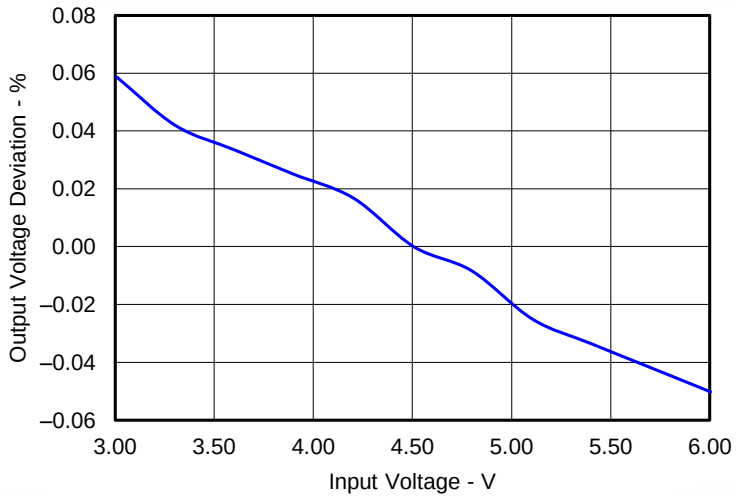


Figure 3. TPS57112EVM Line Regulation

2.5 Load Transients

Figure 4 shows the TPS57112EVM response to a load step. The current step is from 25% to 75% of maximum rated load at 5 V input.

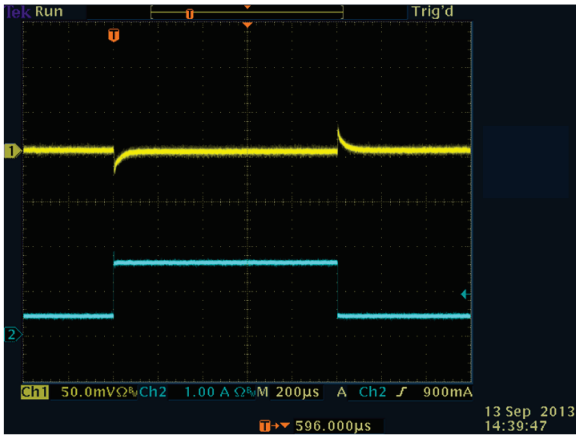


Figure 4. TPS57112EVM Load Transient

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2.6 Loop Response

Figure 5 shows the TPS57112EVM loop-response characteristics. Gain and phase plots are shown for a V_{IN} voltage of 5 V and a load current of 1 A.

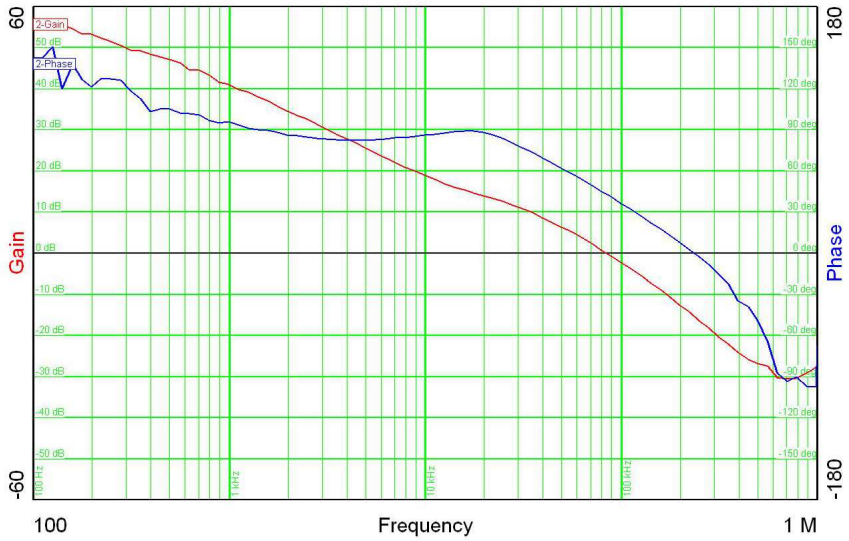


Figure 5. TPS57112EVM Loop-Response Measurement

2.7 Output Voltage Ripple

Figure 6 shows the TPS57112EVM output voltage ripple. The output current is the rated full load current of 2 A and V_{IN} = 5 V. The ripple voltage is measured directly across the output capacitors.

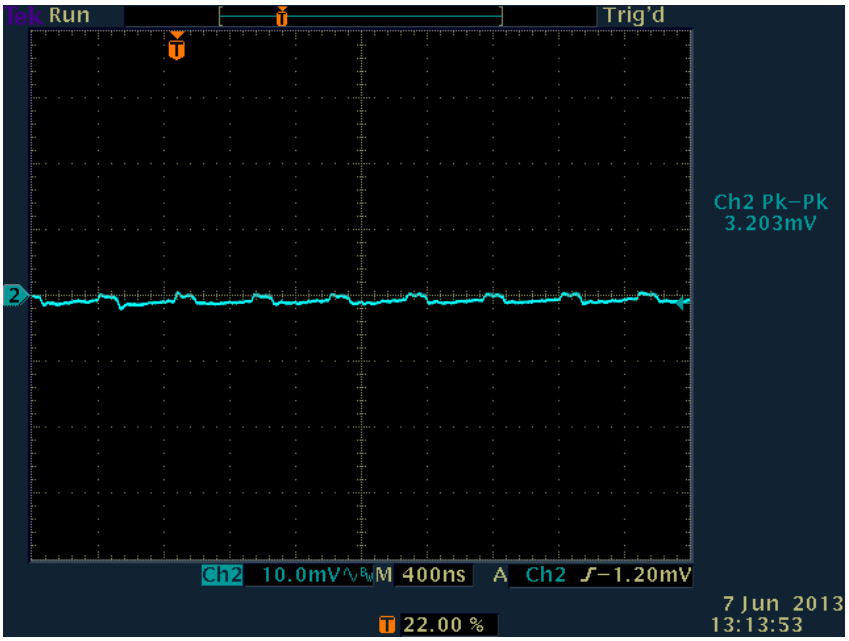


Figure 6. TPS57112EVM Output Ripple

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2.8 Power Up

Figure 7 and Figure 8 show the start-up waveforms for the TPS57112EVM. In Figure 8, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R_3 and R_4 resistor divider network. In Figure 9, the input voltage is applied initially and the output is inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins, and the output voltage ramps up to the externally set value of 1.2 V. The input voltage for these plots is 5 V and the load is 1 Ω.

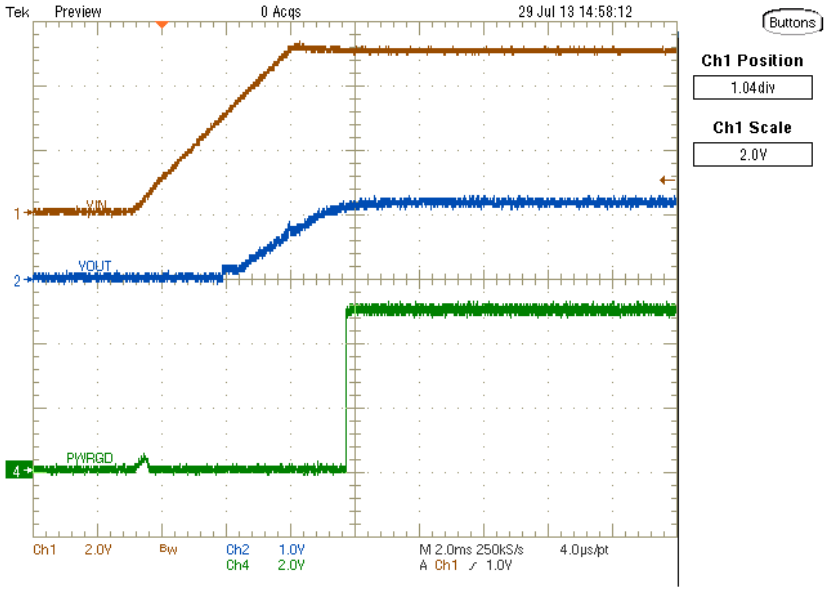


Figure 7. TPS57112EVM Startup Relative to V_{IN}

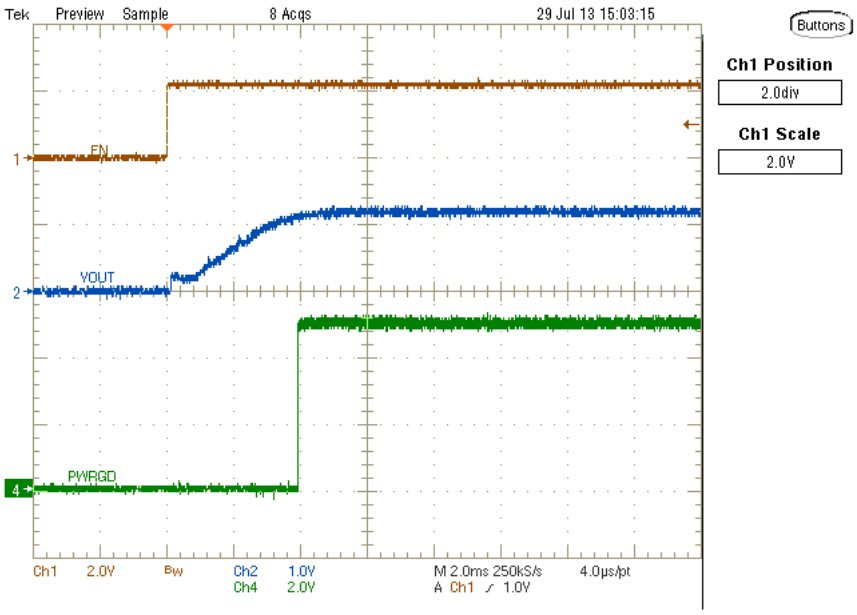


Figure 8. TPS57112EVM Startup Relative to Enable

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3 Board Layout

This section provides a description of TPS57112EVM board layout and layer illustrations.

3.1 Layout

Figure 9, Figure 10, Figure 11, and Figure 12 show the board layout for the TPS57112EVM.

The top-side layer of the EVM contains the main traces for V_{IN}, V_{OUT}, and V_{PH}. Also on the top-side layer are connections for the remaining pins of the TPS57112-Q1 device and a large area filled with ground. The bottom-side layer contains some components and another large area filled with ground. The top-side ground areas are connected to the bottom ground plane with multiple vias placed around the board including four vias directly under the TPS57112-Q1 device to provide a thermal path from the top-side ground area to the bottom-side ground plane.

The input decoupling capacitors (C2, C3, C4, and C5) and bootstrap capacitor (C11) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also located close to the IC on the bottom of the board. For the TPS57112-Q1 device, an additional input bulk capacitor can be required depending on the EVM connection to the input supply.

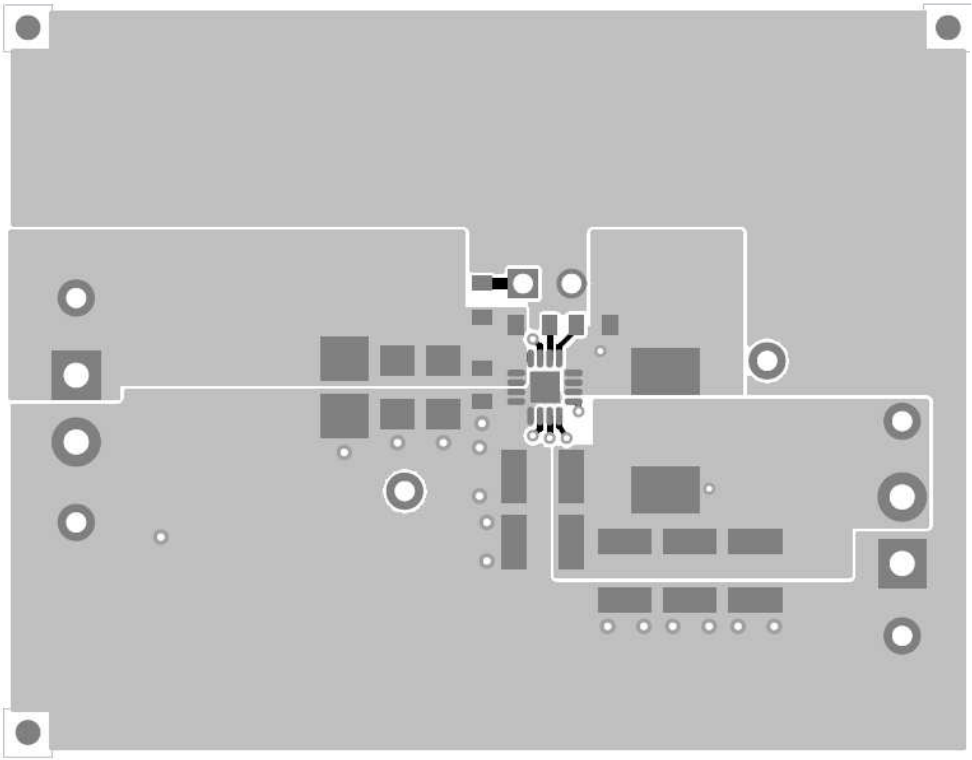


Figure 9. TPS57112EVM Top-Side Layout

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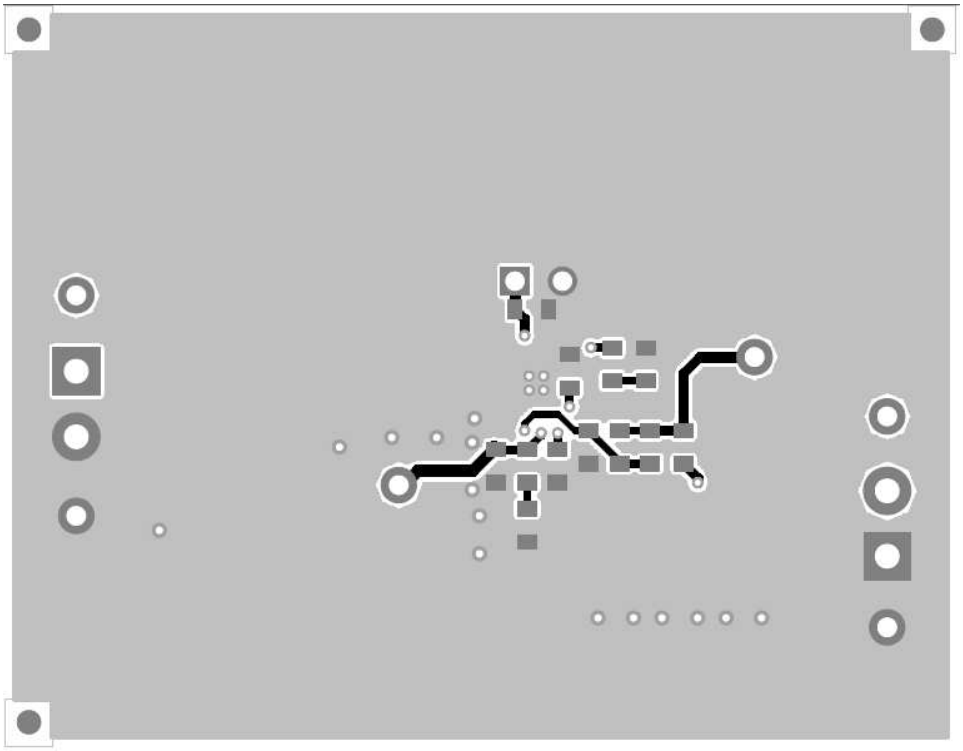


Figure 10. TPS57112EVM Bottom-Side Layout

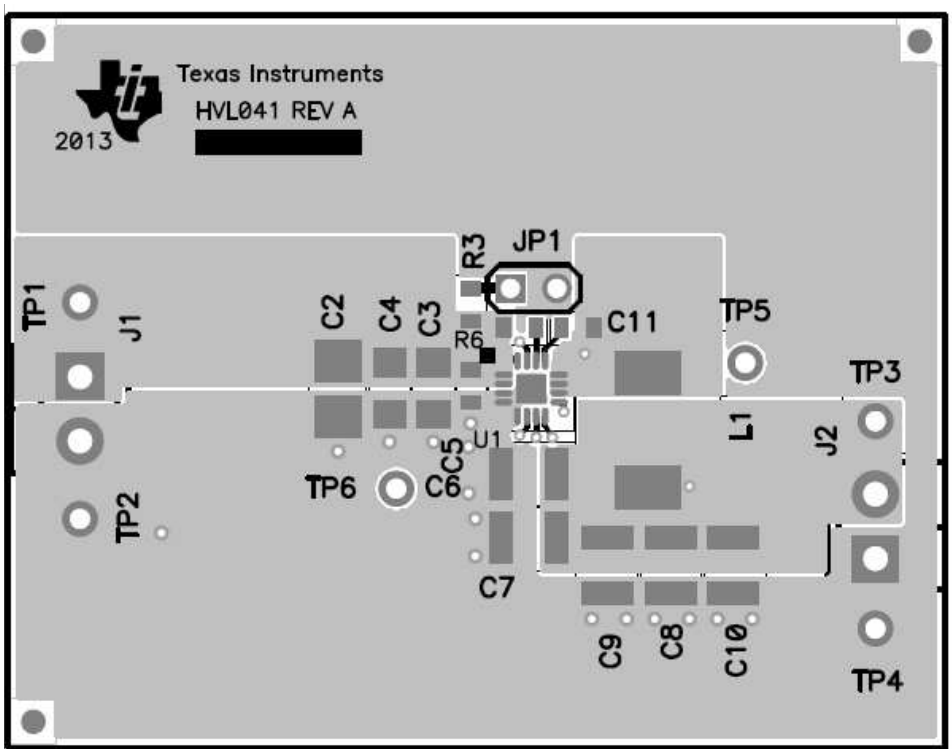


Figure 11. TPS57112EVM Top-Side Assembly

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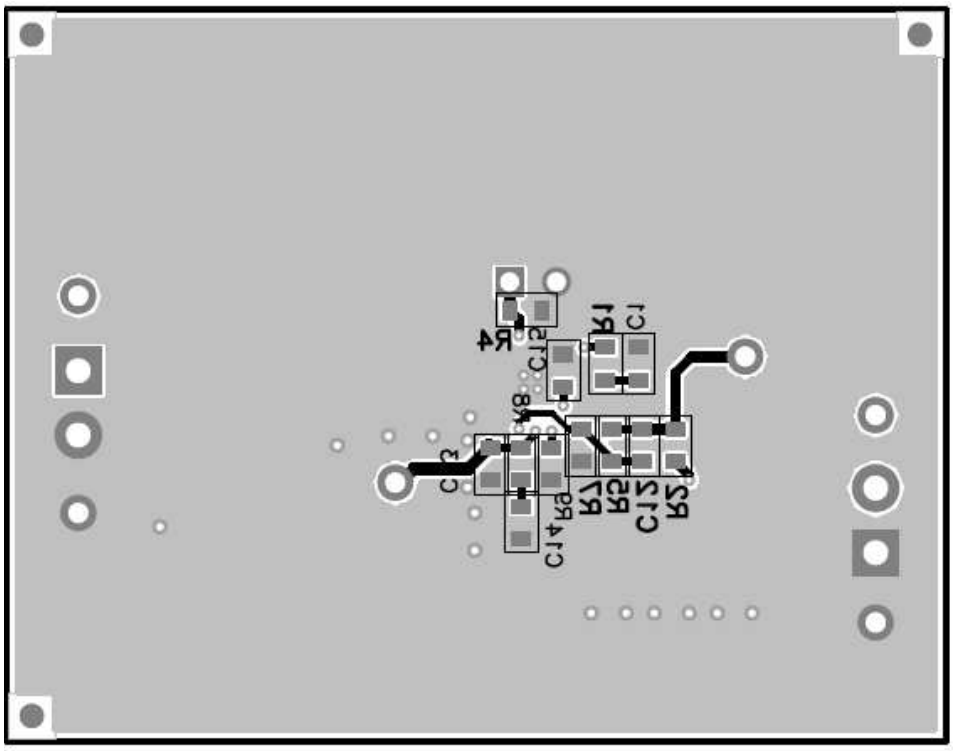


Figure 12. TPS57112EVM Bottom-Side Assembly

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4 Schematic and Bill of Materials

4.1 Schematic

Figure 13 is the schematic of the TPS57112EVM.

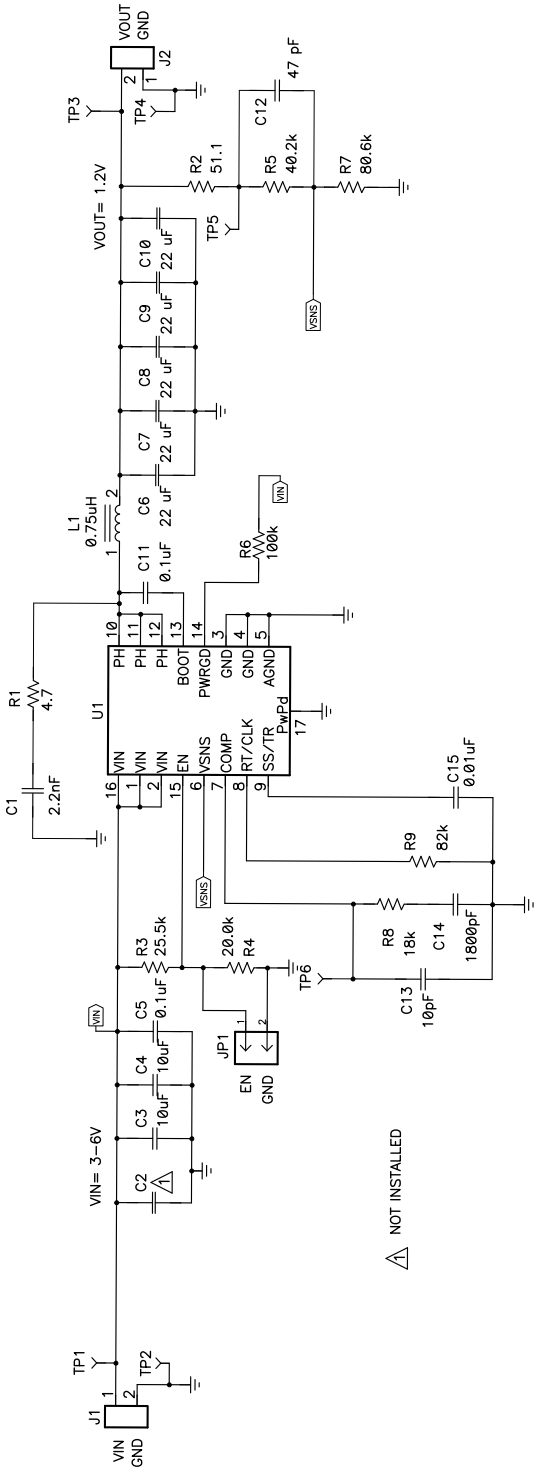


Figure 13. TPS57112EVM Schematic

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4.2 Bill of Materials

Table 5 lists the bill of materials for the TPS57112EVM.

Table 5. TPS57112EVM Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	2.2 nF	Capacitor, Ceramic, 16 V, X7R, 10%	603	GRM188R71C222KA01D-ND	Murata
0	C2	Open	Capacitor, Ceramic	Multi sizes	Engineering Only	Standard
2	C3, C4	10 µF	Capacitor, Ceramic, 10 V, X5R, 20%	1206	C3216X5R1A106M160AB	TDK
2	C5, C11	0.1 µF	Capacitor, Ceramic, 25 V, X5R, 10%	603	C1608X5R1H104K080AA	TDK
5	C6, C7, C8, C9, C10	22 µF	Capacitor, Ceramic, 10 V, X5R, 20%	1210	C3225X5R1A226M230AA	TDK
1	C12	47 pF	Capacitor, Ceramic, 50 V, C0G, 5%	603	C1608C0G1H470J080AA	TDK
1	C13	10 pF	Capacitor, Ceramic, 50 V, C0G	603	C1608C0G1H100D080AA	TDK
1	C14	1800 pF	Capacitor, Ceramic, 50 V, X7R, 10%	603	GRM188R71H182KA01D	Murata
1	C15	0.01 µF	Capacitor, Ceramic, 16 V, X7R, 15%	603	GRM188R71C103KA01D	Murata
2	J1, J2	ED555/2DS	Terminal Block, 2-pin, 6 A, 3,5 mm	0.27 × 0.25 inch	ED555/2DS	OST
1	JP1	PEC02SAAN	Header, Male 2-pin, 100-mil spacing	0.100 inch × 2	PEC36SAAN	Sullins
1	L1	0.75 µH	Inductor, SMT, 10 A, 7.5 mΩ	0.255 x 0.270 inch	FDV0630-R75M	TOKO
1	R1	4.7	Resistor, Chip, 1/16 W, 1%	603	CRCW06034R70FNEA	Vishay
1	R2	51.1	Resistor, Chip, 1/16 W, 1%	603	3-1879335-7	TE
1	R3	25.5k	Resistor, Chip, 1/16 W, 1%	603	9-1879337-8	TE
1	R4	20.0k	Resistor, Chip, 1/16 W, 1%	603	8-1879337-8	TE
1	R5	40.2k	Resistor, Chip, 1/16 W, 1%	603	1-1879338-8	TE
1	R6	100k	Resistor, Chip, 1/16 W, 1%	603	5-1879338-6	TE
1	R7	80.6k	Resistor, Chip, 1/16 W, 1%	603	4-1879338-7	TE
1	R8	18.0k	Resistor, Chip, 1/16 W, 1%	603	8-1879337-4	TE
1	R9	82k	Resistor, Chip, 1/16 W, 1%	603	1623002-2	TE
4	TP1, TP2, TP5, TP6	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
2	TP3, TP4	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keystone
1	—	—	Shunt, 100-mil, Black	0.1	929950-00	3M
1	U1	TPS57112-Q1	IC, DC-DC Converter, 2.95 V to 6 V, 2 A	QFN-16	TPS57112QRTERQ1	TI
1	—	—	PCB, 2 inch × 1.5 inch × 0.062 inch	—	HVL041-001	Any

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