

# BTLC1000ZR-XPRO PCB Specification

## Table of Contents

<b>1</b>	<b>GENERAL INFORMATION.....</b>	<b>3</b>
<b>1.1</b>	<b>Board identification.....</b>	<b>3</b>
<b>1.2</b>	<b>Contact persons for PCB issues. ....</b>	<b>3</b>
<b>2</b>	<b>PCB SPECIFICATION .....</b>	<b>3</b>
<b>2.1</b>	<b>Manufacturing data .....</b>	<b>3</b>
<b>2.2</b>	<b>Layer stackup .....</b>	<b>4</b>
<b>2.3</b>	<b>Gerber files.....</b>	<b>4</b>
<b>2.4</b>	<b>Special via considerations .....</b>	<b>5</b>
<b>2.5</b>	<b>Placement of fabrication ID mark .....</b>	<b>5</b>
<b>3</b>	<b>PANELIZING.....</b>	<b>5</b>
<b>4</b>	<b>QUALITY OF SILKSCREEN LAYERS .....</b>	<b>5</b>

## 1 General information

### 1.1 Board identification

Name: BTLC1000ZR-XPRO

Board identification number: A08-2579 Rev 2

### 1.2 Contact persons for PCB issues.

- Manager: Karthik Narayana, karthik.narayana@atmel.com, +91 44 4540 1189
- CAD Engineer: Thangaraj, Thangaraj.vellaichamy@atmel.com, +91 44 4540 1190

## 2 PCB specification

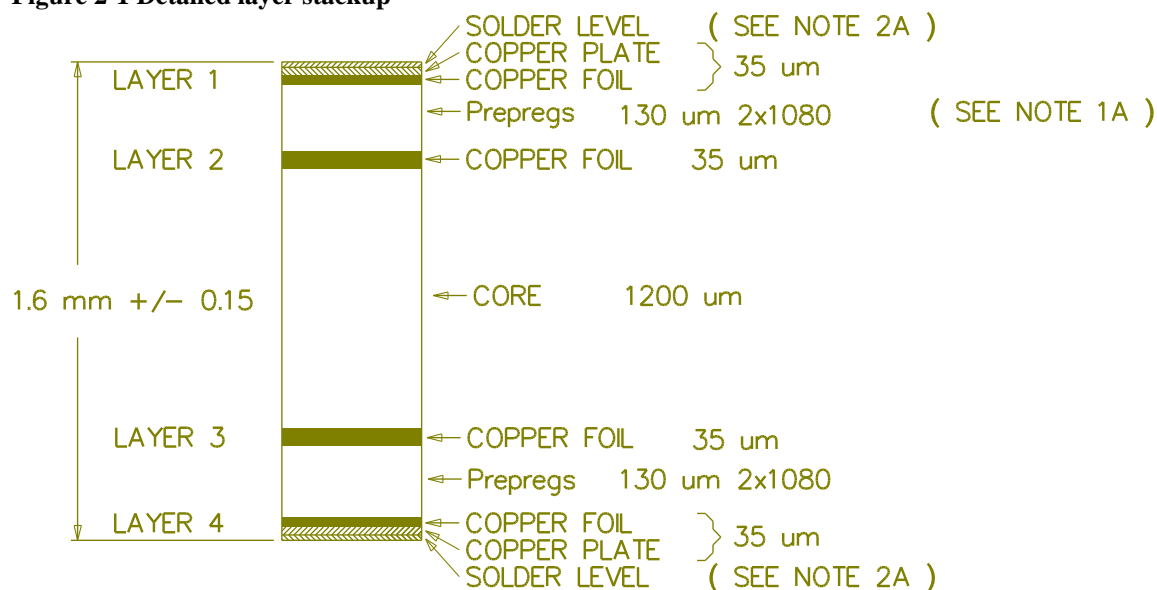
### 2.1 Manufacturing data

- Size: 66.5mm x 30 mm
- PCB material: FR-4, 1.6mm thickness
- Layers: 4
- Finish: ENIG
- Minimum via hole size: 0.3mm
- Minimum via pad size: 0.6mm
- Minimum track width: 0.2mm
- Minimum spacing: 0.15mm
- Solder mask color: Dark BLUE
- Silk-screen color: White

## 2.2 Layer stackup

Figure 2-1 shows the detailed layer stackup for this PCB.

**Figure 2-1 Detailed layer stackup**



NOTE 1A: DIELECTRIC FR4  
2A: SURFACE PROTECTION: Chemical Gold

THE BOARD MUST BE RoHS COMPLIANT

## DETAIL A ( CROSS-SECTION )

SCALE = NONE

## 2.3 Gerber files

**Table 2-1 Layer stackup corresponding Gerber files (listed from top to bottom)**

File name	Description
A08-2579_pcb_rev2.GTP	Gerber file for top paste-mask
A08-2579_pcb_rev2.GTO	Gerber file for top overlay (silkscreen)
A08-2579_pcb_rev2.GTS	Gerber file for top solder-mask
A08-2579_pcb_rev2.GTL	Gerber file for top layer - L1
A08-2579_pcb_rev2.GP1	Gerber file for internal plane layer -L2 (GND layer-Negative)
A08-2579_pcb_rev2.G1	Gerber file for internal layer- L3
A08-2579_pcb_rev2.GBL	Gerber file for bottom signal layer -L4
A08-2579_pcb_rev2.GBS	Gerber file for bottom solder-mask
A08-2579_pcb_rev2.GBO	Gerber file for bottom overlay (silkscreen)
A08-2579_pcb_rev2.GM1	Gerber file for mechanical 1 layer (board outline)
A08-2579_pcb_rev2.DRR	Drill file report
A08-2579_pcb_rev2.txt	Hole Drill file

## **2.4 *Special via considerations***

All plated through holes with solder mask covered area need to be Tented /filled on both side of the PCB with solder mask.

## **2.5 *Placement of fabrication ID mark***

The fabrication ID mark should be placed on the bottom Silk layer

# **3 Panelizing**

When making panels for this board the following issues should be considered.

- Fiducial marks should be placed on the panel.

# **4 Quality of silkscreen layers**

The silkscreen layers for the PCB must be of high quality for several reasons:

- Very small text is used
- Text is close to pads and therefore the mask must be centered properly on the board
- The PCB is used for development boards and therefore the silkscreen is an essential part of the overall product quality.