

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

General Description

The MAX9702 combines a highly efficient Class D speaker amplifier with a high-linearity Class AB headphone amplifier. This ensures maximum battery life in speaker mode and maximum performance in headphone mode. The MAX9702 delivers up to 1.1W per channel into an 8Ω load and 1.8W into a 4Ω load from a 5V power supply. Maxim's 2nd-generation, spread-spectrum modulation scheme renders the traditional Class D output filter unnecessary.

The MAX9702 speaker amplifier offers two modulation schemes: a fixed-frequency (FFM) mode and a spread-spectrum (SSM) mode that reduces EMI-radiated emissions. The MAX9702 speaker amplifier features a fully differential architecture, full-bridged (BTL) output, and comprehensive click-and-pop suppression. The MAX9702 speaker amplifier features high 75dB PSRR, low 0.07% THD+N, and SNR in excess of 97dB. Short-circuit and thermal-overload protection prevent the device from being damaged during a fault condition.

The headphone amplifier uses Maxim's DirectDrive™ architecture that produces a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors, saving cost, board space, and component height. A high 80dB PSRR and low 0.02% THD+N ensures clean, low-distortion amplification of the audio signal.

An I²C interface sets the speaker and headphone gain, mono, stereo, and mute functions.

The MAX9702 is available in a 28-pin thin QFN-EP (5mm x 5mm x 0.8mm) package. The MAX9702 is specified over the extended -40°C to +85°C temperature range.

Applications

Cellular Phones
Notebook PCs
PDAs
Handheld Gaming Consoles

Pin Configurations appear at end of data sheet.

Features

- ◆ Spread-Spectrum Modulation Reduces EMI Emissions
- ◆ Programmable Mono, Stereo, Mute, and Mix Functions
- ◆ 1.1W Stereo Output (8Ω, V_{DD} = 5V)
- ◆ 48mW Headphone Output (32Ω, V_{DD} = 3.3V)
- ◆ 1.8W Stereo Output (4Ω, V_{DD} = 5V)
- ◆ 94% Efficiency (R_L = 8Ω, P_O = 1.1W)
- ◆ High 73dB PSRR (f = 217Hz)
- ◆ I²C Programmable Gain Up to +21dB
- ◆ Integrated Click-and-Pop Suppression
- ◆ Low-Power Shutdown Mode (0.1μA)
- ◆ Short-Circuit and Thermal-Overload Protection
- ◆ ±8kV (HBM) ESD-Protected Headphone Driver Outputs

Ordering Information

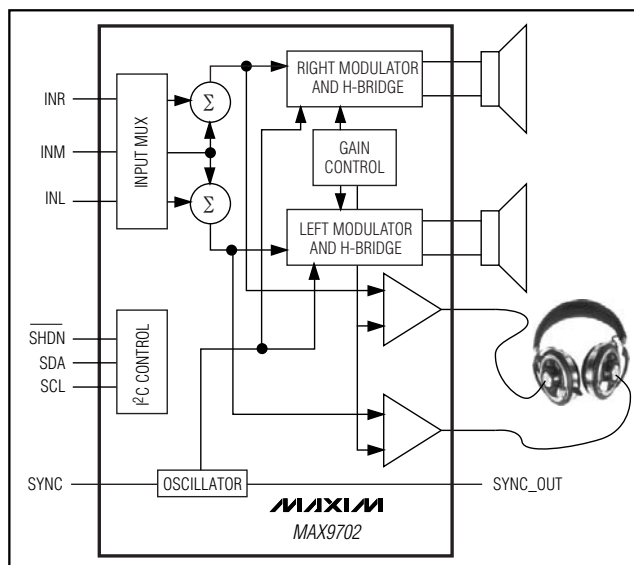
PART	PIN-PACKAGE	I ² C SLAVE ADDRESS	PKG CODE
MAX9702ETI+	28 TQFN-EP*	1001100	T2855-6
MAX9702BETI+	28 TQFN-EP*	1001110	T2855-6

Note: All devices specified for -40°C to +85°C operating temperature range.

*EP = Exposed paddle.

+ Denotes lead-free package.

Simplified Block Diagram



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ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	+6V
PV _{DD} to PGND	+6V
CPV _{DD} to CPGND	+6V
CPV _{SS} to V _{SS}	±0.3V
CPV _{SS} to CPGND	-6V to +0.3V
V _{SS} to CPGND	-6V to +0.3V
C1N	(CPV _{SS} - 0.3V) to (CPGND + 0.3V)
C1P	(CPGND - 0.3V) to (CPV _{DD} + 0.3V)
HP ₋ to GND	(CPV _{SS} - 0.3V) to (CPV _{DD} + 0.3V)
GND to PGND and CPGND	±0.3V
V _{DD} to PV _{DD} and CPV _{DD}	±0.3V
SDA, SCL to GND	-0.3V to +6V
All Other Pins to GND	-0.3V to (V _{DD} + 0.3V)
Continuous Current In/Out of PV _{DD} , PGND, CPV _{DD} , CPGND, OUT ₋	±600mA

Continuous Current In/Out of HP ₋	±120mA
Continuous Input Current CPV _{SS}	+260mA
Continuous Input Current (all other pins)	±20mA
Duration of OUT ₋ Short Circuit to GND or PV _{DD}	Continuous
Duration of Short Circuit Between OUT ₋	Continuous
Duration of HP ₋ Short Circuit to GND or PV _{DD}	Continuous
Continuous Power Dissipation (T _A = +70°C) 28-Pin Thin QFN (derate 21.3mW/°C above +70°C)	1702mW
Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V)

(V_{DD} = PV_{DD} = CPV_{DD} = $\overline{\text{SHDN}}$ = 3.3V, GND = PGND = CPGND = 0V, SYNC = V_{DD} (SSM), speaker gain = +12dB, headphone gain = +1dB. Speaker load R_L connected between OUT+ and OUT-, unless otherwise noted, R_L = ∞. Headphone load R_{LH} connected between HPR/HPL to GND. C_{BIAS} = 1μF to GND, 1μF capacitor between C1P and C1N, C_{VSS} = 1μF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply Voltage Range	V _{DD}	Inferred from PSRR test	2.5		5.5	V
Quiescent Current	I _{DD}	HPS = GND, speaker mode		10	15	mA
		HPS = V _{DD} , headphone mode		7	11	mA
Shutdown Current	I _{SHDN}	Hard shutdown, $\overline{\text{SHDN}}$ = GND		0.1	10	μA
		Soft shutdown (see f ² C section)		22	30	
Input Resistance	R _{IN}	Stereo left and right	16.5	24	31.5	kΩ
		Mono channel	8.4	12	15.6	
Debounce Delay	t _{DEBOUNCE}	Delay from HPS transition to headphone/speaker turn-on		65		ms
Turn-On Time	t _{ON}	Time from $\overline{\text{SHDN}}$ transition to full operation				
		HPS = GND (SP mode)		85		ms
		HPS = V _{DD} (HP mode)		85		
Turn-Off Time	t _{OFF}			0		ms
Input Bias Voltage	V _{BIAS}		1.125	1.25	1.375	V
SPEAKER AMPLIFIERS (HPS = GND)						
Output Offset Voltage	V _{OS}	T _A = +25°C		±9	±40	mV
		T _{MIN} to T _{MAX}			±50	
Power-Supply Rejection Ratio (Note 3)	PSRR	V _{DD} = 2.5V to 5.5V	54	75		dB
		100mV _{p-p} ripple, V _{IN} = 0V, T _A = +25°C		75		
		f _{RIPPLE} = 217Hz				
		f _{RIPPLE} = 20kHz		55		

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ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V) (continued)

(V_{DD} = P_{VDD} = CP_{VDD} = $\overline{\text{SHDN}}$ = 3.3V, GND = PGND = CPGND = 0V, SYNC = V_{DD} (SSM), speaker gain = +12dB, headphone gain = +1dB. Speaker load R_L connected between OUT+ and OUT-, unless otherwise noted, R_L = ∞. Headphone load R_{LH} connected between HPR/HPL to GND. C_{BIAS} = 1μF to GND, 1μF capacitor between C1P and C1N, C_{VSS} = 1μF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Power	P _{OUT}	THD+N = 1%, T _A = +25°C, f = 1kHz, V _{DD} = 3.3V		R _L = 8Ω	470			mW
				R _L = 4Ω	700			
Total Harmonic Distortion Plus Noise	THD+N	R _L = 8Ω (P _{OUT} = 400mW), f = 1kHz			0.07			%
		R _L = 4Ω (P _{OUT} = 600mW), f = 1kHz			0.13			
Signal-to-Noise Ratio	SNR	V _{OUT} = 2V _{RMS} , R _L = 8Ω	BW = 22Hz to 22kHz	FFM	86.5			dB
				SSM	87.5			
		A-weighted	FFM	91.5				
			SSM	91.5				
Oscillator Frequency	f _S	SYNC = GND			1000	1100	1200	kHz
		SYNC = float			1250	1340	1450	
		SYNC = V _{DD}			1150 ±50			
SYNC Frequency Lock Range	f _{SYNC}				1000	2000		kHz
SYNC_OUT Capacitance Drive	C _{SYNC_OUT}				100			pF
Click-and-Pop Level	K _{CP}	Peak voltage, 32 samples/second, A-weighted (Note 3)		Into shutdown	56			dB
				Out of shutdown	48			
Efficiency	η	P _{OUT} = 2 x 500mW, f _{IN} = 1kHz, R _L = 8Ω, L = 68μH			94			%
Gain (see f _C Section)	A _V	B2 = 0	B1 = 0	B0 = 0	0			dB
		B2 = 0	B1 = 0	B0 = 1	+3			
		B2 = 0	B1 = 1	B0 = 0	+6			
		B2 = 0	B1 = 1	B0 = 1	+9			
		B2 = 1	B1 = 0	B0 = 0	+12			
		B2 = 1	B1 = 0	B0 = 1	+15			
		B2 = 1	B1 = 1	B0 = 0	+18			
		B2 = 1	B1 = 1	B0 = 1	+21			
Channel-to-Channel Gain Tracking					±0.2			%
Crosstalk		L to R, R to L, f = 10kHz, R _L = 8Ω, P _{OUT} = 300mW			65			dB

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ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V) (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = $\overline{\text{SHDN}}$ = 3.3V, GND = PGND = CPGND = 0V, SYNC = V_{DD} (SSM), speaker gain = +12dB, headphone gain = +1dB. Speaker load R_L connected between OUT+ and OUT-, unless otherwise noted, R_L = ∞. Headphone load R_{LH} connected between HPR/HPL to GND. C_{BIAS} = 1μF to GND, 1μF capacitor between C1P and C1N, C_{VSS} = 1μF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
HEADPHONE AMPLIFIERS (HPS = V _{DD})							
Output Offset Voltage	V _{OS}	T _A = +25°C		±1.8	±6	mV	
		T _{MIN} to T _{MAX}			±8		
Power-Supply Rejection Ratio (Note 4)	PSRR	V _{DD} = 2.5V to 5.5V		66	75	dB	
		100mV _{P-P} ripple, V _{IN} = 0V, T _A = +25°C	f _{RIPPLE} = 217Hz	73			
			f _{RIPPLE} = 20kHz	53			
Output Power	P _{OUT}	THD+N = 1%, V _{DD} = 3.3V, T _A = +25°C	R _L = 32Ω	48		mW	
			R _L = 16Ω	47			
Total Harmonic Distortion Plus Noise	THD+N	R _L = 16Ω (P _{OUT} = 40mW, f = 1kHz)		0.03		%	
		R _L = 32Ω (P _{OUT} = 32mW, f = 1kHz)		0.015			
Signal-to-Noise Ratio	SNR	V _{OUT} = 1V _{RMS} , R _L = 32Ω	BW = 22Hz to 22kHz	95.5		dB	
			A-weighted	97.9			
Charge-Pump Frequency	f _{CP}			f _{OSC} /2		kHz	
Click-and-Pop Level	K _{CP}	Peak voltage, 32 samples/second, A-weighted (Note 3)	Into shutdown	65		dB	
			Out of shutdown	85			
Slew Rate	SR	±1V output step		0.3		V/μs	
Gain (see f _C Section)	A _V	B4 = 0	B3 = 0	-2		dB	
		B4 = 0	B3 = 1	+1			
		B4 = 1	B3 = 0	+4			
		B4 = 1	B3 = 1	+7			
Channel-to-Channel Gain Tracking				±0.2		%	
Capacitance Drive	C _L	No sustained oscillations		300		pF	
Crosstalk		L to R, R to L, f = 10kHz, R _L = 16Ω, P _{OUT} = 10mW		70		dB	
HP_ Resistance to GND		In speaker mode		1		kΩ	
DIGITAL INPUTS ($\overline{\text{SHDN}}$, SYNC, SDA, SCL, HPS)							
Input Voltage High, $\overline{\text{SHDN}}$, SYNC, HPS	V _{INH}			2		V	
Input Voltage High, SCL	V _{INH}			0.7 x V _{DD}		V	
Input Voltage Low, $\overline{\text{SHDN}}$, SYNC, HPS	V _{INL}			0.8		V	

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ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V) (continued)

(V_{DD} = P_{VDD} = CP_{VDD} = $\overline{\text{SHDN}}$ = 3.3V, GND = PGND = CPGND = 0V, SYNC = V_{DD} (SSM), speaker gain = +12dB, headphone gain = +1dB. Speaker load R_L connected between OUT+ and OUT-, unless otherwise noted, R_L = ∞. Headphone load R_{LH} connected between HPR/HPL to GND. C_{BIAS} = 1μF to GND, 1μF capacitor between C1P and C1N, C_{VSS} = 1μF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Low, SDA, SCL	V _{INL}				0.3 x V _{DD}	V
Input Hysteresis, SDA, SCL	V _{HYS}			0.05 x V _{DD}		V
Input Capacitance SDA, SCL	C _{IN}			10		pF
Input Leakage Current, $\overline{\text{SHDN}}$, SCL	I _{IN}				±1	μA
Input Leakage Current, HPS	I _{IN}			±10		μA
SYNC Input Current		In play mode		25		μA
HPS Pullup Resistance				600		kΩ
DIGITAL OUTPUTS (SYNC_OUT)						
Output Voltage High	V _{OH}	I _{OH} = 3mA	2.4			V
Output Voltage Low	V _{OL}	I _{OL} = 3mA			0.4	V
Output Fall Time, SDA	t _F				300	ns

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V)

(V_{DD} = P_{VDD} = CP_{VDD} = $\overline{\text{SHDN}}$ = 5V, GND = PGND = CPGND = 0V, SYNC = V_{DD} (SSM), speaker gain = +12dB, headphone gain = +1dB. Speaker load R_L connected between OUT+ and OUT-, unless otherwise noted, R_L = ∞. Headphone load R_{LH} connected between HPR/HPL to GND. C_{BIAS} = 1μF to GND, 1μF capacitor between C1P and C1N, C_{VSS} = 1μF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Quiescent Current	I _{DD}	HPS = GND, speaker mode		14		mA	
		HPS = V _{DD} , headphone mode		8			
Shutdown Current	I _{SHDN}	Hard shutdown, $\overline{\text{SHDN}}$ = GND		0.2		μA	
		Soft shutdown (see <i>I²C</i> section)		25			
SPEAKER AMPLIFIERS (HPS = GND)							
Power-Supply Rejection Ratio (Note 3)	PSRR	100mV _{P-P} ripple, V _{IN} = 0V, T _A = +25°C	f _{RIPPLE} = 217Hz		73		dB
			f _{RIPPLE} = 20kHz		50		
Output Power	P _{OUT}	THD+N = 1%, T _A = +25°C, f = 1kHz	V _{DD} = 5V	R _L = 8Ω	1100		mW
				R _L = 4Ω	1800		

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ELECTRICAL CHARACTERISTICS (V_{DD} = 5V) (continued)

(V_{DD} = P_{VDD} = CP_{VDD} = $\overline{\text{SHDN}}$ = 5V, GND = PGND = CPGND = 0V, SYNC = V_{DD} (SSM), speaker gain = +12dB, headphone gain = +1dB. Speaker load R_L connected between OUT+ and OUT-, unless otherwise noted, R_L = ∞. Headphone load R_{LH} connected between HPR/HPL to GND. C_{BIAS} = 1μF to GND, 1μF capacitor between C1P and C1N, C_{VSS} = 1μF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	R _L = 8Ω (P _{OUT} = 900mW), f = 1kHz			0.08		%	
		R _L = 4Ω (P _{OUT} = 1500mW), f = 1kHz			0.18			
Signal-to-Noise Ratio	SNR	V _{OUT} = 2V _{RMS} , R _L = 8Ω	BW = 22Hz to 22kHz	FFM	88		dB	
				SSM	87			
			A-weighted	FFM	91			
				SSM	89			
Click-and-Pop Level	K _{CP}	Peak voltage, 32 samples/second, A-weighted (Note 4)	Into shutdown		61.5		dB	
			Out of shutdown		44			
Efficiency	η	P _{OUT} = 1W, f _{IN} = 1kHz, R _L = 8Ω, L = 68μH			95		%	
Channel-to-Channel Gain Tracking					±0.2		%	
Crosstalk		L to R, R to L, f = 10kHz, R _L = 8Ω, P _{OUT} = 300mW			65		dB	
HEADPHONE AMPLIFIERS (HPS = V _{DD})								
Power-Supply Rejection Ratio (Note 4)	PSRR	100mV _{p-p} ripple, V _{IN} = 0V, T _A = +25°C	f _{RIPPLE} = 217Hz		78		dB	
			f _{RIPPLE} = 20kHz		53			
Output Power	P _{OUT}	THD+N = 1%, T _A = +25°C, R _L = 32Ω			45		mW	
Total Harmonic Distortion Plus Noise	THD+N	R _L = 32Ω (P _{OUT} = 32mW, f = 1kHz)			0.03		%	
Signal-to-Noise Ratio	SNR	V _{OUT} = 1V _{RMS} , R _L = 32Ω	BW = 22Hz to 22kHz		94.7		dB	
			A-weighted		97.4			
Click-and-Pop Level	K _{CP}	Peak voltage, 32 samples/second, A-weighted (Notes 3, 4)	Into shutdown		67		dB	
			Out of shutdown		83			
Channel-to-Channel Gain Tracking					±0.2		%	
Crosstalk		L to R, R to L, f = 10kHz, R _L = 32Ω, P _{OUT} = 10mW			70		dB	

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I²C TIMING CHARACTERISTICS

(V_{DD} = P_{VDD} = CP_{VDD} = $\overline{\text{SHDN}}$ = 3.3V, GND = PGND = CPGND = 0V, SYNC = V_{DD} (SSM), speaker gain = +12dB, headphone gain = +1dB. Speaker load R_L connected between OUT+ and OUT-, unless otherwise noted. R_L = ∞. Headphone load R_{LH} connected between HPR/HPL and GND. C_{BIAS} = 1μF to GND, 1μF capacitor between C1P and C1N, C_{VSS} = 1μF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figure 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock	f _{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t _{BUF}		1.3			μs
Hold Time (Repeated) START Condition	t _{HD, STA}		0.6			μs
Repeated START Condition Setup Time	t _{SU, STA}		0.6			μs
STOP Condition Setup Time	t _{SU, STO}		0.6			μs
Data Hold Time	t _{HD, DAT}		0		0.9	μs
Data Setup Time	t _{SU, DAT}		100			ns
SCL Clock Low Period	t _{LOW}		1.3			μs
SCL Clock High Period	t _{HIGH}		0.6			μs
Rise Time of SDA and SCL, Receiving	t _R	(Note 5)	20 + 0.1C _b		300	ns
Fall Time of SDA and SCL, Receiving	t _F	(Note 5)	20 + 0.1C _b		300	ns
Fall Time of SDA, Transmitting	t _F	(Note 5)	20 + 0.1C _b		250	ns
Pulse Width of Spike Suppressed	t _{SP}		0		50	ns
Capacitive Load for Each Bus Line	C _b				400	pF

Note 1: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.

Note 2: Speaker mode testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 4Ω, L = 34μH, R_L = 8Ω, L = 68μH.

Note 3: Amplifier inputs (STEREO/MONO) connected to GND through C_{IN}.

Note 4: Speaker mode testing performed with an 8Ω resistive load in series with a 68μH inductive load connected across BTL output. Headphone mode testing performed with 32Ω resistive load connected to GND. Mode transitions are controlled by $\overline{\text{SHDN}}$. K_{CP} level is calculated as: 20 x log[(peak voltage under normal operation at rated power level)/(peak voltage during mode transition, no input signal)]. Units are expressed in dB.

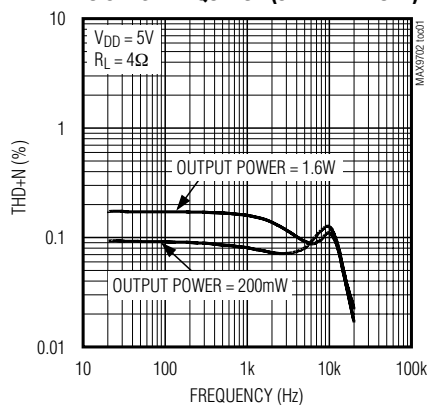
Note 5: C_b = total capacitance of one bus line in pF.

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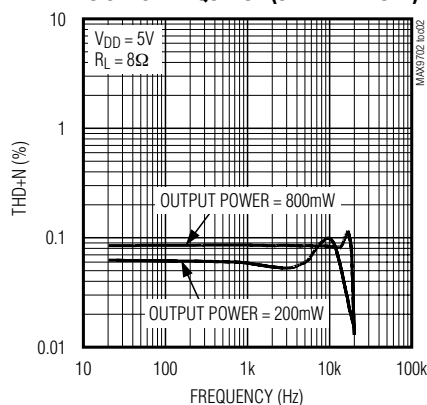
Typical Operating Characteristics

($V_{DD} = PV_{DD} = \overline{SHDN} = 3.3V$, $GND = PGND = 0V$, $SYNC = V_{DD}$ (SSM), speaker gain = 12dB.)

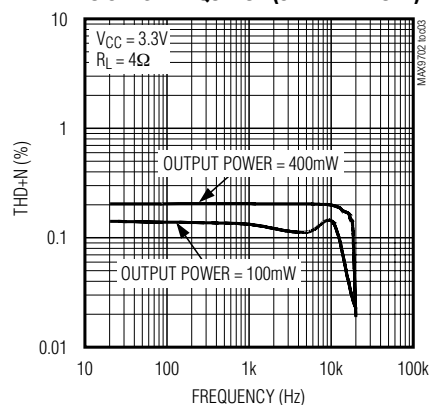
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SPEAKER MODE)



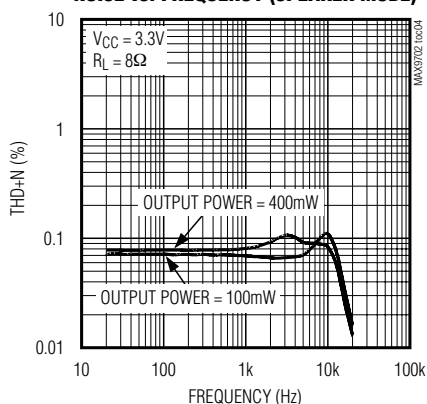
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SPEAKER MODE)



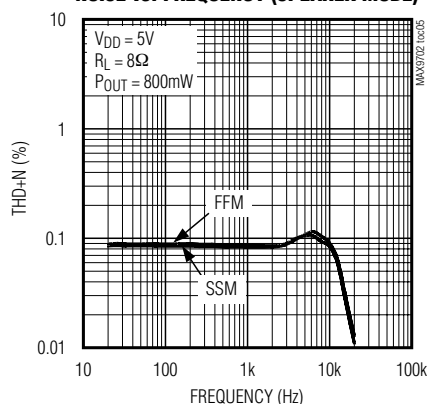
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SPEAKER MODE)



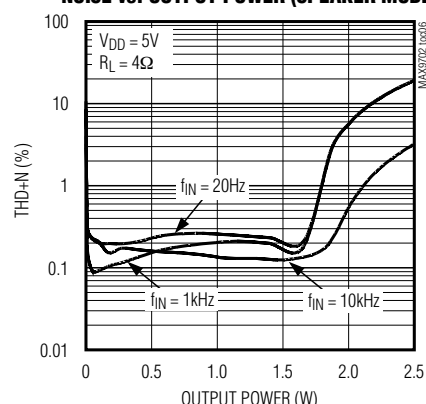
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SPEAKER MODE)



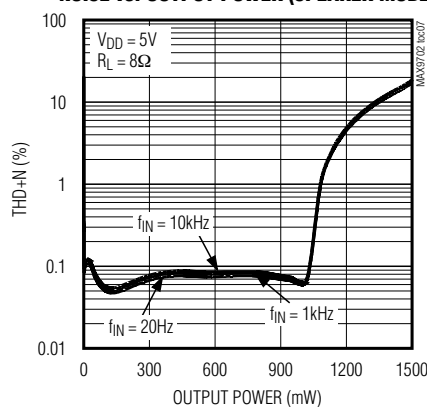
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SPEAKER MODE)



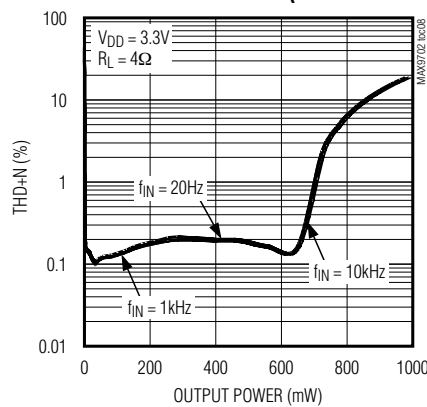
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



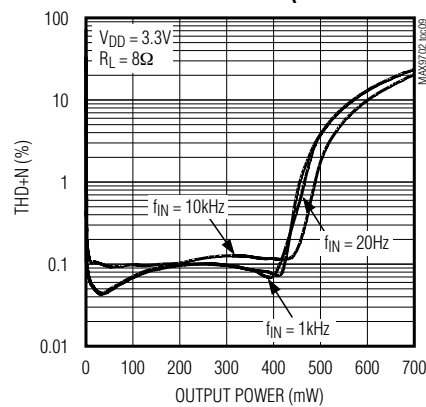
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)

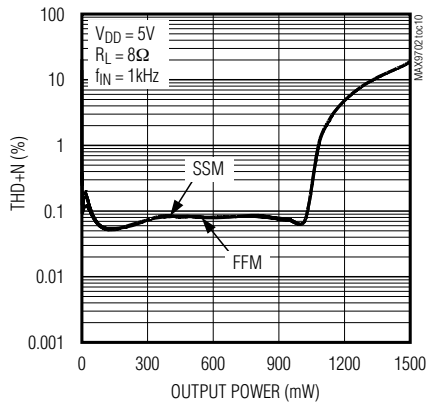


1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

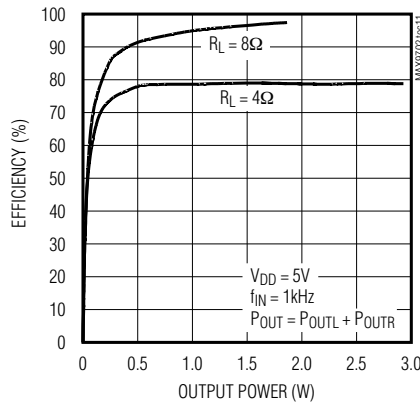
Typical Operating Characteristics (continued)

($V_{DD} = P_{VDD} = \overline{SHDN} = 3.3V$, $GND = PGND = 0V$, $SYNC = V_{DD}$ (SSM), speaker gain = 12dB.)

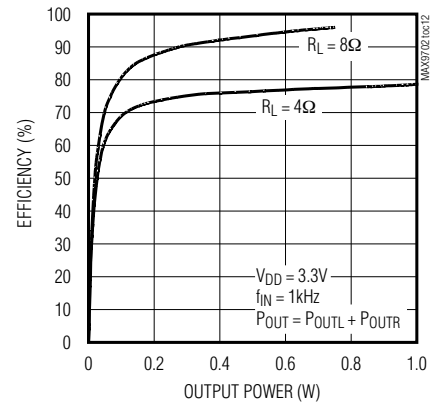
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



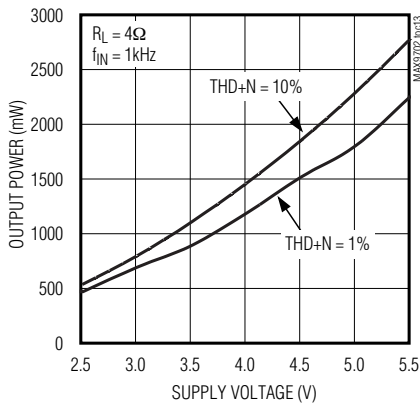
EFFICIENCY vs. OUTPUT POWER (SPEAKER MODE)



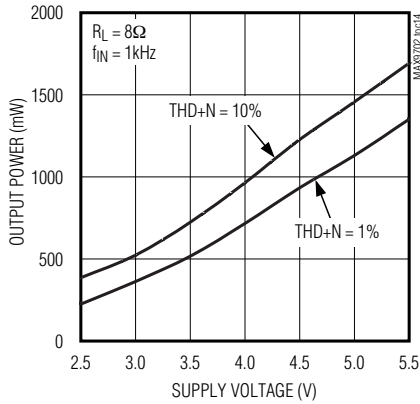
EFFICIENCY vs. OUTPUT POWER (SPEAKER MODE)



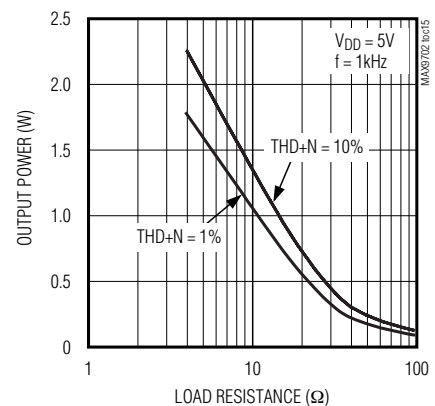
OUTPUT POWER vs. SUPPLY VOLTAGE



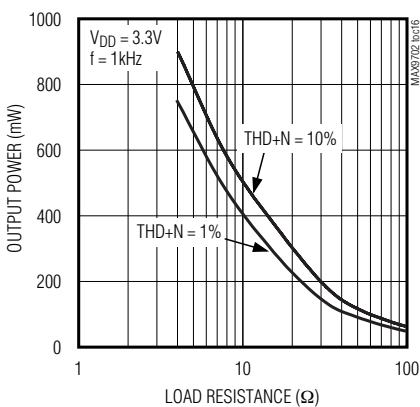
OUTPUT POWER vs. SUPPLY VOLTAGE



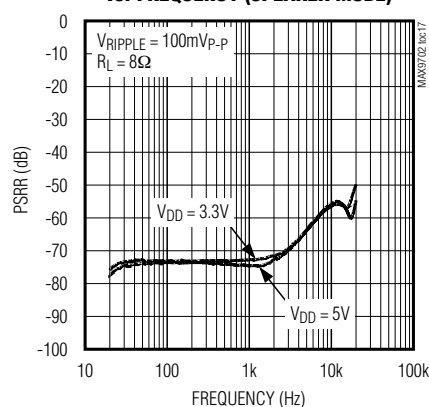
OUTPUT POWER vs. LOAD RESISTANCE



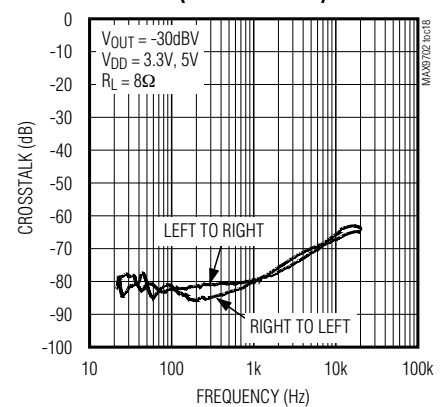
OUTPUT POWER vs. LOAD RESISTANCE



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (SPEAKER MODE)



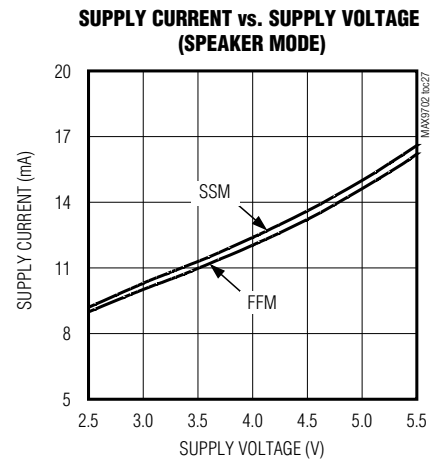
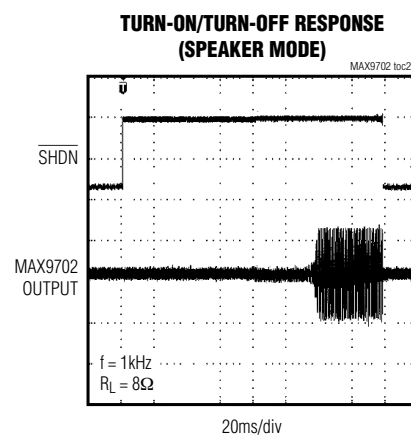
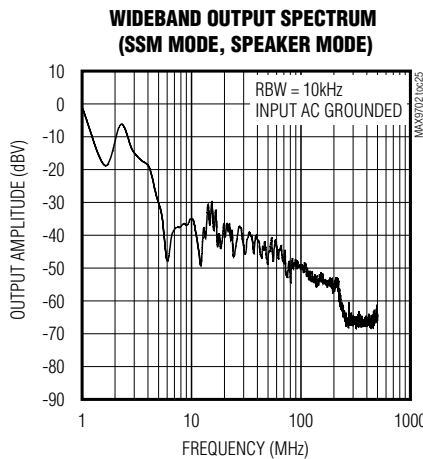
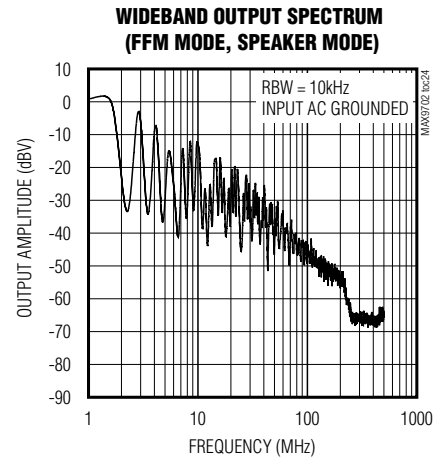
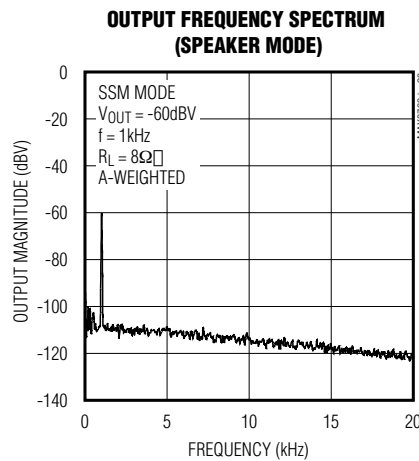
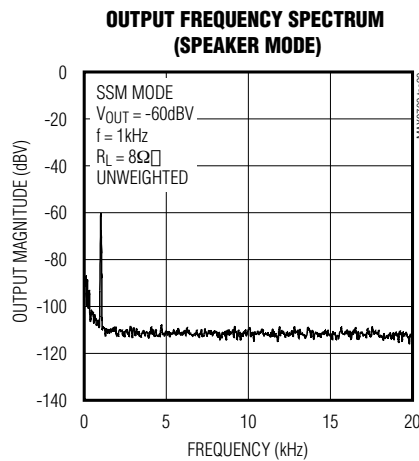
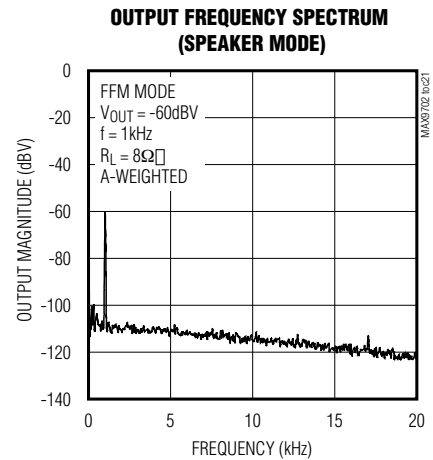
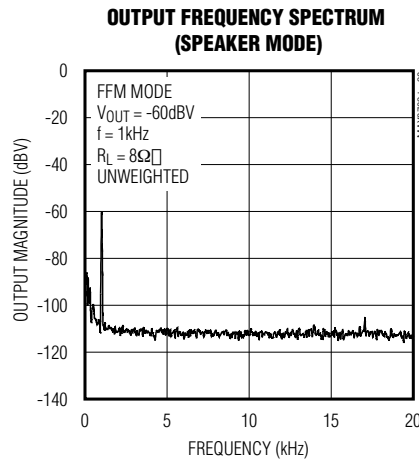
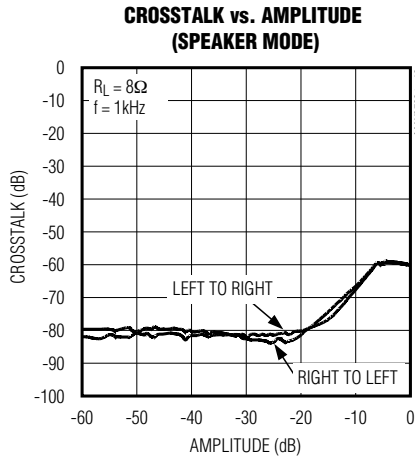
CROSSTALK vs. FREQUENCY (SPEAKER MODE)



1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Typical Operating Characteristics (continued)

($V_{DD} = PV_{DD} = \overline{SHDN} = 3.3V$, $GND = PGND = 0V$, $SYNC = V_{DD}$ (SSM), speaker gain = 12dB.)

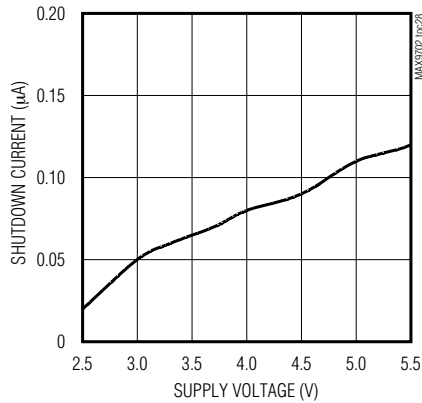


1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

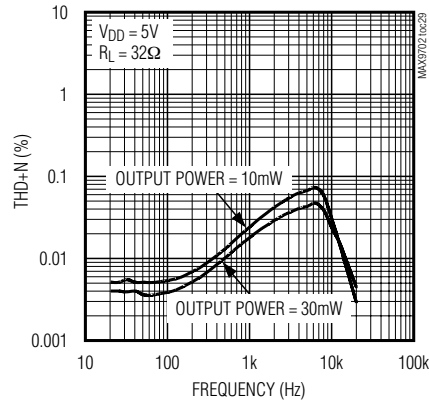
Typical Operating Characteristics (continued)

($V_{DD} = PV_{DD} = \overline{SHDN} = 3.3V$, $GND = PGND = 0V$, $SYNC = V_{DD}$ (SSM), speaker gain = 12dB.)

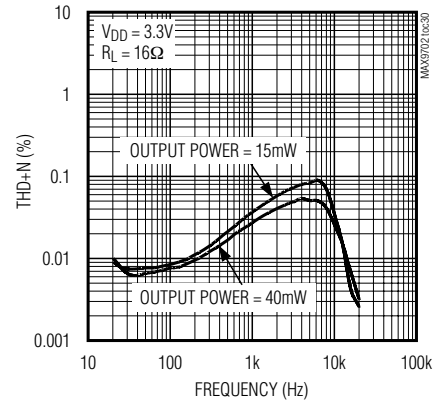
**SHUTDOWN CURRENT vs. SUPPLY VOLTAGE
(SPEAKER MODE)**



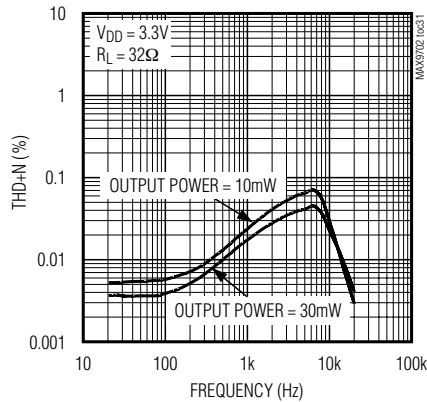
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



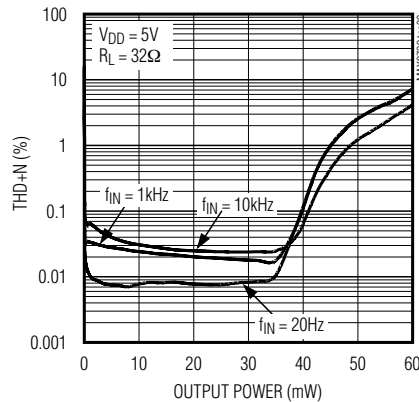
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



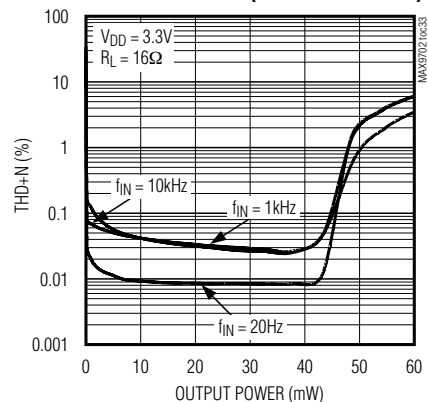
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



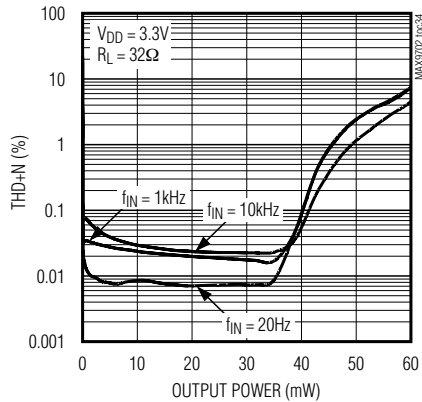
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



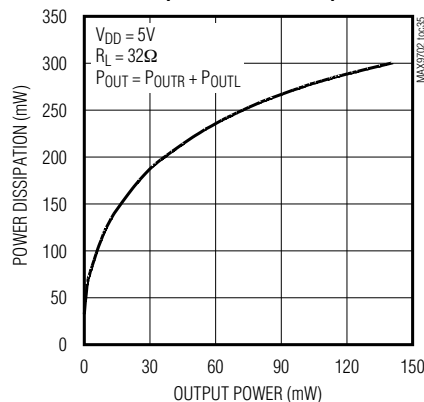
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



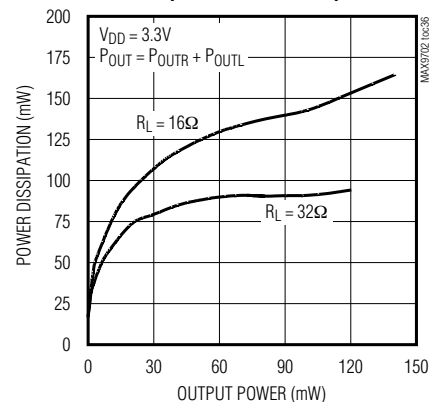
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



POWER DISSIPATION vs. OUTPUT POWER (HEADPHONE MODE)



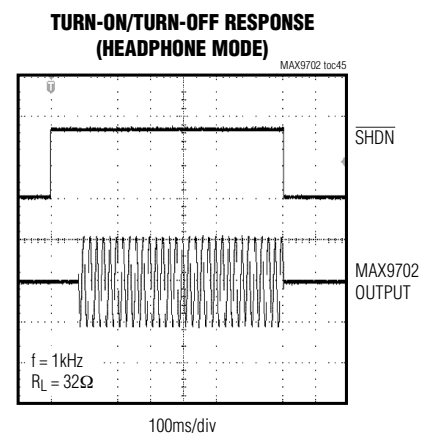
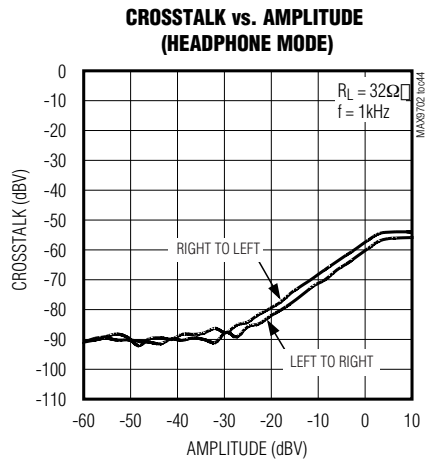
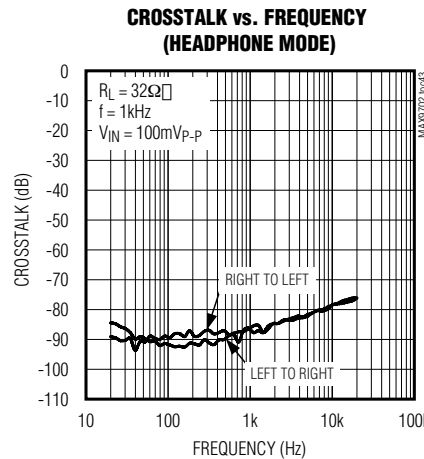
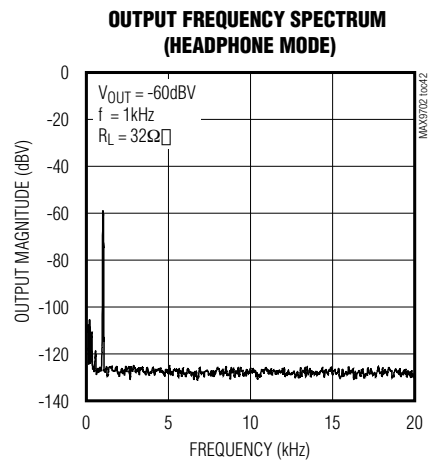
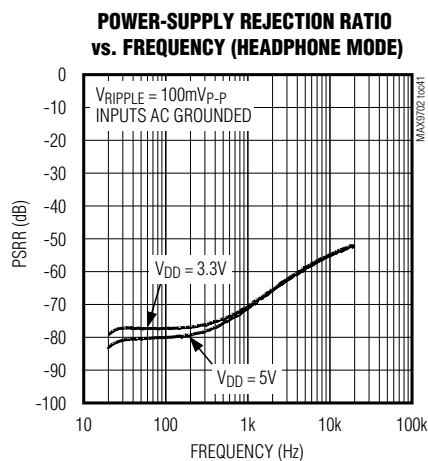
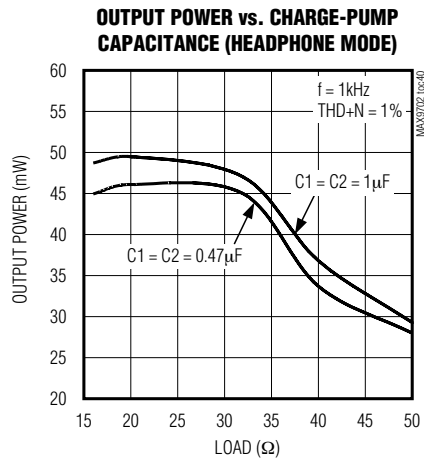
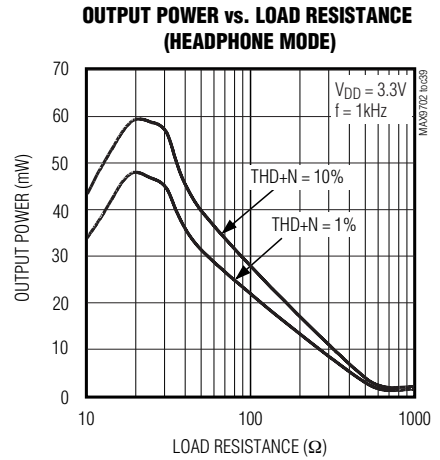
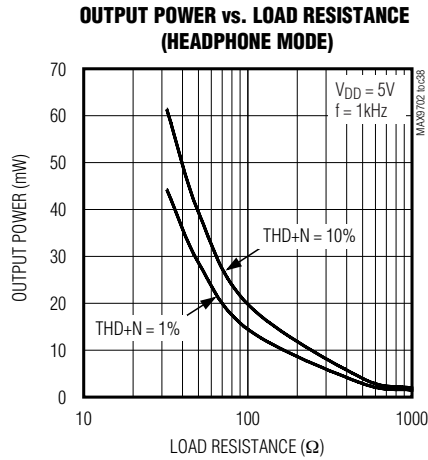
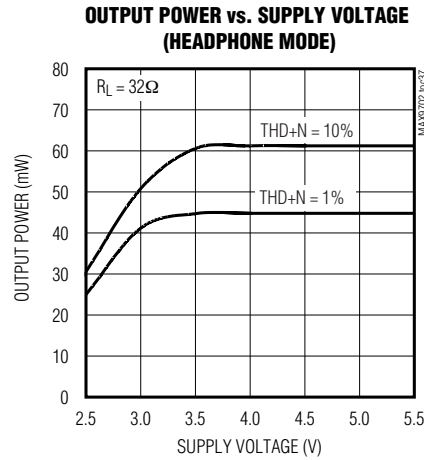
POWER DISSIPATION vs. OUTPUT POWER (HEADPHONE MODE)



1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Typical Operating Characteristics (continued)

($V_{DD} = PV_{DD} = \overline{SHDN} = 3.3V$, $GND = PGND = 0V$, $SYNC = V_{DD}$ (SSM), speaker gain = 12dB.)



1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Pin Description

MAX9702

PIN	NAME	FUNCTION
1, 22	PVDD	H-Bridge Power Supply. Connect to VDD and bypass each PVDD with a 0.1µF capacitor to PGND.
2	SYNC_OUT	Clock Signal Output. Float SYNC_OUT if not used.
3	SCL	I ² C Serial Clock. Connect a pullup resistor to VDD (see I ² C Interface section).
4	SDA	I ² C Serial Data. Connect a pullup resistor to VDD (see I ² C Interface section).
5	BIAS	Common-Mode Voltage. Bypass to GND with a 1µF capacitor.
6	SYNC	Frequency Mode Select: SYNC = GND: Fixed-frequency mode with f _S = 1100kHz. SYNC = Float: Fixed-frequency mode with f _S = 1340kHz. SYNC = VDD: Spread-spectrum mode with f _S = 1150kHz ±50kHz. SYNC = Clocked: Fixed-frequency mode with f _S = external clock frequency.
7	CPVDD	Charge-Pump Power Supply. Connect to VDD and bypass to CPGND with a 1µF capacitor.
8	C1P	Charge-Pump Flying-Capacitor Positive Terminal. Connect a 1µF capacitor from C1P to C1N.
9	CPGND	Charge-Pump Power Ground. Connect to PGND.
10	C1N	Charge-Pump Flying-Capacitor Negative Terminal. Connect a 1µF capacitor from C1N to C1P.
11	CPVSS	Charge-Pump Negative Output. Bypass with a 1µF capacitor to CPGND.
12	VSS	Headphone Amplifier Negative Supply. Connect to CPVSS.
13	HPL	Left-Channel Headphone Output
14	HPR	Right-Channel Headphone Output
15	VDD	Analog Power Supply. Bypass with a 1µF capacitor to GND.
16	GND	Analog Ground. Connect to PGND.
17	INR	Right-Channel Audio Input
18	INL	Left-Channel Audio Input
19	INM	Mono Audio Input
20	HPS	Headphone Sense: HPS = VDD: Headphone mode. HPS = GND: Speaker mode.
21	$\overline{\text{SHDN}}$	Active-Low Shutdown. Connect to VDD for normal operation.
23	OUTR+	Right-Channel Positive Amplifier Output
24	OUTR-	Right-Channel Negative Amplifier Output
25, 26	PGND	Power Ground. Connect to GND.
27	OUTL-	Left-Channel Negative Amplifier Output
28	OUTL+	Left-Channel Positive Amplifier Output
EP	EP	Exposed Pad. The external pad lowers the package's thermal impedance by providing a direct heat conduction path from the die to the printed circuit board. The exposed pad is internally connected to VSS. Connect the exposed thermal pad to an isolated plane if possible or to VSS.

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Detailed Description

The MAX9702 is a 1.8W, filterless, stereo Class D audio power amplifier and DirectDrive stereo headphone amplifier. The MAX9702 SSM amplifier features significant improvements to switch-mode amplifier technology. The MAX9702 offers Class AB performance with Class D efficiency and minimal board space. The device offers mix, mute, mono and stereo input modes, eight selectable gains, and a low-power shutdown mode—all programmable through an I²C interface.

The MAX9702 stereo headphone amplifier features Maxim's DirectDrive architecture, which eliminates the large output-coupling capacitors required by conventional single-supply headphone amplifiers. A negative supply (V_{SS}) is created internally by inverting the positive supply (CPV_{DD}). Powering the amplifiers from CPV_{DD} and CPV_{SS} increases the dynamic range of the amplifiers to almost twice that of other single-supply amplifiers, increasing the total available output power.

The DirectDrive outputs of the MAX9702 are biased at GND (see Figure 7). The benefit of this 0V bias is that the amplifier outputs do not have a DC component, eliminating the need for large DC-blocking capacitors. Eliminating the DC-blocking capacitors on the output saves board space, system cost, and improves frequency response.

The MAX9702 features extensive click-and-pop suppression circuitry on both speaker and headphone amplifiers to eliminate audible clicks-and-pops on start-up and shutdown.

The MAX9702 features an input multiplexer/mixer that allows three different audio sources to be selected or mixed. An I²C-compatible interface allows serial communication between the MAX9702 and a microcontroller. The MAX9702 is available with two different I²C addresses allowing two MAX9702s to share the same bus (see Table 2). The internal command register controls the shutdown status of the MAX9702, sets the maximum gain of the amplifier, and controls the mono/stereo/mixed/mute MUX inputs (see Table 3).

Class D Speaker Amplifier

Spread-spectrum modulation and synchronizable switching frequency significantly reduce EMI emissions. Comparators monitor the audio inputs and compare the complementary input voltages to a sawtooth waveform. The comparators trip when the input magnitude of the sawtooth exceeds their corresponding input voltage. Both comparators reset at a fixed time after the

rising edge of the second comparator trip point, generating a minimum-width pulse (t_{ON(MIN)}, 100ns typ) at the output of the second comparator (Figure 1). As the input voltage increases or decreases, the duration of the pulse at one output increases while the other output pulse duration remains the same. This causes the net voltage across the speaker (V_{OUT+} - V_{OUT-}) to change. The minimum-width pulse helps the device to achieve high levels of linearity.

Operating Modes

Fixed-Frequency (FFM) Mode

The MAX9702 features two fixed-frequency modes. Connect SYNC to GND to select a 1.1MHz switching frequency. Float SYNC to select a 1.34MHz switching frequency. The frequency spectrum of the MAX9702 consists of the fundamental switching frequency and its associated harmonics (see the Wideband FFT graph in *Typical Operating Characteristics*). Program the switching frequency such that the harmonics do not fall within a sensitive frequency band (Table 1). Audio reproduction is not affected by changing the switching frequency.

Spread-Spectrum (SSM) Mode

The MAX9702 features a unique spread-spectrum mode that flattens the wideband spectral components, improving EMI emissions that may be radiated by the speaker and cables. This mode is enabled by setting SYNC = V_{DD} to enable SSM (Table 1). In SSM mode, the switching frequency varies randomly by ±50kHz around the center frequency (1.15MHz). The modulation scheme remains the same, but the period of the sawtooth waveform changes from cycle to cycle (Figure 2). Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequency. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes (Figure 3). A proprietary amplifier topology ensures this does not corrupt the noise floor in the audio bandwidth.

Table 1. Operating Modes

SYNC	MODE
GND	FFM with f _{OSC} = 1100kHz
FLOAT	FFM with f _{OSC} = 1340kHz
V _{DD}	SSM with f _{OSC} = 1150kHz ±50kHz
Clocked	FFM with f _{OSC} = external clock frequency

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

MAX9702

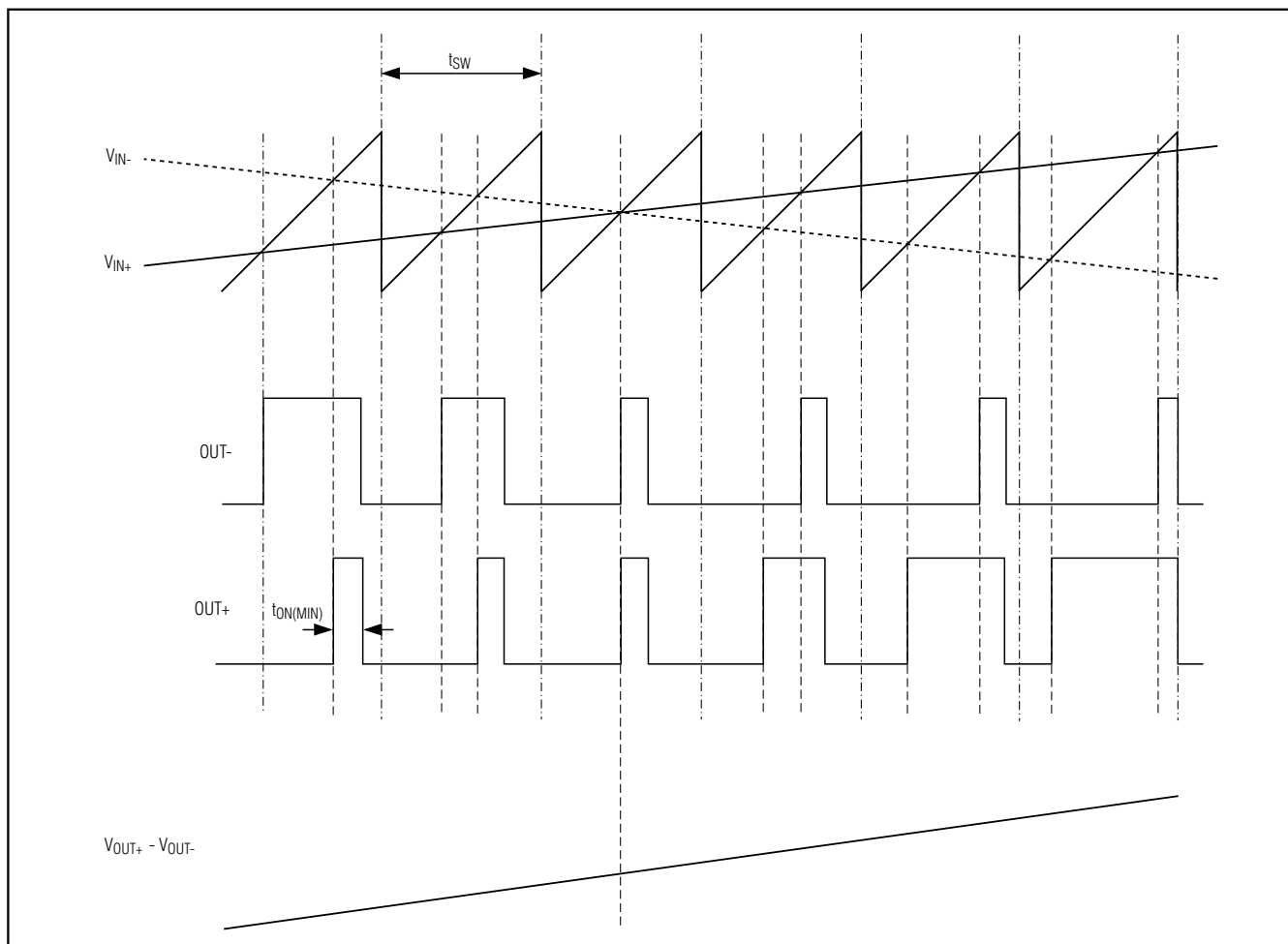


Figure 1. MAX9702 Outputs with an Input Signal Applied

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

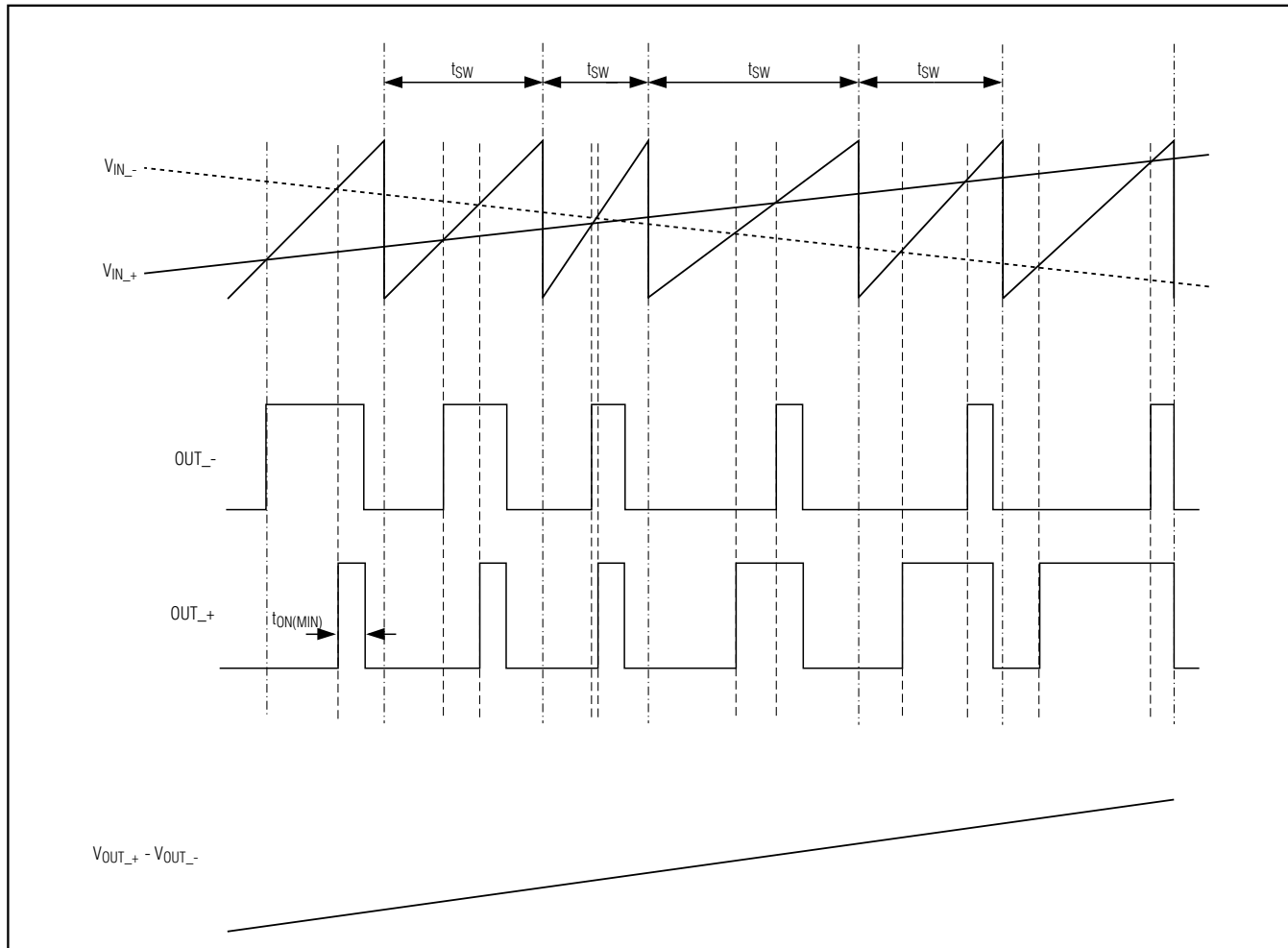


Figure 2. MAX9702 Output with an Input Signal Applied (SSM Mode)

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

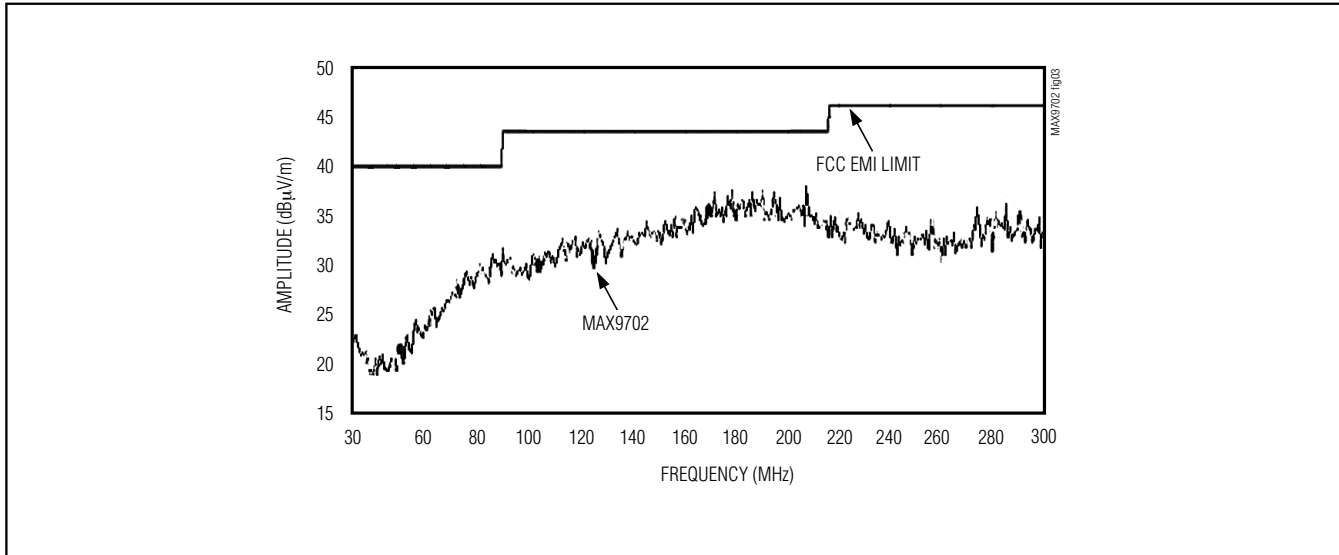


Figure 3. MAX9702 EMI with 76mm of Speaker Cable

External Clock Mode

The SYNC input allows the MAX9702 to be synchronized to an external clock, or another Maxim Class D amplifier, creating a fully synchronous system, minimizing clock intermodulation, and allocating spectral components of the switching harmonics to insensitive frequency bands. Applying a TTL clock signal between 1MHz and 2MHz to SYNC synchronizes the MAX9702. The period of the SYNC clock can be randomized, allowing the MAX9702 to be synchronized to another Maxim Class D amplifier operating in SSM mode.

SYNC_OUT allows several Maxim Class D amplifiers to be cascaded. The synchronized output minimizes interference due to clock intermodulation caused by the switching spread between single devices using SYNC_OUT. The modulation scheme remains the same when using SYNC_OUT, and audio reproduction is not affected (see Figure 4).

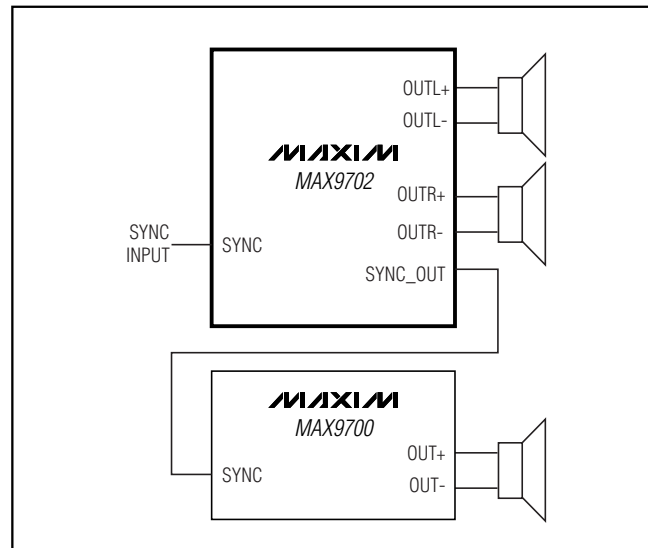


Figure 4. Cascading Two Amplifiers

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Filterless Modulation/Common-Mode Idle

The MAX9702 uses Maxim's unique modulation scheme that eliminates the LC filter required by traditional Class D amplifiers, improving efficiency, reducing component count, conserving board space and system cost. Conventional Class D amplifiers output a 50% duty-cycle square wave when no signal is present. With no filter, the square wave appears across the load as a DC voltage, resulting in finite load current, increasing power consumption, especially when idling. When no signal is present at the input of the MAX9702, the outputs switch as shown in Figure 5. Because the MAX9702 drives the speaker differentially, the two outputs cancel each other, resulting in no net idle mode voltage across the speaker, minimizing power consumption.

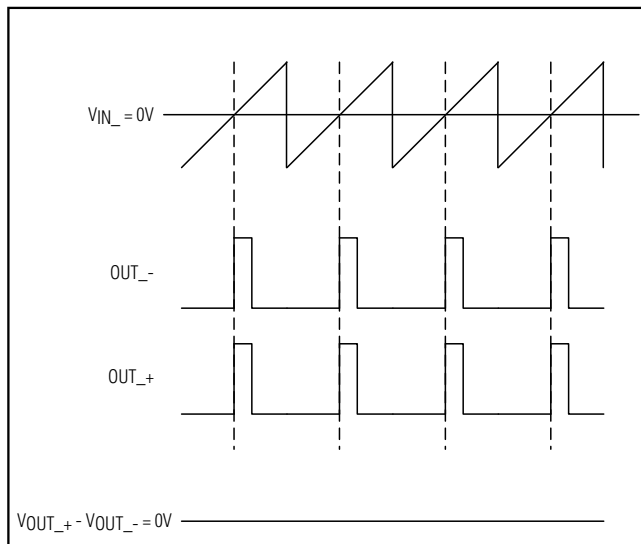


Figure 5. MAX9702 Outputs with No Input Signal

Efficiency

Efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current-steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78%; however, that efficiency is only exhibited at peak output powers. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the MAX9702 still exhibits >80% efficiencies under the same conditions (Figure 6).

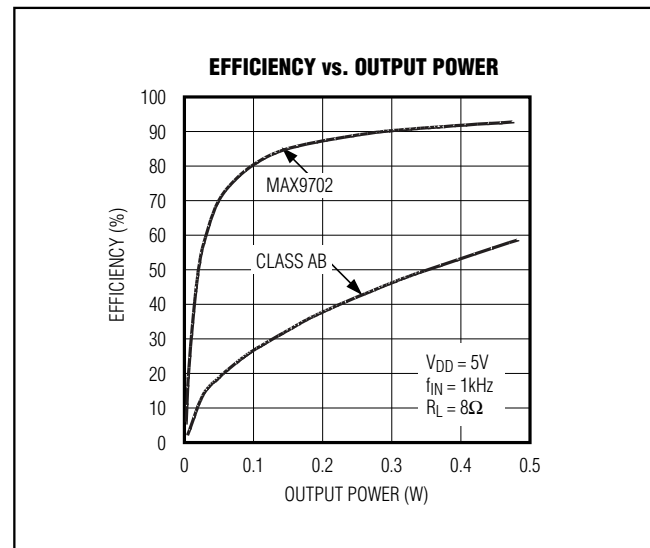


Figure 6. MAX9702 Efficiency vs. Class AB Efficiency

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Headphone Amplifier

In conventional single-supply headphone amplifiers, the output-coupling capacitor is a major contributor of audible clicks and pops. Upon startup, the amplifier charges the coupling capacitor to its bias voltage, typically half the supply. Likewise, during shutdown the capacitor is discharged to GND. This results in DC shift across the capacitor, which in turn, appears as an audible transient at the speaker. Since the MAX9702 headphone amplifier does not require output-coupling capacitors, this does not arise.

The MAX9702 offers four headphone amplifier gain settings controlled through the I²C interface. Headphone amplifier gains of -2dB, +1dB, +4dB, and +7dB are set by command register bits 3 and 4 (Table 5). Additionally, the MAX9702 features extensive click-and-pop suppression that eliminates any audible transient sources internal to the device.

In most applications, the output of the preamplifier driving the MAX9702 has a DC bias of typically half the supply. During startup, the input-coupling capacitor is charged to the preamplifier's DC bias voltage through the RF of the MAX9702, resulting in a DC shift across the capacitor and an audible click-and-pop. An internal delay of 40ms eliminates the clicks-and-pops caused by the input filter.

DirectDrive

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply) for maximum dynamic range. Large-coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the headphone outputs of the MAX9702 to be biased at GND, almost doubling dynamic range while operating from a single supply. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220 μ F, typ) tantalum capacitors, the MAX9702 charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the

Typical Operating Characteristics for details of the possible capacitor sizes. There is a low DC voltage on the driver outputs due to amplifier offset. However, the offset of the MAX9702 is typically 1.1mV, which, when combined with a 32 Ω load, results in less than 56 μ A of DC current flow to the headphones.

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal. Previous attempts at eliminating the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC bias voltage of the headphone amplifiers. This method raises some issues:

- 1) The sleeve is typically grounded to the chassis. Using the midrail biasing approach, the sleeve must be isolated from system ground, complicating product design.
- 2) During an ESD strike, the driver's ESD structures are the only path to system ground. Thus, the driver must be able to withstand the full ESD strike.
- 3) When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in possible damage to the drivers.

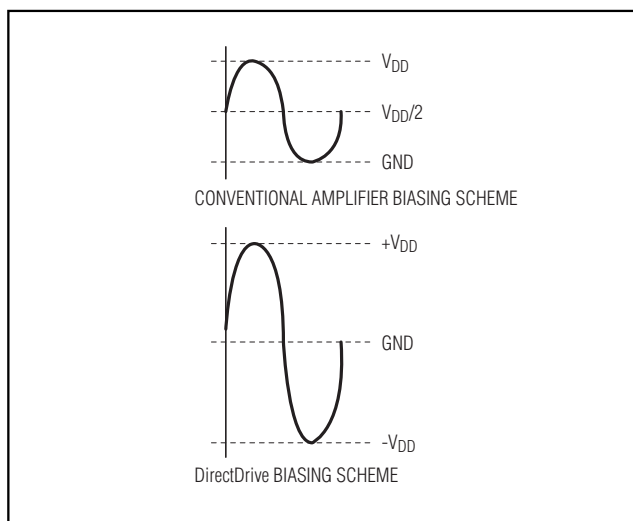


Figure 7. Traditional Amplifier Output vs. MAX9702 DirectDrive Output

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Charge Pump

The MAX9702 features a low-noise charge pump. The switching frequency of the charge pump is 1/2 the switching frequency of the Class D amplifier. When SYNC is driven externally, the charge pump switches at 1/2 f_{SYNC} . When $\text{SYNC} = V_{\text{DD}}$, the charge pump switches with a spread-spectrum pattern. The nominal switching frequency is well beyond the audio range, and thus does not interfere with the audio signals, resulting in an SNR of 97dB. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the charge pump, the di/dt noise caused by the parasitic bond wire and trace inductance is minimized. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the size of C2 (see *Typical Application Circuit*). The charge pump is active in both speaker and headphone modes.

Input Multiplexer/Mixer

The MAX9702 features an input multiplexer/mixer that allows three different audio sources to be selected and mixed. Command register bits 5 and 6 select the input channel (see Table 6), and the audio signal is output to the active amplifier. When the mono path is selected (bit 6 = 0, bit 5 = 1), the mono input is present on both the outputs (with a gain according to Tables 4 and 5). When the stereo path is selected, the left and right inputs are present on the outputs (with a gain according to Tables 4 and 5). When in mixer mode, the mono input is added to each of the stereo inputs and present at the output (with a gain according to Tables 4 and 5). The mono and stereo signals are attenuated by 6dB prior to mixing to maintain dynamic range. In mute, none of input signals is present at output.

Headphone Sense Input (HPS)

The headphone sense input (HPS) monitors the headphone jack, and automatically configures the MAX9702 based on the voltage applied at HPS. A voltage of less than 0.8V sets the MAX9702 to speaker mode. A voltage of greater than 2V disables the bridge amplifiers and enables the headphone amplifiers.

For automatic headphone detection, connect HPS to the control pin of a 3-wire headphone jack as shown in Figure 8. With no headphone present, the output impedance of the headphone amplifier pulls HPS to less than 0.8V. When a headphone plug is inserted into the jack, the control pin is disconnected from the tip

contact and HPS is pulled to V_{DD} through the internal 600k Ω pullup resistor. When driving HPS from an external logic source, drive HPS low when the MAX9702 is shut down. Place a 10k Ω resistor in series with HPS and the headphone jack to ensure $\pm 8\text{kV}$ ESD protection.

Click-and-Pop Suppression

The MAX9702 features comprehensive click-and-pop suppression that eliminates audible transients on start-up and shutdown. While in shutdown, the H-bridge is in a high-impedance state. During startup or power-up, the input amplifiers are muted and an internal loop sets the modulator bias voltages to the correct levels, preventing clicks and pops when the H-bridge is subsequently enabled.

Current-Limit and Thermal Protection

The MAX9702 features current limiting and thermal protection to protect the device from short circuits and overcurrent conditions. The headphone amplifier pulses in the event of an overcurrent condition. The speaker amplifiers' current-limiting protection clamps the output current without shutting down the outputs. This can result in a distorted output.

The MAX9702 has thermal protection that disables the device into shutdown at +120°C until the temperature decreases to +110°C.

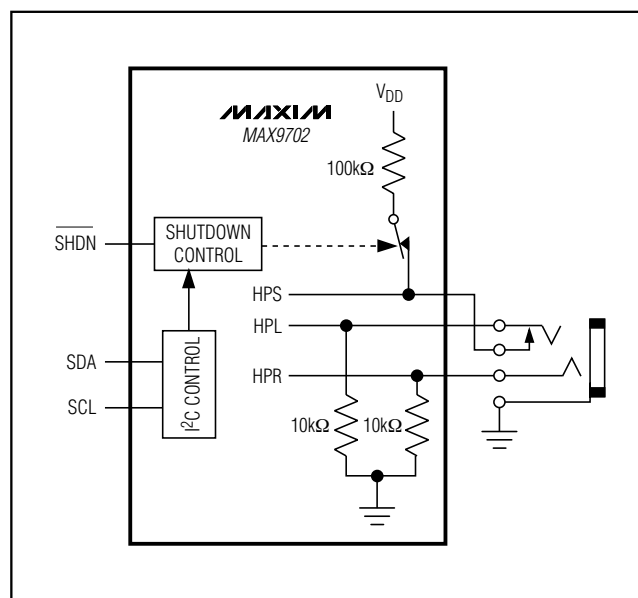


Figure 8. HPS Configuration

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

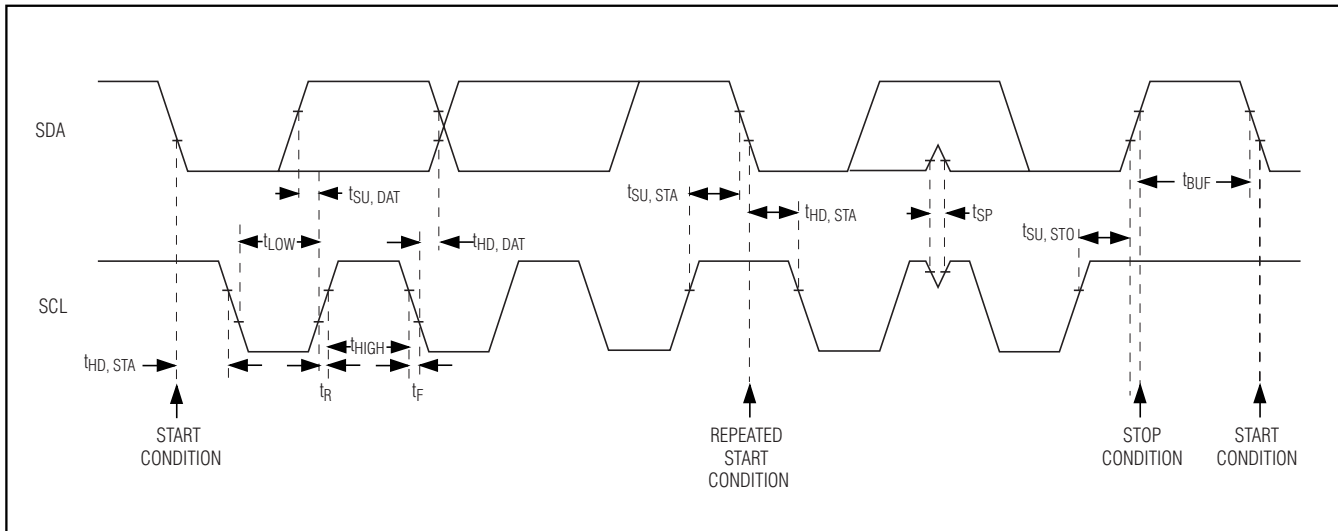


Figure 9. 2-Wire Serial-Interface Timing Diagram

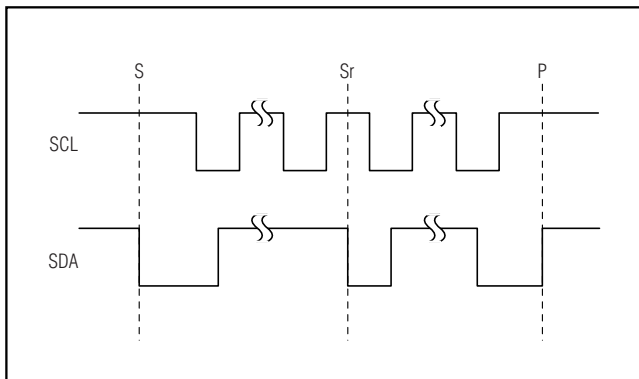


Figure 10. START, STOP, and REPEATED START Conditions

I²C Interface

The MAX9702 features an I²C 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX9702 and the master at clock rates up to 400kHz. Figure 9 shows the 2-wire interface timing diagram. The MAX9702 is a receive-only slave device relying on the master to generate the SCL signal. The MAX9702 cannot write to the SDA bus except to acknowledge the receipt of data from the master. The MAX9702 does not acknowledge a read command from the master. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus.

A master device communicates to the MAX9702 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) con-

dition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX9702 SDA line operates as both an input and an open-drain output. A pullup resistor, greater than 500Ω, is required on the SDA bus. The MAX9702 SCL line operates as an input only. A pullup resistor, greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9702 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 10). A START (S) condition from the master signals the beginning of a transmission to the MAX9702. The master terminates transmission and frees the bus by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

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Early STOP Conditions

The MAX9702 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

Slave Address

The MAX9702 is available with one of two preset slave addresses (see Table 2). The address is defined as the 7 most significant bits (MSBs) followed by the Read/Write bit. The address is the first byte of information sent to the MAX9702 after the START condition. The MAX9702 is a slave device only capable of being written to. The Read/Write bit must always be a zero when configuring the MAX9702. The MAX9702 does not acknowledge the receipt of its address even if R/W is set to 1.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9702 uses to handshake receipt each byte of data (see Figure 11). The MAX9702 pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may attempt communication.

Write Data Format

A write to the MAX9702 includes transmission of a START condition, the slave address with the R/W bit set to zero (see Table 2), 1 byte of data to configure the command register, and a STOP condition. Figure 12 illustrates the proper format for one frame.

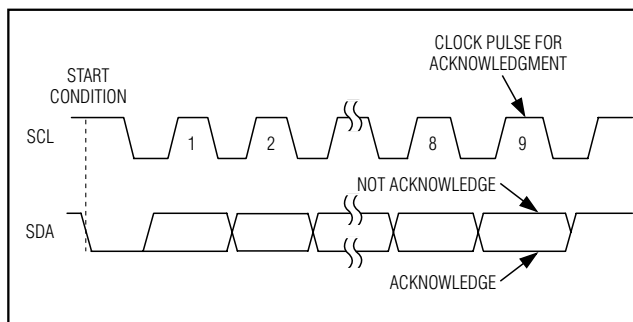


Figure 11. Acknowledge

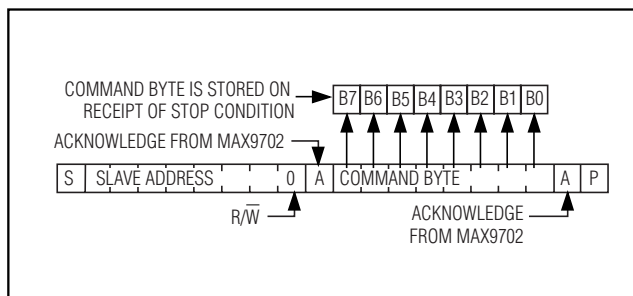


Figure 12. Write Data Format Example

The MAX9702 only accepts write data, but it acknowledges the receipt of its address byte with the R/W bit set high. The MAX9702 does not write to the SDA bus in the event that the R/W bit is set high. Subsequently, the master reads all 1s from the MAX9702. Always set the R/W bit to zero to avoid this situation.

Table 2. MAX9702 Address Map

PART	MAX9702 SLAVE ADDRESS							
	A6	A5	A4	A3	A2	A1	A0	R/W
MAX9702	1	0	0	1	1	0	0	0
MAX9702B	1	0	0	1	1	1	0	0

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Command Register

The MAX9702 has one command register that is used to set speaker and headphone gain, select an input mode, and enable/disable shutdown. Table 3 describes the function of the bits contained in the command register.

Programmable Speaker Gain

The MAX9702 has eight internally set speaker gains selected by B0–B2 (see Table 4).

Programmable Headphone Gain

The MAX9702 has four headphone gain settings selected by B3 and B4 (see Table 5).

Programmable Input Modes

The MAX9702 features a multiplexer that selects between the stereo and mono inputs. The mux also

acts as a mixer when the mono and stereo inputs are enabled at the same time. The MUTE function disables the input signal to the output. All modes are selected through B5 and B6 (see Table 6).

The MIX function attenuates and mixes the MONO and STEREO signals. Each input signal is attenuated by 6dB prior to being mixed. This attenuation preserves headroom at the output. The output signal is represented by the following equation when in MIX mode:

$$(OUT_{-} + (-)OUT_{++}) \text{ or } HP_{-} = \left(\frac{IN_{-} + INM}{2} \right) \times A_V$$

where A_V is the amplifier gain.

Table 3. Command Bits and Description

BIT	FUNCTION	DEFAULT
B0	Speaker gain-setting bit	0
B1	Speaker gain-setting bit	0
B2	Speaker gain-setting bit	1
B3	Headphone gain-setting bit	1
B4	Headphone gain-setting bit	0
B5	MONO enable bit (0 = Mute)	0
B6	STEREO enable bit (0 = Mute)	1
B7	Shutdown bit (1 = normal, 0 = shutdown)	1

Table 4. Programmable Speaker Gain

B2	B1	B0	FUNCTION	GAIN (dB)
0	0	0	Speaker gain	+0
0	0	1	Speaker gain	+3
0	1	0	Speaker gain	+6
0	1	1	Speaker gain	+9
1	0	0	Speaker gain	+12
1	0	1	Speaker gain	+15
1	1	0	Speaker gain	+18
1	1	1	Speaker gain	+21

Table 5. Programmable Headphone Gain

B4	B3	FUNCTION	GAIN (dB)
0	0	Headphone gain	-2
0	1	Headphone gain (default)	+1
1	0	Headphone gain	+4
1	1	Headphone gain	+7

Table 6. Programmable Input Modes

B6	B5	FUNCTION
0	0	MUTE (no input on the output)
0	1	MONO (MONO input sent to the output)
1	0	STEREO (left and right inputs sent to the outputs) (default)
1	1	MIX (MONO and STEREO inputs are mixed and output)

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Shutdown

The MAX9702 features a 0.1μA shutdown mode that reduces power consumption to extend battery life. Shutdown is controlled by the hardware or software interface. Drive $\overline{\text{SHDN}}$ low to disable the drive amplifiers, bias circuitry, charge pump, and set the headphone amplifier output impedance to 1kΩ. Similarly, the MAX9702 enters shutdown when bit 7 (B7) in the control register is set to zero. Connect SHDN to V_{DD} and set bit 7 = 1 for normal operation (see Table 7). The I²C interface is active and the contents of the command register are not affected when in shutdown. This allows the master to write to the MAX9702 while in shutdown.

Table 7. Shutdown Control ($\overline{\text{SHDN}}$)

B7	FUNCTION
0	Soft shutdown
1	Normal operation

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's PWM output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency. The traditional PWM scheme uses large differential output swings $2 \times V_{DD(P-P)}$ and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

The MAX9702 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square wave output. By eliminating the output filter, this results in a smaller, less costly, more efficient solution.

Because the frequency of the MAX9702 output is well beyond the bandwidth of most speakers, voice coil movement due to the square wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power may be damaged. For optimum results, use a speaker with a series inductance $>10\mu\text{H}$. Typical 8Ω speakers, for portable audio applications, exhibit series inductances in the range of 20μH to 100μH.

Class D Output Offset

Unlike a Class AB amplifier, the output offset voltage of Class D amplifiers does not noticeably increase quiescent current draw when a load is applied. This is due to the power conversion of the Class D amplifier. For

example, an 8mV DC offset across an 8Ω load results in 1mA extra current consumption in a Class AB device. In the Class D case, an 8mV offset into 8Ω equates to an additional power drain of 8μW. Due to the high efficiency of the Class D amplifier, this represents an additional quiescent current draw of $8\mu\text{W}/(V_{DD}/100 \times \eta)$, which is on the order of a few microamps.

DC-Coupled Input

The input amplifier can accept DC-coupled inputs that are biased to the amplifier's bias voltage. DC-coupling eliminates the input-coupling capacitors, reducing component count to potentially one external component (see the *System Diagram*). However, the highpass filtering effect of the capacitors is lost, allowing low-frequency signals to feed through to the load.

Power Supplies

The MAX9702 has different supplies for each portion of the device, allowing for the optimum combination of headroom power dissipation and noise immunity. The speaker amplifiers are powered from PV_{DD}. PV_{DD} can range from 2.5V to 5.5V and must be connected to the same potential as V_{DD}. The headphone amplifiers are powered from V_{DD} and V_{SS}. V_{DD} is the positive supply of the headphone amplifiers and can range from 2.5V to 5.5V. V_{SS} is the negative supply of the headphone amplifiers. Connect V_{SS} to CPV_{SS}. The charge pump is powered by CPV_{DD}. Connect CPV_{DD} to V_{DD} for normal operation. The charge pump inverts the voltage at CPV_{DD}, and the resulting voltage appears at CPV_{SS}. The remainder of the device is powered by V_{DD}.

Component Selection

Input Filter

An input capacitor, C_{IN}, in conjunction with the input impedance of the MAX9702 forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

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Other considerations when designing the input filter include the constraints of the overall system and the actual frequency band of interest. Although high-fidelity audio calls for a flat-gain response between 20Hz and 20kHz, portable voice-reproduction devices such as cellular phones and two-way radios need only concentrate on the frequency range of the spoken human voice (typically 300Hz to 3.5kHz). In addition, speakers used in portable devices typically have a poor response below 300Hz. Taking these two factors into consideration, the input filter may not need to be designed for a 20Hz to 20kHz response, saving both board space and cost due to the use of smaller capacitors.

Output Filter

The MAX9702 does not require an output filter. The device passes FCC emissions standards with 75mm of unshielded speaker cables. However, output filtering can be used if a design is failing radiated emissions due to board layout or cable length, or the circuit is near EMI-sensitive devices. Use a ferrite bead filter when radiated frequencies above 10MHz are of concern. Use an LC filter when radiated frequencies below 10MHz are of concern, or when long leads (>200mm) connect the amplifier to the speaker. Figure 13 shows optional speaker amplifier output filters.

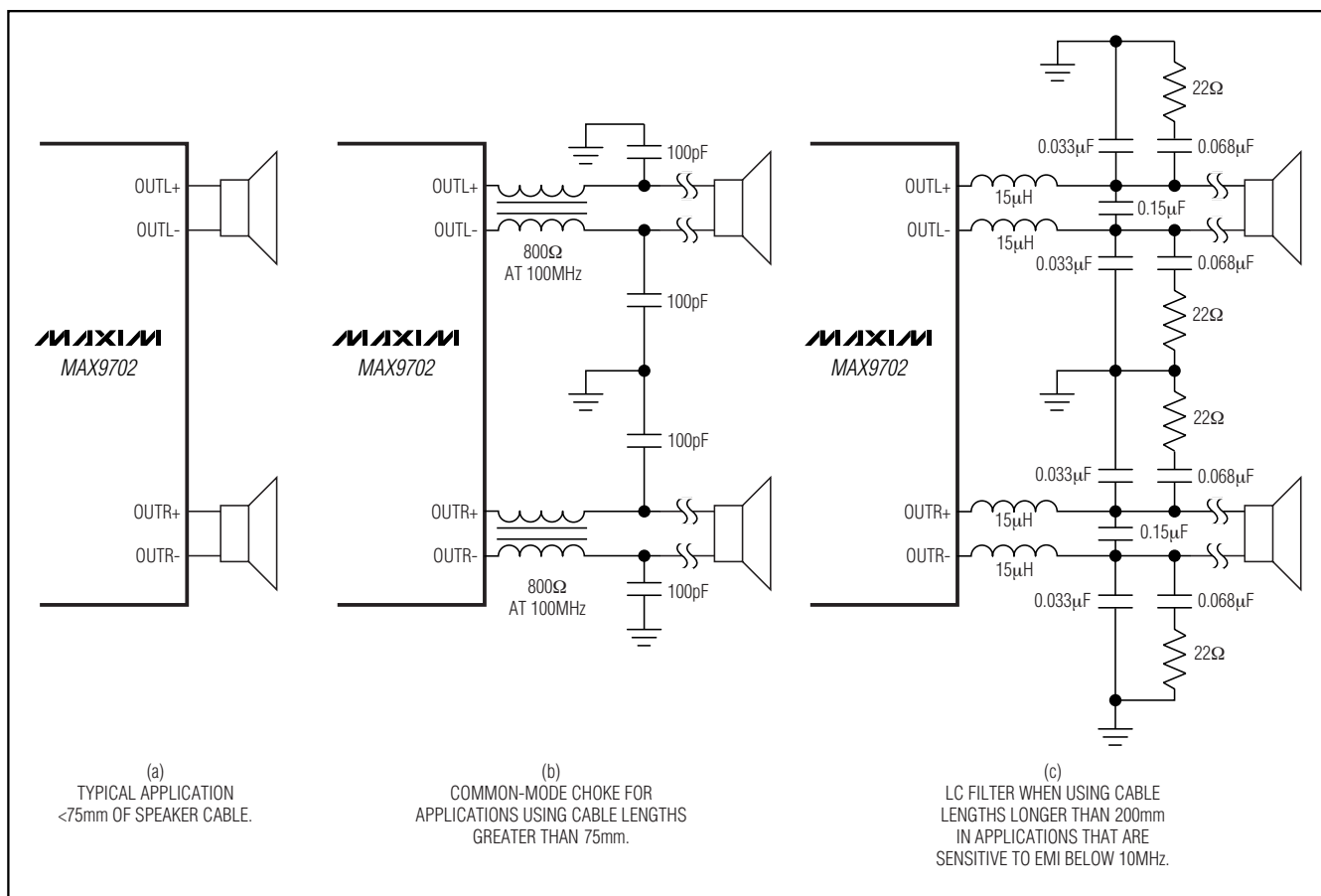


Figure 13. Optional Speaker Amplifier Output Filter

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BIAS Capacitor

BIAS is the output of the internally generated DC bias voltage. The BIAS bypass capacitor, C_{BIAS} , improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the clickless/popless, startup/shutdown DC bias waveforms for the speaker amplifiers. Bypass BIAS with a $1\mu\text{F}$ capacitor to GND.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than $100\text{m}\Omega$ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. Most surface-mount ceramic capacitors satisfy the ESR requirement. For best performance over the extended temperature range, select capacitors with an X7R dielectric. Table 8 lists suggested manufacturers.

Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the output resistance of the charge pump. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 reduces the charge-pump output resistance to an extent. Above $1\mu\text{F}$, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Output Capacitor (C2)

The output capacitor value and ESR directly affect the ripple at CPV_{SS} . Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics*.

CPVDD Bypass Capacitor

The CPV_{DD} bypass capacitor (C3) lowers the output impedance of the power supply and reduces the impact of the MAX9702's charge-pump switching tran-

sients. Bypass CPV_{DD} with C3 to PGND and place it physically close to the CPV_{DD} and PGND. Use a value for C3 that is equal to C1.

Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Large traces also aid in moving heat away from the package. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Connect PGND and GND together at a single point on the PC board. Route all traces that carry switching transients away from GND and the traces/components in the audio signal path.

Connect all of the power-supply inputs (CPV_{DD} , V_{DD} , and PV_{DD}) together. Bypass PV_{DD} with a $0.1\mu\text{F}$ capacitor to PGND and CPV_{DD} with a $1\mu\text{F}$ capacitor to PGND. Bypass V_{DD} with $1\mu\text{F}$ capacitor to GND. Place the bypass capacitors as close to the MAX9702 as possible. Place a bulk capacitor between PV_{DD} and PGND, if needed.

Use large, low-resistance output traces. Current drawn from the outputs increases as load impedance decreases. High-output trace resistance decreases the power delivered to the load. Large output, supply, and GND traces decrease the thermal impedance of the system, allowing more heat to move from the MAX9702 to the air.

The MAX9702 thin QFN-EP package features an exposed thermal pad on its underside. This pad lowers the package's thermal impedance by providing a direct-heat conduction path from the die to the printed circuit board. The exposed pad is internally connected to V_{SS} . **Connect the exposed pad to an isolated plane if possible or to V_{SS} .**

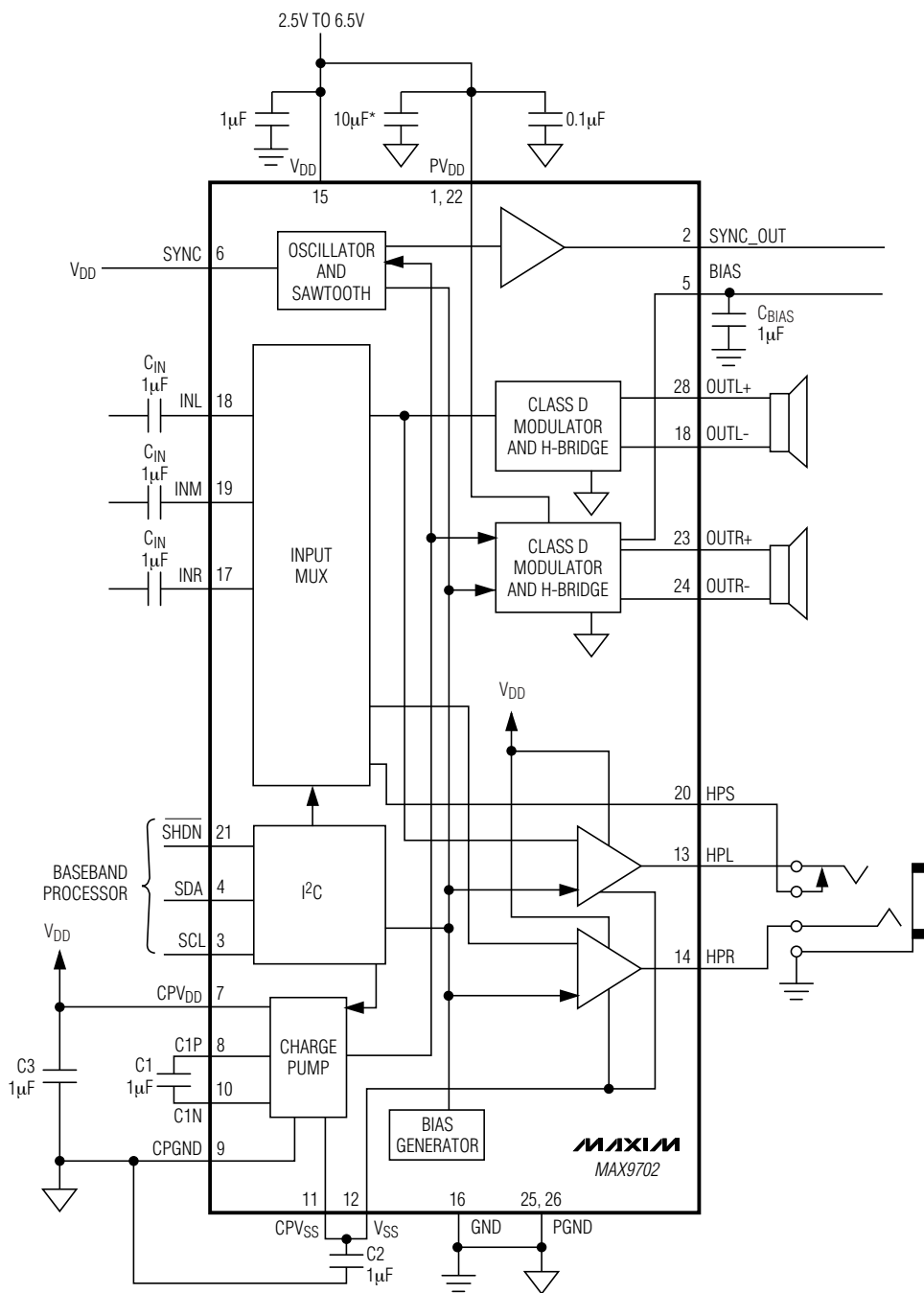
Table 8. Suggested Capacitor Manufacturers

SUPPLIER	PHONE	FAX	WEBSITE
Taiyo Yuden	800-348-2496	847-925-0899	www.t-yuden.com
TDK	807-803-6100	847-390-4405	www.component.tdk.com

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Functional Diagram/Typical Operating Circuit

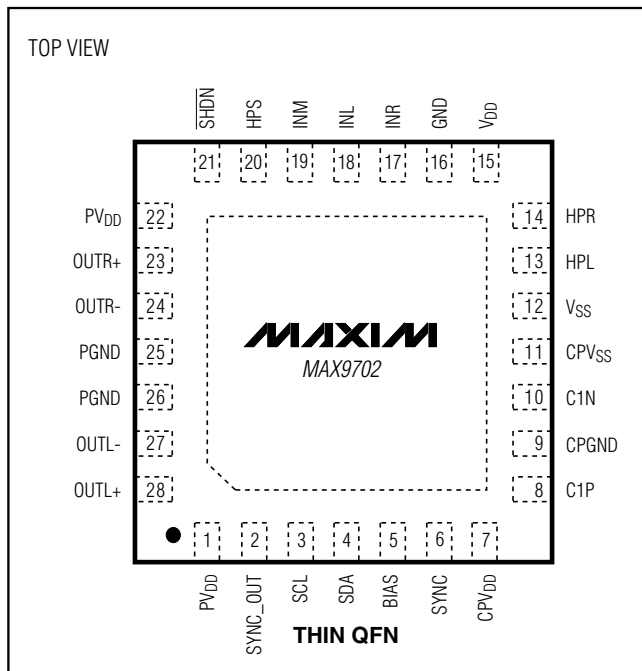
MAX9702



*BULK CAPACITANCE IF NEEDED

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Pin Configuration



Chip Information

TRANSISTOR COUNT: 10,435

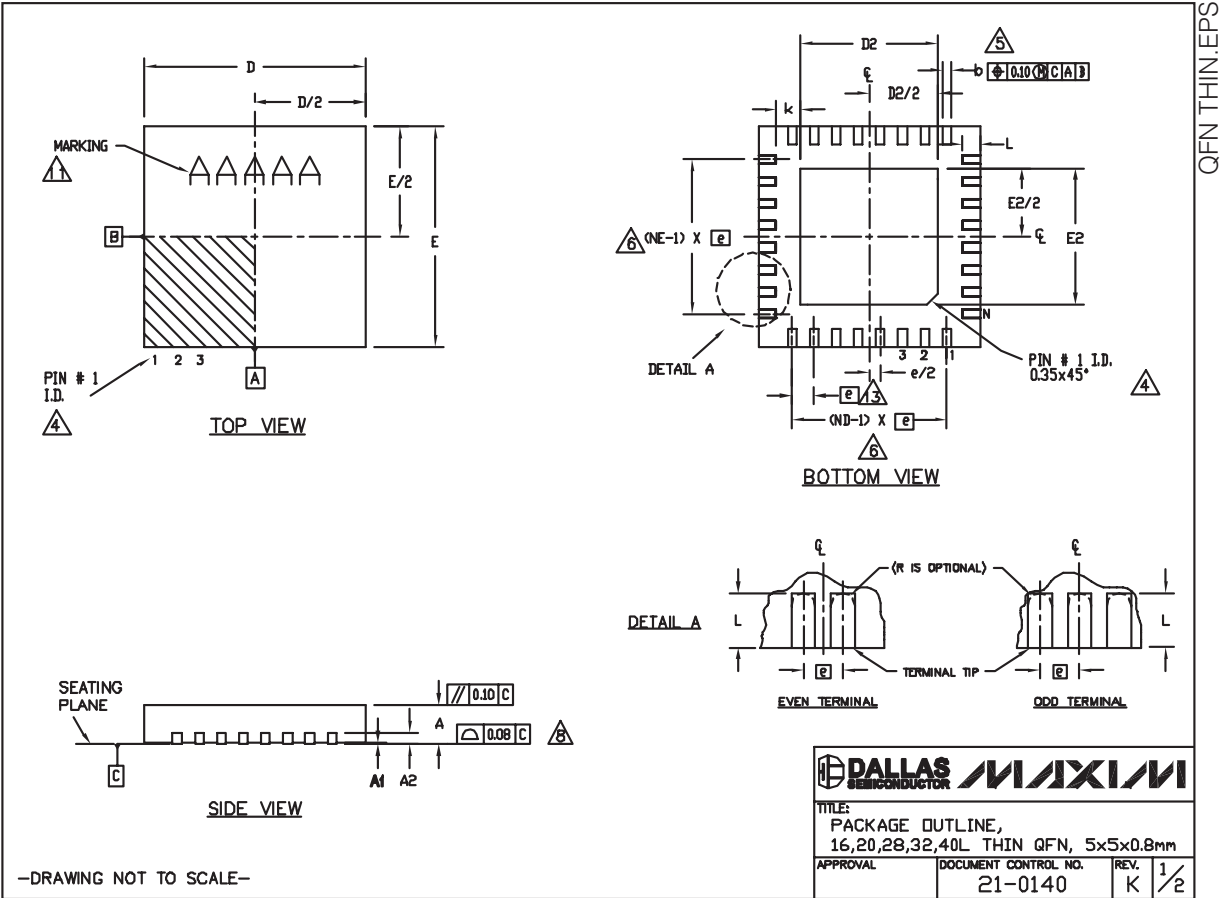
PROCESS: BICMOS

MAX9702

1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



1.8W, Filterless, Stereo, Class D Audio Power Amplifier and DirectDrive Stereo Headphone Amplifier

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	VHBB			VHHC			VHHD-1			VHHD-2			-----		

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC M0220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ± 0.05 .

—DRAWING NOT TO SCALE—

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60



TITLE:
PACKAGE OUTLINE,
16,20,28,32,40L THIN QFN, 5x5x0.8mm

APPROVAL

DOCUMENT CONTROL NO.
21-0140

REV.
K 1/2

The MAX9702 thin QFN-EP package features an exposed thermal pad on its underside. This pad lowers the package's thermal impedance by providing a direct-heat conduction path from the die to the printed circuit board. The exposed pad is internally connected to VSS. Connect the exposed thermal pad to an isolated plane.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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