19-2466; Rev 1; 6/09

Low-Power, 14-Bit Analog-to-Digital Converters with Parallel Interface

General Description

The MAX1065/MAX1066 14-bit, low-power successive approximation analog-to-digital converters (ADCs) feature automatic power-down, a factory-trimmed internal clock, and a high-speed, 14-bit-wide (MAX1065) or byte-wide (MAX1066) parallel interface. The devices operate from a single 4.75V to 5.25V analog supply and a 2.7V to 5.25V digital supply.

The MAX1065/MAX1066 use an internal 4.096V reference or an external reference. The MAX1065/MAX1066 consume only 1.8mA at a sampling rate of 165ksps with external reference and 2.7mA with internal reference. AutoShutdown™ reduces supply current to 0.1mA at 10ksps.

The MAX1065/MAX1066 are ideal for high-performance, battery-powered, data-acquisition applications. Excellent dynamic performance and low-power consumption in a small package make the MAX1065/MAX1066 the best choice for circuits with demanding power consumption and space requirements.

The 14-bit-wide MAX1065 is available in a 28-pin TSSOP package, and the byte-wide MAX1066 is available in a 20-pin TSSOP package. Both devices are available in either the 0°C to +70°C commercial, or the -40°C to +85°C extended temperature range.

Applications

Temperature Sensor/Monitor

Industrial Process Control

I/O Boards

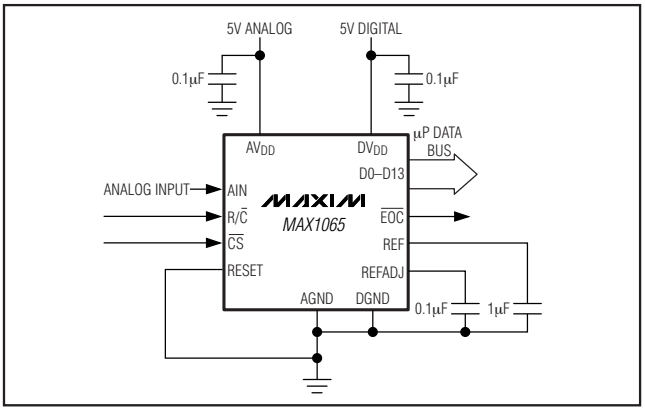
Data-Acquisition Systems

Cable/Harness Tester

Accelerometer Measurements

Digital Signal Processing

Typical Operating Circuit



Features

- **14-Bit-Wide (MAX1065) and Byte-Wide (MAX1066) Parallel Interface**
- **High Speed: 165ksps Sample Rate**
- **Accurate: ±1LSB DNL (max), ±1LSB INL (max)**
- **4.096V, 35ppm/°C Internal Reference**
- **External Reference Range 3.8V to 5.25V**
- **Single 4.75V to 5.25V Analog Supply Voltage**
- **2.7V to 5.25V Digital Supply Voltage**
- **Low Supply Current**
  - **1.8mA (External Reference)**
  - **2.7mA (Internal Reference)**
  - **0.1mA AutoShutdown Mode (10ksps, External Reference)**
- **Small Footprint**
  - **28-Pin TSSOP Package (14-Bit Wide)**
  - **20-Pin TSSOP Package (Byte Wide)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL
MAX1065ACUI	0°C to 70°C	28 TSSOP	±1
MAX1065BCUI	0°C to 70°C	28 TSSOP	±2
MAX1065CCUI	0°C to 70°C	28 TSSOP	±3
MAX1065AEUI	-40°C to +85°C	28 TSSOP	±1
MAX1065BEUI	-40°C to +85°C	28 TSSOP	±2
MAX1065CEUI	-40°C to +85°C	28 TSSOP	±3
MAX1066ACUP	0°C to 70°C	20 TSSOP	±1
MAX1066BCUP	0°C to 70°C	20 TSSOP	±2
MAX1066CCUP	0°C to 70°C	20 TSSOP	±3
MAX1066AEUP	-40°C to +85°C	20 TSSOP	±1
MAX1066BEUP	-40°C to +85°C	20 TSSOP	±2
MAX1066CEUP	-40°C to +85°C	20 TSSOP	±3

Pin Configurations appear at end of data sheet.

AutoShutdown is a trademark of Maxim Integrated Products, Inc.

Low-Power, 14-Bit Analog-to-Digital Converters with Parallel Interface

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
AIN, REF, REFADJ to AGND.....-0.3V to (AV_{DD} + 0.3V)
$\overline{CS}$, HBEN, R/$\overline{C}$, RESET to DGND .....-0.3V to +6V
Digital Output (D13–D0, $\overline{EOC}$)
to DGND .....-0.3V to (DV_{DD} + 0.3V)
Maximum Continuous Current Into Any Pin 50mA

Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 10.9mW/°C above +70°C) 879mW
28-Pin TSSOP (derate 12.8mW/°C above +70°C) 1026mW
Operating Temperature Ranges
MAX106_ _CU_.....0°C to +70°C
MAX106_ _EU_.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = 5V, external reference = 4.096V, C_{REF} = 1µF, C_{REFADJ} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution	N		14			Bits
Relative Accuracy (Note 1)	INL	MAX106_A			±1	LSB
		MAX106_B			±2	
		MAX106_C			±3	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Transition Noise		RMS noise, includes quantization noise		0.32		LSB_{RMS}
Offset Error				0.2	1	mV
Gain Error		(Note 2)		±0.002	±0.02	%FSR
Offset Drift				0.6		ppm/°C
Gain Drift				0.2		ppm/°C
DYNAMIC PERFORMANCE ($f_{IN(SINE-WAVE)}$ = 1kHz, V_{IN} = 4.096V_{P-P}, 165ksps)						
Signal-to-Noise Plus Distortion	SINAD		81	84		dB
Signal-to-Noise Ratio	SNR		82	84		dB
Total Harmonic Distortion	THD			-99	-86	dB
Spurious-Free Dynamic Range	SFDR		87	102		dB
Full-Power Bandwidth		-3dB point		4		MHz
Full-Linear Bandwidth		SINAD > 81dB		20		kHz
CONVERSION RATE						
Sample Rate	f_{SAMPLE}				165	ksps
Aperture Delay				40		ns
Aperture Jitter				100		ps
ANALOG INPUT						
Input Range	V_{AIN}		0		V_{REF}	V
Input Capacitance	C_{AIN}			40		pF

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = 5V, external reference = 4.096V, C_{REF} = 1µF, C_{REFADJ} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERNAL REFERENCE							
REF Output Voltage	V_{REF}			4.056	4.096	4.136	V
REF Output Tempco	TC_{REF}				±35		ppm/°C
REF Short-Circuit Current	I_{REFSC}				±10		mA
Capacitive Bypass at REFADJ	C_{REFADJ}			0.1			µF
Capacitive Bypass at REF	C_{REF}			1			µF
REFADJ Input Leakage Current	I_{REFADJ}				20		µA
EXTERNAL REFERENCE							
REFADJ Buffer Disable Threshold		To power-down the internal reference		AV_{DD} - 0.4		AV_{DD} - 0.1	V
REF Input Voltage Range		Internal reference disabled (Note 3)		3.8		AV_{DD} - 0.2	V
REF Input Current	I_{REF}	V_{REF} = 4.096V, f_{SAMPLE} = 165ksps			14	25	µA
		Shutdown mode			±0.1		
DIGITAL INPUTS/OUTPUTS ($\overline{CS}$, R/$\overline{C}$, $\overline{EOC}$, D0–D13, RESET, HBEN)							
Input High Voltage	V_{IH}			0.7 x DV_{DD}			V
Input Low Voltage	V_{IL}					0.3 x DV_{DD}	V
Input Leakage Current	I_{IN}	V_{IH} = 0 or DV_{DD}			±0.1	±1	µA
Input Hysteresis	V_{HYST}				0.1		V
Input Capacitance	C_{IN}				15		pF
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA, DV_{DD} = 2.7V to 5.25V, AV_{DD} = 5.25V		D_{VDD} - 0.4			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA, DV_{DD} = 2.7V to 5.25V, AV_{DD} = 5.25V				0.4	V
Three-State Leakage Current	I_{OZ}	D0–D13			±0.1	±10	µA
Three-State Output Capacitance	C_{OZ}				15		pF
POWER REQUIREMENTS							
Analog Supply Voltage	AV_{DD}			4.75		5.25	V
Digital Supply Voltage	DV_{DD}			2.7		AV_{DD}	V
Analog Supply Current	I_{AVDD}	Internal reference	165ksps		3.2	3.6	mA
			100ksps		2.6		
			10ksps		1.9		
			1ksps		1.8		
		External reference	165ksps		2.4	2.8	
			100ksps		1.8		
			10ksps		0.8		
			1ksps		0.2		

Low-Power, 14-Bit Analog-to-Digital Converters with Parallel Interface

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = 5V, external reference = 4.096V, C_{REF} = 1µF, C_{REFADJ} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Supply Current	I_{DVDD}	D0–D13 = all zeros	165ksps		0.5	0.7	mA
			100ksps		0.3		
			10ksps		0.03		
			1ksps		0.003		
Shutdown Supply Current (Note 4)	I_{SHDN}	Full power-down	I_{AVDD}		0.05	5	mA
			I_{DVDD}		0.5	6	µA
		REF and REF buffer enabled (standby mode)	I_{AVDD}		1.0	1.2	mA
			I_{DVDD}		0.5	5	µA
Power-Supply Rejection Ratio (Note 5)	PSRR	AV_{DD} = 5V, ±5%, full-scale input			68		dB

TIMING CHARACTERISTICS (Figures 1 and 2)

(AV_{DD} = 4.75V to 5.25V, DV_{DD} = 2.7V to AV_{DD}, external reference = 4.096V, C_{REF} = 1µF, C_{REFADJ} = 0.1µF, $C_{D13–D0}$, $C_{\overline{EOC}}$ = 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

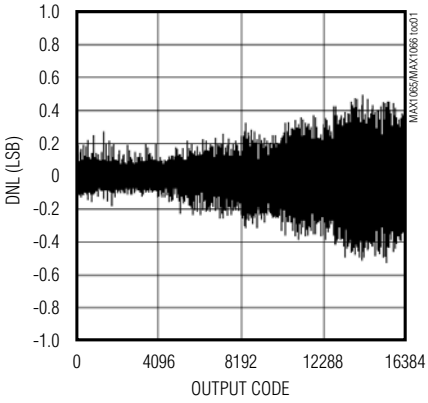
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.1			µs
Conversion Time	t_{CONV}					4.7	
$\overline{CS}$ Pulse Width High	t_{CSH}	(Note 6)		40			ns
$\overline{CS}$ Pulse Width Low	t_{CSL}	(Note 6)	V_{DVDD} = 4.75V to 5.25V	40			ns
			V_{DVDD} = 2.7V to 4.74V	60			
R/$\overline{C}$ to $\overline{CS}$ Fall Setup Time	t_{DS}			0			ns
R/$\overline{C}$ to $\overline{CS}$ Fall Hold Time	t_{DH}	V_{DVDD} = 4.75V to 5.25V		40			ns
		V_{DVDD} = 2.7V to 5.25V		60			
$\overline{CS}$ to Output Data Valid	t_{DO}	V_{DVDD} = 4.75V to 5.25V				40	ns
		V_{DVDD} = 2.7V to 4.74V				80	
HBEN Transition To Output Data Valid (MAX1066 only)	t_{DO1}	V_{DVDD} = 4.75V to 5.25V				40	ns
		V_{DVDD} = 2.7V to 4.74V				80	
$\overline{EOC}$ Fall To $\overline{CS}$ Fall	t_{DV}			0			ns
$\overline{CS}$ Rise To $\overline{EOC}$ Rise	t_{EOC}	V_{DVDD} = 4.75V to 5.25V				40	ns
		V_{DVDD} = 2.7V to 4.74V				80	
Bus Relinquish Time (Note 6)	t_{BR}	V_{DVDD} = 4.75V to 5.25V				40	ns
		V_{DVDD} = 2.7V to 4.74V				80	

Note 1: Relative accuracy is the deviation of the analog value at any code from its theoretical value after offset and gain errors have been removed.
Note 2: Offset nulled.
Note 3: Guaranteed by design, not production tested.
Note 4: Maximum specification is limited by automated test equipment.
Note 5: Defined as the change in positive full scale caused by a ±5% variation in the nominal supply.
Note 6: To ensure best performance, finish reading the data and wait t_{BR} before starting a new acquisition.

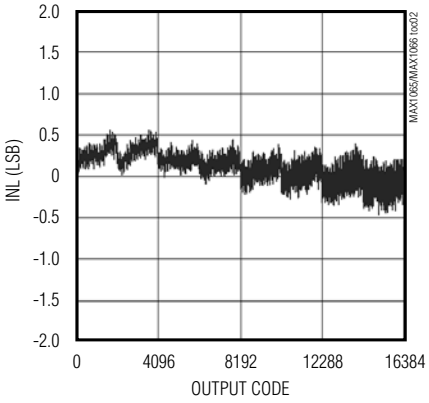
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = 5V, external reference = 4.096V, C_{REF} = 1µF, C_{REFADJ} = 0.1µF, T_A = +25°C, unless otherwise noted.)

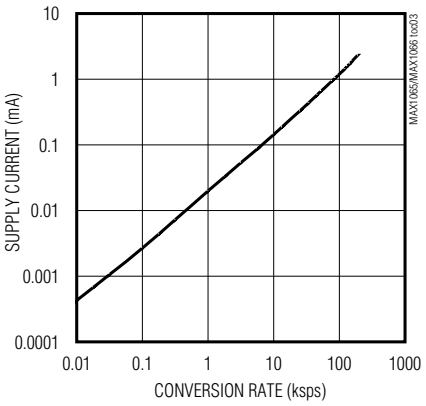
DNL vs. OUTPUT CODE



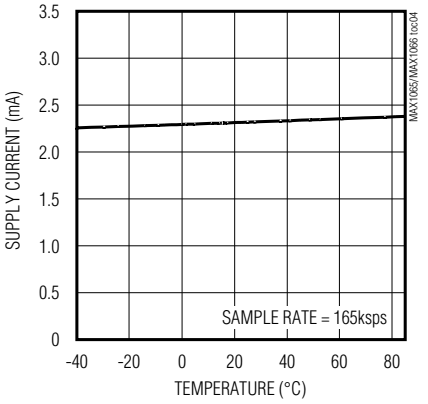
INL vs. OUTPUT CODE



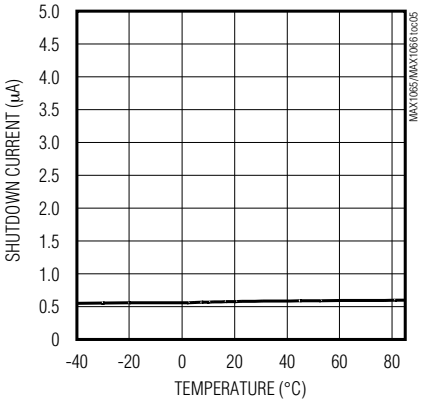
I_{AVDD} + I_{DVDD} SUPPLY CURRENT vs. SAMPLE RATE



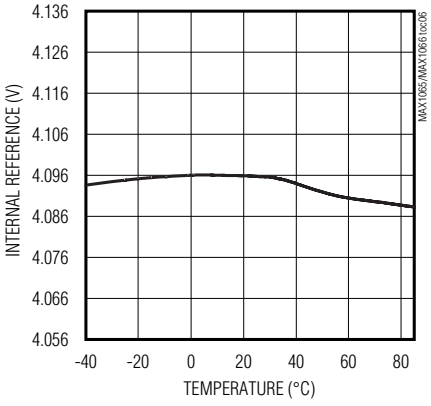
I_{AVDD} + I_{DVDD} SUPPLY CURRENT vs. TEMPERATURE



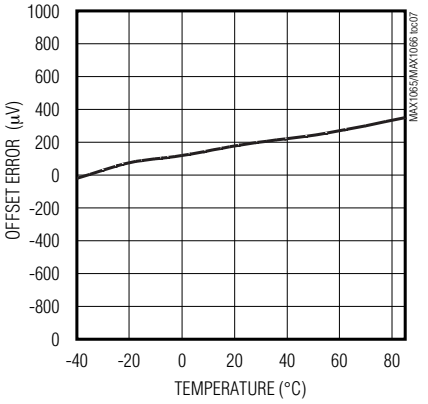
I_{AVDD} + I_{DVDD} SHUTDOWN CURRENT vs. TEMPERATURE



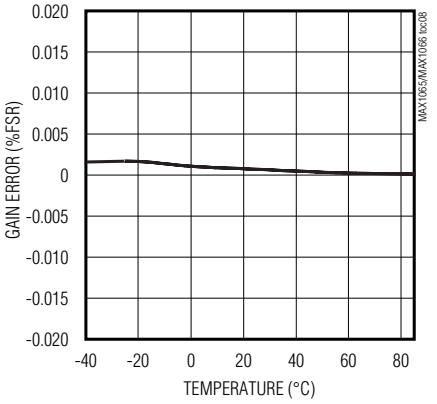
INTERNAL REFERENCE vs. TEMPERATURE



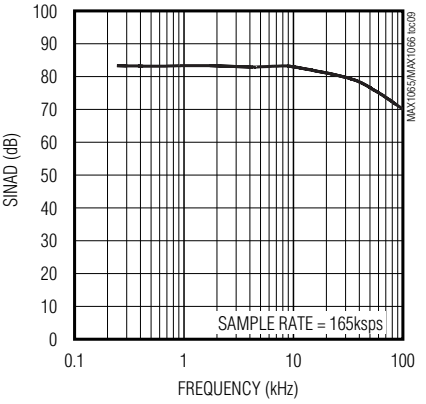
OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. TEMPERATURE



SINAD vs. FREQUENCY

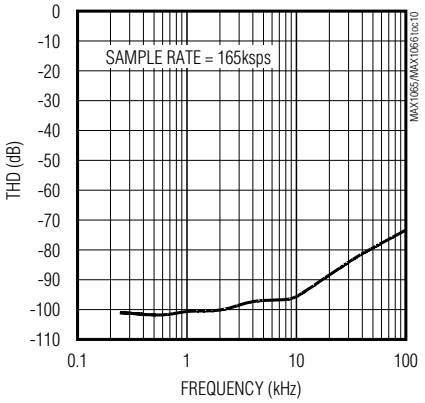


Low-Power, 14-Bit Analog-to-Digital Converters with Parallel Interface

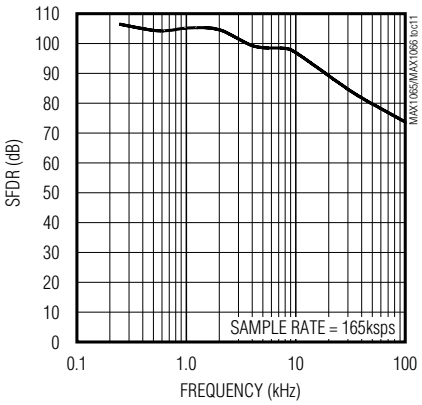
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, external reference = 4.096V, C_{REF} = 1µF, C_{REFADJ} = 0.1µF, T_A = +25°C, unless otherwise noted.)

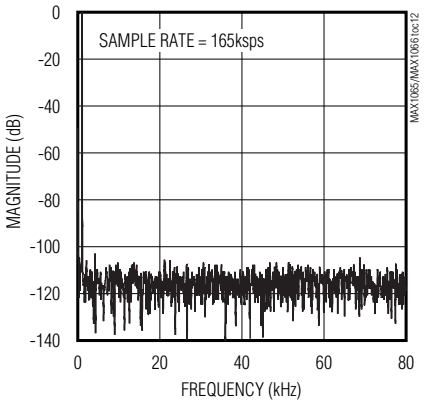
TOTAL HARMONIC DISTORTION vs. FREQUENCY



SPURIOUS-FREE DYNAMIC RANGE vs. FREQUENCY



FFT AT 1kHz



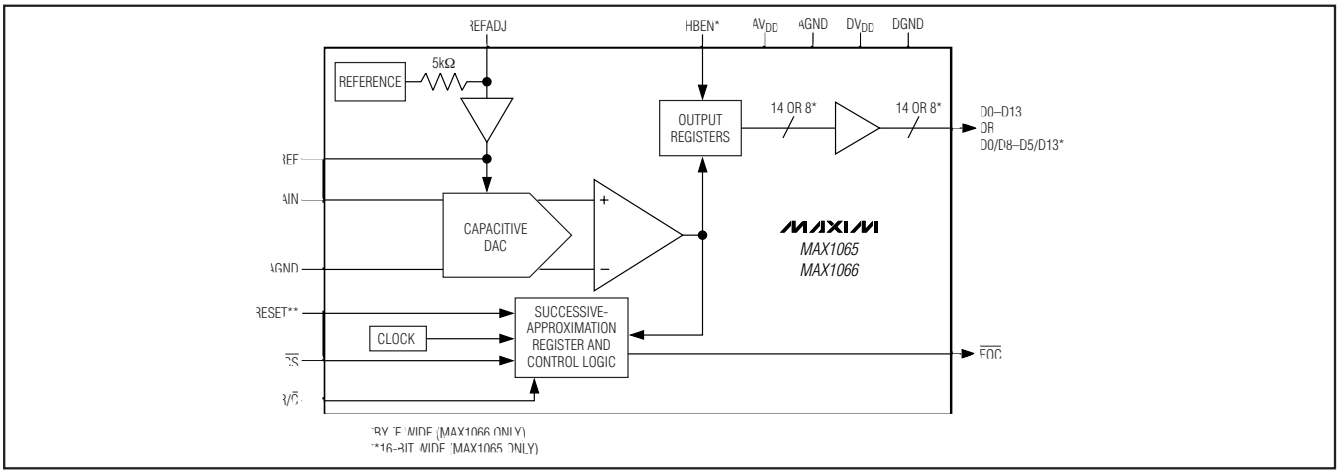
Pin Description

PIN		NAME		FUNCTION
MAX1065	MAX1066	MAX1065	MAX1066	
1	1	D6	D4/D12	Three-State Digital Data Output
2	2	D7	D5/D13	Three-State Digital Data Output. D13 is the MSB.
3	3	D8	D6/0	Three-State Digital Data Output
4	4	D9	D7/0	Three-State Digital Data Output
5	—	D10	—	Three-State Digital Data Output
6	—	D11	—	Three-State Digital Data Output
7	—	D12	—	Three-State Digital Data Output
8	—	D13	—	Three-State Digital Data Output (MSB)
9	5	R/$\overline{C}$		Read/$\overline{Convert}$ Input. Power up and put the MAX1065/MAX1066 in acquisition mode by holding R/$\overline{C}$ low during the first falling edge of $\overline{CS}$. During the second falling edge of $\overline{CS}$ the level on R/$\overline{C}$ determines whether the reference and reference buffer power down or remain on after conversion. Set R/$\overline{C}$ high during the second falling edge of $\overline{CS}$ to power down the reference and buffer, or set R/$\overline{C}$ low to leave the reference and buffer powered up. Set R/$\overline{C}$ high during the third falling edge of $\overline{CS}$ to put valid data on the bus.
10	6	$\overline{EOC}$		End Of Conversion. $\overline{EOC}$ drives low when conversion is complete.
11	7	AV_{DD}		Analog Supply Input. Bypass with a 0.1µF capacitor to AGND.
12	8	AGND		Analog Ground. Primary analog ground (star ground).
13	9	AIN		Analog Input
14	10	AGND		Analog Ground. Connect Pin 14 to Pin 12 (MAX1065). Connect Pin 10 to Pin 8 (MAX1066).

Pin Description (continued)

PIN		NAME		FUNCTION
MAX1065	MAX1066	MAX1065	MAX1066	
15	11	REFADJ		Reference Buffer Output. Bypass REFADJ with a 0.1µF capacitor to AGND for internal reference mode. Connect REFADJ to AV_{DD} to select external reference mode.
16	12	REF		Reference Input/Output. Bypass REF with a 1µF capacitor to AGND for internal reference mode. External reference input when in external reference mode.
17	—	RESET		Reset Input. Logic high resets the device.
—	13	HBEN		High Byte-Enable Input. Used to multiplex the 14-bit conversion result. 1: Most significant byte available on the data bus. 0: Least significant byte available on the data bus.
18	14	$\overline{CS}$		Convert Start. The first falling edge of $\overline{CS}$ powers up the device and enables acquire mode when R/$\overline{C}$ is low. The second falling edge of $\overline{CS}$ starts conversion. The third falling edge of $\overline{CS}$ loads the result onto the bus when R/$\overline{C}$ is high.
19	15	DGND		Digital Ground
20	16	DV_{DD}		Digital Supply Voltage. Bypass with a 0.1µF capacitor to DGND.
21	17	N.C.	D0/D8	No Connection. Do Not Connect (MAX1065). Three-State Digital Data Output (MAX1066).
22	18	N.C.	D1/D9	No Connection. Do Not Connect (MAX1065). Three-State Digital Data Output (MAX1066).
23	19	D0	D2/D10	Three-State Digital Data Output
24	20	D1	D3/D11	Three-State Digital Data Output
25	—	D2	—	Three-State Digital Data Output
26	—	D3	—	Three-State Digital Data Output
27	—	D4	—	Three-State Digital Data Output
28	—	D5	—	Three-State Digital Data Output

Functional Diagram



Low-Power, 14-Bit Analog-to-Digital Converters with Parallel Interface

Detailed Description

Converter Operation

The MAX1065/MAX1066 use a successive-approximation (SAR) conversion technique with an inherent track-and-hold (T/H) stage to convert an analog input into a 14-bit digital output. Parallel outputs provide a high-speed interface to most microprocessors (µPs). The *Functional Diagram* shows a simplified internal architecture of the MAX1065/MAX1066. Figure 3 shows a typical application circuit for the MAX1066.

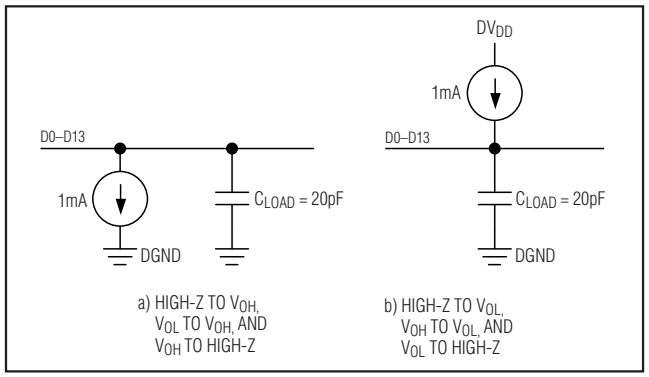


Figure 1. Load Circuits for D0–D13 Enable Time, $\overline{CS}$ to D0–D13 Delay Time and Bus Relinquish Time

Analog Input

The equivalent input circuit is shown in Figure 4. A switched capacitor digital-to-analog converter (DAC) provides an inherent track-and-hold function. The single-ended input is connected between AIN and AGND.

Input Bandwidth

The ADC's input-tracking circuitry has a 4MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, use antialias filtering.

Internal protection diodes, which clamp the analog input to AV_{DD} and/or AGND, allow the input to swing from AGND - 0.3V to AV_{DD} + 0.3V, without damaging the device.

If the analog input exceeds 300mV beyond the supplies, limit the input current to 10mA.

Track and Hold (T/H)

In track mode, the analog signal is acquired on the internal hold capacitor. In hold mode, the T/H switches open and the capacitive DAC samples the analog input.

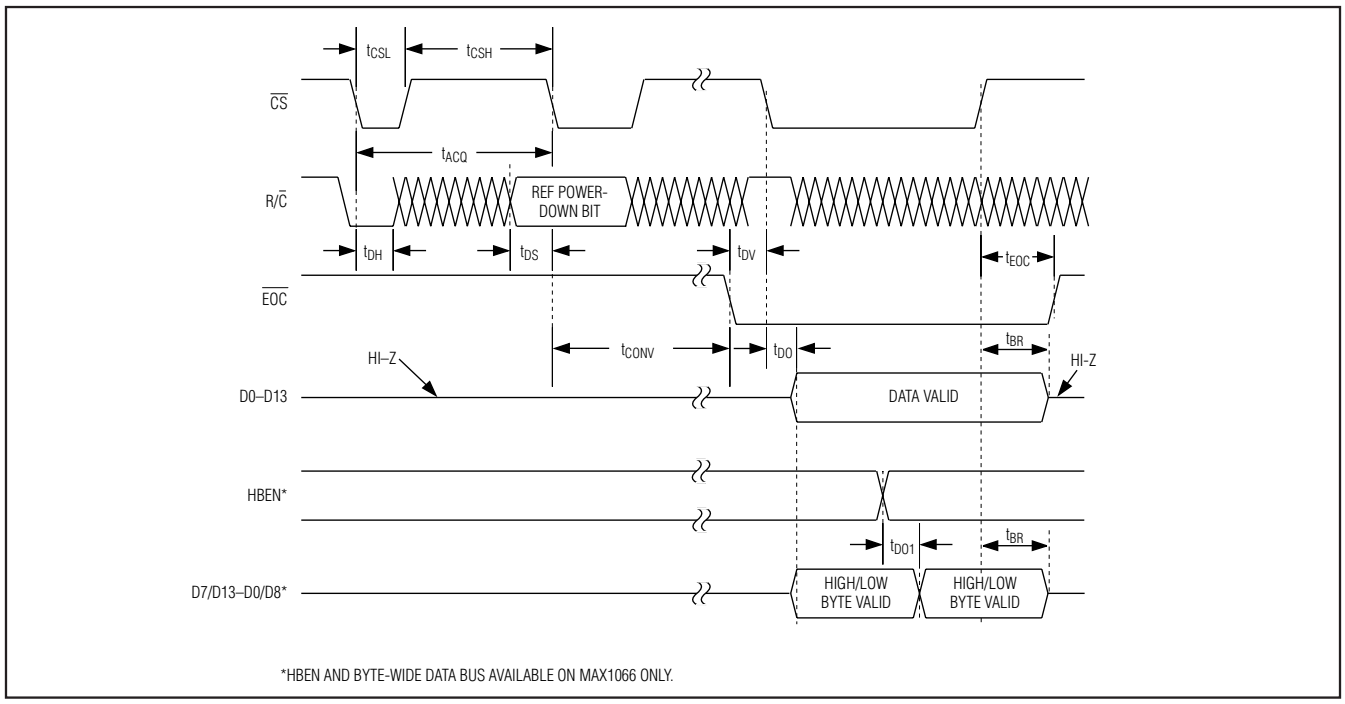


Figure 2. MAX1065/MAX1066 Timing Diagram

During the acquisition, the analog input (AIN) charges capacitor C_{DAC}. The acquisition ends on the second falling edge of $\overline{CS}$. At this instant, the T/H switches open. The retained charge on C_{DAC} represents a sample of the input.

In hold mode, the capacitive DAC adjusts during the remainder of the conversion time to restore node ZERO to zero within the limits of 14-bit resolution. At the end of the conversion, force $\overline{CS}$ low to put valid data on the bus.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time (t_{ACQ}) is the maximum time the device takes to acquire the signal. Use the following formula to calculate acquisition time:

$$t_{ACQ} = 11(R_S + R_{IN}) \times 35pF$$

where $R_{IN} = 800\Omega$, R_S = the input signal's source impedance, and t_{ACQ} is never less than 1.1µs. A source impedance less than 1kΩ does not significantly affect the ADC's performance.

To improve the input-signal bandwidth under AC conditions, drive AIN with a wideband buffer (>4MHz) that can drive the ADC's input capacitance and settle quickly.

Power-Down Modes

Select standby mode or shutdown mode with the R/$\overline{C}$ bit during the second falling edge of $\overline{CS}$ (see *Selecting Standby or Shutdown Mode* section). The MAX1065/MAX1066 automatically enter either standby mode, reference and buffer on, or shutdown, reference and buffer off, after each conversion depending on the status of R/$\overline{C}$ during the second falling edge of $\overline{CS}$.

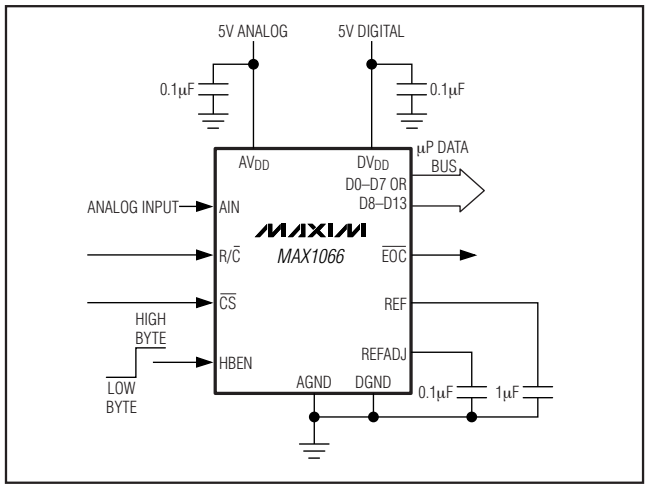


Figure 3. Typical Application Circuit for MAX1066

Internal Clock

The MAX1065/MAX1066 generate an internal conversion clock. This frees the microprocessor from the burden of running the SAR conversion clock. Total conversion time after entering hold mode (second falling edge of $\overline{CS}$) to end-of-conversion ($\overline{EOC}$) falling is 4.7µs (max).

Applications Information

Starting a Conversion

$\overline{CS}$ and R/$\overline{C}$ control acquisition and conversion in the MAX1065/MAX1066 (Figure 2). The first falling edge of $\overline{CS}$ powers up the device and puts it into acquisition mode if R/$\overline{C}$ is low. The convert start is ignored if R/$\overline{C}$ is high. When powering up from shutdown, the MAX1065/MAX1066 needs at least 10ms (C_{REFADJ} = 0.1µF, C_{REF} = 1µF) for the internal reference to wake up and settle before starting the conversion. The ADC may wake up from shutdown to an unknown state. Put the ADC in a known state by completing one "dummy" conversion. The MAX1065/ MAX1066 will be in a known state, ready for actual data acquisition, after the completion of the dummy conversion. A dummy conversion consists of one full conversion cycle.

The MAX1065 provides an alternative reset function to reset the device (see *RESET* section).

Selecting Standby or Shutdown Mode

The MAX1065/MAX1066 have a selectable standby or low-power shutdown mode. In standby mode, the ADC's internal reference and reference buffer do not power down between conversions, eliminating the need to wait for the reference to power up before performing the next conversion. Shutdown mode powers down the reference and reference buffer after completing a conversion. Supply current is greatly reduced when in shutdown mode. The reference and reference buffer require a minimum of 10ms (C_{REFADJ} = 0.1µF, C_{REF} = 1µF) to power up and settle from shutdown.

The state of R/$\overline{C}$ at the second falling edge of $\overline{CS}$ selects which power-down mode the MAX1065/MAX1066 enters upon conversion completion. Holding R/$\overline{C}$ low causes the MAX1065/MAX1066 to enter standby mode. The reference and buffer are left on after the conversion completes. R/$\overline{C}$ high causes the MAX1065/MAX1066 to enter shutdown mode and shut down the reference and buffer after conversion (Figures 5 and 6).

When using an external reference, set the REF power-down bit high for lowest current operation.

Low-Power, 14-Bit Analog-to-Digital Converters with Parallel Interface

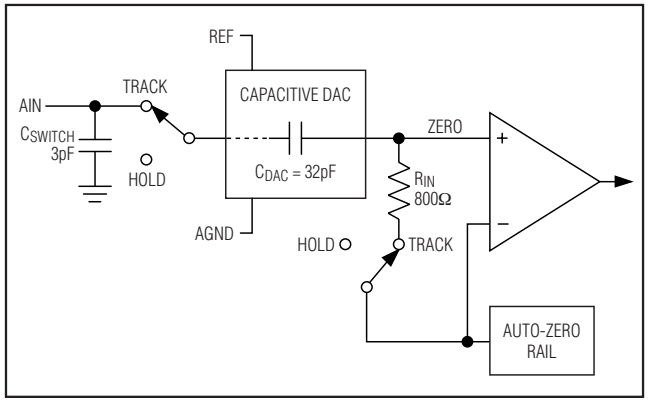


Figure 4. Equivalent Input Circuit

Standby Mode

While in standby mode, the supply current is reduced to less than 1mA (typ). The next falling edge of $\overline{CS}$ with R/$\overline{C}$ low causes the MAX1065/MAX1066 to exit standby mode and begin acquisition. The reference and reference buffer remain active to allow quick turn-on time. Standby mode allows significant power savings while running at the maximum sample rate.

Shutdown Mode

In shutdown mode, the reference and reference buffer are shut down between conversions. Shutdown mode reduces supply current to 0.5µA (typ) immediately after the conversion. The falling edge of $\overline{CS}$ with R/$\overline{C}$ low causes the reference and buffer to wake up and enter acquisition mode. To achieve 14-bit accuracy, allow 10ms (C_{REFADJ} = 0.1µF, C_{REF} = 1µF) for the internal reference to wake up. Increase wakeup time proportionally when using larger values of C_{REFADJ} and C_{REF}.

Internal and External Reference

Internal Reference

The internal reference of the MAX1065/MAX1066 is internally buffered to provide 4.096V (typ) output at REF. Bypass REF to AGND and REFADJ to AGND with 1µF and 0.1µF respectively. Fine adjustments can be made to the internal reference voltage by sinking or sourcing current at REFADJ. The input impedance at REFADJ is nominally 5kΩ. The internal reference voltage is adjustable to ±1.5% with the circuit of Figure 7.

External Reference

An external reference can be placed at either the input (REFADJ) or the output (REF) of the MAX1065/MAX1066's internal buffer amplifier. When connecting an external reference to REFADJ, the input impedance is typically 5kΩ. Using the buffered REFADJ input makes buffering the external reference unnecessary; however, the internal buffer output must be bypassed at REF with a 1µF capacitor.

Connect REFADJ to AV_{DD} to disable the internal buffer. Directly drive REF using an external reference. During conversion, the external reference must be able to drive 100µA of DC load current and have an output impedance of 10Ω or less. REFADJ's impedance is typically 5kΩ. The DC input impedance of REF is 40kΩ minimum.

For optimal performance, buffer the reference through an op amp and bypass REF with a 1µF capacitor. Consider the MAX1065/MAX1066's equivalent input noise (80μV_{RMS}) when choosing a reference.

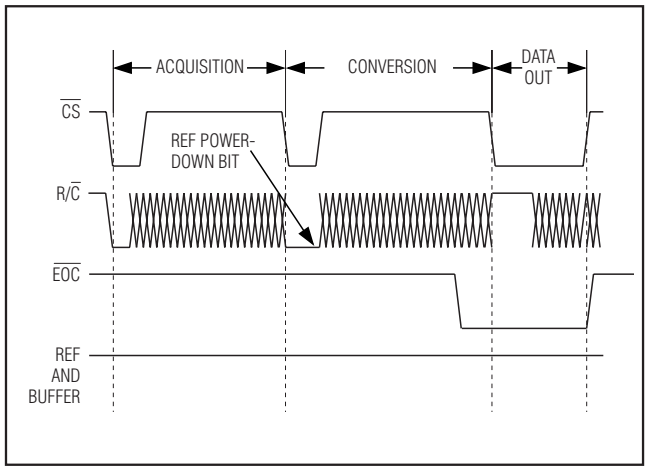


Figure 5. Selecting Standby Mode

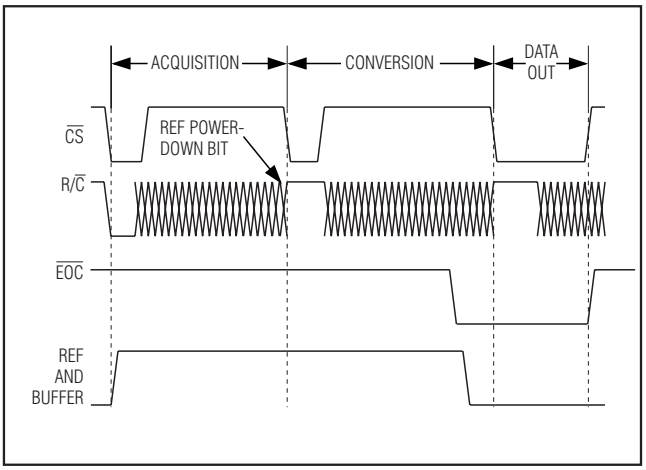


Figure 6. Selecting Shutdown Mode

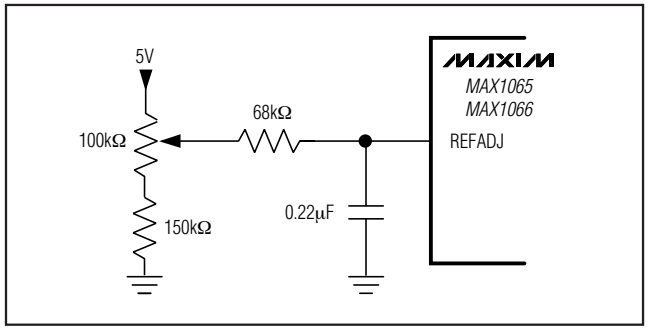


Figure 7. MAX1065/MAX1066 Reference Adjust Circuit

Reading the Conversion Result

$\overline{EOC}$ is provided to flag the microprocessor when a conversion is complete. The falling edge of $\overline{EOC}$ signals that the data is valid and ready to be output to the bus.

D0–D13 are the parallel outputs of the MAX1065/MAX1066. These three-state outputs allow for direct connection to a microcontroller I/O bus. The outputs remain high-impedance during acquisition and conversion. Data is loaded onto the bus with the third falling edge of $\overline{CS}$ with R/$\overline{C}$ high after t_{DO}ns. Bringing $\overline{CS}$ high forces the output bus back to high-impedance. The MAX1065/MAX1066 then waits for the next falling edge of $\overline{CS}$ to start the next conversion cycle (Figure 2).

The MAX1065 loads the conversion result onto a 14-bit-wide data bus while the MAX1066 has a byte-wide output format. HBEN toggles the output between the most/least significant byte. The least significant byte is loaded onto the output bus when HBEN is low and the most significant byte is on the bus when HBEN is high (Figure 2).

RESET

Toggle RESET with $\overline{CS}$ high. The next falling edge of $\overline{CS}$ will begin acquisition. This reset is an alternative to the dummy conversion explained in the *Starting a Conversion* section.

Transfer Function

Figure 8 shows the MAX1065/MAX1066 output transfer function. The output is coded in standard binary.

Input Buffer

Most applications require an input buffer amplifier to achieve 14-bit accuracy. If the input signal is multiplexed, the input channel should be switched immediately after acquisition, rather than near the end of or after a conversion. This allows more time for the input buffer amplifier to respond to a large step-change in input signal. The input amplifier must have a high enough slew rate to complete

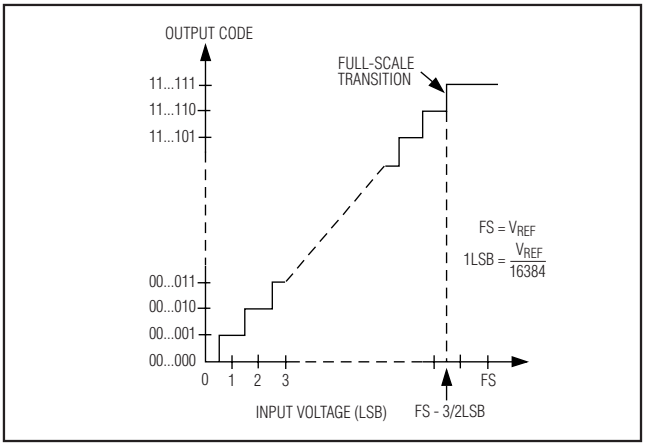


Figure 8. MAX1065/MAX1066 Transfer Function

the required output voltage change before the beginning of the acquisition time. At the beginning of acquisition, the internal sampling capacitor array connects to AIN (the amplifier output) causing some output disturbance. Ensure that the sampled voltage has settled to within the required limits before the end of the acquisition time. If the frequency of interest is low, AIN can be bypassed with a large enough capacitor to charge the internal sampling capacitor with very little ripple. However, for AC use, AIN must be driven by a wideband buffer (at least 10MHz), which must be stable with the ADC's capacitive load (in parallel with any AIN bypass capacitor used) and also settle quickly. An example of this circuit using the MAX4434 is given in Figure 9.

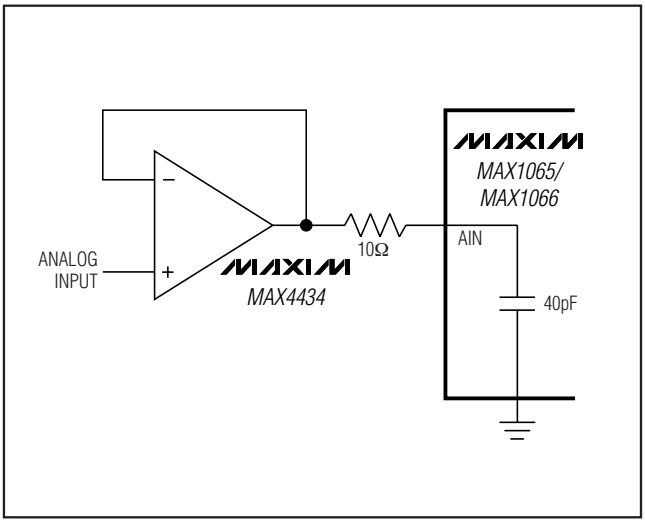


Figure 9. MAX1065/MAX1066 Fast Settling Input Buffer

Low-Power, 14-Bit Analog-to-Digital Converters with Parallel Interface

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital ground planes with only one point connecting the two ground systems (analog and digital) as close to the device as possible.

Route digital signals far away from sensitive analog and reference inputs. If digital lines must cross analog lines, do so at right angles to minimize coupling digital noise onto the analog lines. If the analog and digital sections share the same supply, then isolate the digital and analog supply by connecting them with a low-value (10Ω) resistor or ferrite bead.

The ADC is sensitive to high-frequency noise on the AV_{DD} supply. Bypass AV_{DD} to AGND with a 0.1µF capacitor in parallel with a 1µF to 10µF low-ESR capacitor and the smallest capacitor closest to the device. Keep capacitor leads short to minimize stray inductance.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1065/MAX1066 are measured using the end-point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of 1LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter and Delay

Aperture jitter is the sample-to-sample variation in the time between samples. Aperture delay is the time between the rising edge of the sampling clock and the instant when the actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N-bits):

$$SNR = (6.02 \times N + 1.76)dB$$

where N = 14 bits.

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals.

$$SINAD(dB) = 20 \times \log\left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}}\right]$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left[\frac{\left(\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}\right)}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

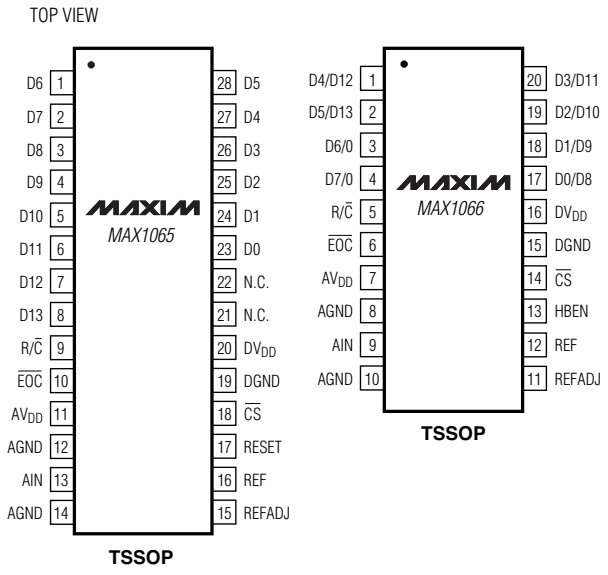
Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest frequency component.

Chip Information

TRANSISTOR COUNT: 15,140

PROCESS: BiCMOS

Pin Configurations



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 SSOP	U28-1	21-0066
20 SSOP	U20-2	21-0066

Low-Power, 14-Bit Analog-to-Digital Converters with Parallel Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/02	Initial release	—
1	6/09	Modified specifications to include reference buffer	3, 4