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## MAX77654

# Ultra-Low Power PMIC Featuring Single-Inductor, 3-Output Buck-Boost, 2-LDOs, Power-Path Charger for Small Li+, and Ship Mode

## General Description

The MAX77654 provides highly-integrated battery charging and power supply solutions for low-power applications where size and efficiency are critical. The IC features a SIMO buck-boost regulator that provides three independently programmable power rails from a single inductor to minimize total solution size. Two 100mA LDOs provide ripple rejection for audio and other noise-sensitive applications. The LDOs can also be configured as load switches to manage power consumption by disconnecting external blocks when not required. A highly-configurable linear charger supports a wide range of Li+ battery capacities and includes battery temperature monitoring for additional safety (JEITA).

This device includes three GPIOs and an analog multiplexer that switches several internal voltage and current signals to an external node for monitoring with an external ADC. A bidirectional I<sup>2</sup>C serial interface allows for configuring and checking the status of the devices. An internal on/off controller provides a controlled startup sequence for the regulators and provides supervisory functionality while they are on. Numerous factory programmable options allow the device to be tailored for many applications, enabling faster time to market.

## Applications

- Bluetooth Headphones, Hearables
- Wireless Speakers
- Fitness, Health, and Activity Monitors
- Wearables
- Safety and Security Monitors
- Sensor Nodes
- Portable Consumer Devices
- Internet of Things (IoT)

## Benefits and Features

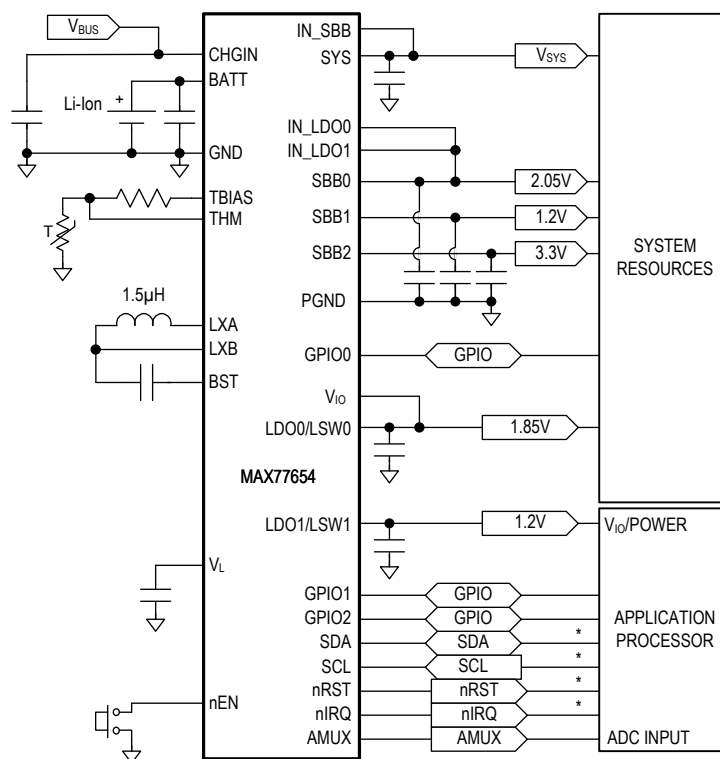
- Highly Integrated
  - 3x Output, Single-Inductor Multiple-Output (SIMO) Buck-Boost Regulator
    - Supports Wide Output Voltage Range from 0.8V to 5.5V for all SIMO Channels
  - 2x 100mA LDO/LSW
  - Smart Power Selector™ Li+/Li-Poly Charger
  - 3x GPIO Resources
  - Analog MUX Output for Power Monitoring
  - Factory Ship Mode (< 200nA I<sub>Q</sub>)
  - Watchdog Timer
- Low Power
  - 0.3μA Shutdown Current
  - 6μA Operating Current (3 SIMO Channels + 2 LDOs)
- Charger Optimized for Small Battery Size
  - Programmable Fast-Charge Current from 7.5mA to 300mA
  - Programmable Battery Regulation Voltage from 3.6V to 4.6V
  - Programmable Termination Current from 0.375mA to 45mA
  - JEITA Battery Temperature Monitors Adjust Charge Current and Battery Regulation Voltage for Safe Charging
- Flexible and Configurable
  - I<sup>2</sup>C-Compatible Interface and GPIO
  - Factory OTP Options Available
- Small Size
  - 6.52mm<sup>2</sup> Wafer-Level Package (WLP)
  - 30-Bump, 0.4mm Pitch, 6x5 Array
  - Small Total Solution Size (29.7mm<sup>2</sup>)

**Ordering Information** appears at end of data sheet.

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.



## Simplified Block Diagram



\*PULLUP RESISTORS NOT DRAWN

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## Absolute Maximum Ratings

|                                                      |                               |                                                                                                                    |                     |
|------------------------------------------------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------|---------------------|
| nIRQ, nRST to GND .....                              | -0.3V to $V_{SYS} + 0.3V$     | IN_SBB to PGND .....                                                                                               | -0.3V to +6.0V      |
| nEN to GND (Note 1) .....                            | -0.3V to $V_{CCINT} + 0.3V$   | LXA Continuous Current (Note 3) .....                                                                              | 1.2A <sub>RMS</sub> |
| SCL, SDA, GPIO to GND .....                          | -0.3V to $V_{IO} + 0.3V$      | LXB Continuous Current (Note 3) .....                                                                              | 1.2A <sub>RMS</sub> |
| CHGIN to GND .....                                   | -0.3V to +30.0V               | SBB0, SBB1, SBB2 to PGND .....                                                                                     | -0.3V to +6.0V      |
| SYS, BATT to GND .....                               | -0.3V to +6.0V                | BST to IN_SBB .....                                                                                                | -0.3V to +6.0V      |
| SYS to IN_SBB .....                                  | -0.3V to +0.3V                | BST to LXB .....                                                                                                   | -0.3V to +6.0V      |
| VL to GND .....                                      | -0.3V to +6.0V                | SBB0, SBB1, SBB2 Short-Circuit Duration .....                                                                      | Continuous          |
| AMUX, THM, TBIAS to GND .....                        | -0.3V to +6.0V                | PGND to GND .....                                                                                                  | -0.3V to +0.3V      |
| nIRQ, nRST, SDA, AMUX, GPIO Continuous Current ..... | ±20mA                         | Operating Temperature Range .....                                                                                  | -40°C to +85°C      |
| CHGIN Continuous Current .....                       | 1.2A <sub>RMS</sub>           | Junction Temperature .....                                                                                         | +150°C              |
| SYS Continuous Current .....                         | 1.2A <sub>RMS</sub>           | Storage Temperature Range .....                                                                                    | -65°C to +150°C     |
| BATT Continuous Current (Note 2) .....               | 1.2A <sub>RMS</sub>           | Soldering Temperature (reflow) .....                                                                               | +260°C              |
| LDO0, LDO1 to GND .....                              | -0.3V to $V_{IN\_LDO} + 0.3V$ | Continuous Power Dissipation (Multilayer Board, $T_A = +70^\circ\text{C}$ ,<br>derate 20.4mW/°C above +70°C) ..... | 1632mW              |
| IN_LDO0, IN_LDO1, $V_{IO}$ to GND .....              | -0.3V to $V_{SYS} + 0.3V$     |                                                                                                                    |                     |

**Note 1:**  $V_{CCINT}$  is internally connected to either BATT or VL. See the [nEN Internal Pullup Resistors to  \$V\_{CCINT}\$](#)  section for more details.

**Note 2:** Do not repeatedly hot-plug a source to the BATT terminal at a rate greater than 10Hz. Hot plugging low impedance sources results in an ~8A momentary (~2μs) current spike.

**Note 3:** Do not externally bias LXA or LXB. LXA has internal clamping diodes to PGND and IN\_SBB. LXB has an internal low-side clamping diode to PGND and an internal high-side clamping diode that dynamically connects to a selected SIMO output. It is normal for these diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to  $V_{SBB0} + 0.3V$ .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### WLP

|                                              |                                                |
|----------------------------------------------|------------------------------------------------|
| Package Code                                 | N302C2+1                                       |
| Outline Number                               | <a href="#">21-100307</a>                      |
| Land Pattern Number                          | <a href="#">Refer to Application Note 1891</a> |
| <b>Thermal Resistance, Four-Layer Board:</b> |                                                |
| Junction to Ambient ( $\theta_{JA}$ )        | 49°C/W (2s2p board)                            |

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{CHGIN} = 0V$ ,  $V_{SYS} = V_{BATT} = V_{IN\_SBB} = V_{IN\_LDOx} = 3.7V$ ,  $V_{IO} = 1.8V$ , limits are 100% production tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                      | SYMBOL         | CONDITIONS                                                                                                                               |                                                                                      | MIN | TYP | MAX | UNITS   |
|--------------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|-----|-----|-----|---------|
| Operating Voltage Range        | $V_{SYS}$      |                                                                                                                                          |                                                                                      | 2.7 |     | 5.5 | V       |
| Shutdown Supply Current        | $I_{SHDN}$     | Current measured into BATT and SYS and IN_SBB and IN_LDOx, all resources are off (LDO0, LDO1, SBB0, SBB1, SBB2), $T_A = +25^\circ C$     | Main bias is off (CNFG_GLBL.SBIA_EN = 0); this is the standby state                  |     | 0.3 | 1   | $\mu A$ |
|                                |                |                                                                                                                                          | Main bias is on in low-power mode (CNFG_GLBL.SBIA_EN = 1, CNFG_GLBL.SBIA_LPM = 1)    |     | 1   |     |         |
|                                |                |                                                                                                                                          | Main bias is on in normal-power mode (CNFG_GLBL.SBIA_EN = 1, CNFG_GLBL.SBIA_LPM = 0) |     | 28  |     |         |
| Main Bias Quiescent Current    | $I_Q$          | Main bias is in normal-power mode (CNFG_GLBL.SBIA_LPM = 0)                                                                               |                                                                                      |     | 28  |     | $\mu A$ |
| Quiescent Supply Current       | $I_Q$          | Current measured into BATT and SYS and IN_SBB and IN_LDOx; LDO0, LDO1, SBB0, SBB1, SBB2 are enabled with no load watchdog timer disabled | Main bias is in low-power mode (CNFG_GLBL.SBIA_LPM = 1)                              |     | 6   | 13  | $\mu A$ |
| BATT Factory-Ship Mode Current | $I_{BATT-FSM}$ | Factory-ship mode (BATT to SYS switch open), $T_A = +25^\circ C$ , $V_{BATT} = 3.7V$ , $V_{SYS} = V_{INLDO0} = V_{INLDO1} = 0V$          |                                                                                      |     | 0.2 | 1   | $\mu A$ |

## Electrical Characteristics—Global Resources

( $V_{SYS} = 3.7V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                      | SYMBOL         | CONDITIONS        | MIN | TYP | MAX | UNITS |
|------------------------------------------------|----------------|-------------------|-----|-----|-----|-------|
| <b>GENERAL CHARACTERISTICS</b>                 |                |                   |     |     |     |       |
| Main Bias Enable Time                          | $t_{SBIA\_EN}$ |                   |     | 0.5 |     | ms    |
| <b>VOLTAGE MONITORS / POWER-ON RESET (POR)</b> |                |                   |     |     |     |       |
| POR Threshold                                  | $V_{POR}$      | $V_{SYS}$ falling | 1.6 | 1.9 | 2.1 | V     |
| POR Threshold Hysteresis                       |                |                   |     | 100 |     | mV    |

## Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.7V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                      | SYMBOL                   | CONDITIONS                                                    |                                                                          | MIN                      | TYP                      | MAX                      | UNITS |
|------------------------------------------------|--------------------------|---------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------|--------------------------|--------------------------|-------|
| VOLTAGE MONITORS / UNDERVOLTAGE LOCKOUT (UVLO) |                          |                                                               |                                                                          |                          |                          |                          |       |
| UVLO Threshold                                 | V <sub>SYSUVLO</sub>     | V <sub>SYS</sub> falling, UVLO_F[3:0] = 0xA ( <i>Note 5</i> ) |                                                                          | 2.5                      | 2.6                      | 2.7                      | V     |
|                                                |                          | V <sub>SYS</sub> falling, UVLO_F[3:0] = 0xF ( <i>Note 5</i> ) |                                                                          | 2.75                     | 2.85                     | 2.95                     |       |
| UVLO Threshold Hysteresis                      | V <sub>SYSUVLO_HYS</sub> | UVLO_H[3:0] = 0x5 ( <i>Note 5</i> )                           |                                                                          |                          | 300                      |                          | mV    |
| VOLTAGE MONITORS / OVERVOLTAGE LOCKOUT (OVLO)  |                          |                                                               |                                                                          |                          |                          |                          |       |
| OVLO Threshold                                 | V <sub>SYSOVLO</sub>     | V <sub>SYS</sub> rising                                       |                                                                          | 5.70                     | 5.85                     | 6.00                     | V     |
| THERMAL MONITORS                               |                          |                                                               |                                                                          |                          |                          |                          |       |
| Overtemperature-Lockout Threshold              | T <sub>OTLO</sub>        | T <sub>J</sub> rising                                         |                                                                          |                          | 165                      |                          | °C    |
| Thermal Alarm Temperature 1                    | T <sub>JAL1</sub>        | T <sub>J</sub> rising                                         |                                                                          |                          | 80                       |                          | °C    |
| Thermal Alarm Temperature 2                    | T <sub>JAL2</sub>        | T <sub>J</sub> rising                                         |                                                                          |                          | 100                      |                          | °C    |
| Thermal Alarm Temperature Hysteresis           |                          |                                                               |                                                                          |                          | 15                       |                          | °C    |
| ENABLE INPUT (nEN)                             |                          |                                                               |                                                                          |                          |                          |                          |       |
| nEN Input Leakage Current                      | I <sub>nEN_LKG</sub>     | V <sub>nEN</sub> = V <sub>SYS</sub> = 5.5V                    | T <sub>A</sub> = +25°C                                                   | -1                       | ±0.001                   | +1                       | µA    |
|                                                |                          |                                                               | T <sub>A</sub> = +85°C                                                   |                          | ±0.01                    |                          |       |
| nEN Input Falling Threshold                    | V <sub>TH_nEN_F</sub>    | nEN Falling                                                   |                                                                          | V <sub>CCINT</sub> - 1.4 | V <sub>CCINT</sub> - 1.0 |                          | V     |
| nEN Input Rising Threshold                     | V <sub>TH_nEN_R</sub>    | nEN Rising                                                    |                                                                          |                          | V <sub>CCINT</sub> - 0.9 | V <sub>CCINT</sub> - 0.6 | V     |
| V <sub>CC</sub> Internal                       | V <sub>CCINT</sub>       | <i>(Note 4)</i>                                               | V <sub>CHGIN</sub> = 0V, battery is present (V <sub>BATT</sub> is valid) | V <sub>BATT</sub>        |                          | V                        |       |
|                                                |                          |                                                               | V <sub>CHGIN</sub> = 5V, not suspended (CNFG_CHG_G.U SBS = 0)            | V <sub>L</sub>           |                          |                          |       |
| Debounce Time                                  | t <sub>DBNC_nEN</sub>    | CNFG_GLBL.DBEN_nEN = 0                                        |                                                                          | 500                      |                          | µs                       |       |
|                                                |                          | CNFG_GLBL.DBEN_nEN = 1                                        |                                                                          | 30                       |                          | ms                       |       |
| Manual Reset Time                              | t <sub>MRST</sub>        | CNFG_GLBL.T_MRT = 1                                           |                                                                          | 14                       | 16                       | 20                       | s     |
|                                                |                          | CNFG_GLBL.T_MRT = 0                                           |                                                                          | 7                        | 8                        | 10.5                     |       |
| nEN Internal Pullup                            | R <sub>nEN-PU</sub>      | Pullup to V <sub>CCINT</sub>                                  | PU_DIS = 0                                                               | 200                      |                          | kΩ                       |       |
|                                                |                          |                                                               | PU_DIS = 1                                                               | 10000                    |                          |                          |       |
| OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)             |                          |                                                               |                                                                          |                          |                          |                          |       |
| Output Voltage Low                             | V <sub>OL</sub>          | I <sub>SINK</sub> = 2mA                                       |                                                                          | 0.4                      |                          | V                        |       |
| Output Falling Edge Time                       | t <sub>f_nIRQ</sub>      | C <sub>IRQ</sub> = 25pF                                       |                                                                          | 2                        |                          | ns                       |       |

## Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.7V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                           | SYMBOL                | CONDITIONS                                                                                                             |                        | MIN                   | TYP    | MAX | UNITS |
|-------------------------------------|-----------------------|------------------------------------------------------------------------------------------------------------------------|------------------------|-----------------------|--------|-----|-------|
| Leakage Current                     | I <sub>nIRQ_LKG</sub> | V <sub>SYS</sub> = V <sub>IO</sub> = 5.5V<br>nIRQ is high impedance (no interrupts)<br>V <sub>nIRQ</sub> = 0V and 5.5V | T <sub>A</sub> = +25°C | -1                    | ±0.001 | +1  | μA    |
|                                     |                       |                                                                                                                        | T <sub>A</sub> = +85°C | ±0.01                 |        |     |       |
| OPEN-DRAIN RESET OUTPUT (nRST)      |                       |                                                                                                                        |                        |                       |        |     |       |
| Output Voltage Low                  | V <sub>OL</sub>       | I <sub>SINK</sub> = 2mA                                                                                                |                        | 0.4                   |        |     | V     |
| Output Falling Edge Time            | t <sub>f_nRST</sub>   | C <sub>RST</sub> = 25pF                                                                                                |                        | 2                     |        |     | ns    |
| nRST Deassert Delay Time            | t <sub>RSTODD</sub>   | See <a href="#">Figure 10</a> and <a href="#">Figure 11</a> for more information                                       |                        | 5.12                  |        |     | ms    |
| nRST Assert Delay Time              | t <sub>RSTOAD</sub>   |                                                                                                                        |                        | 10.24                 |        |     | ms    |
| Leakage Current                     | I <sub>nRST_LKG</sub> | V <sub>SYS</sub> = V <sub>IO</sub> = 5.5V<br>nRST is high impedance (no reset)<br>V <sub>nRST</sub> = 0V and 5.5V      | T <sub>A</sub> = +25°C | -1                    | ±0.001 | +1  | μA    |
|                                     |                       |                                                                                                                        | T <sub>A</sub> = +85°C | ±0.01                 |        |     |       |
| GENERAL PURPOSE INPUT/OUTPUT (GPIO) |                       |                                                                                                                        |                        |                       |        |     |       |
| Input Voltage Low                   | V <sub>IL</sub>       | V <sub>IO</sub> = 1.8V                                                                                                 |                        | 0.3 x V <sub>IO</sub> |        |     | V     |
| Input Voltage High                  | V <sub>IH</sub>       | V <sub>IO</sub> = 1.8V                                                                                                 |                        | 0.7 x V <sub>IO</sub> |        |     | V     |
| Input Leakage Current               | I <sub>GPI_LKG</sub>  | CNFG_GPIOx.DIR = 1<br>V <sub>IO</sub> = 5.5V<br>V <sub>GPIO</sub> = 0V and 5.5V                                        | T <sub>A</sub> = +25°C | -1                    | ±0.001 | +1  | μA    |
|                                     |                       |                                                                                                                        | T <sub>A</sub> = +85°C | ±0.01                 |        |     |       |
| Output Voltage Low                  | V <sub>OL</sub>       | I <sub>SINK</sub> = 2mA                                                                                                |                        | 0.4                   |        |     | V     |
| Output Voltage High                 | V <sub>OH</sub>       | I <sub>SOURCE</sub> = 1mA                                                                                              |                        | 0.8 x V <sub>IO</sub> |        |     | V     |
| Input Debounce Time                 | t <sub>DBNC_GPI</sub> | CNFG_GPIOx.DBEN_GPI = 1                                                                                                |                        | 30                    |        |     | ms    |
| Output Falling Edge Time            | t <sub>f_GPIO</sub>   | C <sub>GPIO</sub> = 25pF                                                                                               |                        | 3                     |        |     | ns    |
| Output Rising Edge Time             | t <sub>r_GPIO</sub>   | C <sub>GPIO</sub> = 25pF                                                                                               |                        | 3                     |        |     | ns    |
| FLEXIBLE POWER SEQUENCER            |                       |                                                                                                                        |                        |                       |        |     |       |
| FPS Startup Delay                   | t <sub>FPS_DLY</sub>  |                                                                                                                        |                        | 1.43                  |        |     | ms    |
| Power-Up Event Periods              | t <sub>EN</sub>       | See <a href="#">Figure 9</a>                                                                                           |                        | 1.28                  |        |     | ms    |
| Power-Down Event Periods            | t <sub>DIS</sub>      | See <a href="#">Figure 9</a>                                                                                           |                        | 2.56                  |        |     | ms    |

**Note 4:** See the [nEN Internal Pullup Resistors to  \$V\_{CCINT}\$](#)  section for more details.

**Note 5:** Programmed at Maxim's factory.

## Electrical Characteristics—Smart Power Selector Charger

( $V_{CHGIN} = 5.0V$ ,  $V_{SYS} = 4.5V$ ,  $V_{BATT} = 4.2V$ , limits are 100% production tested at  $T_A = +25^{\circ}C$ , limits over the operating temperature range ( $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                 | SYMBOL            | CONDITIONS                                                                                                                                              | MIN  | TYP  | MAX  | UNITS   |
|-------------------------------------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------|
| <b>DC INPUT</b>                           |                   |                                                                                                                                                         |      |      |      |         |
| CHGIN Valid Voltage Range                 | $V_{CHGIN}$       | Initial CHGIN voltage before enabling charging                                                                                                          | 4.10 |      | 7.25 | V       |
| CHGIN Standoff Voltage Range              | $V_{STANDOFF}$    | DC rising                                                                                                                                               |      | 28   |      | V       |
| CHGIN Overvoltage Threshold               | $V_{CHGIN\_OVP}$  | DC rising                                                                                                                                               | 7.25 | 7.50 | 7.75 | V       |
| CHGIN Overvoltage Hysteresis              |                   |                                                                                                                                                         |      | 100  |      | mV      |
| CHGIN Undervoltage Lockout                | $V_{CHGIN\_UVLO}$ | DC rising                                                                                                                                               | 3.9  | 4.0  | 4.1  | V       |
| CHGIN Undervoltage-Lockout Hysteresis     |                   |                                                                                                                                                         |      | 500  |      | mV      |
| Input Current-Limit Range                 | $I_{CHGIN\_LIM}$  | $V_{SYS} = V_{SYS\_REG} - 100mV$ , programmable in 95mA steps                                                                                           | 95   |      | 475  | mA      |
| Input Current-Limit Accuracy              |                   | $I_{CHGIN\_LIM} = 95mA$ , $V_{SYS} = V_{SYS\_REG} - 100mV$                                                                                              | 90   | 95   | 100  | mA      |
|                                           |                   | $I_{CHGIN\_LIM} = 475mA$ , $V_{SYS} = V_{SYS\_REG} - 100mV$                                                                                             |      | 475  | 500  |         |
| Minimum Input Voltage Regulation Range    | $V_{CHGIN\_MIN}$  | $V_{CHGIN}$ falling due to loading conditions and/or high-impedance charge source, programmable in 100mV increments with CNFG_CHG_B.VCHGIN_MIN[2:0]     | 4.0  |      | 4.7  | V       |
| Minimum Input Voltage Regulation Accuracy |                   | $V_{CHGIN\_MIN} = 4.5V$ (CNFG_CHG_B.VCHGIN_MIN[2:0] = 0b101), $I_{CHGIN}$ reduced by 10%                                                                | 4.32 | 4.50 | 4.68 | V       |
| Charger Input Debounce Timer              | $t_{CHGIN\_DB}$   | $V_{CHGIN} = 5V$ , time before CHGIN is allowed to deliver current to SYS or BATT                                                                       | 100  | 120  | 140  | ms      |
| <b>SUPPLY AND QUIESCENT CURRENTS</b>      |                   |                                                                                                                                                         |      |      |      |         |
| CHGIN Supply Current                      | $I_{CHGIN}$       | $V_{CHGIN} = 5V$ , charger is not in USB suspend (CNFG_CHG_G.USBS = 0), charging is finished (STAT_CHG_B.CHG_DTLS[3:0] indicates done), $I_{SYS} = 0mA$ |      | 1.0  | 1.8  | mA      |
|                                           |                   | $V_{CHGIN} = 0V$ to $1V$ , $V_{BATT} = 3.3V$ , $I_{SYS} = 0mA$                                                                                          |      |      | 50   | $\mu A$ |
| CHGIN Suspend Supply Current              | $I_{CHGIN\_SUS}$  | $V_{CHGIN} = 5V$ , charger in USB suspend (CNFG_CHG_G.USBS = 1)                                                                                         |      |      | 50   | $\mu A$ |
| BATT Bias Current                         | $I_{BATT\_BIAS}$  | $V_{CHGIN} = 5V$ , charger is not in USB suspend (CNFG_CHG_G.USBS = 0), charging is finished (STAT_CHG_B.CHG_DTLS[3:0] indicates done), $I_{SYS} = 0mA$ |      | 5    |      | $\mu A$ |

## Electrical Characteristics—Smart Power Selector Charger (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{SYS} = 4.5V$ ,  $V_{BATT} = 4.2V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                     | SYMBOL                | CONDITIONS                                                                                                                                              |                                                                               | MIN  | TYP | MAX  | UNITS   |
|-----------------------------------------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|------|-----|------|---------|
| PREQUALIFICATION                              |                       |                                                                                                                                                         |                                                                               |      |     |      |         |
| Charge Current Soft-Start Slew Time           |                       | Zero to full-scale                                                                                                                                      |                                                                               | 1    |     |      | ms      |
| Prequalification Voltage Threshold Range      | V <sub>PQ</sub>       | Programmable in 100mV steps with CNFG_CHG_C.CHG_PQ[2:0]                                                                                                 |                                                                               | 2.3  |     | 3.0  | V       |
| Prequalification Voltage Threshold Accuracy   |                       | V <sub>PQ</sub> = 3.0V                                                                                                                                  |                                                                               | -3   |     | +3   | %       |
| Prequalification Mode Charge Current          | I <sub>PQ</sub>       | V <sub>BATT</sub> = 2.5V<br>V <sub>PQ</sub> = 3.0V<br>Expressed as a percentage of I <sub>FAST-CHG</sub>                                                | CNFG_CHG_B.I_P<br>Q = 0                                                       | 10   |     |      | %       |
|                                               |                       |                                                                                                                                                         | CNFG_CHG_B.I_P<br>Q = 1                                                       | 20   |     |      |         |
| Prequalification Safety Timer                 | t <sub>PQ</sub>       | V <sub>BATT</sub> < V <sub>PQ</sub> = 3.0V                                                                                                              |                                                                               | 27   | 30  | 33   | minutes |
| FAST-CHARGE                                   |                       |                                                                                                                                                         |                                                                               |      |     |      |         |
| Fast-Charge Voltage Range                     | V <sub>FAST-CHG</sub> | I <sub>BATT</sub> = 0mA, programmable in 25mV steps with CNFG_CHG_G.CHG_CV[5:0]                                                                         |                                                                               | 3.6  |     | 4.6  | V       |
| Fast-Charge Voltage Accuracy                  |                       | I <sub>BATT</sub> = 0mA                                                                                                                                 | V <sub>FAST-CHG</sub> = 4.3V, V <sub>SYS</sub> = 4.5V, T <sub>A</sub> = +25°C | -0.5 |     | +0.5 | %       |
|                                               |                       |                                                                                                                                                         | V <sub>FAST-CHG</sub> = 3.6V to 4.6V, V <sub>SYS</sub> = 4.8V                 |      |     | 1.0  |         |
| Fast-Charge Current Range                     | I <sub>FAST-CHG</sub> | Programmable in 7.5mA steps with CNFG_CHG_E.CHG_CC[5:0]                                                                                                 |                                                                               | 7.5  |     | 300  | mA      |
| Fast-Charge Current Accuracy                  |                       | T <sub>A</sub> = +25°C, V <sub>BATT</sub> = V <sub>FAST-CHG</sub> - 300mV                                                                               | I <sub>FAST-CHG</sub> = 15mA                                                  | -1.5 |     | +1.5 | %       |
|                                               |                       |                                                                                                                                                         | I <sub>FAST-CHG</sub> = 300mA                                                 | -2.0 |     | +2.0 |         |
| Fast-Charge Current Accuracy over Temperature |                       | Across all current settings, V <sub>BATT</sub> = V <sub>FAST-CHG</sub> - 300mV, T <sub>A</sub> = -40°C to +85°C                                         |                                                                               | -10  |     | +10  | %       |
| Fast-Charge Safety Timer Range                | t <sub>FC</sub>       | Programmable in 2 hour increments or disabled with CNFG_CHG_E.T_FAST_CHG[1:0], time measured from prequal. done to timer fault                          |                                                                               | 3    |     | 7    | hours   |
| Fast-Charge Safety Timer Accuracy             |                       | t <sub>FC</sub> = 3 hours                                                                                                                               |                                                                               | -10  |     | +10  | %       |
| Fast-Charge Safety Timer Suspend Threshold    |                       | Fast-charge CC mode, fast-charge safety timer paused when charge current drops below this threshold, expressed as a percentage of I <sub>FAST-CHG</sub> |                                                                               | 20   |     |      | %       |
| Junction Temperature Regulation Setting Range | T <sub>J-REG</sub>    | Programmable in 10°C steps with CNFG_CHG_D.TJ_REG[2:0]                                                                                                  |                                                                               | 60   |     | 100  | °C      |

## Electrical Characteristics—Smart Power Selector Charger (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{SYS} = 4.5V$ ,  $V_{BATT} = 4.2V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                       | SYMBOL               | CONDITIONS                                                                                                                                                                                      |                        | MIN  | TYP  | MAX  | UNITS   |
|-------------------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------|------|------|---------|
| Junction Temperature Regulation Loop Gain       | G <sub>TJ-REG</sub>  | Rate at which I <sub>FAST-CHG</sub> /I <sub>PQ</sub> is reduced to maintain T <sub>J-REG</sub> , expressed as a percentage of I <sub>FAST-CHG</sub> /I <sub>PQ</sub> per degree centigrade rise |                        |      | -5.4 |      | %/°C    |
| TERMINATION AND TOP-OFF                         |                      |                                                                                                                                                                                                 |                        |      |      |      |         |
| End-of-Charge Termination Current               | I <sub>TERM</sub>    | CNFG_CHG_C.I_TERM[1:0] = 0b00 expressed as a percentage of I <sub>FAST-CHG</sub>                                                                                                                |                        | 5    |      | %    |         |
|                                                 |                      | CNFG_CHG_C.I_TERM[1:0] = 0b01 expressed as a percentage of I <sub>FAST-CHG</sub>                                                                                                                |                        | 7.5  |      |      |         |
|                                                 |                      | CNFG_CHG_C.I_TERM[1:0] = 0b10 expressed as a percentage of I <sub>FAST-CHG</sub>                                                                                                                |                        | 8.5  | 10   |      | 11.5    |
|                                                 |                      | CNFG_CHG_C.I_TERM[1:0] = 0b11 expressed as a percentage of I <sub>FAST-CHG</sub>                                                                                                                |                        | 15   |      |      |         |
| Top-Off Timer Range                             | t <sub>TO</sub>      | I <sub>BATT</sub> < I <sub>TERM</sub> , programmable in 5 minute steps with CNFG_CHG_C.T_TOPOFF[2:0]                                                                                            |                        | 0    |      | 35   | minutes |
| Top-Off Timer Accuracy                          |                      | t <sub>TO</sub> = 10 minutes                                                                                                                                                                    |                        | -10  |      | +10  | %       |
| Charge Restart Threshold                        | V <sub>RESTART</sub> | Charging is finished (STAT_CHG_B.CHG_DTLS[3:0] indicates done)<br>Charging resumes when V <sub>BATT</sub> < V <sub>FAST-CHG</sub> - V <sub>RESTART</sub>                                        |                        | 65   | 150  |      | mV      |
| End-of-Charge Termination Current Accuracy      |                      | I <sub>FAST-CHG</sub> = 15mA, I <sub>TERM</sub> = 1.5mA (10% of I <sub>FAST-CHG</sub> ), T <sub>A</sub> = +25°C                                                                                 |                        | 1.35 | 1.5  | 1.65 | mA      |
|                                                 |                      | I <sub>FAST-CHG</sub> = 300mA, I <sub>TERM</sub> = 30mA (10% of I <sub>FAST-CHG</sub> ), T <sub>A</sub> = +25°C                                                                                 |                        | 27   | 30   | 33   |         |
| End-of-Charge Termination Current Glitch Filter |                      |                                                                                                                                                                                                 |                        |      | 60   |      | µs      |
| DEVICE ON-RESISTANCE AND LEAKAGE                |                      |                                                                                                                                                                                                 |                        |      |      |      |         |
| BATT to SYS On-Resistance                       |                      | V <sub>BATT</sub> = 3.7V, I <sub>BATT</sub> = 300mA, V <sub>CHGIN</sub> = 0V, battery is discharging to SYS                                                                                     |                        |      | 100  | 150  | mΩ      |
| Charger FET Leakage Current                     |                      | V <sub>SYS</sub> = 4.5V, V <sub>BATT</sub> = 0V, charger disabled                                                                                                                               | T <sub>A</sub> = +25°C |      | 0.1  | 1.0  | µA      |
|                                                 |                      |                                                                                                                                                                                                 | T <sub>A</sub> = +85°C |      | 1    |      |         |
| CHGIN to SYS On-Resistance                      |                      | V <sub>CHGIN</sub> = 4.65V, I <sub>CHGIN</sub> = 400mA                                                                                                                                          |                        |      | 600  |      | mΩ      |
| Input FET Leakage Current                       |                      | V <sub>CHGIN</sub> = 0V, V <sub>SYS</sub> = 4.2V, body-switched diode reverse biased                                                                                                            | T <sub>A</sub> = +25°C |      | 0.1  | 1.0  | µA      |
|                                                 |                      |                                                                                                                                                                                                 | T <sub>A</sub> = +85°C |      | 1    |      |         |
| SYSTEM NODE                                     |                      |                                                                                                                                                                                                 |                        |      |      |      |         |
| System Voltage Regulation Range                 | V <sub>SYS-REG</sub> | Programmable in 25mV steps with CNFG_CHG_D.VSYS_REG[4:0]                                                                                                                                        |                        | 4.1  |      | 4.8  | V       |

## Electrical Characteristics—Smart Power Selector Charger (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{SYS} = 4.5V$ ,  $V_{BATT} = 4.2V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                       | SYMBOL        | CONDITIONS                                                                                                                                                                                                                              | MIN                                     | TYP                | MAX  | UNITS |
|-------------------------------------------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|--------------------|------|-------|
| System Voltage Regulation Accuracy              | $V_{SYS}$     | $V_{SYS-REG} = 4.5V$ ,<br>$I_{SYS} = 1mA$                                                                                                                                                                                               | $T_A = +25^\circ C$<br>4.41             | 4.50               | 4.59 | V     |
|                                                 |               |                                                                                                                                                                                                                                         | $T_A = -40^\circ C$ to<br>$+85^\circ C$ | 4.365              | 4.5  | 4.635 |
| Minimum System Voltage Regulation Loop Setpoint | $V_{SYS-MIN}$ | $V_{CHGIN} = 5V$ , $V_{SYS-REG} = 4.5V$ , $V_{SYS} < V_{SYS-REG}$ due to $I_{CHGIN} = I_{CHGIN-LIM}$ (input in current limit), battery charging, $I_{BATT}$ reduced to 50% of $I_{FAST-CHG}$ (minimum system voltage regulation active) | 4.34                                    | 4.4                | 4.45 | V     |
| Supplement Mode System Voltage Regulation       |               | $I_{SYS} = 150mA$                                                                                                                                                                                                                       |                                         | $V_{BATT} - 0.15V$ |      | V     |

## Electrical Characteristics—Adjustable Thermistor Temperature Monitors

( $V_{CHGIN} = 5.0V$ ,  $V_{SYS} = 4.5V$ ,  $V_{BATT} = 4.2V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                | SYMBOL                | CONDITIONS                                                                                                                        | MIN   | TYP     | MAX   | UNITS      |
|------------------------------------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------|-------|---------|-------|------------|
| <b>JEITA TEMPERATURE MONITORS</b>        |                       |                                                                                                                                   |       |         |       |            |
| TBIAS Voltage                            | $V_{TBIAS}$           | CNFG_CHG_F.THM_EN = 1, $V_{CHGIN} = 5V$                                                                                           |       | 1.25    |       | V          |
| JEITA Cold Threshold Range               | $V_{COLD}$            | Voltage rising threshold, programmable with CNFG_CHG_A.THM_COLD[1:0] in $5^\circ C$ increments when using an NTC $\beta = 3380K$  | 0.867 |         | 1.024 | V          |
| JEITA Cool Threshold Range               | $V_{COOL}$            | Voltage rising threshold, programmable with CNFG_CHG_A.THM_COOL[1:0] in $5^\circ C$ increments when using an NTC $\beta = 3380K$  | 0.747 |         | 0.923 | V          |
| JEITA Warm Threshold Range               | $V_{WARM}$            | Voltage falling threshold, programmable with CNFG_CHG_A.THM_WARM[1:0] in $5^\circ C$ increments when using an NTC $\beta = 3380K$ | 0.367 |         | 0.511 | V          |
| JEITA Hot Threshold Range                | $V_{HOT}$             | Voltage falling threshold, programmable with CNFG_CHG_A.THM_HOT[1:0] in $5^\circ C$ increments when using an NTC $\beta = 3380K$  | 0.291 |         | 0.411 | V          |
| Temperature Threshold Accuracy           |                       | Voltage threshold accuracy expressed as temperature for an NTC $\beta = 3380K$                                                    |       | $\pm 3$ |       | $^\circ C$ |
| Temperature Threshold Hysteresis         |                       | Temperature hysteresis set on each voltage threshold for an NTC $\beta = 3380K$                                                   |       | 3       |       | $^\circ C$ |
| JEITA Modified Fast-Charge Voltage Range | $V_{FAST-CHG\_JEITA}$ | $I_{BATT} = 0mA$ , programmable in 25mV steps, battery is either cool or warm                                                     | 3.6   |         | 4.6   | V          |
| JEITA Modified Fast-Charge Current Range | $I_{FAST-CHG\_JEITA}$ | Programmable in 7.5mA steps, battery is either cool or warm                                                                       | 7.5   |         | 300   | mA         |



## Electrical Characteristics—Analog Multiplexer

( $V_{CHGIN} = 5.0V$ ,  $V_{SYS} = 4.5V$ ,  $V_{BATT} = 4.2V$ , limits are 100% production tested at  $T_A = +25^{\circ}C$ , limits over the operating temperature range ( $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                          | SYMBOL                    | CONDITIONS                                                                                               |                        | MIN   | TYP  | MAX | UNITS |
|----------------------------------------------------|---------------------------|----------------------------------------------------------------------------------------------------------|------------------------|-------|------|-----|-------|
| ANALOG MULTIPLEXER                                 |                           |                                                                                                          |                        |       |      |     |       |
| Full-Scale Voltage                                 | V <sub>FS</sub>           |                                                                                                          |                        | 1.25  |      |     | V     |
| Channel Switching Time                             |                           |                                                                                                          |                        | 0.3   |      |     | μs    |
| Off Leakage Current                                |                           | V <sub>AMUX</sub> = 0V,<br>AMUX is high impedance                                                        | T <sub>A</sub> = +25°C | 1     | 500  |     | nA    |
|                                                    |                           |                                                                                                          | T <sub>A</sub> = +85°C | 1     |      |     | μA    |
| CHGIN POWER MEASUREMENT                            |                           |                                                                                                          |                        |       |      |     |       |
| CHGIN Current Monitor Gain                         | G <sub>ICHGIN</sub>       | V <sub>FS</sub> corresponds to maximum I <sub>CHGIN-LIM</sub> setting                                    |                        | 2.632 |      |     | V/A   |
| CHGIN Voltage Monitor Gain                         | G <sub>VCHGIN</sub>       | V <sub>FS</sub> corresponds to V <sub>CHGIN_OVP</sub>                                                    |                        | 0.167 |      |     | V/V   |
| BATT AND SYS POWER MEASUREMENT                     |                           |                                                                                                          |                        |       |      |     |       |
| Battery Charge Current Monitor Gain                | G <sub>IBATT-CHG</sub>    | V <sub>FS</sub> corresponds to 100% of I <sub>FAST-CHG</sub> setting (CNFG_CHG_E.CHG_CC[5:0])            |                        | 12.5  |      |     | mV/%  |
| Charge Current Monitor Accuracy                    |                           | I <sub>FAST-CHG</sub> = 15mA, T <sub>A</sub> = +25°C, V <sub>BATT</sub> = V <sub>FAST-CHG</sub> - 300mV  |                        | -3.5  | +3.5 |     | %     |
|                                                    |                           | I <sub>FAST-CHG</sub> = 300mA, T <sub>A</sub> = +25°C, V <sub>BATT</sub> = V <sub>FAST-CHG</sub> - 300mV |                        | -3.5  | +3.5 |     |       |
| Charge Current Monitor Accuracy over Temperature   |                           | Across all current settings, V <sub>BATT</sub> = V <sub>FAST-CHG</sub> - 300mV                           |                        | -10   | +10  |     | %     |
| Battery Discharge Monitor Full-Scale Current Range | I <sub>DISCHG-SCALE</sub> | Programmable with CNFG_CHG_I.IMON_DISCHG_SCALE[3:0]                                                      |                        | 8.2   | 300  |     | mA    |
| Battery Discharge Current Monitor Accuracy         |                           | 15mA to 300mA battery discharge current, I <sub>DISCHG-SCALE</sub> = 300mA                               |                        | -15   | +15  |     | %     |
| Battery Discharge Current Monitor Offset           |                           | I <sub>BATT</sub> = 0mA                                                                                  |                        | -0.5  | +0.8 |     | mA    |
| Battery-Voltage Monitor Gain                       | G <sub>VBATT</sub>        | V <sub>FS</sub> corresponds to maximum V <sub>FAST-CHG</sub> setting                                     |                        | 0.272 |      |     | V/V   |
| SYS Voltage Monitor Gain                           | G <sub>VSYS</sub>         | V <sub>FS</sub> corresponds to maximum V <sub>SYS-REG</sub> setting                                      |                        | 0.26  |      |     | V/V   |
| THM AND TBIAS VOLTAGE MEASUREMENT                  |                           |                                                                                                          |                        |       |      |     |       |
| THM Voltage Monitor Gain                           | G <sub>VTHM</sub>         |                                                                                                          |                        | 1     |      |     | V/V   |
| TBIAS Voltage Monitor Gain                         | G <sub>VTBIAS</sub>       |                                                                                                          |                        | 1     |      |     | V/V   |

## Electrical Characteristics—SIMO Buck-Boost

( $V_{SYS} = 3.7V$ ,  $V_{IN\_SBB} = 3.7V$ ,  $C_{SBBx} = 10\mu F$ ,  $L = 1.5\mu H$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                             | SYMBOL              | CONDITIONS                                                                                                             |                                 | MIN   | TYP   | MAX   | UNITS |
|-------------------------------------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------|---------------------------------|-------|-------|-------|-------|
| GENERAL CHARACTERISTICS / OUTPUT VOLTAGE RANGE (SBB0) |                     |                                                                                                                        |                                 |       |       |       |       |
| Programmable Output Voltage Range                     |                     |                                                                                                                        |                                 | 0.8   |       | 5.5   | V     |
| Output DAC Bits                                       |                     |                                                                                                                        |                                 |       | 7     |       | bits  |
| Output DAC LSB Size                                   |                     |                                                                                                                        |                                 |       | 50    |       | mV    |
| GENERAL CHARACTERISTICS / OUTPUT VOLTAGE RANGE (SBB1) |                     |                                                                                                                        |                                 |       |       |       |       |
| Programmable Output Voltage Range                     |                     |                                                                                                                        |                                 | 0.8   |       | 5.5   | V     |
| Output DAC Bits                                       |                     |                                                                                                                        |                                 |       | 7     |       | bits  |
| Output DAC LSB Size                                   |                     |                                                                                                                        |                                 |       | 50    |       | mV    |
| GENERAL CHARACTERISTICS / OUTPUT VOLTAGE RANGE (SBB2) |                     |                                                                                                                        |                                 |       |       |       |       |
| Programmable Output Voltage Range                     |                     |                                                                                                                        |                                 | 0.8   |       | 5.5   | V     |
| Output DAC Bits                                       |                     |                                                                                                                        |                                 |       | 7     |       | bits  |
| Output DAC LSB Size                                   |                     |                                                                                                                        |                                 |       | 50    |       | mV    |
| OUTPUT VOLTAGE ACCURACY                               |                     |                                                                                                                        |                                 |       |       |       |       |
| Output Voltage Accuracy                               |                     | V <sub>SBBx</sub> falling, threshold where LXA switches high; specified as a percentage of target output voltage       | T <sub>A</sub> = +25°C          | -3.0  |       | +3.0  | %     |
|                                                       |                     |                                                                                                                        | T <sub>A</sub> = -40°C to +85°C | -4.55 |       | +4.55 |       |
| TIMING CHARACTERISTICS                                |                     |                                                                                                                        |                                 |       |       |       |       |
| Enable Delay                                          |                     | Delay time from the SIMO receiving its first enable signal to when it begins to switch in order to service that output |                                 |       | 60    |       | μs    |
| Soft-Start Slew Rate                                  | dV/dt <sub>SS</sub> |                                                                                                                        |                                 | 3.3   | 5.0   | 6.6   | mV/μs |
| POWER STAGE CHARACTERISTICS                           |                     |                                                                                                                        |                                 |       |       |       |       |
| LXA Leakage Current                                   |                     | SBB0, SBB1, SBB2 are disabled, V <sub>IN_SBB</sub> = 5.5V, V <sub>LXA</sub> = 0V, or 5.5V                              | T <sub>A</sub> = +25°C          | -1.0  | ±0.1  | +1.0  | μA    |
|                                                       |                     |                                                                                                                        | T <sub>A</sub> = +85°C          |       | ±1.0  |       |       |
| LXB Leakage Current                                   |                     | SBB0, SBB1, SBB2 are disabled, V <sub>IN_SBB</sub> = 5.5V, V <sub>LXA</sub> = 0V or 5.5V, all V <sub>SBBx</sub> = 5.5V | T <sub>A</sub> = +25°C          | -1.0  | ±0.1  | +1.0  | μA    |
|                                                       |                     |                                                                                                                        | T <sub>A</sub> = +85°C          |       | ±1.0  |       |       |
| BST Leakage Current                                   |                     | V <sub>IN_SBB</sub> = 5.5V, V <sub>LXB</sub> = 5.5V, V <sub>BST</sub> = 11V,                                           | T <sub>A</sub> = +25°C          |       | +0.01 | +1.0  | μA    |
|                                                       |                     |                                                                                                                        | T <sub>A</sub> = +85°C          |       | +0.1  |       |       |

## Electrical Characteristics—SIMO Buck-Boost (continued)

( $V_{SYS} = 3.7V$ ,  $V_{IN\_SBB} = 3.7V$ ,  $C_{SBBx} = 10\mu F$ ,  $L = 1.5\mu H$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                       | SYMBOL                | CONDITIONS                                                                                                                                                    | MIN                 | TYP   | MAX  | UNITS    |
|---------------------------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-------|------|----------|
| Disabled Output Leakage Current |                       | SBB0, SBB1, SBB2 are disabled, active-discharge disabled ( $ADE\_SBBx = 0$ ), $V_{SBBx} = 5.5V$ , $V_{LXB} = 0V$ , $V_{SYS} = V_{IN\_SBB} = V_{BST} = 5.5V$ , | $T_A = +25^\circ C$ | +0.1  | +1.0 | $\mu A$  |
|                                 |                       |                                                                                                                                                               | $T_A = +85^\circ C$ | +0.2  |      |          |
| Active Discharge Resistance     | $R_{AD\_SBBx}$        | SBB0, SBB1, SBB2 are disabled, active discharge enabled ( $CNFG\_SBBx\_B.ADE\_SBBx = 1$ )                                                                     | 80                  | 140   | 260  | $\Omega$ |
| <b>CONTROL SCHEME</b>           |                       |                                                                                                                                                               |                     |       |      |          |
| Peak Current Limit              | $I_{P\_SBB}$ (Note 6) | $CNFG\_SBBx\_B.IP\_SBBx[1:0] = 0b11$                                                                                                                          | -18%                | 0.335 | +18% | A        |
|                                 |                       | $CNFG\_SBBx\_B.IP\_SBBx[1:0] = 0b10$                                                                                                                          | -14%                | 0.500 | +14% |          |
|                                 |                       | $CNFG\_SBBx\_B.IP\_SBBx[1:0] = 0b01$                                                                                                                          | -8%                 | 0.750 | +8%  |          |
|                                 |                       | $CNFG\_SBBx\_B.IP\_SBBx[1:0] = 0b00$                                                                                                                          | -7%                 | 1.000 | +7%  |          |

**Note 6:** Typical values align with bench observations using the stated conditions with an inductor. Minimum and maximum values are tested in production with DC currents without an inductor. See the *Typical Operating Characteristics* SIMO switching waveforms to gain more insight on this specification.

## Electrical Characteristics—Low Dropout Linear Regulator (LDO)/Load Switch (LSW)

( $V_{SYS} = 3.7V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                           | SYMBOL              | CONDITIONS                                                               | MIN  | TYP | MAX   | UNITS   |
|-------------------------------------|---------------------|--------------------------------------------------------------------------|------|-----|-------|---------|
| <b>LDO0/1</b>                       |                     |                                                                          |      |     |       |         |
| Input Voltage Range                 | $V_{IN\_LDOx}$      | LDO mode                                                                 | 1.71 |     | 5.5   | V       |
|                                     |                     | Switch mode                                                              | 1.3  |     | 5.5   |         |
| Quiescent Supply Current            | $I_{IN\_LDOx}$      | $I_{OUT\_LDOx} = 0$                                                      |      | 1.4 | 2.1   | $\mu A$ |
|                                     |                     | $I_{OUT\_LDOx} = 0$ , switch mode                                        |      | 0.5 | 1     |         |
| Quiescent Supply Current In Dropout | $I_{IN\_DRP\_LDOx}$ | $I_{OUT\_LDOx} = 0$ , $V_{IN\_LDOx} = 2.9V$ , $V_{LDOx} = 3V$            |      | 2.1 | 4.6   | $\mu A$ |
| Maximum Output Current              | $I_{OUT\_LDOx}$     | $V_{IN\_LDOx} > 1.8V$                                                    | 100  |     |       | mA      |
|                                     |                     | $V_{IN\_LDOx} = 1.8V$ or lower                                           | 50   |     |       |         |
| Output Voltage                      | $V_{OUT\_LDOx}$     |                                                                          | 0.8  |     | 3.975 | V       |
| Output Accuracy                     |                     | $V_{IN\_LDOx} = (V_{OUT\_LDOx} + 0.5V)$ or higher, $I_{OUT\_LDOx} = 1mA$ | -3.1 |     | +3.1  | %       |
| Dropout Voltage                     | $V_{DRP\_LDOx}$     | $V_{IN\_LDOx} = 3V$ , LDOx programmed to 3V, $I_{OUT\_LDOx} = 100mA$     |      |     | 100   | mV      |
| Line Regulation                     |                     | $V_{IN\_LDOx} = (V_{OUT\_LDOx} + 0.5V)$ to 5.5V                          | -0.5 |     | +0.5  | %/V     |

## Electrical Characteristics—Low Dropout Linear Regulator (LDO)/Load Switch (LSW) (continued)

( $V_{SYS} = 3.7V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                   | SYMBOL         | CONDITIONS                                                                        | MIN | TYP      | MAX   | UNITS         |
|-----------------------------|----------------|-----------------------------------------------------------------------------------|-----|----------|-------|---------------|
| Load Regulation             |                | $V_{IN\_LDOx} = 1.8V$ or higher, $I_{OUT\_LDOx} = 100\mu A$ to $100mA$            |     | 0.001    | 0.005 | %/mA          |
| Line Transient              |                | $V_{IN\_LDOx} = 4V$ to $5V$ , 200ns rise time                                     |     | $\pm 35$ |       | mV            |
|                             |                | $V_{IN\_LDOx} = 4V$ to $5V$ , 1 $\mu s$ rise time                                 |     | $\pm 25$ |       |               |
| Load Transient              |                | $I_{OUT\_LDOx} = 100\mu A$ to $10mA$ , 200ns rise time                            |     | 100      |       | mV            |
|                             |                | $I_{OUT\_LDOx} = 100\mu A$ to $100mA$ , 200ns rise time                           |     | 200      |       |               |
| Active Discharge Resistance | $R_{AD\_LDOx}$ |                                                                                   | 42  | 80       | 200   | $\Omega$      |
| Switch Mode On-Resistance   | $R_{ON\_LDOx}$ | $V_{IN\_LDOx} = 2.7V$ , $I_{OUT\_LDOx} = 100mA$                                   |     |          | 0.8   | $\Omega$      |
|                             |                | $V_{IN\_LDOx} = 1.8V$ , $I_{OUT\_LDOx} = 50mA$                                    |     |          | 1     |               |
|                             |                | $V_{IN\_LDOx} = 1.3V$ , $I_{OUT\_LDOx} = 5mA$                                     |     |          | 3     |               |
| Slew Rate                   |                | $I_{OUT\_LDOx} = 0mA$ , time from 10% to 90% of final register value              |     | 1.4      |       | V/ms          |
|                             |                | $I_{OUT\_LDOx} = 0mA$ , time from 10% to 90% of final register value, switch mode |     | 1.4      |       |               |
| Short Circuit Current Limit |                | $V_{IN\_LDOx} = 2.7V$ , $V_{OUT\_LDOx} = GND$                                     | 170 | 380      | 620   | mA            |
|                             |                | $V_{IN\_LDOx} = 2.7V$ , $V_{OUT\_LDOx} = 2.55V$ , switch mode                     | 170 | 370      |       |               |
| Output Noise                |                | 10Hz to 100kHz, $V_{IN\_LDOx} = 5V$ , $V_{OUT\_LDOx} = 3.3V$                      |     | 150      |       | $\mu V_{RMS}$ |
|                             |                | 10Hz to 100kHz, $V_{IN\_LDOx} = 5V$ , $V_{OUT\_LDOx} = 2.5V$                      |     | 125      |       |               |
|                             |                | 10Hz to 100kHz, $V_{IN\_LDOx} = 5V$ , $V_{OUT\_LDOx} = 1.2V$                      |     | 90       |       |               |
|                             |                | 10Hz to 100kHz, $V_{IN\_LDOx} = 5V$ , $V_{OUT\_LDOx} = 0.9V$                      |     | 80       |       |               |
| Output DAC Bits             |                |                                                                                   |     | 7        |       | bits          |
| Output DAC LSB Size         |                |                                                                                   |     | 25       |       | mV            |

## Electrical Characteristics—I<sup>2</sup>C Serial Communication

( $V_{SYS} = 3.7V$ ,  $V_{IO} = 1.8V$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER              | SYMBOL   | CONDITIONS                                                                 | MIN | TYP | MAX | UNITS   |
|------------------------|----------|----------------------------------------------------------------------------|-----|-----|-----|---------|
| <b>POWER SUPPLY</b>    |          |                                                                            |     |     |     |         |
| $V_{IO}$ Voltage Range | $V_{IO}$ |                                                                            | 1.7 | 1.8 | 3.6 | V       |
| $V_{IO}$ Bias Current  |          | $V_{IO} = 3.6V$ , $V_{SDA} = V_{SCL} = 0V$ or $3.6V$ , $T_A = +25^\circ C$ | -1  | 0   | +1  | $\mu A$ |
|                        |          | $V_{IO} = 1.7V$ , $V_{SDA} = V_{SCL} = 0V$ or $1.7V$                       | -1  | 0   | +1  |         |

**Electrical Characteristics—I<sup>2</sup>C Serial Communication (continued)**

(V<sub>SYS</sub> = 3.7V, V<sub>IO</sub> = 1.8V, limits are 100% production tested at T<sub>A</sub> = +25°C, limits over the operating temperature range (T<sub>A</sub> = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                                                                                         | SYMBOL                                     | CONDITIONS                                                                | MIN                    | TYP | MAX  | UNITS |
|-------------------------------------------------------------------------------------------------------------------|--------------------------------------------|---------------------------------------------------------------------------|------------------------|-----|------|-------|
| SDA AND SCL I/O STAGE                                                                                             |                                            |                                                                           |                        |     |      |       |
| SCL, SDA Input High Voltage                                                                                       | V <sub>IH</sub>                            | V <sub>IO</sub> = 1.7V to 3.6V                                            | 0.7 x V <sub>IO</sub>  |     |      | V     |
| SCL, SDA Input Low Voltage                                                                                        | V <sub>IL</sub>                            | V <sub>IO</sub> = 1.7V to 3.6V                                            | 0.3 x V <sub>IO</sub>  |     |      | V     |
| SCL, SDA Input Hysteresis                                                                                         | V <sub>HYS</sub>                           |                                                                           | 0.05 x V <sub>IO</sub> |     |      | V     |
| SCL, SDA Input Leakage Current                                                                                    | I <sub>I</sub>                             | V <sub>IO</sub> = 3.6V, V <sub>SCL</sub> = V <sub>SDA</sub> = 0V and 3.6V | -10                    |     | +10  | μA    |
| SDA Output Low Voltage                                                                                            | V <sub>OL</sub>                            | Sinking 20mA                                                              | 0.4                    |     |      | V     |
| SCL, SDA Pin Capacitance                                                                                          | C <sub>I</sub>                             |                                                                           | 10                     |     |      | pF    |
| Output Fall Time from V <sub>IH</sub> to V <sub>IL</sub>                                                          | t <sub>OF</sub> ( <a href="#">Note 7</a> ) |                                                                           | 120                    |     |      | ns    |
| I <sup>2</sup> C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST-MODE PLUS) ( <a href="#">Note 7</a> )      |                                            |                                                                           |                        |     |      |       |
| Clock Frequency                                                                                                   | f <sub>SCL</sub>                           |                                                                           | 0                      |     | 1000 | kHz   |
| Hold Time REPEATED START Condition                                                                                | t <sub>HD_STA</sub>                        |                                                                           | 0.26                   |     |      | μs    |
| SCL Low Period                                                                                                    | t <sub>LOW</sub>                           |                                                                           | 0.5                    |     |      | μs    |
| SCL High Period                                                                                                   | t <sub>HIGH</sub>                          |                                                                           | 0.26                   |     |      | μs    |
| Setup Time REPEATED START Condition                                                                               | t <sub>SU_STA</sub>                        |                                                                           | 0.26                   |     |      | μs    |
| Data Hold Time                                                                                                    | t <sub>HD_DAT</sub>                        |                                                                           | 0                      |     |      | μs    |
| Data Setup Time                                                                                                   | t <sub>SU_DAT</sub>                        |                                                                           | 50                     |     |      | ns    |
| Setup Time for STOP Condition                                                                                     | t <sub>SU_STO</sub>                        |                                                                           | 0.26                   |     |      | μs    |
| Bus Free Time between STOP and START Condition                                                                    | t <sub>BUF</sub>                           |                                                                           | 0.5                    |     |      | μs    |
| Pulse Width of Suppressed Spikes                                                                                  | t <sub>SP</sub>                            | Maximum pulse width of spikes that must be suppressed by the input filter | 50                     |     |      | ns    |
| I <sup>2</sup> C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C <sub>B</sub> = 100pF) ( <a href="#">Note 7</a> ) |                                            |                                                                           |                        |     |      |       |
| Clock Frequency                                                                                                   | f <sub>SCL</sub>                           |                                                                           | 3.4                    |     |      | MHz   |
| Setup Time REPEATED START Condition                                                                               | t <sub>SU_STA</sub>                        |                                                                           | 160                    |     |      | ns    |
| Hold Time REPEATED START Condition                                                                                | t <sub>HD_STA</sub>                        |                                                                           | 160                    |     |      | ns    |
| SCL Low Period                                                                                                    | t <sub>LOW</sub>                           |                                                                           | 160                    |     |      | ns    |
| SCL High Period                                                                                                   | t <sub>HIGH</sub>                          |                                                                           | 60                     |     |      | ns    |
| Data Setup Time                                                                                                   | t <sub>SU_DAT</sub>                        |                                                                           | 10                     |     |      | ns    |

**Electrical Characteristics—I<sup>2</sup>C Serial Communication (continued)**

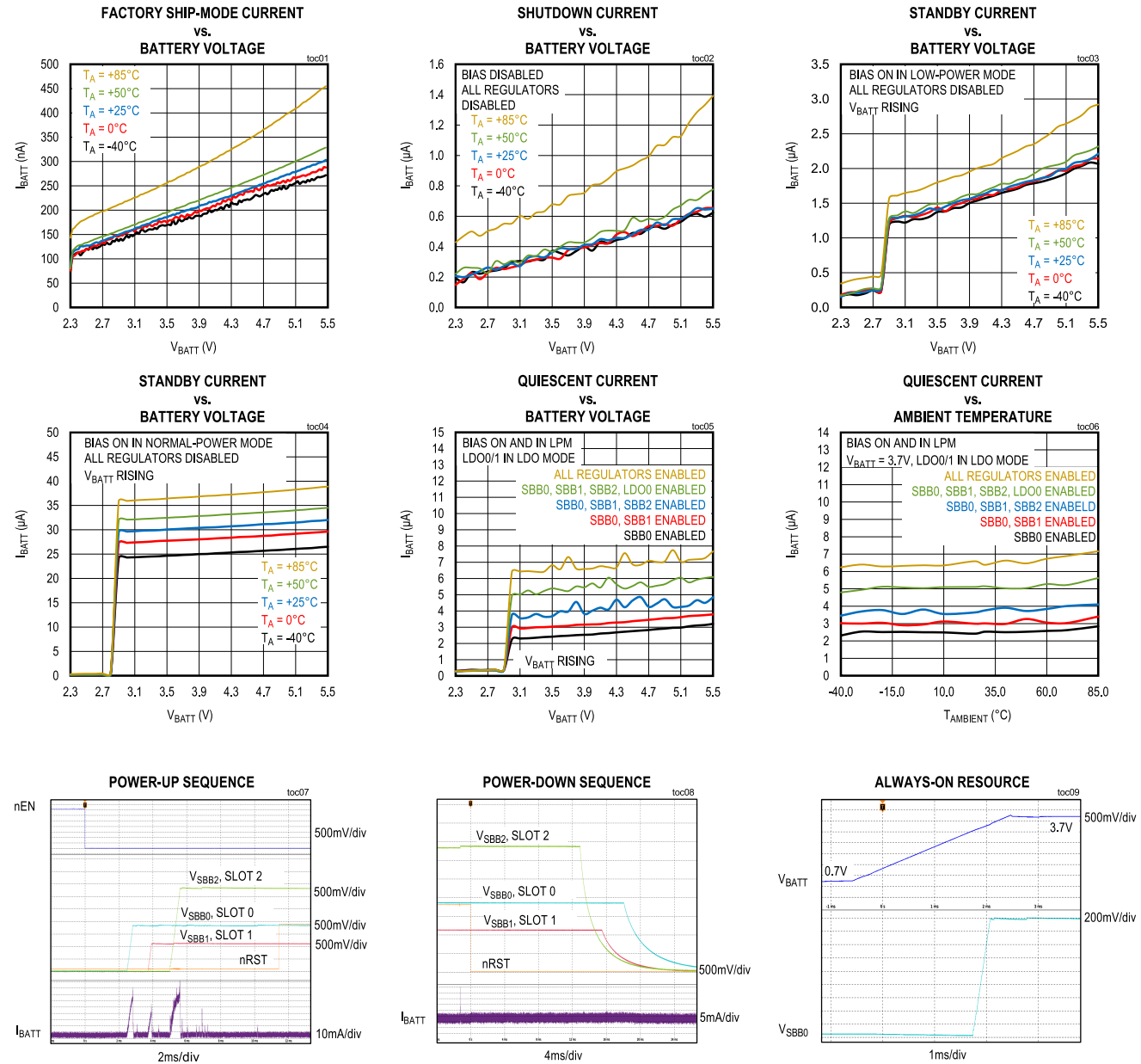
(V<sub>SYS</sub> = 3.7V, V<sub>IO</sub> = 1.8V, limits are 100% production tested at T<sub>A</sub> = +25°C, limits over the operating temperature range (T<sub>A</sub> = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER                                                                                           | SYMBOL              | CONDITIONS                                                                | MIN | TYP | MAX | UNITS |
|-----------------------------------------------------------------------------------------------------|---------------------|---------------------------------------------------------------------------|-----|-----|-----|-------|
| Data Hold Time                                                                                      | t <sub>HD_DAT</sub> |                                                                           | 0   |     | 70  | ns    |
| SCL Rise Time                                                                                       | t <sub>rCL</sub>    | T <sub>A</sub> = +25°C                                                    | 10  |     | 40  | ns    |
| Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit                    | t <sub>rCL1</sub>   | T <sub>A</sub> = +25°C                                                    | 10  |     | 80  | ns    |
| SCL Fall Time                                                                                       | t <sub>fCL</sub>    | T <sub>A</sub> = +25°C                                                    | 10  |     | 40  | ns    |
| SDA Rise Time                                                                                       | t <sub>rDA</sub>    | T <sub>A</sub> = +25°C                                                    | 10  |     | 80  | ns    |
| SDA Fall Time                                                                                       | t <sub>fDA</sub>    | T <sub>A</sub> = +25°C                                                    | 10  |     | 80  | ns    |
| Setup Time for STOP Condition                                                                       | t <sub>SU_STO</sub> |                                                                           | 160 |     |     | ns    |
| Bus Capacitance                                                                                     | C <sub>B</sub>      |                                                                           |     |     | 100 | pF    |
| Pulse Width of Suppressed Spikes                                                                    | t <sub>SP</sub>     | Maximum pulse width of spikes that must be suppressed by the input filter |     | 10  |     | ns    |
| <b>I<sup>2</sup>C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C<sub>B</sub> = 400pF) (Note 7)</b> |                     |                                                                           |     |     |     |       |
| Clock Frequency                                                                                     | f <sub>SCL</sub>    |                                                                           |     |     | 1.7 | MHz   |
| Setup Time REPEATED START Condition                                                                 | t <sub>SU_STA</sub> |                                                                           | 160 |     |     | ns    |
| Hold Time REPEATED START Condition                                                                  | t <sub>HD_STA</sub> |                                                                           | 160 |     |     | ns    |
| SCL Low Period                                                                                      | t <sub>LOW</sub>    |                                                                           | 320 |     |     | ns    |
| SCL High Period                                                                                     | t <sub>HIGH</sub>   |                                                                           | 120 |     |     | ns    |
| Data Setup Time                                                                                     | t <sub>SU_DAT</sub> |                                                                           | 10  |     |     | ns    |
| Data Hold Time                                                                                      | t <sub>HD_DAT</sub> |                                                                           | 0   |     | 150 | ns    |
| SCL Rise Time                                                                                       | t <sub>rCL</sub>    | T <sub>A</sub> = +25°C                                                    | 20  |     | 80  | ns    |
| Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit                    | t <sub>rCL1</sub>   | T <sub>A</sub> = +25°C                                                    | 20  |     | 80  | ns    |
| SCL Fall Time                                                                                       | t <sub>fCL</sub>    | T <sub>A</sub> = +25°C                                                    | 20  |     | 80  | ns    |
| SDA Rise Time                                                                                       | t <sub>rDA</sub>    | T <sub>A</sub> = +25°C                                                    | 20  |     | 160 | ns    |
| SDA Fall Time                                                                                       | t <sub>fDA</sub>    | T <sub>A</sub> = +25°C                                                    | 20  |     | 160 | ns    |
| Setup Time for STOP Condition                                                                       | t <sub>SU_STO</sub> |                                                                           | 160 |     |     | ns    |
| Bus Capacitance                                                                                     | C <sub>B</sub>      |                                                                           |     |     | 400 | pF    |
| Pulse Width of Suppressed Spikes                                                                    | t <sub>SP</sub>     | Maximum pulse width of spikes that must be suppressed by the input filter |     | 10  |     | ns    |

**Note 7:** Design guidance only. Not production tested.

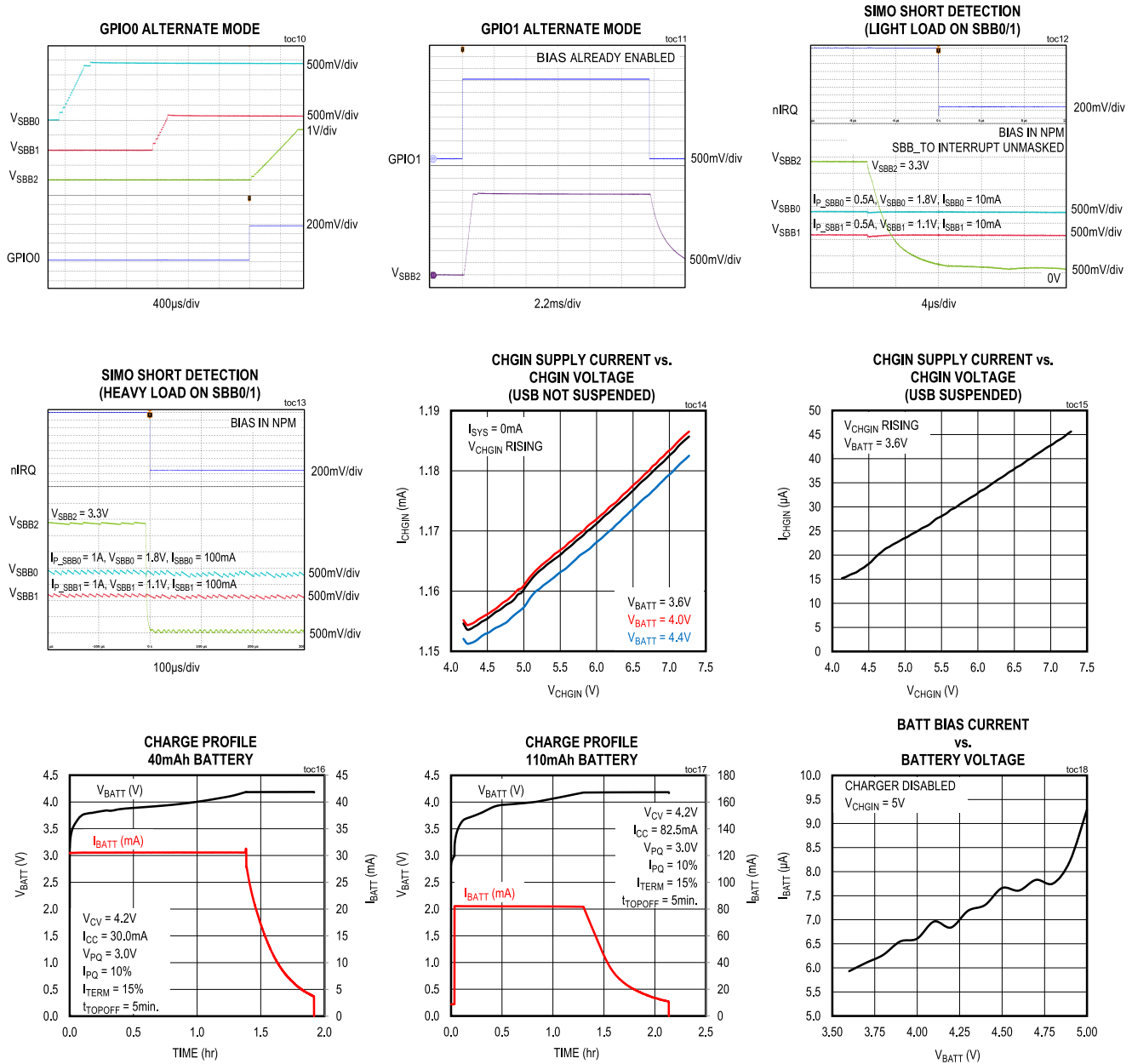
## Typical Operating Characteristics

(Typical Applications Circuit.  $V_{CHGIN} = 0V$ ,  $V_{SYS} = V_{IN\_SBB} = V_{BATT} = 3.7V$ ,  $V_{IO} = 1.8V$ ,  $T_A = +25^\circ C$ ,  $V_{SBB0} = 1.8V$ ,  $I_{P\_SBB0} = 0.5A$ , SBB0 in Buck mode,  $V_{SBB1} = 1.1V$ ,  $I_{P\_SBB1} = 0.5A$ , SBB1 in Buck mode,  $V_{SBB2} = 3.3V$ ,  $I_{P\_SBB2} = 1A$  peak, SBB2 in Buck-Boost mode, unless otherwise noted. Inductor = DFE201612E-2R2M,  $2.2\mu H$ ,  $116m\Omega$ .)



## Typical Operating Characteristics (continued)

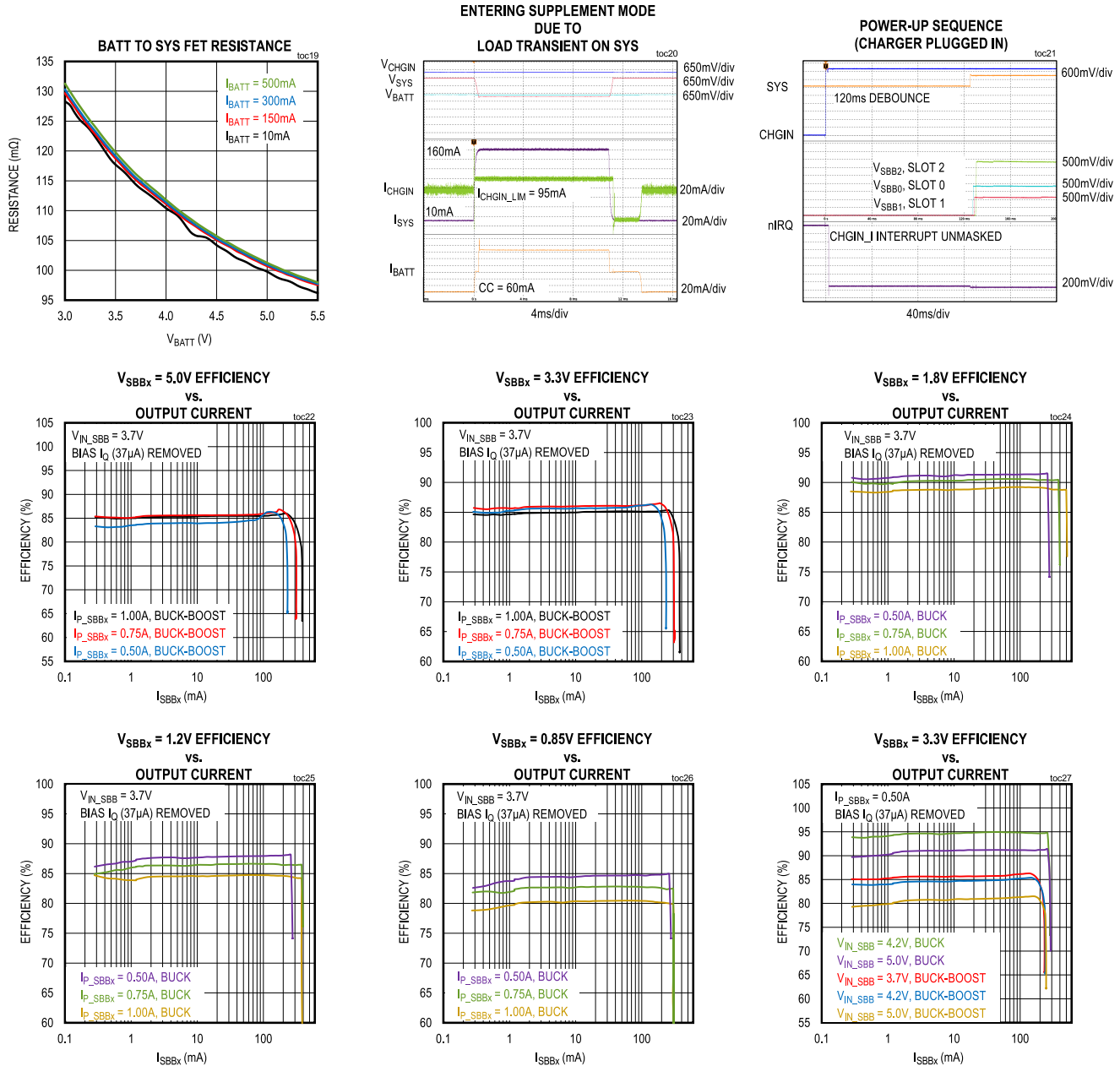
(Typical Applications Circuit.  $V_{CHGIN} = 0V$ ,  $V_{SYS} = V_{IN\_SBB} = V_{BATT} = 3.7V$ ,  $V_{IO} = 1.8V$ ,  $T_A = +25^\circ C$ ,  $V_{SBB0} = 1.8V$ ,  $I_{P\_SBB0} = 0.5A$ , SBB0 in Buck mode,  $V_{SBB1} = 1.1V$ ,  $I_{P\_SBB1} = 0.5A$ , SBB1 in Buck mode,  $V_{SBB2} = 3.3V$ ,  $I_{P\_SBB2} = 1A$  peak, SBB2 in Buck-Boost mode, unless otherwise noted. Inductor = DFE201612E-2R2M, 2.2 $\mu H$ , 116m $\Omega$ .)





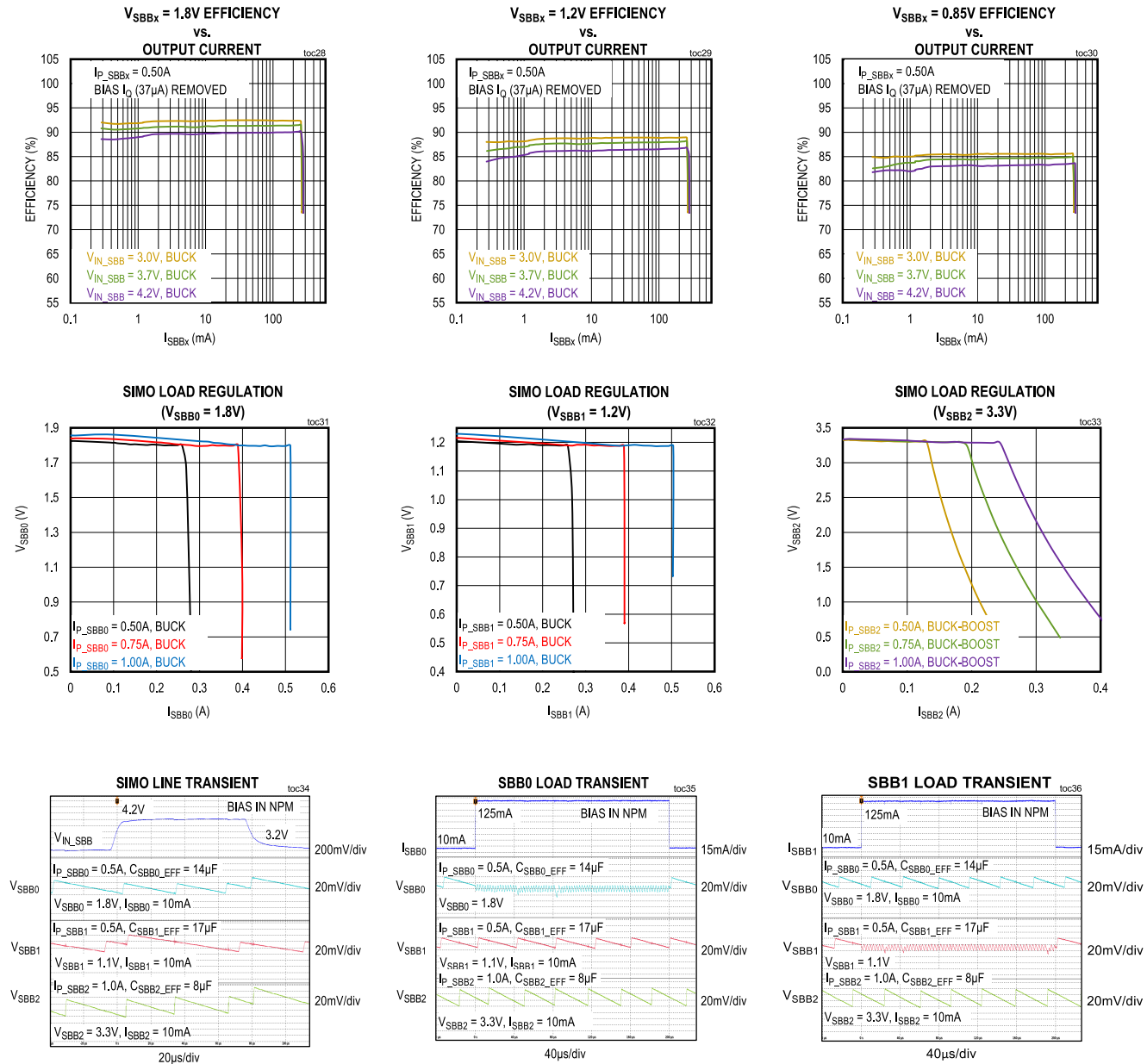
## Typical Operating Characteristics (continued)

(Typical Applications Circuit.  $V_{CHGIN} = 0V$ ,  $V_{SYS} = V_{IN\_SBB} = V_{BATT} = 3.7V$ ,  $V_{IO} = 1.8V$ ,  $T_A = +25^\circ C$ ,  $V_{SBB0} = 1.8V$ ,  $I_{P\_SBB0} = 0.5A$ , SBB0 in Buck mode,  $V_{SBB1} = 1.1V$ ,  $I_{P\_SBB1} = 0.5A$ , SBB1 in Buck mode,  $V_{SBB2} = 3.3V$ ,  $I_{P\_SBB2} = 1A$  peak, SBB2 in Buck-Boost mode, unless otherwise noted. Inductor = DFE201612E-2R2M, 2.2 $\mu H$ , 116m $\Omega$ .)



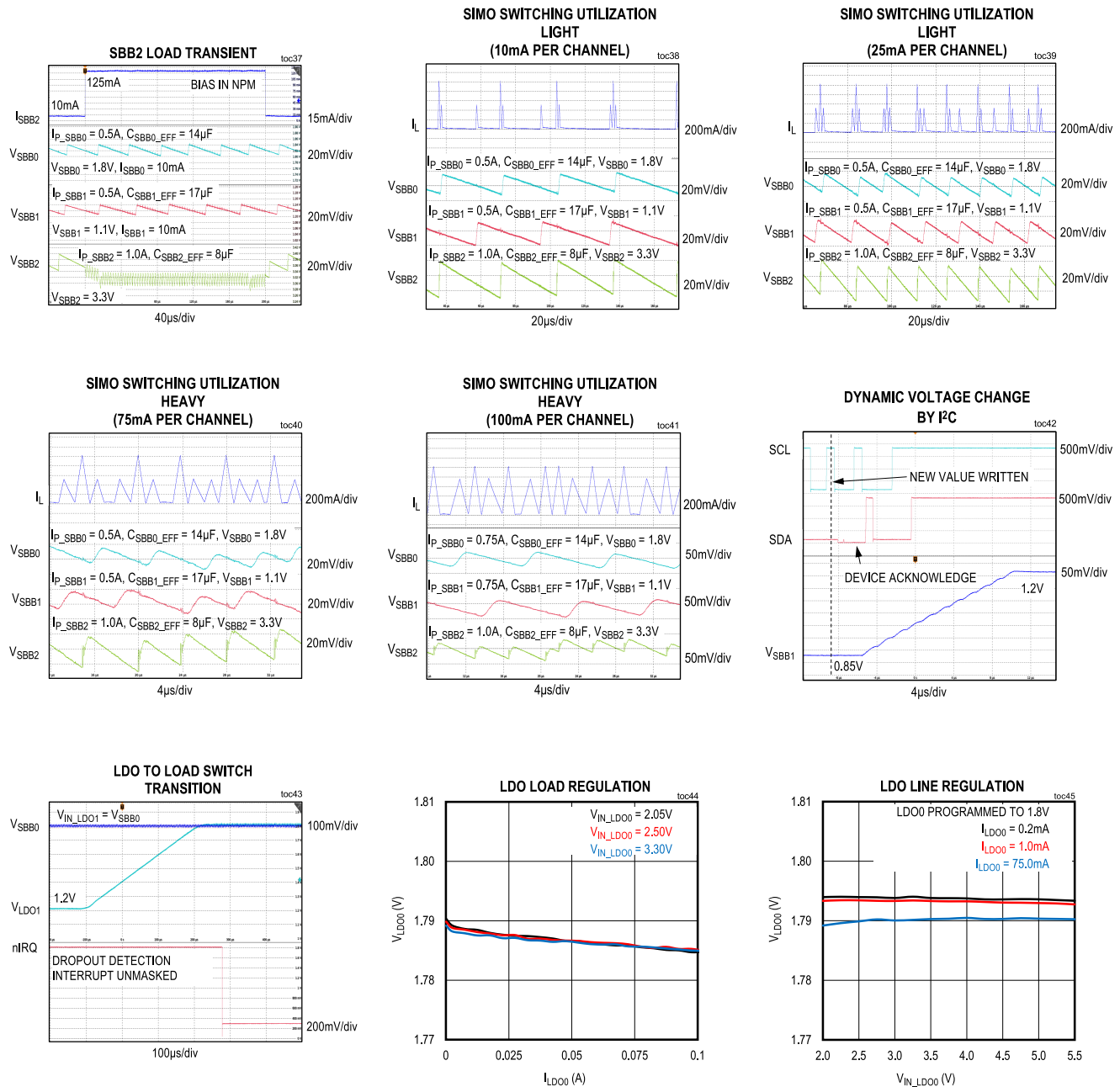
## Typical Operating Characteristics (continued)

(Typical Applications Circuit.  $V_{CHGIN} = 0V$ ,  $V_{SYS} = V_{IN\_SBB} = V_{BATT} = 3.7V$ ,  $V_{IO} = 1.8V$ ,  $T_A = +25^\circ C$ ,  $V_{SBB0} = 1.8V$ ,  $I_{P\_SBB0} = 0.5A$ , SBB0 in Buck mode,  $V_{SBB1} = 1.1V$ ,  $I_{P\_SBB1} = 0.5A$ , SBB1 in Buck mode,  $V_{SBB2} = 3.3V$ ,  $I_{P\_SBB2} = 1A$  peak, SBB2 in Buck-Boost mode, unless otherwise noted. Inductor = DFE201612E-2R2M,  $2.2\mu H$ ,  $116m\Omega$ .)



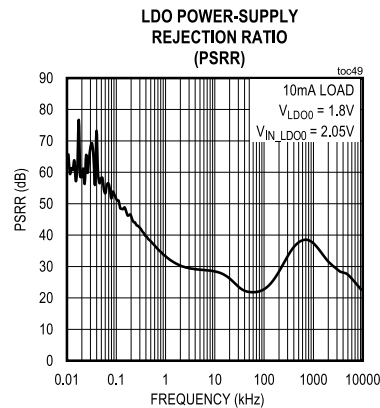
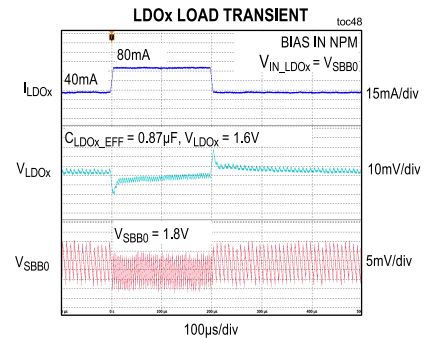
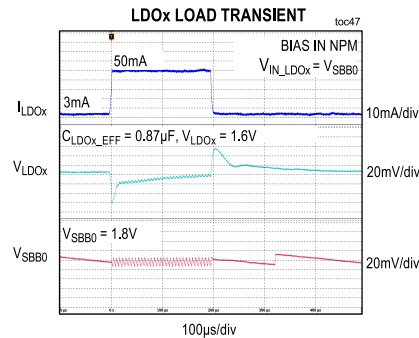
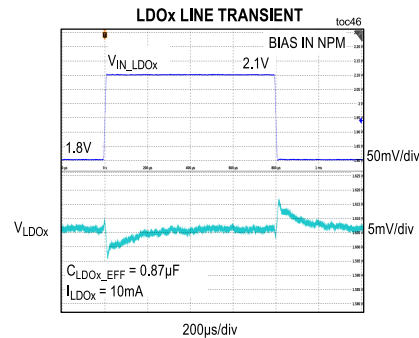
## Typical Operating Characteristics (continued)

(Typical Applications Circuit.  $V_{CHGIN} = 0V$ ,  $V_{SYS} = V_{IN\_SBB} = V_{BATT} = 3.7V$ ,  $V_{IO} = 1.8V$ ,  $T_A = +25^\circ C$ ,  $V_{SBB0} = 1.8V$ ,  $I_{P\_SBB0} = 0.5A$ , SBB0 in Buck mode,  $V_{SBB1} = 1.1V$ ,  $I_{P\_SBB1} = 0.5A$ , SBB1 in Buck mode,  $V_{SBB2} = 3.3V$ ,  $I_{P\_SBB2} = 1A$  peak, SBB2 in Buck-Boost mode, unless otherwise noted. Inductor = DFE201612E-2R2M,  $2.2\mu H$ ,  $116m\Omega$ .)



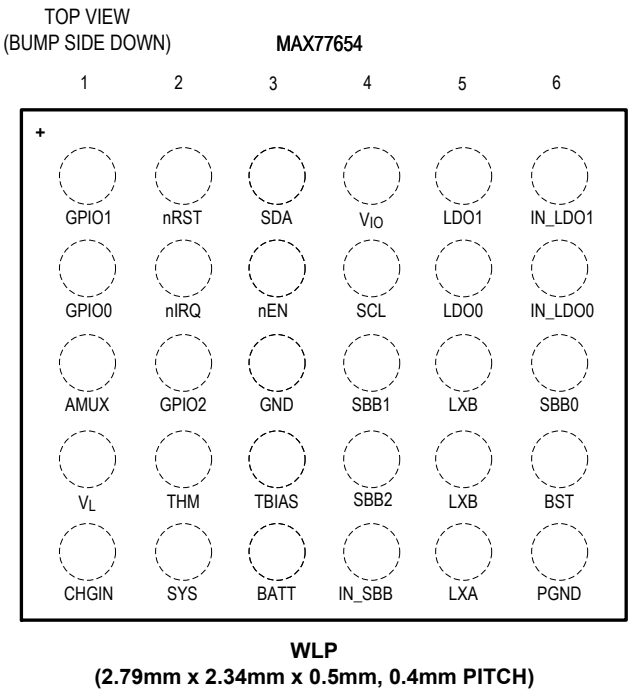
## Typical Operating Characteristics (continued)

(Typical Applications Circuit.  $V_{CHGIN} = 0V$ ,  $V_{SYS} = V_{IN\_SBB} = V_{BATT} = 3.7V$ ,  $V_{IO} = 1.8V$ ,  $T_A = +25^\circ C$ ,  $V_{SBB0} = 1.8V$ ,  $I_{P\_SBB0} = 0.5A$ , SBB0 in Buck mode,  $V_{SBB1} = 1.1V$ ,  $I_{P\_SBB1} = 0.5A$ , SBB1 in Buck mode,  $V_{SBB2} = 3.3V$ ,  $I_{P\_SBB2} = 1A$  peak, SBB2 in Buck-Boost mode, unless otherwise noted. Inductor = DFE201612E-2R2M,  $2.2\mu H$ ,  $116m\Omega$ .)



Pin Configurations

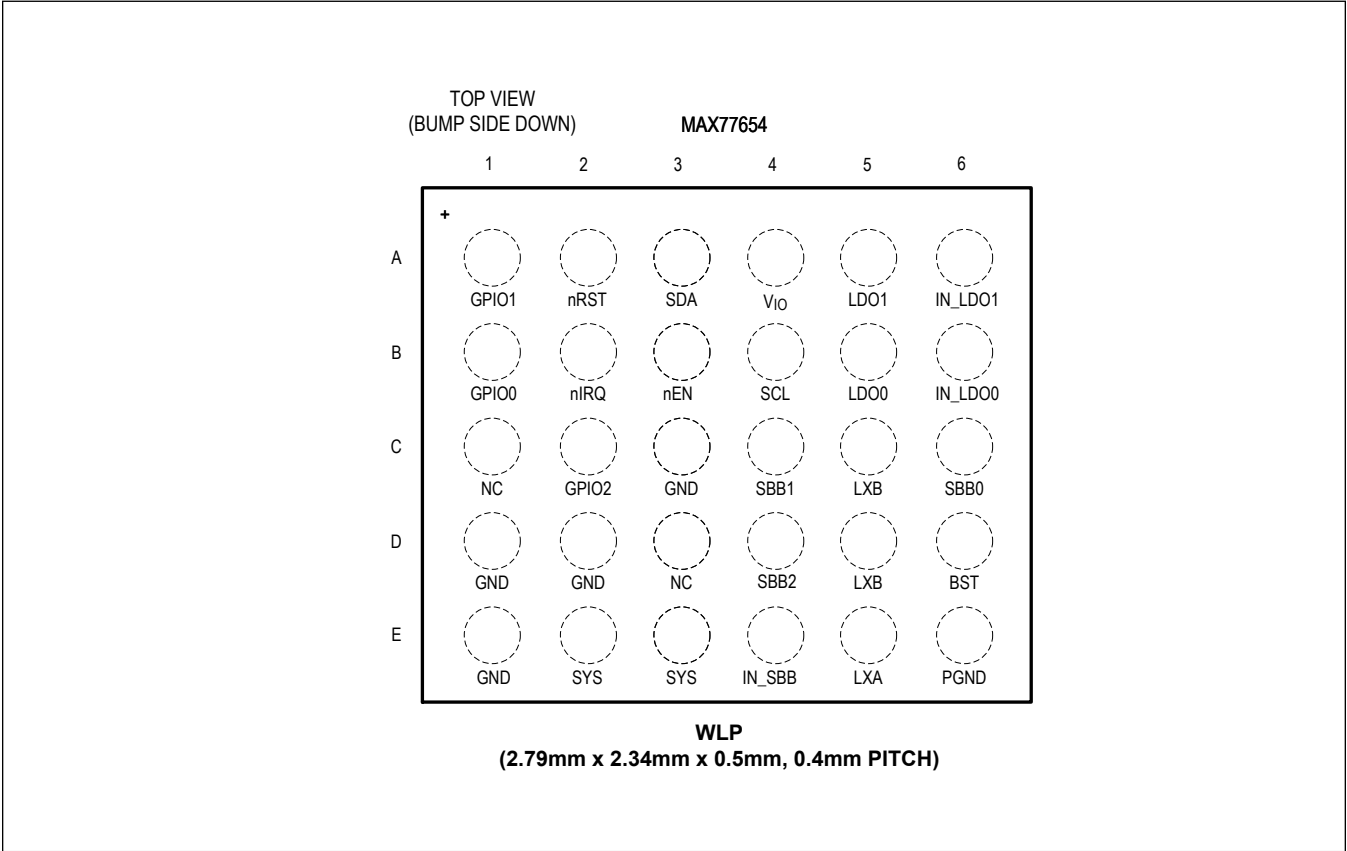
MAX77654xENV



# MAX77654

# Ultra-Low Power PMIC Featuring Single-Inductor, 3-Output Buck-Boost, 2-LDOs, Power-Path Charger for Small Li+, and Ship Mode

## MAX77654xENVN



## Pin Description

| PIN              |                   | NAME  | FUNCTION                                                                                                                                                                                                                                                                                       | TYPE           |
|------------------|-------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| MAX77654xE<br>NV | MAX77654xE<br>NVN |       |                                                                                                                                                                                                                                                                                                |                |
|                  | C1, D3            | NC    | Not connected.                                                                                                                                                                                                                                                                                 |                |
| TOP LEVEL        |                   |       |                                                                                                                                                                                                                                                                                                |                |
| A4               | A4                | VIO   | I2C Interface and GPIO Driver Power                                                                                                                                                                                                                                                            | Power Input    |
| B3               | B3                | nEN   | Active-Low Enable Input. $\overline{\text{EN}}$ supports push-button or slide-switch configurations. If not used, connect $\overline{\text{EN}}$ to SYS and use the CNFG_SBBx_B.EN_SBBx[2:0] and CNFG_LDOx_B.EN_LDOx[2:0] bitfields to enable channels.<br><br>Pulled up internally to VCCINT. | Digital Input  |
| B2               | B2                | nIRQ  | Active-Low, Open-Drain Interrupt Output. Connect a 100k $\Omega$ pullup resistor between $\overline{\text{IRQ}}$ and a voltage equal to or less than V <sub>SYS</sub> .                                                                                                                        | Digital Output |
| A2               | A2                | nRST  | Active-Low, Open-Drain Reset Output. Connect a 100k $\Omega$ pullup resistor between $\overline{\text{RST}}$ and a voltage equal to or less than V <sub>SYS</sub> .                                                                                                                            | Digital Output |
| C2               | C2                | GPIO2 | General Purpose Input/Output. The GPIO I/O stage is internally biased with VIO                                                                                                                                                                                                                 | Digital I/O    |

## Pin Description (continued)

| PIN                    |                   | NAME   | FUNCTION                                                                                                                                                                                                      | TYPE          |
|------------------------|-------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| MAX77654xE<br>NV       | MAX77654xE<br>NVN |        |                                                                                                                                                                                                               |               |
| A1                     | A1                | GPIO1  | General Purpose Input/Output. The GPIO I/O stage is internally biased with $V_{IO}$ .                                                                                                                         | Digital I/O   |
| B1                     | B1                | GPIO0  | General Purpose Input/Output. The GPIO I/O stage is internally biased with $V_{IO}$ .                                                                                                                         | Digital I/O   |
| B4                     | B4                | SCL    | I <sup>2</sup> C Clock                                                                                                                                                                                        | Digital Input |
| A3                     | A3                | SDA    | I <sup>2</sup> C Data                                                                                                                                                                                         | Digital I/O   |
| C3                     | C3, D1, D2,<br>E1 | GND    | Quiet Ground. Connect GND to PGND, and the low-impedance ground plane of the PCB.                                                                                                                             | Ground        |
| <b>CHARGER</b>         |                   |        |                                                                                                                                                                                                               |               |
| E1                     | —                 | CHGIN  | Charger Input. Connect to a DC charging source. Bypass to GND with a 4.7µF ceramic capacitor.                                                                                                                 | Power Input   |
| E2                     | E2, E3            | SYS    | System Power Output. SYS provides power to the system resources as well as the control logic of the device. Connect to IN_SBB and bypass to GND with a 22µF ceramic capacitor.                                | Power Output  |
| E3                     | —                 | BATT   | Li+ Battery Connection. Connect to positive battery terminal. Bypass to GND with a 4.7µF ceramic capacitor.                                                                                                   | Power I/O     |
| D1                     | —                 | VL     | Internal Charger 3V Logic Supply Powered from CHGIN. Bypass to GND with a 1µF ceramic capacitor. Do not load $V_L$ externally.                                                                                | Power Output  |
| D3                     | —                 | TBIAS  | Thermistor Bias Supply. Connect a resistor equal to the NTCs room temperature resistance between TBIAS and THM. Do not load TBIAS with any other external circuitry. If not used, leave the pin disconnected. | Analog        |
| D2                     | —                 | THM    | Thermistor Monitor. Thermally couple an NTC to the battery and connect between THM and GND. If not used, connect THM directly to ground.                                                                      | Analog Input  |
| C1                     | —                 | AMUX   | Analog Multiplexer Output. Connect to system ADC to perform conversions on charger power signals.                                                                                                             | Analog Output |
| <b>SIMO BUCK-BOOST</b> |                   |        |                                                                                                                                                                                                               |               |
| E4                     | E4                | IN_SBB | SIMO Power Input. Connect IN_SBB to SYS and bypass to PGND with a minimum of 10µF ceramic capacitor as close as possible to the IN_SBB pin.                                                                   | Power Input   |
| C6                     | C6                | SBB0   | SIMO Buck-Boost Output 0. SBB0 is the power output for channel 0 of the SIMO buck-boost. Bypass SBB0 to PGND with a 10µF ceramic capacitor. If not used, see the <a href="#">Unused Outputs</a> section.      | Power Output  |
| C4                     | C4                | SBB1   | SIMO Buck-Boost Output 1. SBB1 is the power output for channel 1 of the SIMO buck-boost. Bypass SBB1 to PGND with a 10µF ceramic capacitor. If not used, see the <a href="#">Unused Outputs</a> section.      | Power Output  |
| D4                     | D4                | SBB2   | SIMO Buck-Boost Output 2. SBB2 is the power output for channel 2 of the SIMO buck-boost. Bypass SBB0 to PGND with a 10µF ceramic capacitor. If not used, see the <a href="#">Unused Outputs</a> section.      | Power Output  |
| D6                     | D6                | BST    | SIMO Power Input for the High-Side Output NMOS Drivers. Connect a 3300pF ceramic capacitor between BST and LXB.                                                                                               | Power Input   |

## Pin Description (continued)

| PIN              |                   | NAME    | FUNCTION                                                                                                                                                                                                                             | TYPE         |
|------------------|-------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
| MAX77654xE<br>NV | MAX77654xE<br>NVN |         |                                                                                                                                                                                                                                      |              |
| D5, C5           | D5, C5            | LXB     | Switching Node B. LXB is driven between PGND and SBBx when SBBx is enabled. LXB is driven to PGND when all SIMO channels are disabled. Connect a 1.5μH inductor between LXA and LXB.                                                 | Power Input  |
| E5               | E5                | LXA     | Switching Node A. LXA is driven between PGND and IN_SBB when any SIMO channel is enabled. LXA is driven to PGND when all SIMO channels are disabled. Connect a 1.5μH inductor between LXA and LXB.                                   | Power I/O    |
| E6               | E6                | PGND    | Power ground for the SIMO low-side FETs. Connect PGND to GND, and the low-impedance ground plane of the PCB.                                                                                                                         | Ground       |
| <b>LDO</b>       |                   |         |                                                                                                                                                                                                                                      |              |
| B6               | B6                | IN_LDO0 | Linear Regulator Input. If connected to a SIMO output with a short trace, IN_LDO0 can share the output's capacitor. Otherwise, bypass with a 2.2μF ceramic capacitor to ground. If not used, connect to ground or leave unconnected. | Power Input  |
| A6               | A6                | IN_LDO1 | Linear Regulator Input. If connected to a SIMO output with a short trace, IN_LDO1 can share the output's capacitor. Otherwise, bypass with a 2.2μF ceramic capacitor to ground. If not used, connect to ground or leave unconnected. | Power Input  |
| B5               | B5                | LDO0    | Linear Regulator Output 0. Bypass with a 1.0μF ceramic capacitor to GND. If not used, disable LDO0 and connect this pin to ground or leave unconnected.                                                                              | Power Output |
| A5               | A5                | LDO1    | Linear Regulator Output 1. Bypass with a 1.0μF ceramic capacitor to GND. If not used, disable LDO1 and connect this pin to ground or leave unconnected.                                                                              | Power Output |



# MAX77654

# Ultra-Low Power PMIC Featuring Single-Inductor, 3-Output Buck-Boost, 2-LDOs, Power-Path Charger for Small Li+, and Ship Mode

## Detailed Description

The MAX77654 provides a highly-integrated battery charging and power management solution for low-power applications. The linear charger can charge various Li+ batteries with a wide range of charge current and charger termination voltage options. Temperature monitoring and JEITA compliance settings add additional functionality and safety to the charger.

Five regulators are integrated within this device (see [Table 1](#)). A single-inductor, multiple output (SIMO) buck-boost regulator efficiently provides three independently programmable power rails. Two 100mA low-dropout linear regulators (LDOs) provide ripple rejection for audio and other noise sensitive applications.

This device includes other features such as an analog multiplexer that switches several internal voltage and current signals to an external node for monitoring with an external ADC. A bidirectional I<sup>2</sup>C serial interface allows for configuring and checking the status of the device. An internal on/off controller provides regulator sequencing and supervisory functionality for the device.

Table 1. Regulator Summary

| REGULATOR NAME | REGULATOR TOPOLOGY | MAXIMUM I <sub>OUT</sub> (mA) | V <sub>IN</sub> RANGE | MAX77654 V <sub>OUT</sub> RANGE/ RESOLUTION |
|----------------|--------------------|-------------------------------|-----------------------|---------------------------------------------|
| SBB0           | SIMO               | Up to 500*                    | 2.7 to 5.5V           | 0.8 to 5.5V in 50mV steps                   |
| SBB1           | SIMO               | Up to 500*                    | 2.7 to 5.5V           | 0.8 to 5.5V in 50mV steps                   |
| SBB2           | SIMO               | Up to 500*                    | 2.7 to 5.5V           | 0.8 to 5.5V in 50mV steps                   |
| LDO0/1         | PMOS LDOs          | 100                           | 1.7 to 5.5V           | 0.8 to 3.975V in 25mV steps                 |

\*Shared capacity with other SBBx channels. See the [SIMO Available Output Current](#) section for more information.

## Part Number Decoding

The MAX77654 has different one-time programmable (OTP) options and variants to support a variety of applications. OTP options set default settings such as output voltage or CHGIN current limit. Variants are versions of MAX77654 with different features. See [Figure 1](#) for how to identify these. [Table 2](#) and [Table 3](#) list all available OTP options and variants. Refer to [Maxim Integrated naming convention](#) for more details.

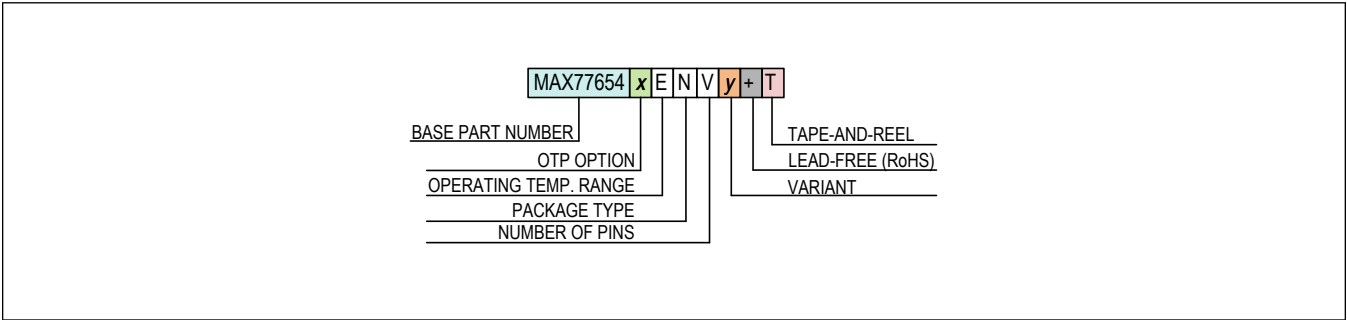


Figure 1. Part Number Decode

Table 2. Variants Table

| VARIANT LETTER                                        | NONE | N   |
|-------------------------------------------------------|------|-----|
| Supports Charger, Analog Multiplexer, and Thermistor? | Yes  |     |
| Supports SIMO Buck-Boost Regulator?                   | Yes  | Yes |
| Supports LDO/LSW?                                     | Yes  | Yes |
| Supports I <sup>2</sup> C Serial Communication?       | Yes  | Yes |

Table 3. OTP Options Table

|          |                |                                  | OTP LETTER AND SETTINGS |             |             |             |             |              |
|----------|----------------|----------------------------------|-------------------------|-------------|-------------|-------------|-------------|--------------|
|          |                | VARIANT                          | NONE                    |             |             |             |             | N            |
| Block    | Bit Field Name | Setting Name                     | A                       | B           | C*          | D           | M           | A            |
| Global   | SBIA_LPM       | Bias Low-Power Mode              | NPM                     | NPM         | NPM         | NPM         | NPM         | NPM          |
|          | DBEN_nEN       | nEN Debounce time                | 500μs                   | 500μs       | 30ms        | 500us       | 500μs       | 500μs        |
|          | nEN_MODE       | nEN Mode                         | Push-Button             | Push-Button | Push-Button | Push-Button | Push-Button | Slide-Switch |
|          | T_MRST         | Manual Reset Time                | 8s                      | 8s          | 8s          | 8s          | 8s          | 8s           |
|          | ALT_GPIO0      | GPIO0 Mode                       | Alt.                    | GPIO        | GPIO        | GPIO        | GPIO        | GPIO         |
|          | ALT_GPIO1      | GPIO1 Mode                       | Alt.                    | GPIO        | GPIO        | GPIO        | Alt.        | GPIO         |
|          | ALT_GPIO2      | GPIO2 Mode                       | Alt.                    | GPIO        | GPIO        | GPIO        | Alt.        | GPIO         |
|          | ADDR           | I <sup>2</sup> C Address (7-bit) | 0x48                    | 0x48        | 0x48        | 0x48        | 0x48        | 0x48         |
|          | DIDM           | Device ID for Metal Options      | 0b0                     | 0b0         | 0b0         | 0b0         | 0b0         | 0b0          |
|          | CID[4:0]       | Chip ID                          | 0x6                     | 0x2         | 0x9         | 0xC         | 0xA         | 0x7          |
| Watchdog | WDT_LOCK       | Watchdog Timer disable control   | Unlocked                | Unlocked    | Unlocked    | Unlocked    | Unlocked    | Unlocked     |
|          | WDT_EN         | Watchdog Timer enable            | Disabled                | Disabled    | Disabled    | Disabled    | Disabled    | Disabled     |
| SIMO     | TV_SBB0[6:0]   | SBB0 V <sub>OUT</sub>            | 1.800V                  | 3.000V      | 4.000V      | 2.050V      | 1.800V      | 1.350V       |
|          | IP_SBB0[1:0]   | SBB0 Inductor Current Peak Limit | 0.500A                  | 1.000A      | 0.500A      | 0.500A      | 0.500A      | 1.000A       |
|          | OP_MODE (SBB0) | SBB0 Operating Mode              | Buck                    | Buck        | Buck-Boost  | Buck        | Buck        | Buck         |
|          | ADE_SBB0       | Active-Discharge Resistor Enable | Enabled                 | Enabled     | Enabled     | Enabled     | Enabled     | Disabled     |
|          | EN_SBB0[2:0]   | SBB0 Enable Control              | Off                     | Off         | Off         | FPS Slot 0  | On          | Off          |
|          | TV_SBB1[6:0]   | SBB1 V <sub>OUT</sub>            | 1.800V                  | 1.800V      | 1.800V      | 1.200V      | 1.100V      | 1.800V       |
|          | IP_SBB1[1:0]   | SBB1 Inductor Current Peak Limit | 0.500A                  | 1.000A      | 0.333A      | 0.500A      | 0.500A      | 1.000A       |
|          | OP_MODE (SBB1) | SBB1 Operating Mode              | Buck                    | Buck        | Buck        | Buck        | Buck        | Buck         |
|          | ADE_SBB1       | Active-Discharge Resistor Enable | Enabled                 | Enabled     | Enabled     | Enabled     | Enabled     | Disabled     |
|          | EN_SBB1[2:0]   | SBB1 Enable Control              | FPS Slot 0              | On          | FPS Slot 0  | FPS Slot 3  | On          | FPS Slot 0   |
|          | TV_SBB2[6:0]   | SBB2 V <sub>OUT</sub>            | 3.500V                  | 3.500V      | 4.000V      | 3.300V      | 3.300V      | 3.300V       |
|          | IP_SBB2[1:0]   | SBB2 Inductor Current Peak Limit | 0.333A                  | 1.000A      | 0.333A      | 0.500A      | 1.000A      | 1.000A       |
|          | OP_MODE (SBB2) | SBB2 Operating Mode              | Buck-Boost              | Buck        | Buck-Boost  | Buck-Boost  | Buck-Boost  | Buck-Boost   |
|          | ADE_SBB2       | Active-Discharge Resistor Enable | Enabled                 | Enabled     | Disabled    | Enabled     | Enabled     | Enabled      |
|          | EN_SBB2[2:0]   | SBB2 Enable Control              | Off                     | Off         | Off         | FPS Slot 0  | On          | FPS Slot 3   |

**Table 3. OTP Options Table (continued)**

|         |                |                                     | OTP LETTER AND SETTINGS |            |         |            |            |            |
|---------|----------------|-------------------------------------|-------------------------|------------|---------|------------|------------|------------|
| LDO     | TV_LDO0[6:0]   | LDO0 V <sub>OUT</sub>               | 1.800V                  | 1.800V     | 1.800V  | 1.850V     | 1.600V     | 1.200V     |
|         | LDO0_MD        | LDO or LSW Mode                     | LDO                     | LDO        | LDO     | LDO        | LDO        | LDO        |
|         | ADE_LDO0       | Active-Discharge Resistor Enable    | Enabled                 | Enabled    | Enabled | Enabled    | Enabled    | Enabled    |
|         | EN_LDO0[2:0]   | LDO0 Enable Control                 | FPS Slot 0              | Off        | Off     | FPS Slot 1 | FPS Slot 3 | FPS Slot 2 |
|         | TV_LDO1[6:0]   | LDO1 V <sub>OUT</sub>               | 3.000V                  | Don't Care | 3.000V  | Don't Care | Don't Care | 1.350V     |
|         | LDO1_MD        | LDO or LSW Mode                     | LDO                     | LSW        | LDO     | LSW        | LSW        | LDO        |
|         | ADE_LDO1       | Active-Discharge Resistor Enable    | Enabled                 | Enabled    | Enabled | Disabled   | Enabled    | Disabled   |
|         | EN_LDO1[2:0]   | LDO1 Enable Control                 | Off                     | Off        | Off     | Off        | FPS Slot 2 | Off        |
| Charger | CHG_EN         | Charger Enable                      | Enabled                 | Enabled    | Enabled | Disabled   | Enabled    |            |
|         | ICHGIN_LIM_DEF | Default Charger Input Current Limit | 95mA                    | 95mA       | 95mA    | 475mA      | 475mA      |            |

*\*Future OTP option. Contact Maxim Integrated for availability.*

## Support Material

The following support materials are available for this device:

- MAX77654 [Register Map](#): Full table of registers that can be read from or written to by I<sup>2</sup>C.
- MAX77654 [Programmer's Guide](#): Basic software implementation guidance.
- MAX77654 [SIMO Calculator](#): Tool to estimate supported maximum current and ripple for specified conditions.

## Top-Level Interconnect Simplified Diagram

[Figure 2](#) shows the same major blocks as the [Typical Applications Circuit](#) with an increased emphasis on the routing between each block. This diagram is intended to familiarize the user with the landscape of the device. Many of the details associated with these signals are discussed throughout the data sheet. At this stage of the data sheet, note the addition of the main bias and clock block that are not shown in the [Typical Applications Circuit](#) section. The main bias and clock block provides voltage, current, and clock references for other blocks as well as many resources for the top-level digital control.

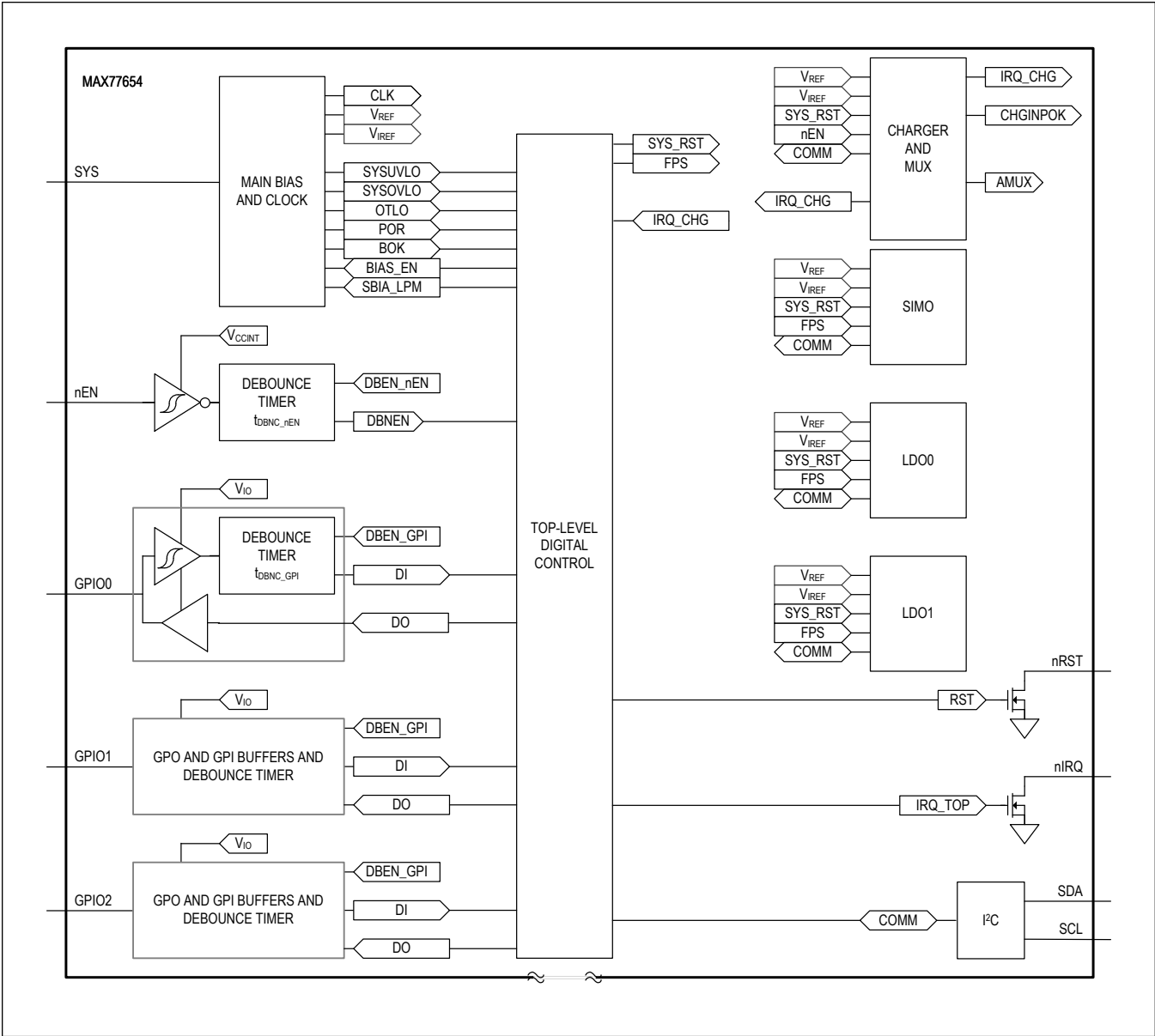


Figure 2. Top-Level Interconnect Simplified Diagram

## Detailed Description—Global Resources

The global resources encompass a set of circuits that serve the entire device and ensure safe, consistent, and reliable operation.

### Features and Benefits

- Voltage Monitors
  - SYS POR (power-on-reset) comparator generates a reset signal upon power-up.
  - SYS undervoltage ensures repeatable behavior when power is applied to and removed from the device.
  - SYS overvoltage monitor inhibits operation with overvoltage power sources to ensure reliability in faulty environments.
- Thermal Monitors
  - +165°C junction temperature shutdown
- Manual Reset
  - 8s or 16s period
- Wake-up Events
  - Charger insertion (with 120ms debounce)
  - nEN input assertion
- Interrupt Handler
  - Interrupt output (nIRQ)
  - All interrupts are maskable
- Push-Button/Slide-Switch On-key (nEN)
  - Configurable push-button/slide-switch functionality
  - 500μs or 30ms debounce timer interfaces directly with mechanical switches
- On/Off Controller
  - Startup/shut-down sequencing
  - Programmable sequencing delay
- GPIO, RST Digital I/Os

### Voltage Monitors

The device monitors the system voltage ( $V_{SYS}$ ) to ensure proper operation using three comparators (POR, UVLO, and OVLO). These comparators include hysteresis to prevent their outputs from toggling between states during noisy system transitions.

#### SYS POR Comparator

The SYS POR comparator monitors  $V_{SYS}$  and generates a power-on reset signal (POR). When  $V_{SYS}$  is below  $V_{POR}$ , the device is held in reset (SYSRST = 1). When  $V_{SYS}$  rises above  $V_{POR}$ , internal signals and on-chip memory stabilize and the device is released from reset (SYSRST = 0).

#### SYS Undervoltage-Lockout Comparator

The SYS undervoltage-lockout (UVLO) comparator monitors  $V_{SYS}$  and generates a SYSUVLO signal when the  $V_{SYS}$  falls below UVLO threshold. The SYSUVLO signal is provided to the top-level digital controller. See [Figure 6](#) and [Table 6](#) for additional information regarding the UVLO comparator:

- When the device is in the STANDBY state, the UVLO comparator is disabled.
- When transitioning out of the STANDBY state, the UVLO comparator is enabled allowing the device to check for sufficient input voltage. If the device has sufficient input voltage, it can transition to the RESOURCE ON state; if there is insufficient input voltage, the device transitions back to the STANDBY state.

### SYS Overvoltage-Lockout Comparator

The device is rated for 5.5V maximum operating voltage ( $V_{SYS}$ ) with an absolute maximum input voltage of 6.0V. An overvoltage-lockout monitor increases the robustness of the device by inhibiting operation when the supply voltage is greater than  $V_{SYSOVLO}$ . See [Figure 6](#) and [Table 6](#) for additional information regarding the OVLO comparator:

- When the device is in the STANDBY state, the OVLO comparator is disabled.

### Chip Identification

The MAX77654 offers different one-time-programmable (OTP) options to, for example, set the default output voltages. These options are identified by the chip identification number, which can be read in the CID register.

### nEN Enable Input

nEN is an active-low internally debounced digital input that typically comes from the system's on-key. The debounce time is programmable with  $CNFG\_GLBL.DBEN\_nEN$ . The primary purpose of this input is to generate a wake-up signal for the PMIC that turns on the regulators. Maskable rising/falling interrupts are available for nEN ( $INT\_GLBL0.nEN\_R$  and  $INT\_GLBL0.nEN\_F$ ) for alternate functionality.

The nEN input can be configured to work either with a push-button ( $CNFG\_GLBL.nEN\_MODE = 0$ ) or a slide-switch ( $CNFG\_GLBL.nEN\_MODE = 1$ ). See [Figure 3](#) for more information. In both push-button mode and slide-switch mode, the on/off controller looks for a falling edge on the nEN input to initiate a power-up sequence.

### nEN Manual Reset

nEN works as a manual reset input when the on/off controller is in the "Resource-On" state. The manual reset function is useful for forcing a power-down in case communication with the processor fails. When nEN is configured for push-button mode and the input is asserted (nEN = LOW) for an extended period ( $t_{MRST}$ ), the on/off controller initiates a power-down sequence and goes to standby mode. When nEN is configured for slide-switch mode and the input is deasserted (nEN = HIGH) for an extended period ( $t_{MRST}$ ), the on/off controller initiates a power-down sequence and goes to standby mode.

### nEN Dual-Functionality: Push-Button vs. Slide-Switch

The nEN digital input can be configured to work with a push-button or a slide-switch. The timing diagram below shows nENs dual functionality for power-on sequencing and manual reset. The default configuration of the device is push-button mode ( $CNFG\_GLBL.nEN\_MODE = 0$ ) and no additional programming is necessary. Applications that use a slide-switch on-key configuration must set  $CNFG\_GLBL.nEN\_MODE = 1$  within  $t_{MRST}$ .

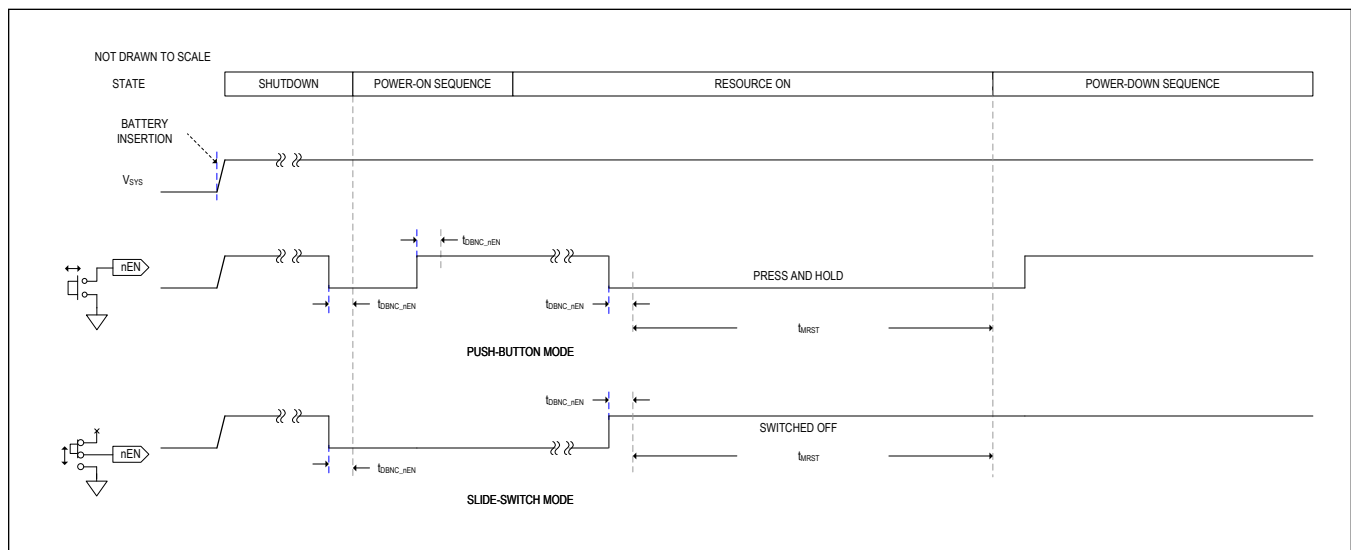


Figure 3. nEN Usage Timing Diagram

**nEN Internal Pullup Resistors to V<sub>CCINT</sub>**

The nEN logic thresholds are referenced to V<sub>CCINT</sub>, an always-on internal voltage domain. There are internal pullup resistors between nEN and V<sub>CCINT</sub> (R<sub>nEN\_PU</sub>), which can be configured with the CNFG\_GLBL\_A.PU\_DIS bit. See [Figure 4](#). While PU\_DIS = 0, the pullup value is approximately 200kΩ. While PU\_DIS = 1, the pullup value is 10MΩ.

V<sub>CCINT</sub> defined by the following conditions:

- V<sub>CCINT</sub> = V<sub>L</sub> (3V typ.) if CHGIN is valid (STAT\_CHG\_B.CHGIN\_DTLS[1:0] = 0b11) and not USB suspended (CNFG\_CHG\_G.USBS = 0).
- V<sub>CCINT</sub> = V<sub>BATT</sub> if CHGIN is invalid (STAT\_CHG\_B.CHGIN\_DTLS[1:0] ≠ 0b11) or CHGIN is valid but USB suspended (CNFG\_CHG\_G.USBS = 1).

Applications using a slide-switch on-key or push-pull digital output connected to nEN can reduce quiescent current consumption by changing pullup strength to 10MΩ. Applications using normally-open, momentary, and push-button on-keys (as shown in [Figure 4](#)) do not create this leakage path and should use the stronger 200kΩ pullup option.

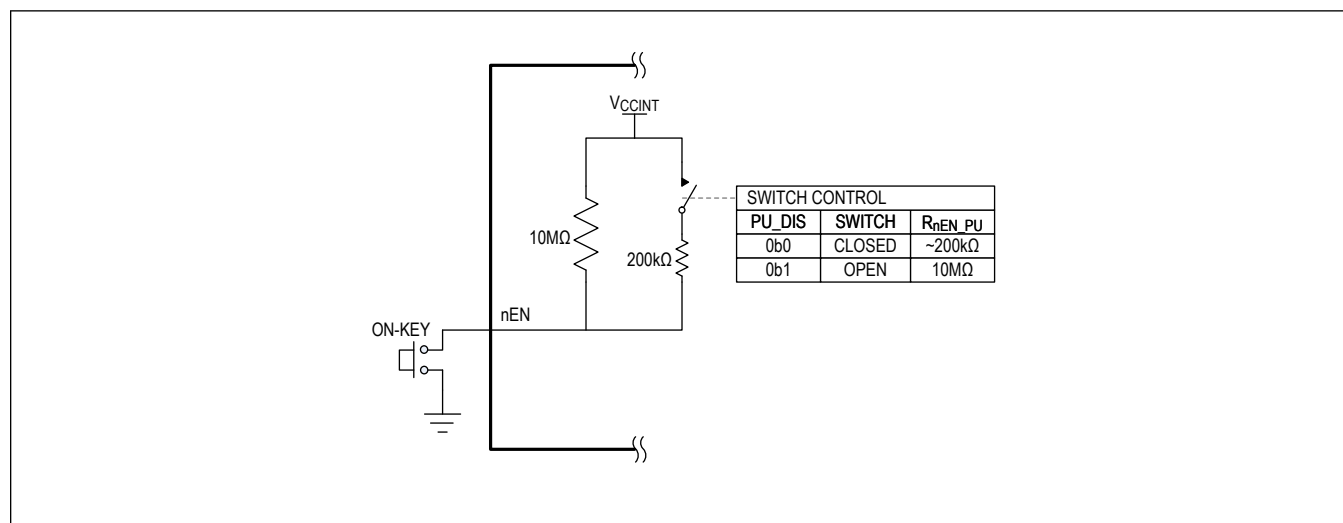


Figure 4. nEN Pullup Resistor Configuration

**Interrupts (nIRQ)**

nIRQ is an active-low, open-drain output that is typically routed to the host processor's interrupt input to signal an important change in device status. See the [Register Map](#) section for a comprehensive list of all interrupt bits and status registers.

A pullup resistor to a voltage less than or equal to V<sub>SYS</sub> is required for this node. nIRQ is the logical *NOR* of all unmasked interrupt bits in the register map.

All interrupts are masked by default. Masked interrupt bits do not cause the nIRQ pin to change. Unmask the interrupt bits to allow nIRQ to assert.

**Reset Output (nRST)**

nRST is an open-drain, active-low output that is typically used to hold the processor in a reset state when the device is powered down. During a power-up sequence, the nRST deasserts after the last regulator in the power-up chain is enabled (t<sub>RSTODD</sub>). During a power-down sequence, the nRST output asserts before any regulator is powered down (t<sub>RSTOAD</sub>). See [Figure 10](#) for nRST timing.

A pullup resistor to a voltage less than or equal to V<sub>SYS</sub> is required for this node.

### General-Purpose Input Output (GPIO)

The provided general-purpose input/output (GPIO) pins increase system flexibility. See [Figure 5](#) for more details.

Clear CNFG\_GPIOx.DIR to configure GPIO as a general-purpose output (GPO). The GPO can either be in push-pull mode (CNFG\_GPIOx.DRV = 1) or open-drain mode (CNFG\_GPIOx.DRV = 0).

- The push-pull output mode is ideal for applications that need fast (~2ns) edges and low power consumption.
- The open-drain mode requires an external pullup resistor (typically 10kΩ–100kΩ). Connect the external pullup resistor to a bias voltage that is less than or equal to  $V_{IO}$ .
  - The open-drain mode can be used to communicate to different logic domains. For example, to send a signal from the GPO on a 1.8V logic domain ( $V_{IO} = 1.8V$ ) to a device on a 1.2V logic domain, connect the external pullup resistor to 1.2V.
  - The open-drain mode can be used to connect several open-drain (or open-collector) devices together on the same bus to create wired logic (wired AND logic is positive-true; wired OR logic is negative-true).
- The general-purpose input (GPI) functions are still available while the pin is configured as a GPO. In other words, the CNFG\_GPIOx.DI (input status) bit still functions and does not collide with the state of the CNFG\_GPIOx.DIR bit.

Set CNFG\_GPIOx.DIR to have the GPIO function as a GPI. The GPI features a 30ms debounce timer ( $t_{DBNC\_GPI}$ ) that can be enabled or disabled with DBEN\_GPI.

- Enable the debounce timer (CNFG\_GPIOx.DBEN\_GPI = 1) if the GPI is connected to a device that can bounce or chatter, like a mechanical switch.
- If the GPI is connected to a circuit with clean logic transitions and no risk of bounce, disable the debounce timer (CNFG\_GPIOx.DBEN\_GPI = 0) to eliminate logic delays. With no debounce timer, the GPI input logic propagates to nIRQ in 10ns.

A dedicated internal oscillator is used to create the 30ms ( $t_{DBNC\_GPI}$ ) debounce timer. To obtain low  $V_{IO}$  supply current, ensure the GPIO voltage is either logic high or logic low. If the GPIO pin is unconnected (either as a GPI or an open-drain GPO) and  $V_{IO}$  is powered, the GPIO voltage trends towards the logic level gray area ( $0.3 \times V_{IO} < V_{GPIO} < 0.7 \times V_{IO}$ ). If  $V_{GPIO}$  is in the gray area,  $V_{IO}$  current can be more than 10μA.

The GPI features edge detectors that feed into the top-level interrupt system of the chip. This allows software to use interrupts to service events associated with a GPI change instead of polling for these changes.

- If the application wants nIRQ to go low **only on a GPI rising edge**, then it should **clear** the GPI rising edge interrupt mask bit (INTM\_GLBL1.GPI\_RM = 0) and **set** the GPI falling edge interrupt mask bit (INTM\_GLBL1.GPI\_FM = 1).
- If the application wants nIRQ to go low **only on a GPI falling edge**, then it should **set** the GPI rising edge interrupt mask bit (INTM\_GLBL1.GPI\_RM = 1) and **clear** the GPI falling edge interrupt mask bit (INTM\_GLBL1.GPI\_FM = 0).
- If the application wants nIRQ to go low **on both GPI falling and rising edges**, then it should **clear** the GPI rising edge interrupt mask bit (INTM\_GLBL1.GPI\_RM = 0) and **clear** the GPI falling edge interrupt mask bit (INTM\_GLBL1.GPI\_FM = 0).



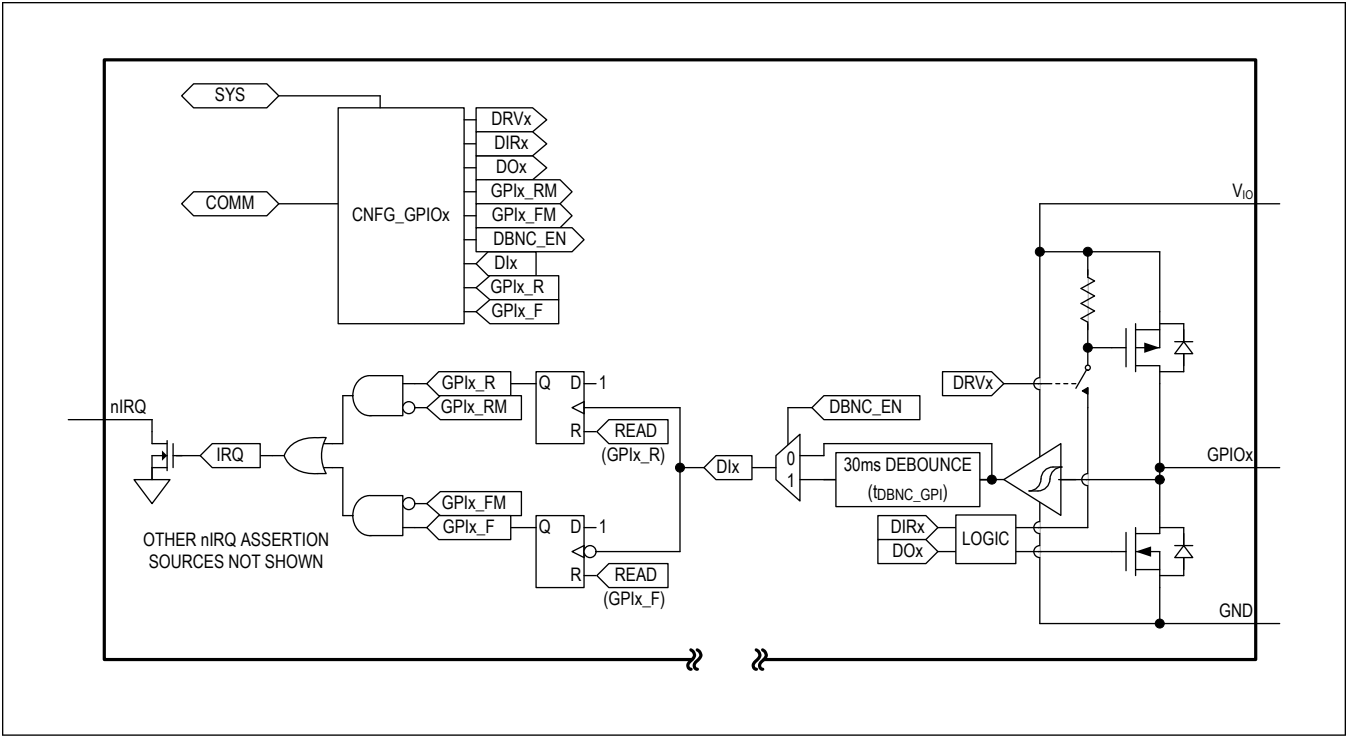


Figure 5. GPIOx Block Diagram

**Alternate Mode**

Each GPIO in the MAX77654 can be configured to have a different function. Whether a particular GPIO is in GPIO mode or alternate mode can be checked by reading the CNFG\_GPIOx.ALT\_GPIOx bit. [Table 4](#) summarizes the alternate functions for each GPIO.

**Table 4. GPIO Mode**

| GPIOx | CNFG_GPIOx REGISTER |                                                                                                      |
|-------|---------------------|------------------------------------------------------------------------------------------------------|
|       | ALT_GPIOx = 0       | ALT_GPIOx = 1                                                                                        |
| GPIO0 | Standard GPIO       | Active-high output of SBB2s flexible power sequencer (FPS) slot.                                     |
| GPIO1 | Standard GPIO       | Active-high input, enable control for SBB2. SBB2 also still powers up and down according to the FPS. |
| GPIO2 | Standard GPIO       | Active-high input, enable control for low-power mode.                                                |

In particular, for GPIO1s alternate mode, SBB2 is enabled if GPIO1 = 1 OR the FPS enables SBB2. See the [Flexible Power Sequencer](#) section for more details. [Table 5](#) summarizes how to enable or disable SBB2 if GPIO1 is configured to be in its alternate mode.

The value of GPIO2 is OR'd with CNFG\_GLBL.SBIA\_LPM, so setting SBIA\_LPM = 1 or setting GPIO2 HIGH requests bias lower-power mode.

**Table 5. Enabling/Disabling SBB2 while GPIO1 is in Alternate Mode**

| GPIO1     | CNFG_SBB2.EN_SBB2[2:0]      |                 |
|-----------|-----------------------------|-----------------|
|           | 0b000 - 0b011, 0b110, 0b111 | 0b100 to 0b0101 |
| GPIO1 = 0 | SBB2 Enabled                | SBB2 Disabled   |
| GPIO1 = 1 | SBB2 Enabled                | SBB2 Enabled    |

### On/Off Controller

The on/off controller monitors multiple power-up (wake-up) and power-down (shutdown) conditions to enable or disable resources that are necessary for the system and its processor to move between its operating modes.

Many systems have one power management controller and one processor and rely on the on/off controller to be the master controller. In this case, the on/off controller receives wake-up events and enables some or all of the regulators to power-up a processor. That processor then manages the system. To conceptualize this master operation, see [Figure 6](#) and [Table 6](#). A typical path through the on/off controller is:

1. Apply a battery and start in the shutdown state.
2. Press the system's on-key (nEN = LOW) and follow transitions 4 and 6 to the resource-on state. If any resources are on the FPS, transitions 7A and 7B are followed.
3. The device performs its desired functions in the resource-on state. When it is ready to turn off, a manual reset first drives the transition through transitions 8A and 8B to the standby state. Afterward, the device automatically follows transition 3 to the shutdown state.

Some systems have several power management blocks, a main processor, and subprocessors. These systems can use this device as a subpower management block for a peripheral portion of circuitry as long as there is an I<sup>2</sup>C port available from a higher level processor. To conceptualize this operation, see [Figure 6](#) and [Table 6](#). A typical path through the on/off controller used in this way is:

1. Apply a battery to the system and start in the shutdown state.
2. When the higher level processor wants to turn on this device's resources, it enables the main bias circuits through I<sup>2</sup>C (CNFG\_GLBL.SBIA\_EN = 1) to transition along path 6 to the resource-on state.
3. The higher level processor can now control this device's resources with I<sup>2</sup>C commands, e.g., turn on/off regulators.
4. When the higher level processor is ready to turn this device off, it turns off everything through I<sup>2</sup>C and then disables the main bias circuits through I<sup>2</sup>C (CNFG\_GLBL.SBIA\_EN = 0) to transition along path 5B to the standby state.

Note that in this style of operation, the CNFG\_GLBL\_SFT\_CTRL[1:0] bits should not be used to turn the device off. The CNFG\_GLBL\_SFT\_CTRL[1:0] bits establish directives to the on/off controller itself that does not make sense in this subpower management block operation. If the processor uses I<sup>2</sup>C commands to enable the device's resources, the processor should also use I<sup>2</sup>C commands to disable them.

## Top Level On/Off Controller

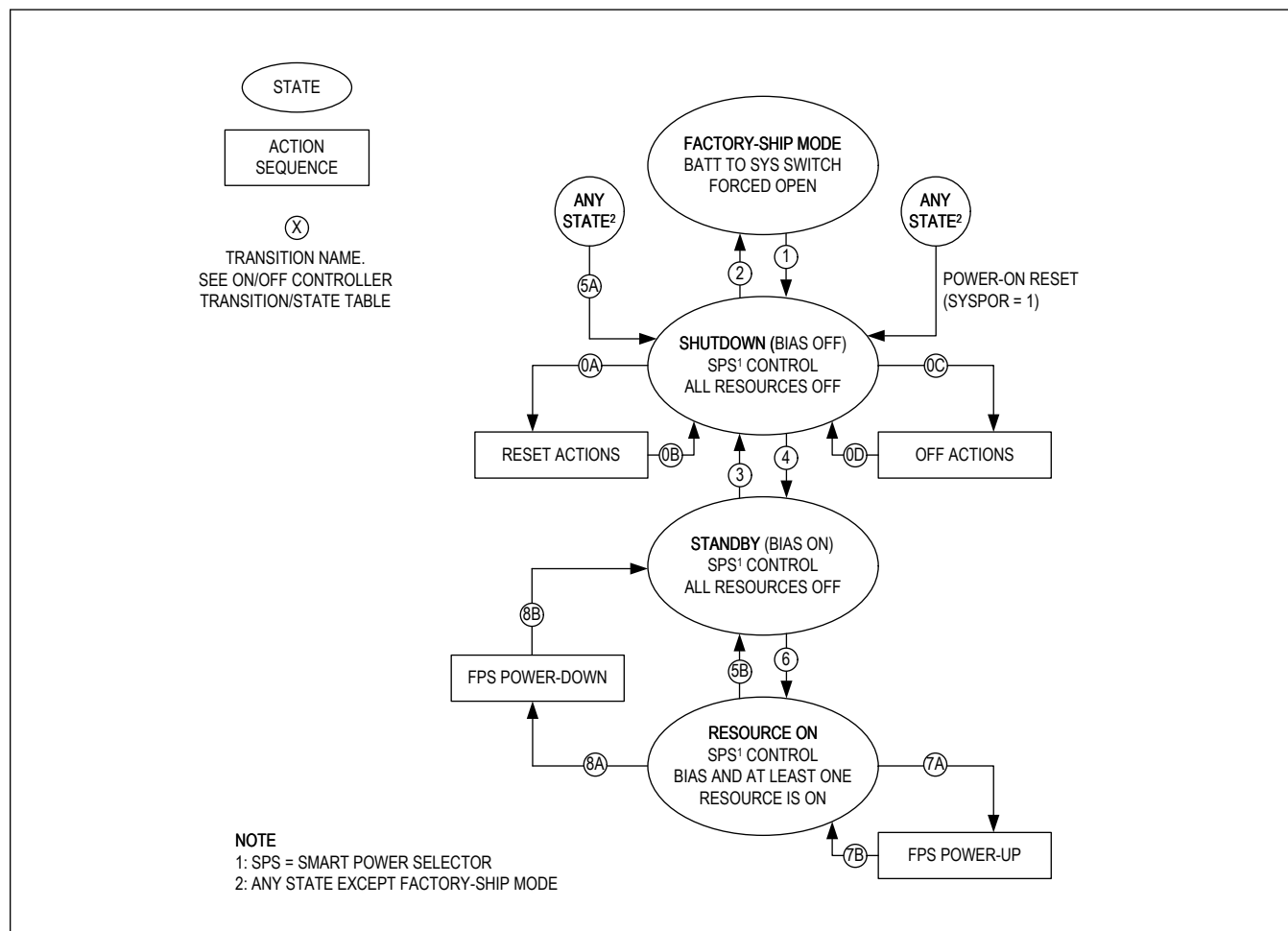


Figure 6. Top Level On/Off Controller State Diagram

## On/Off Controller Transition Table

**Table 6. On/Off Controller Transition/State**

| TRANSITION | CONDITION (TRANSITION HAPPENS WHEN...)                                                                                                                                                                                                                                                                                                                                                                                          |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>0A</b>  | Software cold reset (CNFG_GLBL.SFT_CTRL[1:0] = 0b01) <b>OR</b><br>Watchdog timer expired and caused reset (ERCFLAG.WDT_RST = 1, CNFG_WDT.WDT_MODE = 1)                                                                                                                                                                                                                                                                          |
| <b>0B</b>  | Reset actions completed                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>0C</b>  | Software power-off (CNFG_GLBL.SFT_CTRL[1:0] = 0b10) <b>OR</b><br>Watchdog expired and caused power-off (ERCFLAG.WDT_OFF = 1, CNFG_WDT.WDT_MODE = 0) <b>OR</b><br>Chip over-temperature lockout ( $T_J > T_{OTLO}$ ) <b>OR</b><br>SYS undervoltage lockout ( $V_{SYS} < V_{SYSUVLO} + V_{SYSUVLO\_HYS}$ ) <b>OR</b><br>SYS overvoltage lockout ( $V_{SYS} > V_{SYSOVLO}$ ) <b>OR</b><br>Manual reset occurred (ERCFLAG.MRST = 1) |
| <b>0D</b>  | Off actions completed                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 6. On/Off Controller Transition/State (continued)**

| TRANSITION | CONDITION (TRANSITION HAPPENS WHEN...)                                                                                                                                                                                                                                                                                                                                               |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | CHGIN inserted and 120ms debounce valid (STAT_CHG_B.CHGIN_DTLS[1:0] = 0b11) <b>OR</b><br>nEN asserted and debounced (t <sub>FSM-DB</sub> ) <b>OR</b><br>Power to the IC is removed (V <sub>BATT</sub> < approx. 1.6V) and then reapplied (V <sub>BATT</sub> > V <sub>POR</sub> )                                                                                                     |
| 2          | Factory-ship mode requested (CNFG_GLBL.SFT_CTRL[1:0] = 0b11) <b>AND</b><br>nEN not asserted                                                                                                                                                                                                                                                                                          |
| 3          | <b>NOT</b> (Transition 4)<br>Factory-ship mode requested (CNFG_GLBL.SFT_CTRL[1:0] = 0b11) <b>OR</b><br>Software cold reset (CNFG_GLBL.SFT_CTRL[1:0] = 0b01) <b>OR</b><br>Software power-off (CNFG_GLBL.SFT_CTRL[1:0] = 0b10) <b>OR</b><br>Watchdog timer expired <b>OR</b><br>Manual reset occurred (ERCFLAG.MRT = 1)                                                                |
| 4          | Main bias requested enabled through I <sup>2</sup> C (CNFG_GLBL.SBIA_EN = 1) <b>OR</b><br>Transition 6                                                                                                                                                                                                                                                                               |
| 5A         | Chip over-temperature lockout (T <sub>J</sub> > T <sub>OTLO</sub> ) <b>OR</b><br>SYS undervoltage lockout (V <sub>SYS</sub> < V <sub>SYSUVLO</sub> + V <sub>SYSUVLO_HYS</sub> ) <b>OR</b><br>SYS overvoltage lockout (V <sub>SYS</sub> > V <sub>SYSOVLO</sub> )                                                                                                                      |
| 5B         | <b>NOT</b> (Transition 6) <b>OR</b><br>Factory-ship mode requested (CNFG_GLBL.SFT_CTRL[1:0] = 0b11) <b>OR</b><br>Software cold reset (CNFG_GLBL.SFT_CTRL[1:0] = 0b01) <b>OR</b><br>Software power-off (CNFG_GLBL.SFT_CTRL[1:0] = 0b10) <b>OR</b><br>Watchdog timer expired <b>OR</b><br>Manual reset occurred (ERCFLAG.MRT = 1)                                                      |
| 6          | AMUX is being used (CNFG_CHG_I.MUX_SEL[3:0] ≠ 0b0000) <b>OR</b><br>CHGIN inserted and debounced (STAT_CHG_B.CHGIN_DTLS[1:0] = 0b11) <b>OR</b><br>Any resources force enabled <b>OR</b><br>Internal wake-up flags are set (see the <a href="#">Internal Wake-Up Flags</a> section)                                                                                                    |
| 7A         | FPS power-up sequence has not happened yet <b>AND</b><br>Resources are not forced off <b>AND</b><br>Internal wake-up flags are set (see the <a href="#">Internal Wake-Up Flags</a> section)                                                                                                                                                                                          |
| 7B         | FPS power-up sequence done                                                                                                                                                                                                                                                                                                                                                           |
| 8A         | FPS power-up sequence completed <b>AND</b><br>All resources are force disabled <b>OR</b><br>Factory-ship mode requested (CNFG_GLBL.SFT_CTRL[1:0] = 0b11) <b>OR</b><br>Software cold reset (CNFG_GLBL.SFT_CTRL[1:0] = 0b01) <b>OR</b><br>Software power-off (CNFG_GLBL.SFT_CTRL[1:0] = 0b10) <b>OR</b><br>Watchdog timer expired <b>OR</b><br>Manual reset occurred (ERCFLAG.MRT = 1) |
| 8B         | FPS power-down sequence finished                                                                                                                                                                                                                                                                                                                                                     |

**Internal Wake-Up Flags**

After transitioning to the shutdown state because of a reset, to allow the device to power-up again, internal wake-up flags are set to remember the wake-up request. In [Figure 6](#) and [Table 6](#), these internal wake-up flags trigger transitions 6 and 7A. The internal wake-up flags are set when any of the following happen:

- nEN is debounced (see the [nEN Enable Input](#) section)
  - For example, after a push-button is pressed or a slide-switch switched to HIGH.
- CHGIN is debounced and valid (STAT\_CHG\_B.CHGIN\_DTLS[1:0] = 0b11)
- Software cold reset command sent (CNFG\_GLBL.SFT\_CTRL[1:0] = 0b01)

Reset and Off Sequences

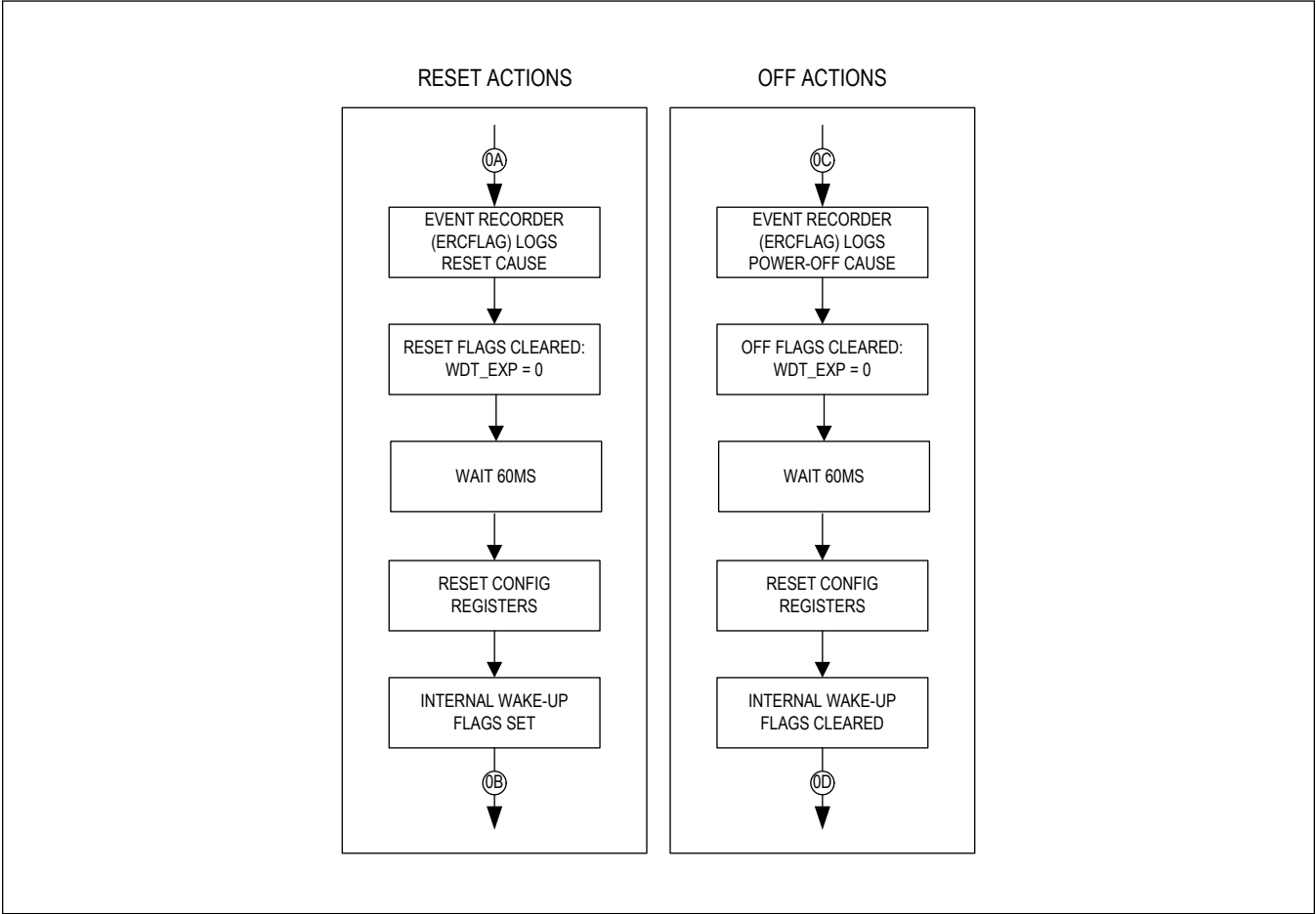


Figure 7. On/Off Controller Reset and Off-Action Sequences

## Power-Up/Down Sequence

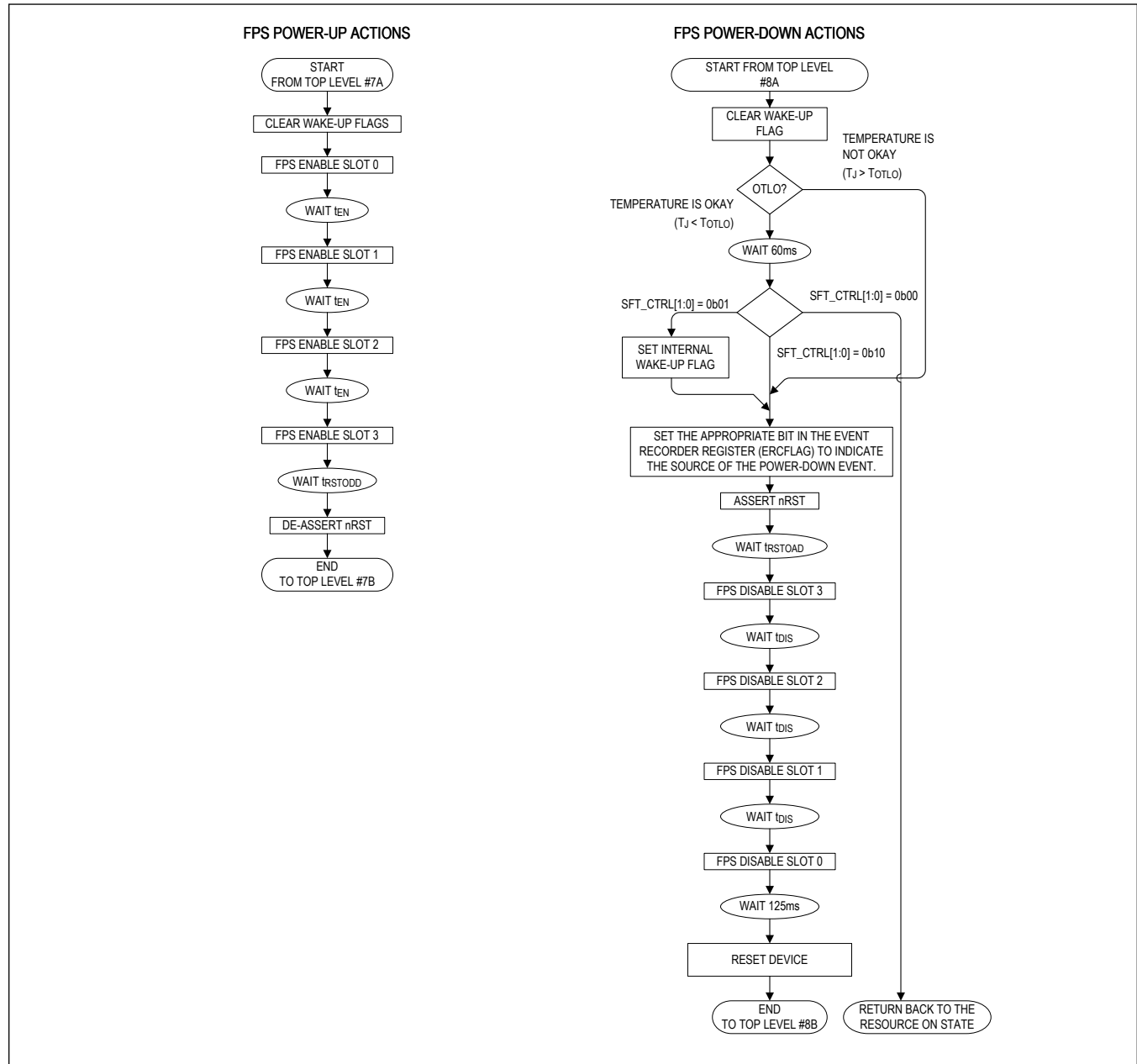


Figure 8. Power-Up/Down Sequence

**Flexible Power Sequencer (FPS)**

The FPS allows resources to power up under hardware or software control. Additionally, each resource can power up independently or among a group of other regulators with adjustable power-up/down delays (sequencing). [Figure 9](#) shows four resources powering up under the control of the flexible power sequencer.

The flexible sequencing structure consists of one master sequencing timer and four slave resources (SBB0, SBB1, SBB2 and LDO0). When the FPS is enabled, a master timer generates four sequencing events for device power-up/down.

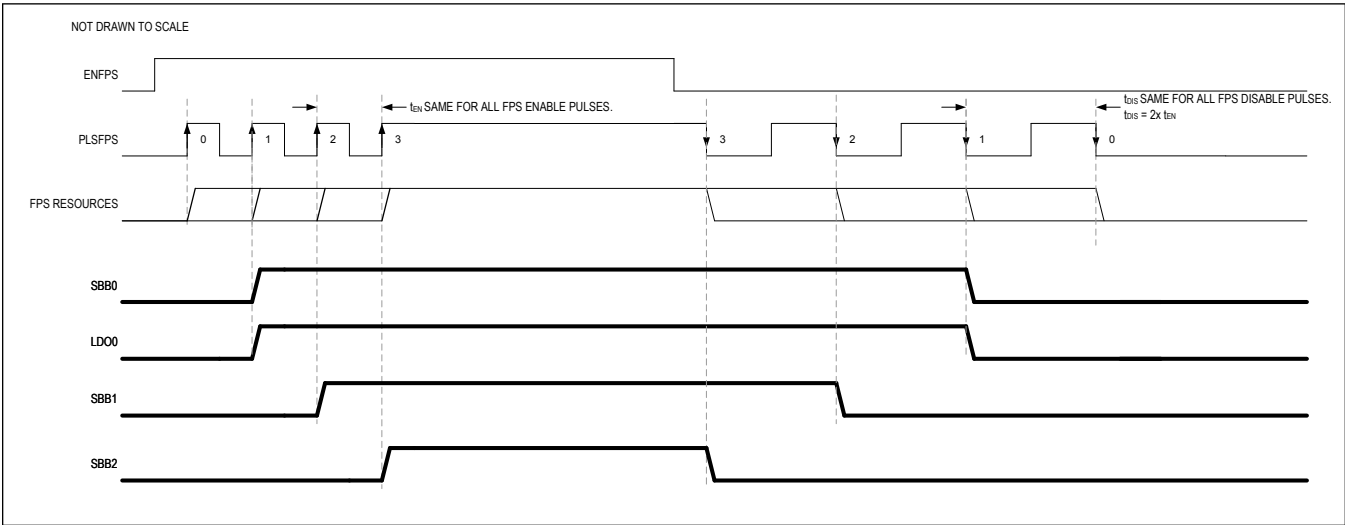


Figure 9. Flexible Power Sequencer Basic Timing Diagram

Startup Timing Diagram Due to nEN

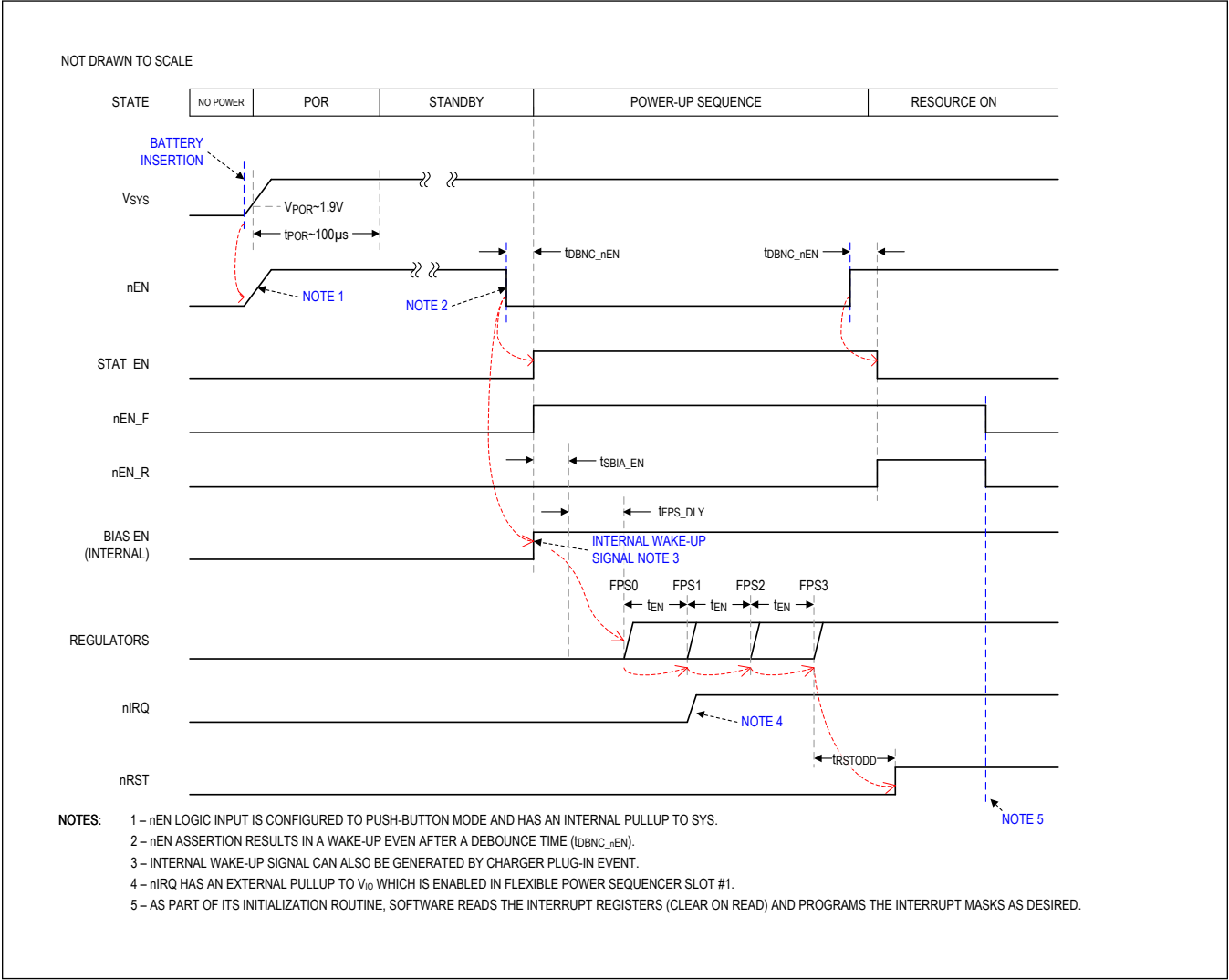


Figure 10. Startup Timing Diagram Due to nEN



## Startup Timing Diagram Due to Charge Source Insertion

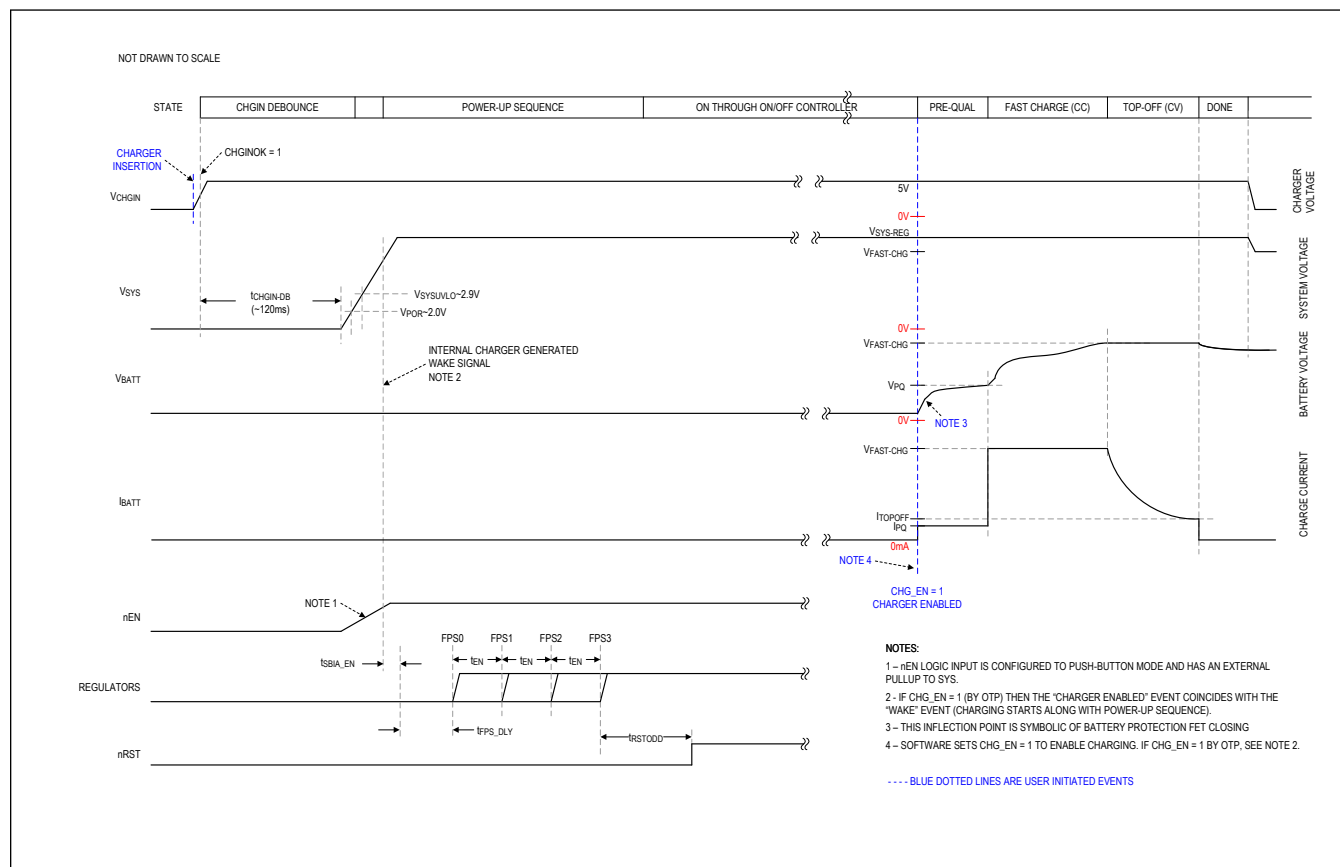


Figure 11. Startup Timing Diagram Due to Charge Source Insertion

## Force Enabled/Disabled Channels

Force enable SIMO and LDO output channels by setting `CNFG_SBBx_B.EN_SBBx[2:0]` (SIMO) or `CNFG_LDOx_B.EN_LDOx[2:0]` (LDO) = 0x6. Depending on the OTP, output channels may already be force enabled by default. Output channels configured this way are independent of the flexible power sequence and start up as soon as `SYS > UVLO` rising. The main bias also automatically turns on.

Likewise, output channels can be force disabled by setting `EN_SBBx[2:0]` or `EN_LDOx[2:0]` = 0x4.

### Factory-Ship Mode State

Factory-ship mode internally disconnects the battery (BATT) from the system (SYS). The battery does not power the system in this mode. Use this mode to preserve battery life if external circuits on SYS cause the battery to leak.

Write `CNFG_GLBL.SFT_CTRL[1:0] = 0b11` using I<sup>2</sup>C to enter factory-ship mode. The IC responds in two different ways depending on the state of the charger input (CHGIN):

- If CHGIN is valid (`STAT_CHG_B.CHGIN_DTLS[1:0] = 0b11`) while `CNFG_GLBL.SFT_CTRL[1:0] = 0b11`, then the IC enters factory-ship mode (internally disconnects BATT from SYS) but SYS is still powered from CHGIN (regulating to  $V_{SYS-REG}$ ). SYS decays to 0V when CHGIN is disconnected.
- If CHGIN is invalid (`STAT_CHG_B.CHGIN_DTLS[1:0] ≠ 0b11`) while `CNFG_GLBL.SFT_CTRL[1:0] = 0b11`, then the IC enters factory-ship mode and SYS decays to 0V.

Factory-ship mode causes many configuration registers to reset (SYSRST). See the [Register Map](#) section for details. I<sup>2</sup>C reads and writes cannot happen in factory-ship mode.

Factory-ship mode exits only after SYS decays below approximately 1.8V. Once this condition is met, there are two ways to exit factory-ship mode:

- Apply a valid DC source at CHGIN for  $t_{CHGIN-DB}$  (120ms typical). Factory-ship mode is unlatched (exited) when the charger input becomes valid from a previously invalid state (`STAT_CHG_B.CHGIN_DTLS[1:0] = 0b00 → 0b11`).
- Assert `nEN` for  $t_{FSM-EXDB}$  (250ms typical) +  $t_{DBNC\_nEN}$ .

Furthermore, this state is unlatched if power is removed from the IC (BATT voltage falls below approximately 1.8V). In all exit cases, the smart power selector controls the interaction between BATT and SYS until factory-ship mode is entered again (see the [Smart Power Selector](#) section).

### Debounced Inputs (nEN, GPI, CHGIN)

`nEN`, `CHGIN`, and `GPI` (when operating as an input), are debounced on both rising and falling edges to reject undesired transitions. The input must be at a stable logic level for the entire debounce period for the output to change its logic state. [Figure 12](#) shows an example timing diagram for the `nEN` debounce.

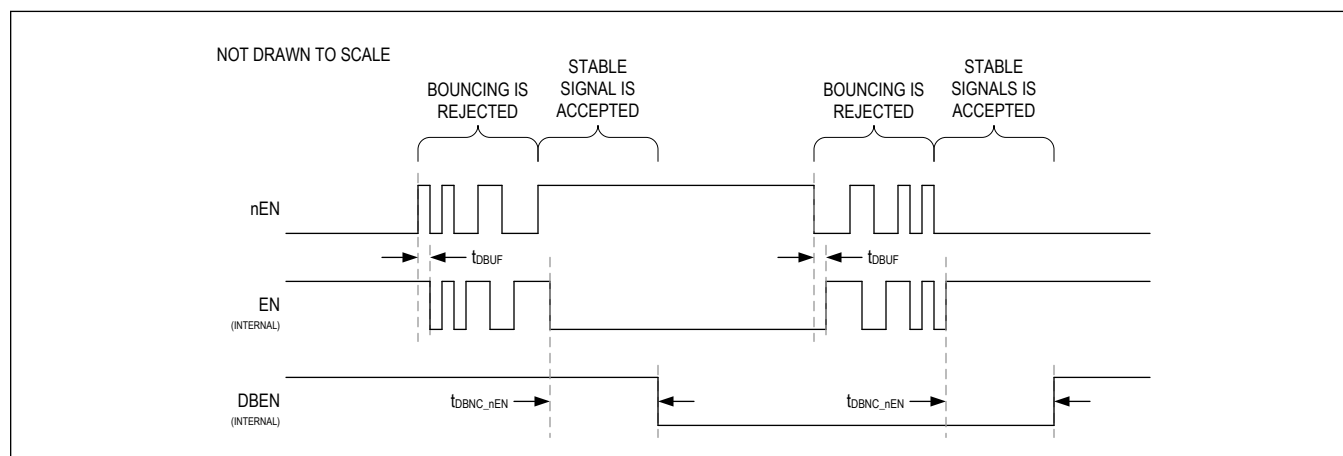


Figure 12. Debounced Inputs

Watchdog Timer (WDT)

The IC features a watchdog timer function for operational safety. If this timer expires without being cleared, the on/off controller causes the IC to enter the shutdown state and resets configuration registers. See the [On/Off Controller](#) and [On/Off Controller Transition Table](#) sections (transitions 0A and 0C) for more details.

Write CNFG\_WDT.WDT\_EN = 1 through I<sup>2</sup>C to enable the timer. The watchdog timer period ( $t_{WD}$ ) is configurable from 16 to 128 seconds in 4 steps with CNFG\_WDT.WDT\_PER[1:0]. The default timer period is 128 seconds. While the watchdog timer is enabled, the CNFG\_WDT.WDT\_CLR bit must be set through I<sup>2</sup>C periodically (within  $t_{WD}$ ) to reset the timer and prevent shutdown. See the [Register Map](#) and [Figure 13](#) for additional details.

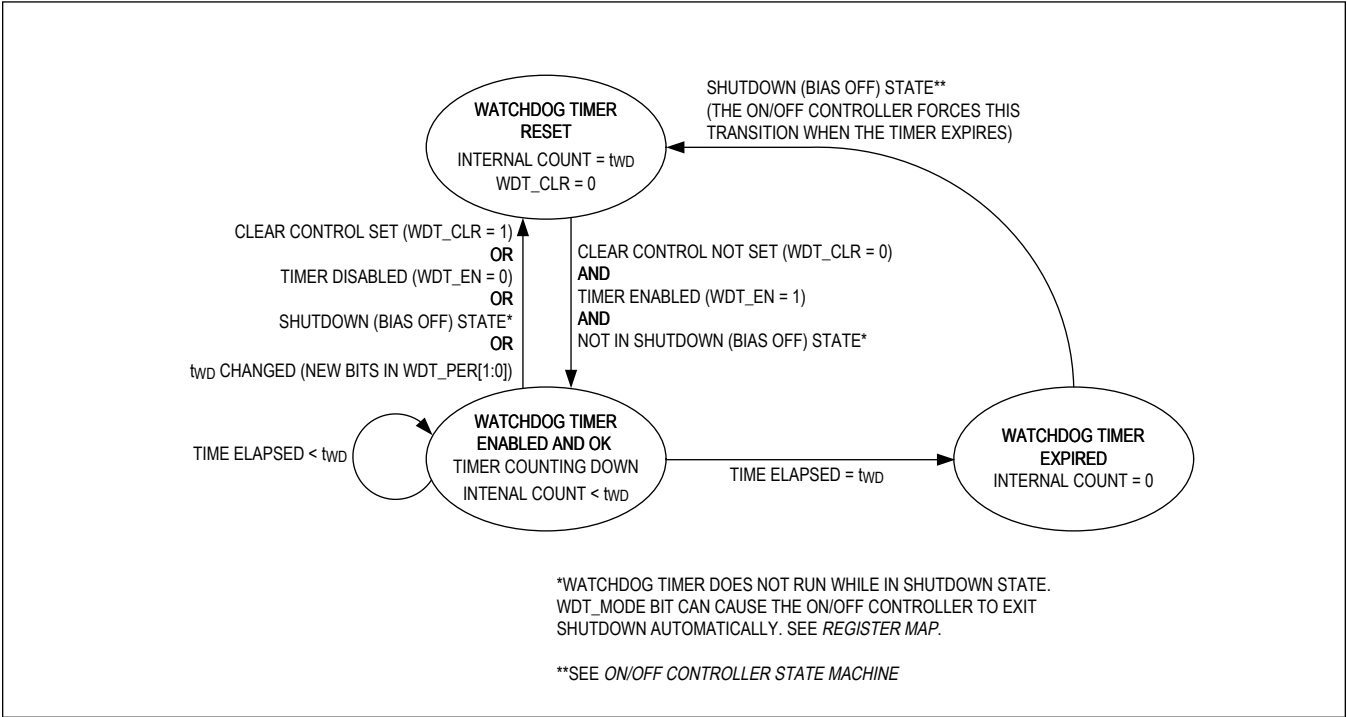


Figure 13. Watchdog Timer State Machine

The timer can be factory-programmed to be enabled by default, disabled by default, or locked from accidental disable. The CNFG\_WDT.WDT\_LOCK bit is read-only and must be configured at the factory. See [Table 7](#) for a full description.

Table 7. Watchdog Timer Factory-Programmed Safety Options

| WDT_LOCK | WDT_EN | FUNCTION                                                                                                                                                                                                                                                                                               |
|----------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0        | 0      | Watchdog timer is disabled by default. Timer can be enabled or disabled by I <sup>2</sup> C writes.                                                                                                                                                                                                    |
| 0        | 1      | Watchdog timer is enabled by default. Timer can be enabled or disabled by I <sup>2</sup> C writes.                                                                                                                                                                                                     |
| 1        | 0      | Watchdog timer is disabled by default. Timer can be enabled by an I <sup>2</sup> C write, but only a SYSRST can reset the CNFG_WDT.WDT_EN value back to 0. Timer can not be disabled by direct I <sup>2</sup> C writes to CNFG_WDT.WDT_EN (write from 1 → 0 is ignored, write from 0 → 1 is accepted). |
| 1        | 1      | Watchdog timer is enabled by default. Nothing can disable the timer.                                                                                                                                                                                                                                   |

## Detailed Description—Smart Power Selector Charger

The linear Li+ charger implements power path with Maxim's Smart Power Selector. This allows separate input current limit and battery charge current settings. Batteries charge faster under the supervision of the Smart Power Selector because charge current is independently regulated and not shared with variable system loads. See the [Smart Power Selector](#) section for more information.

The programmable constant-current charge rate (7.5mA to 300mA) supports a wide range of battery capacities. The programmable input current limit (95mA to 475mA) supports a range of charge sources, including USB. The charger's programmable battery regulation voltage range (3.6V to 4.6V) supports a wide variety of cell chemistries. Small battery capacities are supported; the charger accurately terminates charging by detecting battery currents as low as 0.375mA.

Additionally, the robust charger input withstands overvoltages up to 28V. To enhance charger safety, an NTC thermistor provides temperature monitoring in accordance with the JEITA recommendations. See the [Adjustable Thermistor Temperature Monitors](#) section for more information.

## Charger Symbol Reference Guide

[Table 8](#) lists the names and functions of charger-specific signals and if they can be programmed through I<sup>2</sup>C serial communication. See the [Electrical Characteristics](#) and [Register Map](#) for more information.

**Table 8. Charger Quick Symbol Reference Guide**

| SYMBOL                  | NAME                                      | I <sup>2</sup> C PROGRAMMABLE?          |
|-------------------------|-------------------------------------------|-----------------------------------------|
| V <sub>CHGIN_OVP</sub>  | CHGIN overvoltage threshold               | No                                      |
| V <sub>CHGIN_UVLO</sub> | CHGIN undervoltage-lockout threshold      | No                                      |
| V <sub>CHGIN-MIN</sub>  | Minimum CHGIN voltage regulation setpoint | Yes, through CNFG_CHG_B.VCHGIN_MIN[2:0] |
| I <sub>CHGIN-LIM</sub>  | CHGIN input current limit                 | Yes, through CNFG_CHG_B.ICHGIN_LIM[2:0] |
| V <sub>SYS-REG</sub>    | SYS voltage regulation target             | Yes, through CNFG_CHG_D.VSYS_REG[4:0]   |
| V <sub>SYS-MIN</sub>    | Minimum SYS voltage regulation setpoint   | No, tracks V <sub>SYS-REG</sub>         |
| V <sub>FAST-CHG</sub>   | Fast-charge constant-voltage level        | Yes, through CNFG_CHG_G.CHG_CV[5:0]     |
| I <sub>FAST-CHG</sub>   | Fast-charge constant-current level        | Yes, through CNFG_CHG_G.E.CHG_CC[5:0]   |
| I <sub>PQ</sub>         | Prequalification current level            | Yes, through CNFG_CHG_B.I_PQ            |
| V <sub>PQ</sub>         | Prequalification voltage threshold        | Yes, through CNFG_CHG_C.CHG_PQ[2:0]     |
| I <sub>TERM</sub>       | Termination current level                 | Yes, through CNFG_CHG_C.I_TERM[1:0]     |
| T <sub>J-REG</sub>      | Die temperature regulation setpoint       | Yes, through CNFG_CHG_D.TJ_REG[2:0]     |
| t <sub>PQ</sub>         | Prequalification safety timer             | No                                      |
| t <sub>FC</sub>         | Fast-charge safety timer                  | Yes, through CNFG_CHG_E.T_FAST_CHG[1:0] |
| t <sub>TO</sub>         | Top-off timer                             | Yes, through CNFG_CHG_C.T_TOPOFF[2:0]   |

[Figure 14](#) indicates the high-level functions of each control circuit within the linear charger.

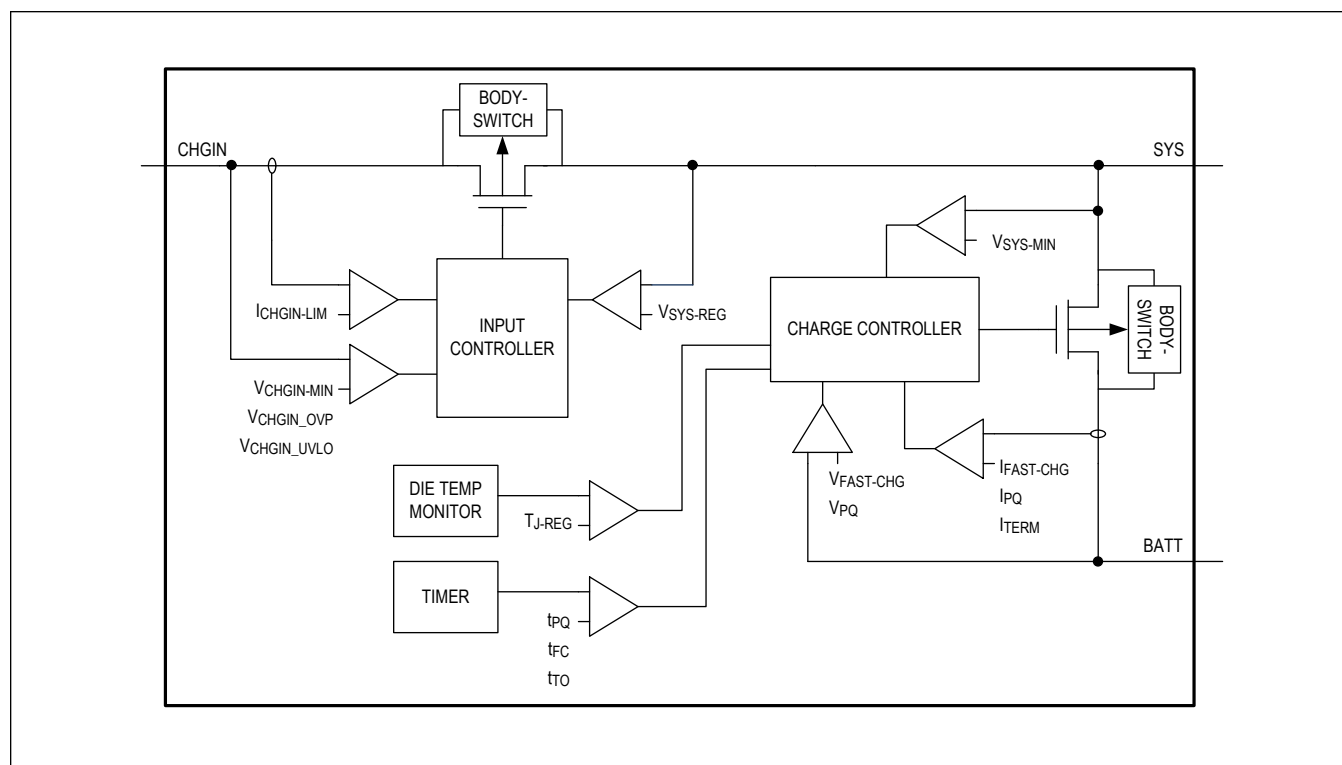


Figure 14. Charger Simplified Control Loops

### Smart Power Selector

The Smart Power Selector seamlessly distributes power from the input (CHGIN) to the battery (BATT) and the system (SYS). The Smart Power Selector basic functions are:

- When the system load current is less than the input current limit, the battery is charged with residual power from the input.
- When a valid input source is connected, the system regulates to  $V_{SYS-REG}$  to power system loads regardless of the battery's voltage (instant on).
- When the system load current exceeds the input current limit, the battery provides additional current to the system (supplement mode).
- When the battery is finished charging and an input source is present to power the system, the battery remains disconnected from the system.
- When the battery is connected and there is no input power, the system is powered from the battery.

### Input Current Limiter

The input current limiter limits CHGIN current to not exceed  $I_{CHGIN-LIM}$  (programmed by CNFG\_CHG\_B.ICHHIN\_LIM[2:0]). A maskable interrupt (INT\_CHG.CHGIN\_CTRL\_I) signals when the input current limit engages. The STAT\_CHG\_A.ICHHIN\_LIM\_STAT bit reflects the state of the current limiter loop.

The default value of  $I_{CHGIN-LIM}$  is factory-programmable to either 95mA or 475mA. The decoding of the CNFG\_CHG\_B.ICHHIN\_LIM[2:0] bitfield changes depending on the factory-programmed default value (see [Table 9](#)). The reset value of this bitfield is always 0b000 regardless of factory option.

**Table 9. Input Current Limit Factory Options**

| ICHGIN_LIM[2:0] | 95mA<br>Factory-Default | 475mA<br>Factory-Default |
|-----------------|-------------------------|--------------------------|
| 0b000           | 95mA                    | 475mA                    |
| 0b001           | 190mA                   | 380mA                    |
| 0b010           | 285mA                   | 285mA                    |
| 0b011           | 380mA                   | 190mA                    |
| 0b100 to 0b111  | 475mA                   | 95mA                     |

CHGIN is capable of withstanding a maximum of 28V with respect to ground. CHGIN suspends power delivery to the system and battery when  $V_{CHGIN}$  exceeds  $V_{CHGIN\_OVP}$  (7.5V, typ). The input circuit also suspends when  $V_{CHGIN}$  falls below  $V_{CHGIN\_UVLO}$  minus 500mV of hysteresis (3.5V, typ). While in OVP or UVLO, the charger remains off and the battery provides power to the system.

Power transfer to SYS is delayed by a 120ms debounce timer ( $t_{CHGIN\_DB}$ ) after a valid DC source is connected to CHGIN. SYS does not begin regulating to  $V_{SYS\_REG}$  until after the timer expires.

The STAT\_CHG\_B.CHGIN\_DTLS[1:0] bitfield continuously indicates the state of CHGINs voltage quality. A maskable interrupt (INT\_CHG.CHGIN\_I) asserts when STAT\_CHG\_B.CHGIN\_DTLS[1:0] changes.

### Minimum Input Voltage Regulation

In the event of a poor-quality charge source, the minimum input voltage regulation loop works to reduce input current if  $V_{CHGIN}$  falls below  $V_{CHGIN\_MIN}$  (programmed by CNFG\_CHG\_B.VCHGIN\_MIN[2:0]). This is important because many commonly used charge adapters feature foldback protection mechanisms where the adapter completely shuts off if its output drops too low. The minimum input voltage regulation loop also prevents  $V_{CHGIN}$  from dropping below  $V_{CHGIN\_UVLO}$  if the cable between the charge source and the charger's input is long or highly resistive.

The input voltage regulation loop improves performance with current limited adapters. If the charger's input current limit is programmed above the current limit of the given adapter, the input voltage loop allows the input to regulate at the current limit of the adapter. The input voltage regulation loop also allows the charger to perform well with adapters that have poor transient load response times.

A maskable interrupt (INT\_CHG.CHGIN\_CTRL\_I) signals when the minimum input voltage regulation loop engages. The state of this loop is reflected by STAT\_CHG\_A.VCHGIN\_MIN\_STAT.

### Minimum System Voltage Regulation

The minimum system voltage regulation loop ensures that the system rail remains close to the programmed SYS regulation voltage ( $V_{SYS-REG}$ ) regardless of system loading. The loop engages when the combined battery charge current and system load current causes the CHGIN input to current limit at  $I_{CHGIN-LIM}$ . When this happens, the minimum system voltage loop reduces charge current in an attempt to keep the input out of current limit, thereby keeping the system voltage above  $V_{SYS-MIN}$  ( $V_{SYS-REG} - 100\text{mV}$ , typ). If this loop reduces battery current to 0 and the system is in need of more current than the input can provide, then the Smart Power Selector overrides the minimum system voltage regulation loop and allows SYS to collapse to BATT for the battery to provide supplement current to the system. The Smart Power Selector automatically reenables the minimum system voltage loop when the supplement event has ended.

A maskable interrupt ( $INT\_CHG\_SYS\_CTRL\_I$ ) asserts to signal a change in  $STAT\_CHG\_A.VSYS\_MIN\_STAT$ . This status bit asserts when the minimum system voltage regulation loop is active.

### Die Temperature Regulation

If the die temperature exceeds  $T_{J-REG}$  (programmed by  $CNFG\_CHG\_D.TJ\_REG[2:0]$ ) the charger attempts to limit the temperature increase by reducing the battery charge current. The  $STAT\_CHG\_A.TJ\_REG\_STAT$  bit asserts whenever charge current is reduced due to this loop. The charger's current sourcing capability to SYS remains unaffected when  $STAT\_CHG\_A.TJ\_REG\_STAT$  is high. A maskable interrupt ( $INT\_CHG.TJ\_REG\_I$ ) asserts to signal a change in  $STAT\_CHG\_A.TJ\_REG\_STAT$ . Use the  $INT\_CHG.TJ\_REG\_I$  interrupt to signal the system processor to reduce loads on SYS to reduce total system temperature.

### Charger State Machine

The battery charger follows a strict state-to-state progression to ensure that a battery is charged safely. The status bitfield  $STAT\_CHG\_B.CHG\_DTLS[3:0]$  reflects the charger's current operational state. A maskable interrupt ( $INT\_CHG.CHG\_I$ ) is available to signal a change in  $STAT\_CHG\_B.CHG\_DTLS[3:0]$ .

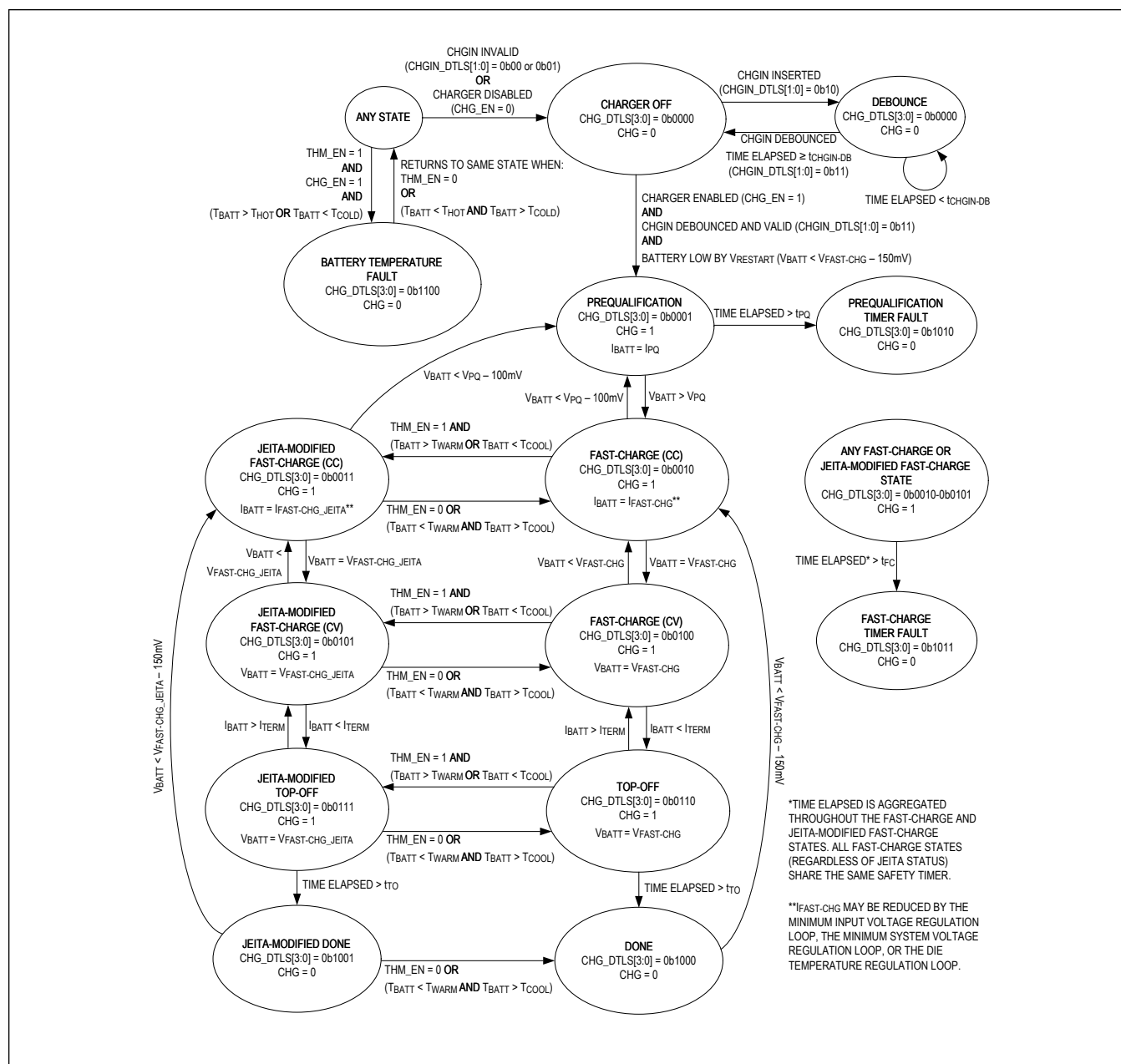


Figure 15. Charger State Diagram

## Charger-Off State

The charger is off when CHGIN is invalid, the charger is disabled, or the battery is fresh.

CHGIN is invalid when the CHGIN input is invalid ( $V_{CHGIN} < V_{CHGIN\_UVLO}$  or  $V_{CHGIN} > V_{CHGIN\_OVP}$ ). While CHGIN is invalid, the battery is connected to the system. CHGIN voltage quality can be separately monitored by the STAT\_CHG\_B.CHGIN\_DTLS[1:0] status bitfield. See the [Register Map](#) section for details.

The charger is disabled when the charger enable bit is 0 (CNFG\_CHG\_B.CHG\_EN = 0). The battery is connected or disconnected to the system depending on the validity of  $V_{CHGIN}$  while CNFG\_CHG\_B.CHG\_EN = 0. See the [Smart Power Selector](#) section.



The battery is fresh when CHGIN is valid and the charger is enabled (CNFG\_CHG\_B.B.CHG\_EN = 1) and the battery is not low by V<sub>RESTART</sub> ( $V_{BATT} > V_{FAST-CHG} - V_{RESTART}$ ). The battery is disconnected from the system and not charged while the battery is fresh. The charger state machine exits this state and begins charging when the battery becomes low by V<sub>RESTART</sub> (150mV, typ). This condition is functionally similar to done state. See the [Done State](#) section.

### Prequalification State

The prequalification state is intended to assess a low-voltage battery's health by charging at a reduced rate. If the battery voltage is less than the V<sub>PQ</sub> threshold, the charger is automatically in prequalification. If the cell voltage does not exceed V<sub>PQ</sub> in 30 minutes (t<sub>PQ</sub>), the charger faults. The prequalification charge rate is a percentage of I<sub>FAST-CHG</sub> and is programmable with CNFG\_CHG\_B.I\_PQ. The prequalification voltage threshold (V<sub>PQ</sub>) is programmable through CNFG\_CHG\_C.CHG\_PQ[2:0].

### Fast-Charge States

When the battery voltage is above V<sub>PQ</sub>, the charger transitions to the fast-charge (CC) state. In this state, the charger delivers a constant current (I<sub>FAST-CHG</sub>) to the cell. The constant current level is programmable from 7.5mA to 300mA by CNFG\_CHG\_E.CHG\_CC[5:0].

When the cell voltage reaches V<sub>FAST-CHG</sub>, the charger state machine transitions to fast-charge (CV). V<sub>FAST-CHG</sub> is programmable with CNFG\_CHG\_G.CHG\_CV[5:0] from 3.6V to 4.6V. The charger holds the battery's voltage constant at V<sub>FAST-CHG</sub> while in the fast-charge (CV) state. As the battery approaches full, the current accepted by the battery reduces. When the charger detects that battery charge current has fallen below I<sub>TERM</sub>, the charger state machine enters the top-off state.

A fast-charge safety timer starts when the state machine enters fast-charge (CC) or JEITA-modified fast-charge (CC) from a non-fast-charge state. The timer continues to run through all fast-charge states regardless of JEITA status. The timer length (t<sub>FC</sub>) is programmable from 3 hours to 7 hours in 2 hour increments with CNFG\_CHG\_E.T\_FAST\_CHG[1:0]. If it is desired to charge without a safety timer, program CNFG\_CHG\_E.T\_FAST\_CHG[1:0] with 0b00 to disable the feature. If the timer expires before the fast-charge states are exited, the charger faults. See the [Fast-Charge Timer Fault State](#) section for more information.

If the charge current falls below 20% of the programmed value during fast-charge (CC), the safety timer pauses. The timer also pauses for the duration of supplement mode events. The STAT\_CHG\_B.TIME\_SUS bit indicates the status of the fast-charge safety timer. See the [Register Map](#) section for more details.

### Top-Off State

Top-off state is entered when the battery charge current falls below I<sub>TERM</sub> during the fast-charge (CV) state. I<sub>TERM</sub> is a percentage of I<sub>FAST-CHG</sub> and is programmable through CNFG\_CHG\_C.I\_TERM[1:0]. While in the top-off state, the battery charger continues to hold the battery's voltage at V<sub>FAST-CHG</sub>. A programmable top-off timer starts when the charger state machine enters the top-off state. When the timer expires, the charger enters the done state. The top-off timer value (t<sub>TO</sub>) is programmable from 0 minutes to 35 minutes with CNFG\_CHG\_C.T\_TOPOFF[2:0]. If it is desired to stop charging as soon as battery current falls below I<sub>TERM</sub>, program t<sub>TO</sub> to 0 minutes.

### Done State

The charger enters the done state when the top-off timer expires. The battery remains disconnected from the system during done. The charger restarts if the battery voltage falls more than V<sub>RESTART</sub> (150mV, typ) below the programmed V<sub>FAST-CHG</sub> value.

### Prequalification Timer Fault State

The prequalification timer fault state is entered when the battery's voltage fails to rise above V<sub>PQ</sub> in t<sub>TO</sub> (30 minutes, typ) from when the prequalification state was first entered. If a battery is too deeply discharged, damaged, or internally shorted, the prequalification timer fault state can occur. During the timer fault state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the prequalification timer fault state, toggle the charger enable (CNFG\_CHG\_B.CHG\_EN) bit or unplug and replug the external voltage source connected to CHGIN.

**Fast-Charge Timer Fault State**

The charger enters the fast-charge timer fault state if the fast-charge safety timer expires. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the fast-charge timer fault state, toggle the charger enable bit (CNFG\_CHG\_B.CHG\_EN) or unplug and replug the external voltage source connected to CHGIN.

**Battery Temperature Fault State**

If the thermistor monitoring circuit reports that the battery is either too hot or too cold to charge (as programmed by CNFG\_CHG\_A.THM\_HOT[1:0] and CNFG\_CHG\_A.THM\_COLD[1:0]), the state machine enters the battery temperature fault state. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. This state can only be entered if the thermistor is enabled (CNFG\_CHG\_F.THM\_EN = 1). Battery temperature fault state has priority over any other fault state, and can be exited when the thermistor is disabled (CNFG\_CHG\_F.THM\_EN = 0) or when the battery returns to an acceptable temperature. When this fault state is exited, the state machine returns to the last state it was in before battery temperature fault state was entered.

All active charger timers (fast-charge safety timer, prequalification timer, or top-off timer) are paused in this state. When the charger exits this state, the prequalification timer resumes while the fast-charge safety and top-off timers reset.

The STAT\_CHG\_A.THM\_DTLS[2:0] bitfield reports battery temperature status. See the [Adjustable Thermistor Temperature Monitors](#) and the [Register Map](#) sections for more information.

**JEITA-Modified States**

If the thermistor is enabled (CNFG\_CHG\_F.THM\_EN = 1), then the charger state machine is allowed to enter the JEITA-modified states. These states are entered if the charger's temperature monitors indicate that the battery temperature is either warm (greater than  $T_{WARM}$ ) or cool (lesser than  $T_{COOL}$ ). See the [Adjustable Thermistor Temperature Monitors](#) section for more information about setting the temperature thresholds.

The charger's current and voltage parameters change from  $I_{FAST-CHG}$  and  $V_{FAST-CHG}$  to  $I_{FAST-CHG\_JEITA}$  and  $V_{FAST-CHG\_JEITA}$  while in the JEITA-modified states. The JEITA modified parameters can be independently set to lower voltage and current values so that the battery can charge safely over a wide range of ambient temperatures. If the battery temperature returns to normal, or the thermistor is disabled (CNFG\_CHG\_.THM\_EN = 0), the charger exits the JEITA-modified states.

### Typical Charge Profile

A typical battery charge profile (and state progression) is illustrated in [Figure 16](#).

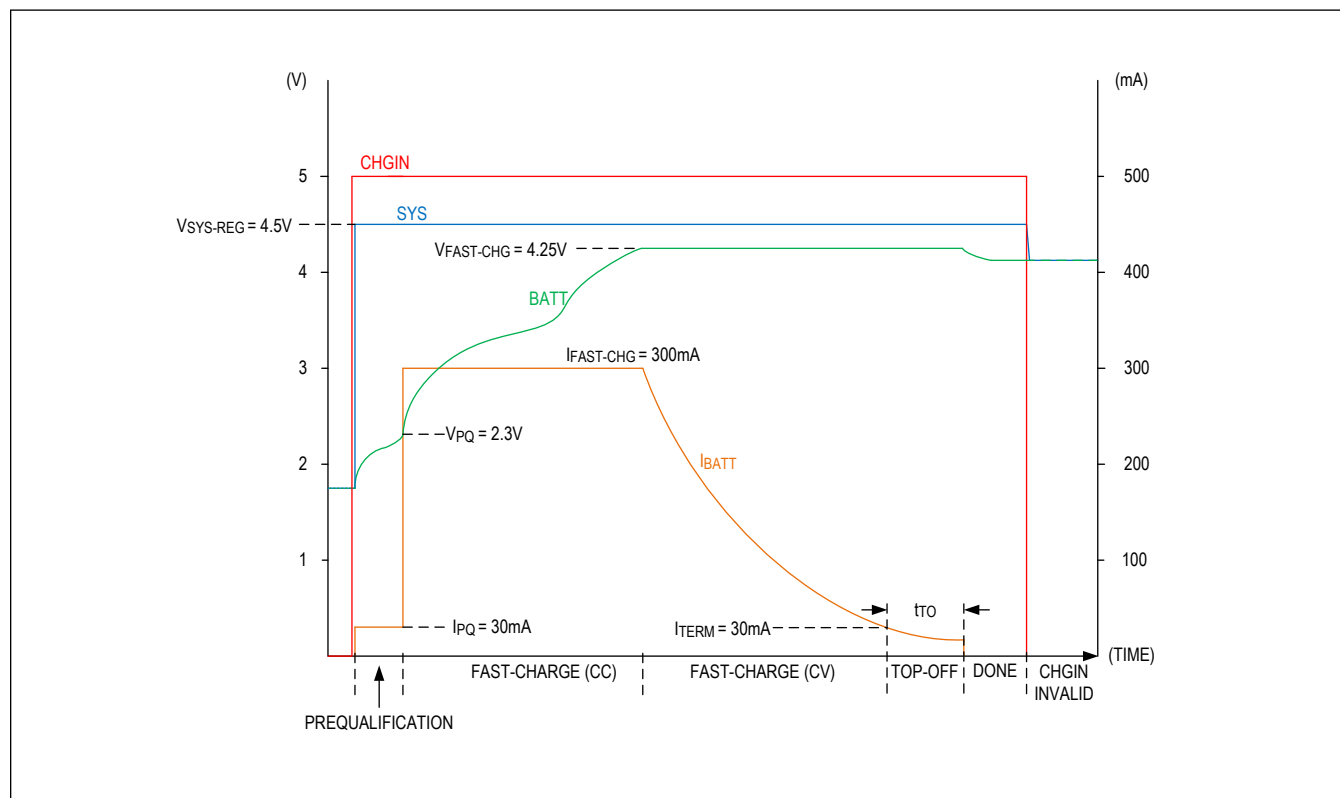


Figure 16. Example Battery Charge Profile

## Charger Applications Information

### Configuring a Valid System Voltage

The Smart Power Selector begins to regulate SYS to  $V_{\text{SYS-REG}}$  when CHGIN is connected to a valid source. To ensure the charger's accuracy specified in the [Electrical Characteristics](#) table, the system voltage must always be programmed at least 200mV above the charger's constant-voltage level ( $V_{\text{FAST-CHG}}$ ). If this condition is not met, then the charger's internal configuration logic forces  $V_{\text{FAST-CHG}}$  to reduce to satisfy the 200mV requirement. If this happens, the charger asserts the INT\_CHG.SYS\_CNFG\_I interrupt to alert the user that a configuration error has been made and that the bits in CNFG\_CHG\_G.CHG\_CV[5:0] have changed to reduce  $V_{\text{FAST-CHG}}$ .

### CHGIN/SYS/BATT Capacitor Selection

Bypass CHGIN to GND with a 4.7 $\mu$ F ceramic capacitor to minimize inductive kick caused by long cables between the DC charge source and the product/IC. Larger values increase decoupling for the linear charger, but increase inrush current from the DC charge source when the product/IC is first connected to a source through a cable/plug. If the DC charging source is an upstream USB device, limit the maximum CHGIN input capacitance based on the appropriate USB specification (typically no more than 10 $\mu$ F).

Bypass SYS to GND with a 22 $\mu$ F ceramic capacitor. This capacitor ensures stability of SYS while it is regulated from CHGIN. Larger values of SYS capacitance increase decoupling for all SYS loads. The effective value of the SYS capacitor must be greater than 4 $\mu$ F and no more than 100 $\mu$ F.

Bypass BATT to GND with a 4.7 $\mu$ F ceramic capacitor. This capacitor stabilizes the BATT voltage regulation loop. The effective value of the BATT capacitor must be greater than 1 $\mu$ F.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

### Detailed Description—Adjustable Thermistor Temperature Monitors

The optional use of a negative temperature coefficient (NTC) thermistor (thermally coupled to the battery) enables the charger to operate safely over the JEITA temperature range. When the thermistor is enabled (CNFG\_CHG\_F.THM\_EN = 1), the charger continuously monitors the voltage at the THM pin in order to sense the temperature of the battery being charged.

See [Figure 17](#) for a visual example of the following:

- If the battery temperature is higher than  $T_{COOL}$  and lower than  $T_{WARM}$ , the battery charges normally with the normal values for  $V_{FAST-CHG}$  and  $I_{FAST-CHG}$ . The charger state machine does not enter JEITA-modified states while the battery temperature is normal.
- If the battery temperature is either above  $T_{WARM}$  but below  $T_{HOT}$ , or, below  $T_{COOL}$  but above  $T_{COLD}$ , the battery charges with the JEITA-modified voltage and current values. These modified values,  $V_{FAST-CHG\_JEITA}$  and  $I_{FAST-CHG\_JEITA}$ , are programmable through CNFG\_CHG\_H.CHG\_CV\_JEITA[5:0] and CNFG\_CHG\_F.CHG\_CC\_JEITA[5:0], respectively. These values are independently programmable from the unmodified  $V_{FAST-CHG}$  and  $I_{FAST-CHG}$  values and can even be programmed to the same values if an automatic response to a warm or cool battery is not desired. The charger state machine enters JEITA-modified states while the battery temperature is outside of normal.
- If the battery temperature is either above  $T_{HOT}$  or below  $T_{COLD}$ , the charger follows the JEITA recommendation and pauses charging. The charger state machine enters battery temperature fault state while charging is paused due to extreme high or low temperatures.

The battery's temperature status is reflected by the STAT\_CHG\_A.THM\_DTLS[2:0] status bitfield. A maskable interrupt (INT\_CHG.THM\_I) signals a change in status. See the [Register Map](#) for more information. To completely disable the charger's automatic response to battery temperature, disable the feature by programming CNFG\_CHG\_F.THM\_EN = 0.

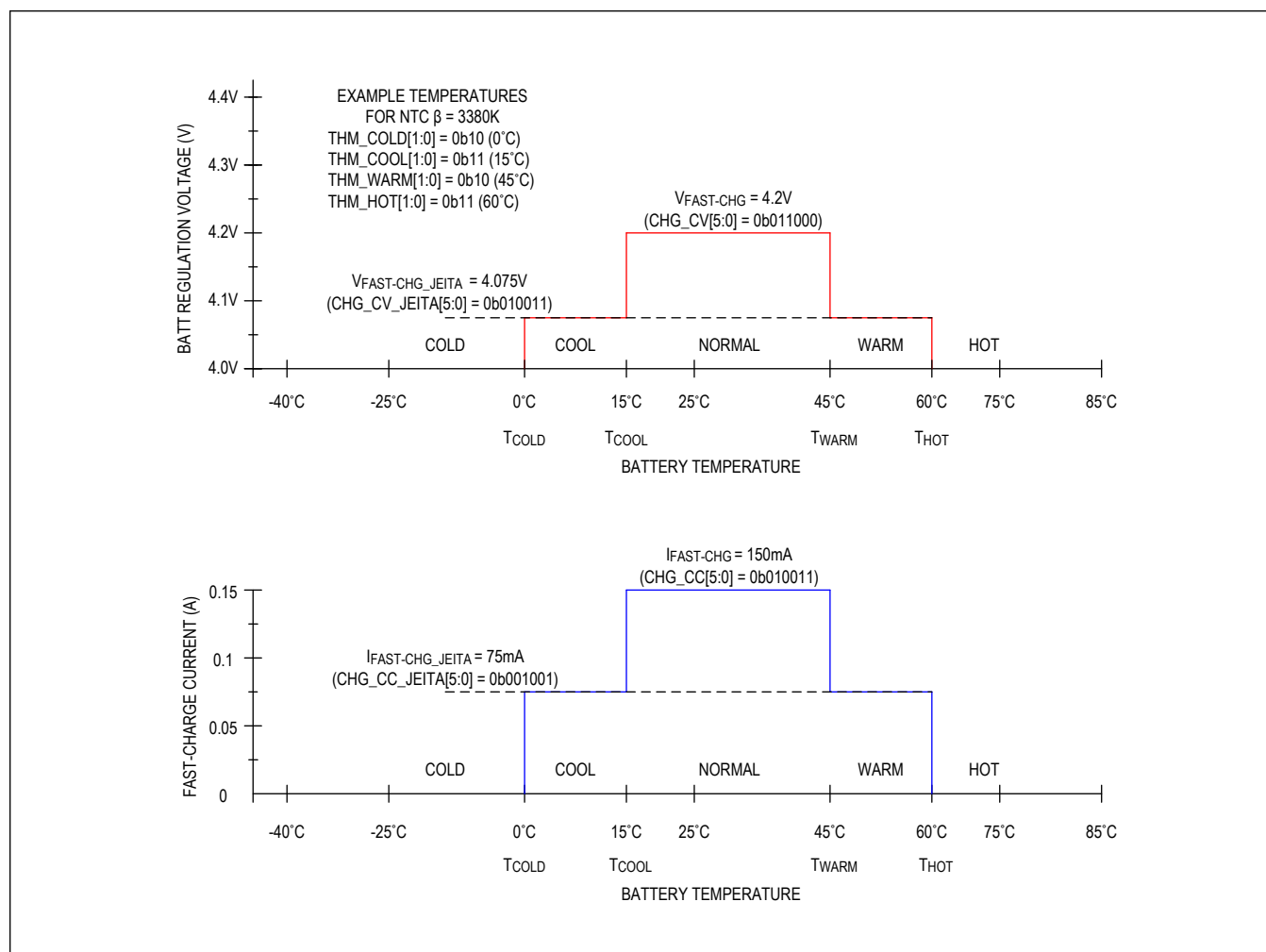


Figure 17. Safe-Charging Profile Example

The voltage thresholds corresponding to the JEITA temperature thresholds are independently programmable through CNFG\_CHG\_A.THM\_HOT[1:0], CNFG\_CHG\_A.THM\_WARM[1:0], CNFG\_CHG\_A.THM\_COOL[1:0], and CNFG\_CHG\_A.THM\_COLD[1:0]. Each threshold can be programmed to one of four voltage options spanning 15°C for an NTC beta of 3380K. See the [Configurable Temperature Thresholds](#) section and the [Register](#) for more information.

## Thermistor Bias

An external ADC can optionally perform conversions on the THM and TBIAS pins to measure the battery's temperature. An on-chip analog multiplexer is used to route these nodes to the AMUX pin. The operation of the analog multiplexer does not interfere with the charger's temperature monitoring comparators or the charger's automatic JEITA response. See the [Analog Multiplexer](#) section for more information.

The NTC thermistor's bias source (TBIAS) follows the simple operation outlined below:

- If CHGIN is valid and the thermistor is enabled (CNFG\_CHG\_F.THM\_EN = 1), the thermistor is biased, so the charger can automatically respond to battery temperature changes.
- If the analog multiplexer connects THM or TBIAS to AMUX, then the thermistor is biased, so an external ADC can perform a meaningful temperature conversion.

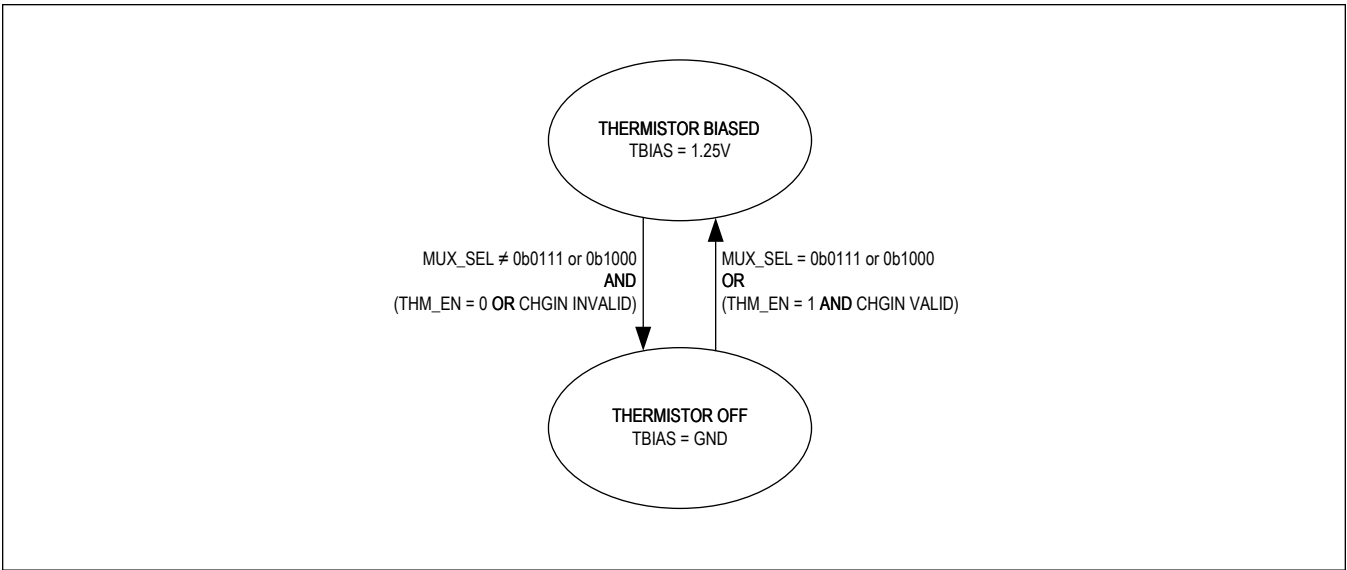


Figure 18. Thermistor Bias State Diagram

The AMUX pin is a buffered output. The operation of the analog multiplexer and external ADC does not collide with the function of the on-chip temperature monitors. Both functions may be used simultaneously with no ill effect.

### Configurable Temperature Thresholds

Temperature thresholds for different NTC thermistor beta values are listed in [Table 10](#). The largest possible programmable temperature range can be realized by using an NTC with a beta of 3380K. Using a larger beta compresses the temperature range. The trip voltage thresholds are programmable with the CNFG\_CHG\_A.THM\_HOT[1:0], CNFG\_CHG\_A.THM\_WARM[1:0], CNFG\_CHG\_A.THM\_COOL[1:0], and CNFG\_CHG\_A.THM\_COLD[1:0] bitfields. All possible programmable trip voltages are listed in [Table 10](#).

**Table 10. Trip Temperatures vs. Trip Voltages for Different NTC  $\beta$**

| TRIP VOLTAGE (V) | TRIP TEMPERATURES (°C) |       |       |       |       |       |
|------------------|------------------------|-------|-------|-------|-------|-------|
|                  | 3380K                  | 3435K | 3940K | 4050K | 4100K | 4250K |
| 1.024            | -10.0                  | -9.5  | -5.6  | -4.8  | -4.5  | -3.5  |
| 0.976            | -5.0                   | -4.6  | -1.1  | -0.5  | -0.2  | 0.6   |
| 0.923            | 0.0                    | 0.3   | 3.3   | 3.8   | 4.1   | 4.8   |
| 0.867            | 5.0                    | 5.3   | 7.7   | 8.1   | 8.3   | 8.9   |
| 0.807            | 10.0                   | 10.2  | 12.0  | 12.4  | 12.5  | 12.9  |
| 0.747            | 15.0                   | 15.1  | 16.4  | 16.6  | 16.7  | 17.0  |
| 0.511            | 35.0                   | 34.8  | 33.5  | 33.3  | 33.2  | 32.9  |
| 0.459            | 40.0                   | 39.8  | 37.8  | 37.4  | 37.3  | 36.8  |
| 0.411            | 45.0                   | 44.7  | 42.0  | 41.5  | 41.3  | 40.7  |
| 0.367            | 50.0                   | 49.6  | 46.2  | 45.6  | 45.3  | 44.6  |
| 0.327            | 55.0                   | 54.5  | 50.4  | 49.7  | 49.3  | 48.4  |
| 0.291            | 60.0                   | 59.4  | 54.6  | 53.7  | 53.3  | 52.2  |

These are theoretical values computed by a formula. Refer to the particular NTC's data sheet for more accurate measured data. In all cases, select the value of  $R_{BIAS}$  to be equal to the NTC's effective resistance at +25°C.

## Applications Information

### Using Different Thermistor $\beta$

If an NTC with a beta larger than 3380K is used and the resulting available programmable temperature range is undesirably small, then two adjusting resistors can be used to expand the temperature range.  $R_S$  and  $R_P$  can be optionally added to the NTC thermistor circuit shown in [Figure 19](#) to expand the range of programmable temperature thresholds.

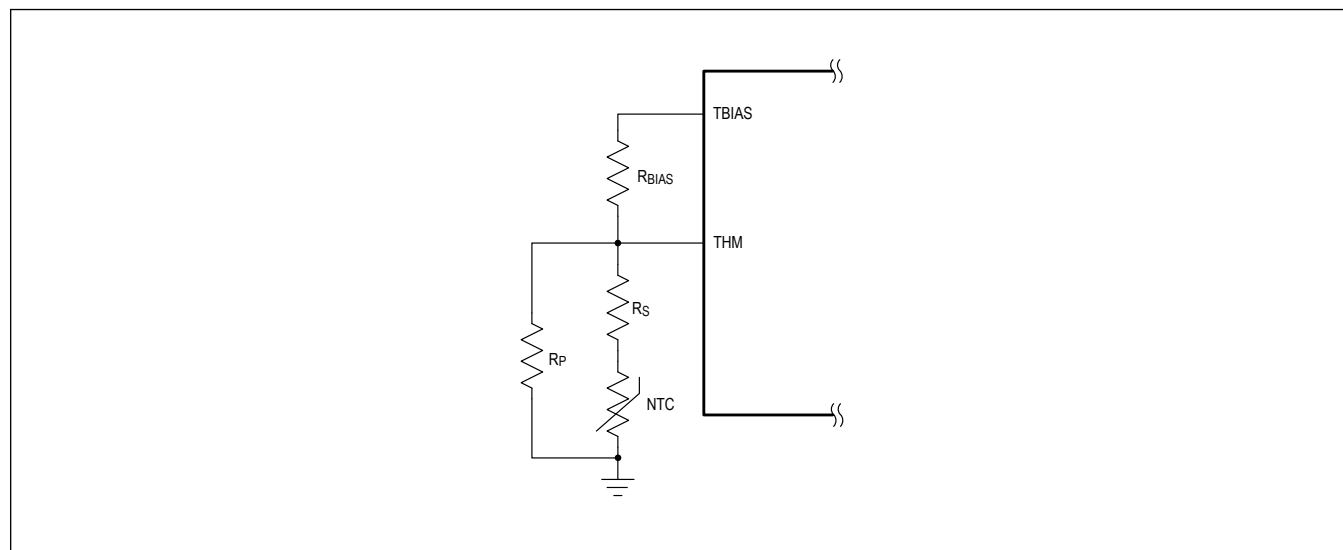


Figure 19. Thermistor Circuit with Adjusting Series and Parallel Resistors

Select values for  $R_S$  and  $R_P$  based on the information shown in [Table 11](#).

**Table 11. Example  $R_S$  and  $R_P$  Correcting Values for NTC  $\beta$  Above 3380K**

| PARAMETER                                             | UNIT | TARGET NTC CASE | CASE 1 |       | CASE 2 |        | CASE 3 |        |
|-------------------------------------------------------|------|-----------------|--------|-------|--------|--------|--------|--------|
| NTC thermistor beta                                   | K    | 3380            | 3940   |       | 4050   |        | 4250   |        |
| 25°C NTC resistance                                   | kΩ   | 10              | 10     |       | 47     |        | 100    |        |
| $R_{BIAS}$                                            |      | 10              | 10     |       | 47     |        | 100    |        |
| Adjusting parallel resistor, $R_P$                    |      | open            | open   | 200   | open   | 680    | open   | 1300   |
| Adjusting series resistor, $R_S$                      |      | short           | short  | 0.62  | short  | 3.3    | short  | 9.1    |
| $R_{NTC}$ at 1.024V <sub>COLD</sub> threshold         |      | 45.24           | 45.24  | 578.5 | 212.6  | 306.1  | 452.4  | 684.8  |
| $R_{NTC}$ at 0.867V <sub>COOL</sub> threshold         |      | 22.61           | 22.61  | 248.8 | 106.3  | 122.7  | 226.1  | 264.7  |
| $R_{NTC}$ at 0.459V <sub>WARM</sub> threshold         |      | 5.81            | 5.81   | 5.36  | 27.3   | 25.1   | 58.1   | 51.7   |
| $R_{NTC}$ at 0.291V <sub>HOT</sub> threshold          |      | 3.04            | 3.04   | 2.46  | 14.3   | 112.7  | 30.4   | 22.0   |
| $T_{ACTUAL}$ at V <sub>COLD</sub><br>(-10°C expected) | °C   | -10.03          | -5.56  | -9.96 | -4.82  | -11.14 | -3.55  | -10.46 |
| $T_{ACTUAL}$ at V <sub>COOL</sub><br>(5°C expected)   |      | 4.98            | 7.66   | 5.76  | 8.10   | 5.33   | 8.86   | 5.94   |
| $T_{ACTUAL}$ at V <sub>WARM</sub><br>(40°C expected)  |      | 40.02           | 37.79  | 39.76 | 37.43  | 39.40  | 36.82  | 39.48  |
| $T_{ACTUAL}$ at V <sub>HOT</sub><br>(60°C expected)   |      | 60.04           | 54.56  | 60.37 | 53.68  | 60.02  | 52.21  | 60.4   |

**NTC Thermistor Selection**

Popular NTC thermistor options are listed in [Table 12](#).

**Table 12. NTC Thermistors**

| MANUFACTURER | PART                    | $\beta$ -CONSTANT (25°C/50°C) | R (Ω) AT 25°C | CASE SIZE |
|--------------|-------------------------|-------------------------------|---------------|-----------|
| TDK          | NTCG063JF223HTBX        | 3380K                         | 22k           | 0201      |
| Murata       | NCP03XH103F05RL         | 3380K                         | 10k           | 0201      |
| Murata       | NCP15XH103F03RC         | 3380K                         | 10k           | 0402      |
| TDK          | NTCG103JX103DT1         | 3380K                         | 10k           | 0402      |
| Cantherm     | CMFX3435103JNT          | 3435K                         | 10k           | 0402      |
| Murata       | NCP15XV103J03RC         | 3900K                         | 10k           | 0402      |
| Panasonic    | ERT-JZEP473J            | 4050K                         | 47k           | 0201      |
| Panasonic    | ABNTC-0402-473J-4100F-T | 4100K                         | 47k           | 0402      |
| Murata       | NCP15WF104F03RC         | 4250K                         | 100k          | 0402      |

**Detailed Description—Analog Multiplexer**

An external ADC can be used to measure the chip's various signals for general functionality or on-the-fly power monitoring. The CNFG\_CHG\_I.MUX\_SEL[3:0] bitfield controls the internal analog multiplexer responsible for connecting the proper channel to the AMUX pin. Each measurable signal is listed in [Table 13](#) with its appropriate multiplexer channel.

The voltage on the AMUX pin is a buffered output that ranges from 0V to  $V_{FS}$  (1.25V, typ). The buffer has 50μA of quiescent current consumption and is only active when a channel is selected (CNFG\_CHG\_I.MUX\_SEL[3:0] ≠ 0b0000). Disable the buffer by programming CNFG\_CHG\_I.MUX\_SEL[3:0] to 0b0000 when not actively converting the voltage on AMUX. The AMUX output is high-impedance while CNFG\_CHG\_I.MUX\_SEL[3:0] is 0b0000.

[Table 13](#) shows how to translate the voltage signal on the AMUX pin to the value of the parameter being measured. See the *Electrical Characteristics* table and the [Register Map](#) for more details.

**Table 13. AMUX Signal Transfer Functions**

| SIGNAL                     | MUX_SEL[3:0] | TRANSFER FUNCTION                                                                              | FULL-SCALE SIGNAL MEANING ( $V_{AMUX} = 1.25V$ )    | ZERO-SCALE SIGNAL MEANING ( $V_{AMUX} = 0V$ ) |
|----------------------------|--------------|------------------------------------------------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------|
| CHGIN pin voltage          | 0b0001       | $V_{CHGIN} = \frac{V_{AMUX}}{G_{VCHGIN}}$                                                      | 7.5V                                                | 0V                                            |
| CHGIN pin current          | 0b0010       | $I_{CHGIN} = \frac{V_{AMUX}}{G_{ICHGIN}}$                                                      | 0.475A                                              | 0A                                            |
| BATT pin voltage           | 0b0011       | $V_{BATT} = \frac{V_{AMUX}}{G_{VBATT}}$                                                        | 4.6V                                                | 0V                                            |
| BATT pin charging current  | 0b0100       | $I_{BATT(CHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$                                  | 100% of $I_{FAST-CHG}$ (CHG_CC[5:0])                | 0% of $I_{FAST-CHG}$                          |
| BATT pin discharge current | 0b0101       | $I_{BATT(DISCHG)} = \frac{(V_{AMUX} - V_{NULL})}{(V_{FS} - V_{NULL})} \times I_{DISCHG-SCALE}$ | 100% of $I_{DISCHG-SCALE}$ (IMON_DISCHG_SCALE[3:0]) | 0% of $I_{DISCHG-SCALE}$                      |



**Table 13. AMUX Signal Transfer Functions (continued)**

| SIGNAL                          | MUX_SEL[3:0] | TRANSFER FUNCTION                     | FULL-SCALE SIGNAL MEANING<br>( $V_{AMUX} = 1.25V$ ) | ZERO-SCALE SIGNAL MEANING<br>( $V_{AMUX} = 0V$ ) |
|---------------------------------|--------------|---------------------------------------|-----------------------------------------------------|--------------------------------------------------|
| BATT pin discharge current NULL | 0b0110       | $V_{NULL} = V_{AMUX}$                 | 1.25V                                               | 0V                                               |
| THM pin voltage                 | 0b0111       | $V_{THM} = V_{AMUX}$                  | 1.25V                                               | 0V                                               |
| TBIAS pin voltage               | 0b1000       | $V_{TBIAS} = V_{AMUX}$                | 1.25V                                               | 0V                                               |
| AGND pin voltage*               | 0b1001       | $V_{AGND} = V_{AMUX}$                 | 1.25V                                               | 0V                                               |
| SYS pin voltage                 | 0b1010       | $V_{SYS} = \frac{V_{AMUX}}{G_{VSYS}}$ | 4.8V                                                | 0V                                               |

\*AGND pin voltage is accessed through a 100Ω (typ) pulldown resistor.

### Measuring Battery Current

Sampling current in the BATT pin is possible at any time or in any mode with an external ADC. For improved accuracy, the analog circuitry used for monitoring battery discharge current is different from the circuitry monitoring battery charge current. [Table 14](#) outlines how to determine the direction of battery current.

**Table 14. Battery Current Direction Decode**

| MEASUREMENT                                                                    | CHARGING OR DISCHARGING INDICATORS |                          |                             |
|--------------------------------------------------------------------------------|------------------------------------|--------------------------|-----------------------------|
|                                                                                | STAT_CHG_B.CHG                     | STAT_CHG_B.CHG_DTLS[3:0] | STAT_CHG_B.CHG_IN_DTLS[1:0] |
| Discharging Battery Current<br>(Positive Battery Terminal<br>Sourcing Current) | <i>Don't care</i>                  | <i>Don't care</i>        | 0b00<br>0b01<br>0b10        |
| Charging Battery Current<br>(Positive Battery Terminal<br>Sinking Current)     | 1                                  | 0b0001 to 0b0111         | 0b11                        |

### Method for Measuring Discharge Current

1. Program the multiplexer to switch to the discharge NULL measurement by changing CNFG\_CHG\_I.MUX\_SEL[3:0] to 0b0110. A NULL conversion must always be performed first to cancel offsets.
2. Wait the appropriate channel switching time (0.3μs, typ).
3. Convert the voltage on the AMUX pin and store as  $V_{NULL}$ .
4. Program the multiplexer to switch to the battery discharge current measurement by changing CNFG\_CHG\_I.MUX\_SEL[3:0] to 0b0101. A nonnulling conversion should be done immediately after a NULL conversion.
5. Wait the appropriate channel switching time (0.3μs, typ).
6. Convert the voltage on the AMUX pin and use the following transfer function to determine the discharge current:

$$I_{BATT(DISCHG)} = \frac{(V_{AMUX} - V_{NULL})}{(V_{FS} - V_{NULL})} \times I_{DISCHG - SCALE}$$

$V_{FS}$  is 1.25V typical.  $I_{DISCHG-SCALE}$  is programmable through `CNFG_CHG_I.IMON_DISCHG_SCALE[3:0]`. The default value is 300mA. If smaller currents are anticipated, then  $I_{DISCHG-SCALE}$  can be reduced for improved measurement accuracy.

### Method for Measuring Charge Current

1. Program the multiplexer to switch to the charge current measurement by changing `CNFG_CHG_I.MUX_SEL[3:0]` to 0b0100.
2. Wait the appropriate channel switching time (0.3μs, typ).
3. Convert the voltage on the AMUX pin and use the following transfer function to determine charging current.

$$I_{BATT(CHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$$

$V_{FS}$  is 1.25V typical.  $I_{FAST-CHG}$  the charger's fast-charge constant-current setting and is programmable through `CNFG_CHG_E.CHG_CC[5:0]`.

### Detailed Description—SIMO Buck-Boost

The device has a micropower single-inductor, multiple-output (SIMO) buck-boost DC-to-DC converter designed for applications that emphasize low supply current and small solution size. A single inductor is used to regulate three separate outputs, saving board space while delivering better total system efficiency than equivalent power solutions using one buck and linear regulators.

The buck-boost configuration utilizes the entire battery voltage range due to its ability to create output voltages that are above, below, or equal to the input voltage. Peak inductor current for each output is programmable to optimize the balance between efficiency, output ripple, EMI, PCB design, and load capability.

To further boost efficiency when the output voltage is always lower than the input, individual channels of the SIMO buck-boost converter can be configured to be in buck mode, reducing switching losses by toggling less switches compared to buck-boost mode. See the [Buck Mode](#) section for more details.

### SIMO Features and Benefits

- Three Output Channels
- Ideal for Low-Power Designs
  - Delivers 500mA at 1.8V Output in Buck Mode and 3.7V Input
  - ±3% Accurate Output Voltage
- Small Solution Size
  - Multiple Outputs from a Single 1.5μH Inductor
- Flexible and Easy to Use
  - Buck and Buck-Boost Modes of Operation
  - Glitchless Transitions Between Buck and Buck-Boost Modes
  - Programmable Peak Inductor Current
  - Programmable On-Chip Active Discharge
- Long Battery Life
  - High Efficiency, > 90% at 1.8V Output in Buck Mode and 3.7V Input
  - Higher Total System Efficiency than Buck + LDOs Solution
  - Low Quiescent Current, 1μA per Output
  - Low Input Operating Voltage, 2.7V (min)

## SIMO Detailed Block Diagram

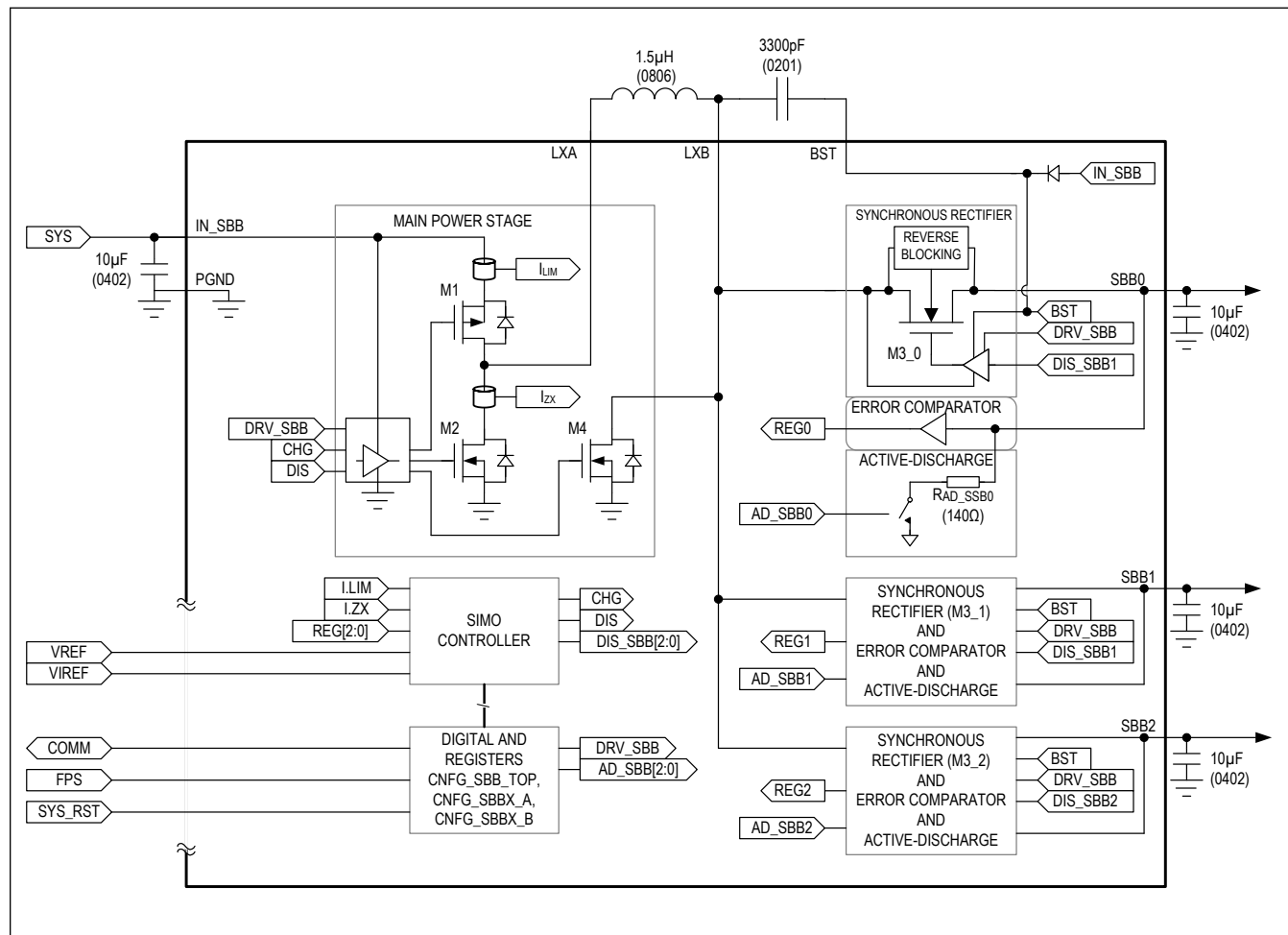


Figure 20. SIMO Detailed Block Diagram

## SIMO Control Scheme

The SIMO buck-boost is designed to service multiple outputs simultaneously. A proprietary controller ensures that all outputs get serviced in a timely manner, even while multiple outputs are contending for the energy stored in the inductor. When no regulator needs service, the state machine rests in a low-power rest state.

When the controller determines that a regulator requires service, it charges the inductor (M1 + M4) until the peak current limit is reached ( $I_{LIM} = CNFG\_SBBx\_B.IP\_SBB[1:0]$ ). The inductor energy then discharges (M2 + M3\_x) into the output until the current reaches zero ( $I_{ZX}$ ). In the event that multiple output channels need servicing at the same time, the controller ensures that no output utilizes all of the switching cycles. Instead, cycles interleave between all the outputs that are demanding service, while outputs that do not need service are skipped.

**Drive Strength**

The SIMO regulator's drive strength for its internal power MOSFETs is adjustable using the CNFG\_SBB\_TOP.DRV\_SBB[1:0] bit field. The ideal value is determined experimentally for each application. For a PCB layout comparable to the MAX77654 EV kit, 0x1 is the best setting and represents a balance between efficiency and EMI. Faster settings result in higher efficiency but generally require stricter layout rules or shielding to avoid additional EMI. Slower settings limit EMI in non-ideal settings (e.g., contained layout, antennae adjacent to the device, etc.). Change the drive strength only once during system initialization.

**SIMO Soft-Start**

The soft-start feature of the SIMO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup ( $dV/dt_{SS}$ ).

More output capacitance results in higher input current surges during startup. The following set of equations and example describes the input current surge phenomenon during startup.

In buck-boost mode, the current into the output capacitor ( $I_{CSBB}$ ) during soft-start is:

$$I_{CSBB} = C_{SBB} \frac{dV}{dt_{SS}} \quad \left( \text{Equation 1} \right)$$

where:

- $C_{SBB}$  is the capacitance on the output of the regulator
- $dV/dt_{SS}$  is the voltage change rate of the output

The input current ( $I_{IN}$ ) during soft-start is:

$$I_{IN} = \frac{(I_{CSBB} + I_{LOAD}) \frac{V_{SBBx}}{V_{IN}}}{\xi} \quad \left( \text{Equation 2} \right)$$

where:

- $I_{CSBB}$  is from the calculation above
- $I_{LOAD}$  is current consumed from the external load
- $V_{SBBx}$  is the output voltage
- $V_{IN}$  is the input voltage
- $\xi$  is the efficiency of the regulator

For example, given the following conditions, the peak input current ( $I_{IN}$ ) during soft-start is ~71mA:

Given:

- $V_{IN}$  is 3.5V
- $V_{SBB2}$  is 3.3V
- $C_{SBB2} = 10\mu F$
- $dV/dt_{SS} = 5mV/\mu s$
- $R_{LOAD2} = 330\Omega$  ( $I_{LOAD2} = 3.3V/330\Omega = 10mA$ )
- $\xi$  is 80%

Calculation:

- $I_{CSBB} = 10\mu F \times 5mV/\mu s$  (from Equation 1)
- $I_{CSBB} = 50mA$
- $I_{IN} = \frac{(50mA + 10mA) \frac{3.3V}{3.5V}}{0.85}$  (from Equation 1)
- $I_{IN} \sim 71mA$

## SIMO Registers

Each SIMO buck-boost channel has a dedicated register to program its target output voltage (CNFG\_SBBx\_A.TV\_SBBx[6:0]) and its peak current limit (CNFG\_SBBx\_B.IP\_SBBx[1:0]). Additional controls are available for enabling/disabling the active-discharge resistors (CNFG\_SBBx\_B.ADE\_SBBx), buck mode (CNFG\_SBBx\_B.OP\_MODE) as well as enabling/disabling the SIMO buck-boost channels (CNFG\_SBBx\_B.EN\_SBBx[2:0]). For a full description of bits, registers, default values, and reset conditions, see the [Register Map](#).

## SIMO Active Discharge Resistance

Each SIMO buck-boost channel has an active-discharge resistor ( $R_{AD\_SBBx}$ ) that is automatically enabled/disabled based on a CNFG\_SBBx\_B.ADE\_SBBx bit and the status of the SIMO regulator. The active discharge feature may be enabled (CNFG\_SBBx\_B.ADE\_SBBx = 1) or disabled (CNFG\_SBBx\_B.ADE\_SBBx = 0) independently for each SIMO channel. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. If the active-discharge resistor is enabled by default, then the active-discharge resistor is on whenever  $V_{SYS}$  is below  $V_{SYSUVLO}$  and above  $V_{POR}$ .

These resistors discharge the output when CNFG\_SBBx\_B.ADE\_SBBx = 1, and their respective SIMO channel is off. If the regulator is forced on through CNFG\_SBBx\_B.EN\_SBBx[2:0] = 0b110 or 0b111, then the resistors do not discharge the output even if the regulator is disabled by the main-bias.

Note that when  $V_{SYS}$  is less than 1.0V, the NMOS transistors that control the active-discharge resistors lose their gate drive and become open.

## SIMO Buck Mode

If the input voltage at IN\_SBB never falls below the output voltage of one or more SIMO converter channels, individual channels can be configured to be in buck mode with the CNFG\_SBBx\_B.OP\_MODE bit. In buck mode, when an output needs service, switch M3\_x remains closed and M4 remains open (see [Figure 20](#)). Only M1 and M2 are toggled as in a traditional buck converter. Efficiency is boosted due to three major factors:

- Reduced switching loss: Buck mode toggles only two switches versus the four in buck-boost mode. Therefore, there are less switching events during which power is consumed.
- Lower inductor core losses: Inductor current changes from 0A to peak current. The larger the change in current the inductor experiences, the more energy is lost in the inductor core in the form of heat. In buck mode, the peak current can be reduced since less inductor current is needed to support a load. Less inductor current is needed because of direct energy transfer. Direct energy transfer occurs while the inductor is charged, when the input (IN\_SBB) is connected directly to the output (SBBx) through the inductor. Therefore, the input not only provides energy to charge the inductor, energy is also supplied to the output capacitor and load devices. Therefore, less current is needed to charge the inductor, which is used to charge the output capacitor in the next switching state.
- Less frequent charging cycles: In buck mode, the inductor is constantly connected to the serviced output during a switching cycle. In comparison, in buck-boost mode, the inductor is connected to the serviced output only when the inductor discharges. Thus, with the same peak inductor current limit, buck mode is capable of supplying higher load current than buck-boost mode. In addition, with the same load current and peak current limit, the switching frequency can be reduced with buck mode.

Maintain a minimum headroom of 0.7V between IN\_SBB and SBBx in buck mode because inductor charge time ( $dt = L \times I_{P\_SBBx} / (V_{IN\_SBB} - V_{SBBx})$ ) increases as the difference between the IN\_SBB and SBBx voltages shrinks. As the inductor current takes longer to reach its peak, the output voltage may take too long to reach its target voltage, and the MAX77654 may trigger a fault flag.

## Applications Information

### SIMO Available Output Current

The available output current on a given SIMO channel is a function of the input voltage, output voltage, the peak current limit setting, and the output current of the other SIMO channels. Maxim offers a calculator (see the [Support Material](#) section) that outlines the available capacity for specific conditions. [Table 15](#) is an extraction from the calculator.

**Table 15. SIMO Available Output Current for Common Applications**

| PARAMETERS          | EXAMPLE 1     | EXAMPLE 2    | EXAMPLE 3       | EXAMPLE 4       |
|---------------------|---------------|--------------|-----------------|-----------------|
| V <sub>IN_MIN</sub> | 2.7V          | 2.7V         | 3.2V            | 3.4V            |
| R <sub>L_DCR</sub>  | 0.1Ω          | 0.1Ω         | 0.1Ω            | 0.12Ω           |
| SBB0                | 1.0V at 100mA | 1.0V at 80mA | 1.2V at 50mA    | 1.2V at 20mA    |
| SBB1                | 1.2V at 75mA  | 1.2V at 50mA | 1.8V at 100mA   | 1.8V at 80mA    |
| SBB2                | 1.8V at 50mA  | 1.8V at 40mA | 3.3V at 30mA    | 3.3V at 10mA    |
| Operating Mode      | Buck          | Buck         | Buck/Buck-Boost | Buck/Buck-Boost |
| I <sub>P_SBB0</sub> | 0.5A          | 0.5A         | 0.5A            | 0.5A            |
| I <sub>P_SBB1</sub> | 0.75A         | 0.5A         | 0.5A            | 0.5A            |
| I <sub>P_SBB2</sub> | 0.5A          | 0.5A         | 0.75A           | 0.5A            |
| Utilized Capacity   | 78%           | 67%          | 76%             | 47%             |

\*ESR<sub>C\_IN</sub> = ESR<sub>C\_OUT</sub> = 5mΩ, L = 1.5μH

### Inductor Selection

Choose an inductance from 1.0μH to 2.2μH; 1.5μH inductors work best for most designs. Larger inductances transfer more energy to the output for each cycle and typically result in larger output voltage ripple and better efficiency. See the [Output Capacitor Selection](#) section for more information on how to size your output capacitor in order to control ripple.

Choose the inductor saturation current to be greater than or equal to the maximum peak current limit setting that is used for all of the SIMO buck-boost channels (I<sub>P\_SBBx</sub>). For example, if SBB0 is set for 0.5A, SBB1 is set for 0.75A, and SBB2 is set for 1.0A, then choose the saturation current to be greater than or equal to 1.0A.

Choose the RMS current rating of the inductor (typically the current at which the temperature rises appreciably) based on the expected load currents for the system. For systems where the expected load currents are not well known, be conservative and choose the RMS current to be greater than or equal to half the higher maximum peak current limit setting [ $I_{RMS} \geq \text{MAX}(I_{P\_SBB0}, I_{P\_SBB1}, I_{P\_SBB2})/\sqrt{3}$ ]. This is a conservative choice because the SIMO buck-boost regulator implements a discontinuous conduction mode (DCM) control scheme, which returns the inductor current to zero each cycle.

Consider the DC-resistance (DCR), AC-resistance (ACR), and solution size of the inductor. Typically, smaller sized inductors have larger DC-resistance and larger AC-resistance that reduces efficiency and the available output current.

Note that many inductor manufacturers have inductor families which contain different versions of core material in order to balance trade-offs between DCR, ACR (i.e., core losses), and component cost. For this SIMO regulator, inductors with the lowest ACR in the 1.0MHz to 2.0MHz region tend to provide the best efficiency.

## Input Capacitor Selection

Choose the input bypass capacitance ( $C_{IN\_SBB}$ ) to be 10 $\mu$ F. Larger values of  $C_{IN\_SBB}$  improve the decoupling for the SIMO regulator.

$C_{IN\_SBB}$  reduces the current peaks drawn from the battery or input power source during SIMO regulator operation and reduces switching noise in the system. The ESR/ESL of the input capacitor should be very low (i.e.,  $ESR \leq 5m\Omega$  and  $ESL \leq 500pH$ ) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

To fully utilize the available input voltage range of the SIMO (5.5V, max), use a capacitor with a voltage rating of 6.3V at minimum.

## Boost Capacitor Selection

Choose the boost capacitance ( $C_{BST}$ ) to be 3.3nF. Smaller values of  $C_{BST}$  ( $< 1nF$ ) result in insufficient gate drive for M3. Larger values of  $C_{BST}$  ( $> 10nF$ ) have the potential to degrade the startup performance. Ceramic capacitors with 0201 or 0402 case size are recommended.

## Output Capacitor Selection

Choose each output bypass capacitance ( $C_{SBBx}$ ) based on the target output voltage ripple ( $\Delta V_{SBBx}$ ): typical values are 22 $\mu$ F. Larger values of  $C_{SBBx}$  improve the output voltage ripple but increase the input surge currents during soft-start and output voltage changes. The output voltage ripple is a function of the inductance (L), the output voltage ( $V_{SBBx}$ ), and the peak current limit setting ( $I_{P\_SBBx}$ ). See Equation 3 to estimate required, effective capacitance.

$$C_{SBBx} = \frac{I_{P\_SBBx}^2 * L}{2 * V_{SBBx} * \Delta V_{SBBx}} \text{ (Equation 3)}$$

Maxim also offers a calculator (see the [Support Materials](#) section) to aid in the selection of the output capacitance. Note that most designs concern themselves with having enough capacitance on the output but there is also a maximum capacitance limitation that is calculated within the SIMO calculator; take care not to exceed the maximum capacitance.

$C_{SBBx}$  is required to keep the output voltage ripple small. The impedance of the output capacitor (ESR, ESL) should be very low (i.e.,  $ESR \leq 5m\Omega$  and  $ESL \leq 500pH$ ) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with increased DC bias voltage. This effect is more pronounced as capacitor case sizes decrease. Due to this characteristic, it is possible for an 0603 case size capacitor to perform well, while an 0402 case size capacitor of the same value performs poorly. The SIMO regulator is stable with low output capacitance (1 $\mu$ F) but the output voltage ripple would be large; consider the effective output capacitance value after initial tolerance, bias voltage, aging, and temperature derating.

**Example Component Selection**

Pick input/output capacitors and the inductor for the given requirements:

- $V_{IN\_SBB}$ , typical = 3.7V

**Table 16. Design Requirements**

|                        | SBB0 | SBB1 | SBB2 |
|------------------------|------|------|------|
| Output Voltage         | 3.3V | 1.8V | 1.2V |
| Maximum Load Current   | 50mA | 60mA | 80mA |
| Maximum Voltage Ripple | 50mV | 30mV | 30mV |

**Inductor, Peak Current Limit, and Input Capacitor**

For the best efficiency, a 2.2 $\mu$ H inductor is chosen. For this example, assume the DFE201612E-2R2M inductor from Murata is used. This particular inductor has 116m $\Omega$  of DCR.

Since the load current is low, first choose the inductor current peak to be 0.333A for all outputs. Next, enter these values into Maxim's SIMO calculator as mentioned previously.

| Symbol                | Value    | Unit         | Per Channel Symbol  | Per Channel Value |       |       | Unit       |
|-----------------------|----------|--------------|---------------------|-------------------|-------|-------|------------|
|                       |          |              |                     | SBB0              | SBB1  | SBB2  |            |
| Input Section         |          |              |                     |                   |       |       |            |
| $V_{IN}$              | 3.7000   | V            | $V_{OUT}$           | 3.300             | 1.800 | 1.200 | V          |
| L                     | 2.20     | $\mu$ H      | $I_{OUT}$           | 50.0              | 60.0  | 80.0  | mA         |
| $r_{L\_DCR}$          | 116      | m $\Omega$   | $C_{OUT}$ Effective | 8.1               | 13.8  | 16.8  | $\mu$ F    |
|                       |          |              | $r_{C\_ESR}$        | 5                 | 5     | 5     | m $\Omega$ |
| $T_{OPERATING}$       | 25       | $^{\circ}$ C | Channel Enabled?    | Yes               | Yes   | Yes   |            |
| Other Inputs          |          |              |                     |                   |       |       |            |
| Device                | MAX77654 |              | $I_{L\_Peak}$       | 0.333             | 0.333 | 0.333 | A          |
|                       |          |              | Operating Mode      | Buck-Boost        | Buck  | Buck  |            |
| Calculation Results   |          |              |                     |                   |       |       |            |
| Inductor Utilization  |          |              |                     |                   |       |       |            |
| Total Utilization     | 141.5%   |              | Utilization         | 57.7%             | 35.7% | 48.1% |            |
| Current and Power     |          |              |                     |                   |       |       |            |
| Output Voltage Ripple |          |              |                     |                   |       |       |            |

**Figure 21. Component Selection—High Utilization**

As shown in [Figure 21](#), the utilization is over 100%, which leads to output voltage droop. To lower utilization, increase the inductor peak current limits. For this example, 1A is used for SBB0 and 0.5A for SBB1 and SBB2. [Figure 22](#) shows utilization less than 80%. Using 0.5A for the inductor peak current limit has the added benefit of increased efficiency.



| Symbol                 | Value    | Unit | Per Channel Symbol                                                                                               | Per Channel Value |       |       | Unit |
|------------------------|----------|------|------------------------------------------------------------------------------------------------------------------|-------------------|-------|-------|------|
|                        |          |      |                                                                                                                  | SBB0              | SBB1  | SBB2  |      |
| Input Section          |          |      |                                                                                                                  |                   |       |       |      |
| V <sub>IN</sub>        | 3.7000   | V    | V <sub>OUT</sub><br><br>I <sub>OUT</sub><br>C <sub>OUT</sub> Effective<br>r <sub>C_ESR</sub><br>Channel Enabled? | 3.300             | 1.800 | 1.200 | V    |
| L                      | 2.20     | μH   |                                                                                                                  | 50.0              | 60.0  | 80.0  | mA   |
| r <sub>L_DCR</sub>     | 116      | mΩ   |                                                                                                                  | 8.1               | 13.8  | 16.8  | μF   |
|                        |          |      |                                                                                                                  | 5                 | 5     | 5     | mΩ   |
| T <sub>OPERATING</sub> | 25       | °C   |                                                                                                                  | Yes               | Yes   | Yes   |      |
| Other Inputs           |          |      |                                                                                                                  |                   |       |       |      |
| Device                 | MAX77654 |      | I <sub>L_Peak</sub>                                                                                              | 1.000             | 0.500 | 0.500 | A    |
|                        |          |      | Operating Mode                                                                                                   | Buck-Boost        | Buck  | Buck  |      |
| Calculation Results    |          |      |                                                                                                                  |                   |       |       |      |
| Inductor Utilization   |          |      |                                                                                                                  |                   |       |       |      |
| Total Utilization      | 75.6%    |      | Utilization                                                                                                      | 19.9%             | 23.7% | 32.0% |      |
| Current and Power      |          |      |                                                                                                                  |                   |       |       |      |
| Output Voltage Ripple  |          |      |                                                                                                                  |                   |       |       |      |

Figure 22. Component Selection—Final Current Peak Limits

To support the selected peak currents, choose 22μF for the input capacitor.

### Output Capacitors

Using Equation 3 and the selected inductor current peak limits, the minimum output capacitances required are:

$$C_{SBB0\_min} = \frac{I_{P\_SBB0}^2 \times L}{2 \times V_{SBB0} \times \Delta V_{SBB0}} = \frac{1^2 \times 2.2 \times 10^{-6} \text{ A}^2 \times \text{H}}{2 \times 3.3 \times 0.05 \text{ V}^2} = 6.67 \mu\text{F}$$

$$C_{SBB1\_min} = \frac{I_{P\_SBB1}^2 \times L}{2 \times V_{SBB1} \times \Delta V_{SBB1}} = \frac{0.5^2 \times 2.2 \times 10^{-6} \text{ A}^2 \times \text{H}}{2 \times 1.8 \times 0.03 \text{ V}^2} = 5.09 \mu\text{F}$$

$$C_{SBB2\_min} = \frac{I_{P\_SBB2}^2 \times L}{2 \times V_{SBB2} \times \Delta V_{SBB2}} = \frac{0.5^2 \times 2.2 \times 10^{-6} \text{ A}^2 \times \text{H}}{2 \times 1.2 \times 0.03 \text{ V}^2} = 7.64 \mu\text{F}$$

For this example, the 22μF GRM188R61A226ME15 is chosen for all three outputs. The effective capacitance after derating is the following:

$$C_{SBB0} = 8.113 \mu\text{F}$$

$$C_{SBB1} = 13.828 \mu\text{F}$$

$$C_{SBB2} = 16.793 \mu\text{F}$$

Go back to the calculator and enter the capacitance for each channel. [Figure 23](#) shows the expected ripples, which fit the requirements.

| Symbol                | Value    | Unit         | Per Channel Symbol          | Per Channel Value |       |       | Unit             |
|-----------------------|----------|--------------|-----------------------------|-------------------|-------|-------|------------------|
|                       |          |              |                             | SBB0              | SBB1  | SBB2  |                  |
| Input Section         |          |              |                             |                   |       |       |                  |
| $V_{IN}$              | 3.7000   | V            | $V_{OUT}$                   | 3.300             | 1.800 | 1.200 | V                |
| $L$                   | 2.20     | $\mu$ H      | $I_{OUT}$                   | 50.0              | 60.0  | 80.0  | mA               |
| $r_{L\_DCR}$          | 116      | m $\Omega$   | $C_{OUT}$ Effective         | 8.1               | 13.8  | 16.8  | $\mu$ F          |
|                       |          |              | $r_{C\_ESR}$                | 5                 | 5     | 5     | m $\Omega$       |
| $T_{OPERATING}$       | 25       | $^{\circ}$ C | Channel Enabled?            | Yes               | Yes   | Yes   |                  |
| Other Inputs          |          |              |                             |                   |       |       |                  |
| Device                | MAX77654 |              | $I_{L\_Peak}$               | 1.000             | 0.500 | 0.500 | A                |
|                       |          |              | Operating Mode              | Buck-Boost        | Buck  | Buck  |                  |
| Calculation Results   |          |              |                             |                   |       |       |                  |
| Inductor Utilization  |          |              |                             |                   |       |       |                  |
| Total Utilization     | 75.6%    |              | Utilization                 | 19.9%             | 23.7% | 32.0% |                  |
| Current and Power     |          |              |                             |                   |       |       |                  |
| Output Voltage Ripple |          |              |                             |                   |       |       |                  |
|                       |          |              | $V_{OUT\_ripple\_no\_load}$ | 42.5              | 23.8  | 21.0  | mV <sub>pp</sub> |
|                       |          |              |                             | 1.3%              | 1.3%  | 1.8%  |                  |
|                       |          |              | $V_{OUT\_ripple\_w\_load}$  | 35.3              | 19.4  | 15.7  | mV <sub>pp</sub> |
|                       |          |              |                             | 1.1%              | 1.1%  | 1.3%  |                  |

Figure 23. Component Selection—Expected Ripple

**Summary**

- $L = 2.2\mu$ H
- $C_{IN\_SBB} = 22\mu$ F
- Total Switching Utilization = 76%

**Table 17. Summary of Design for Component Selection Example**

|                      | SBB0       | SBB1       | SBB2       |
|----------------------|------------|------------|------------|
| $I_{P\_SBBx}$        | 1A         | 0.5A       | 0.5A       |
| $C_{SBBx}$ (nominal) | 22 $\mu$ F | 22 $\mu$ F | 22 $\mu$ F |
| $\Delta V_{SBBx}$    | 35.3mV     | 19.4mV     | 15.7mV     |

Real applications should also consider the minimum input voltage since the battery discharges. The following is a summary using the same components but an input voltage of 3.0V instead. The switching utilization increased to 77.1%, still below 80%.

- $L = 2.2\mu$ H
- $C_{IN\_SBB} = 22\mu$ F
- Total Switching Utilization = 77.1%

**Table 18. Summary of Design with Lower Input Voltage**

|                             | SBB0   | SBB1   | SBB2   |
|-----------------------------|--------|--------|--------|
| I <sub>P_SBBx</sub>         | 1A     | 0.5A   | 0.5A   |
| C <sub>SBBx</sub> (nominal) | 22μF   | 22μF   | 22μF   |
| ΔV <sub>SBBx</sub>          | 35.3mV | 26.9mV | 18.6mV |

**SIMO Switching Frequency**

The SIMO buck-boost regulator uses a pulse frequency modulation (PFM) control scheme. The switching frequency for each output is a function of the operating mode, input voltage, output voltage, load current, and inductance. Output capacitance is a minor factor in SIMO switching frequency. Maxim offers a SIMO calculator (see the [Support Material](#) section) to estimate expected switching frequency.

At no load, switching frequencies can be as low as 10Hz. For the 3.7V input to 1.2V output channel from the [Example Component Selection](#) section, the switching frequency is about 327kHz.

[Table 19](#) lists how different factors increase or decrease switching frequency.

**Table 19. Switching Frequency Control**

| FACTOR                      | INCREASING FREQUENCY | DECREASING FREQUENCY |
|-----------------------------|----------------------|----------------------|
| Inductor Current Peak Limit | Lower peak limit     | Higher peak limit    |
| Operating Mode              | Buck-boost mode      | Buck mode            |
| Inductor                    | Decrease inductance  | Increase inductance  |
| Output Capacitor            | Decrease capacitance | Increase capacitance |
| Input Voltage               | Higher voltage       | Lower voltage        |
| Output Voltage              | Higher voltage       | Lower voltage        |
| Load Current                | Higher current       | Lower current        |

**Unused Outputs**

Do not leave unused outputs unconnected. If an output left unconnected is accidentally enabled, the charged inductor experiences an open circuit, and the output voltage soars above the absolute maximum rating, damaging the device. If an output is not used, do one of the following:

1. Disable the output (CNFG\_SBBx\_B.EN\_SBBx[2:0] = 0x4 or 0x5) and connect the output to ground. If an unused output is default enabled or can be accidentally enabled, do one of the following recommendations instead.
2. Bypass the unused output with a 1μF capacitor to ground.
3. Connect the unused output to IN\_SBB or a different output channel if the unused output is programmed to a lower voltage. Since the output voltage is higher than the unused output, the regulator does not service the unused output even if it is unintentionally enabled.
  1. Note that some OTP options have the active-discharge resistors enabled by default. Connecting an unused output to IN\_SBB is not recommended if the active discharge is enabled by default. If connecting the unused output to a different channel, disable the active-discharge resistor (CNFG\_SBBx\_B.ADE\_SBBx = 0) of the unused channel.

## PCB Layout Guide

### Capacitors

Place decoupling capacitors as close as possible to the IC such that connections from capacitor pads to pin and from capacitor pads to ground pins are short. Keeping the connections short lowers parasitic inductance and resistance, improving performance and shrinking the physical size of hot loops.

If connections to the capacitors are through vias, use multiple vias to minimize parasitics. Also, connect loads to the capacitor pads rather than the device pins.

Most critical are the capacitors for the switching regulator: input capacitor at IN\_SBB and output capacitors at SBBx.

### Input Capacitor at IN\_SBB

Minimize the parasitic inductance from PGND to input capacitor to IN\_SBB to reduce ringing on the LXA voltage.

### Output Capacitors at SBBx

The output capacitors experience large changes in current as the regulator charges (buck mode) and discharges (both modes) the inductor. In buck mode, the capacitor current ramps up at the same rate as mentioned in the previous section. In buck-boost mode, the capacitor current ramps up very quickly. In both modes, the capacitor current ramps down at a rate of  $\frac{dI_{C\_SBBx}}{dt} = \frac{V_{SBBx}}{L}$  from inductor peak current. Since the ramp down can occur in less than 1μs, and the current increases rapidly for buck-boost mode, minimize parasitic inductance from SBBx to output capacitor to PGND.

### Inductor

Keep the inductor close to the IC to reduce trace resistance; however, prioritize any regulator input/output capacitors over the inductor. Use the appropriate trace width from LXA to inductor to LXB to support the peak inductor current. Likewise, if there are vias in the path, use an appropriate amount of vias to support the peak current.

### Ground Connections

As the switching regulator charges and discharges the inductor, current flows from PGND to the input capacitor ground, from output capacitor ground to PGND, or from output capacitor ground to input capacitor ground. Therefore, use a wide, continuous copper plane to connect PGND to the capacitor grounds.

When connecting the GND and PGND pins together, ensure noise from the power ground does not enter the analog ground (where GND is connected). For example, assuming the ground pins are connected through a solid ground plane on an internal layer, one via connecting GND to the internal ground plane may be sufficient to protect GND from most of the noise in the power-ground plane. Likewise, if there are other higher current or noisy circuitry near this device, avoid connecting the GND pin directly to their grounds.

For more guidelines on proper grounding, visit: <https://www.maximintegrated.com/en/design/partners-and-technology/design-technology/ground-layout-board-designers.html>.

## Example PCB Layout

Figure 24 shows an example layout of the top layer.

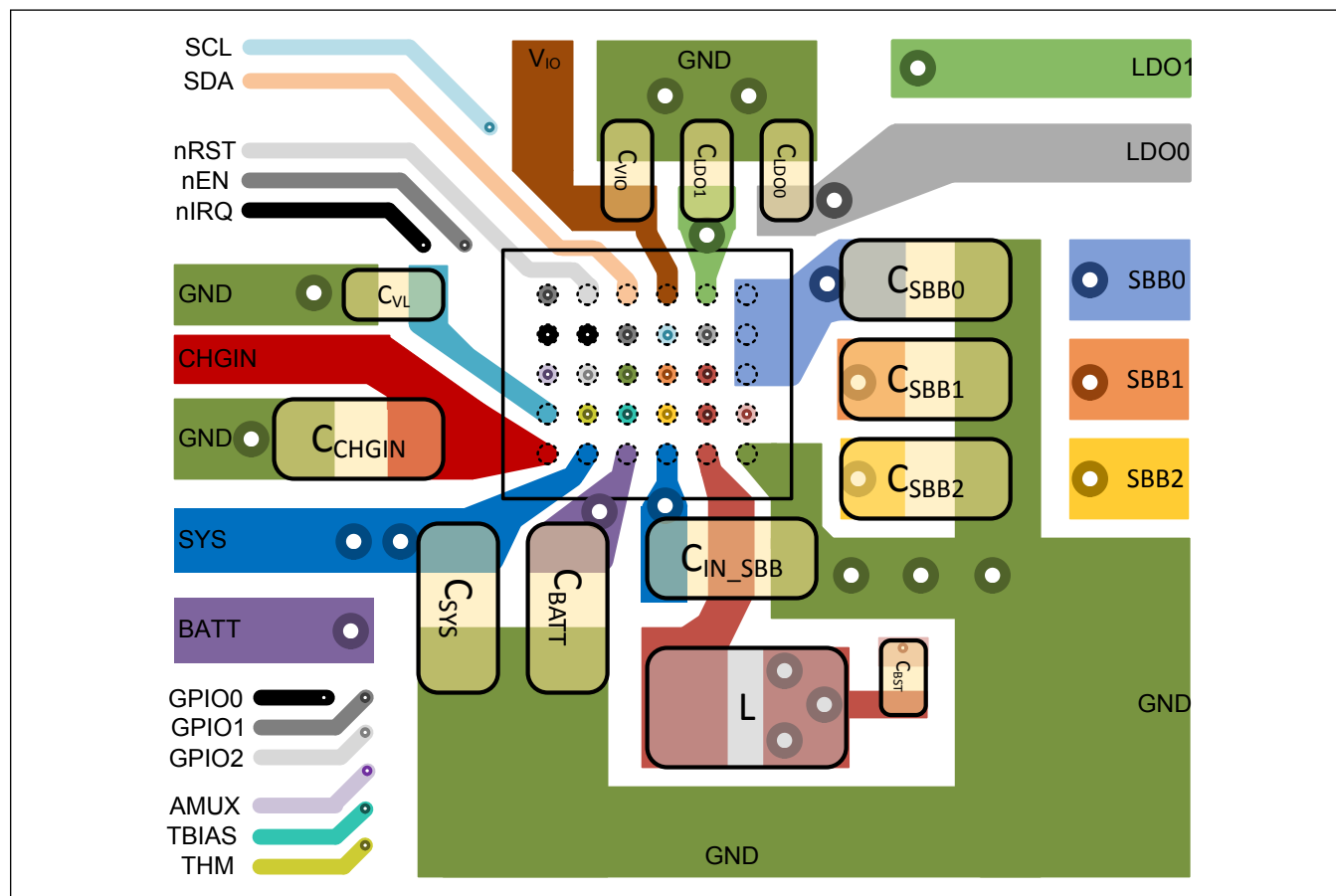


Figure 24. PCB Top-Layer and Component Placement Example

## Detailed Description—Low Dropout Linear Regulator (LDO)/Load Switch (LSW)

The device includes two on-chip low-dropout linear regulators (LDO0/1) that can also be configured as load switches. These LDOs are optimized to have low-quiescent current. The input voltage range ( $V_{IN\_LDOx}$ ) allows it to be powered directly from the main energy source such as a Li-Poly battery or from an intermediate regulator. Each linear regulator delivers up to 100mA.

### Features and Benefits

- 2x 100mA LDO
- LDO Input Voltage Range: 1.71V to 5.5V
- LSW Input Voltage Range: 1.3V to 5.5V
- Adjustable Output Voltage
- 100mV Maximum Dropout Voltage at ECT Conditions
- Programmable On-Chip Active Discharge

## LDO/LSW Simplified Block Diagram

Each LDO/LSW block has one input (IN\_LDOx) and one output (LDOx) and several ports that exchange information with the rest of the device (V<sub>REF</sub>, EN\_LDOx, ADE\_LDOx). V<sub>REF</sub> comes from the main bias circuits. CNFG\_LDOx\_B.EN\_LDOx and CNFG\_LDOx\_B.ADE\_LDOx are register bits for controlling the enable and active-discharge feature, respectively. See the [Register Map](#) for more information.

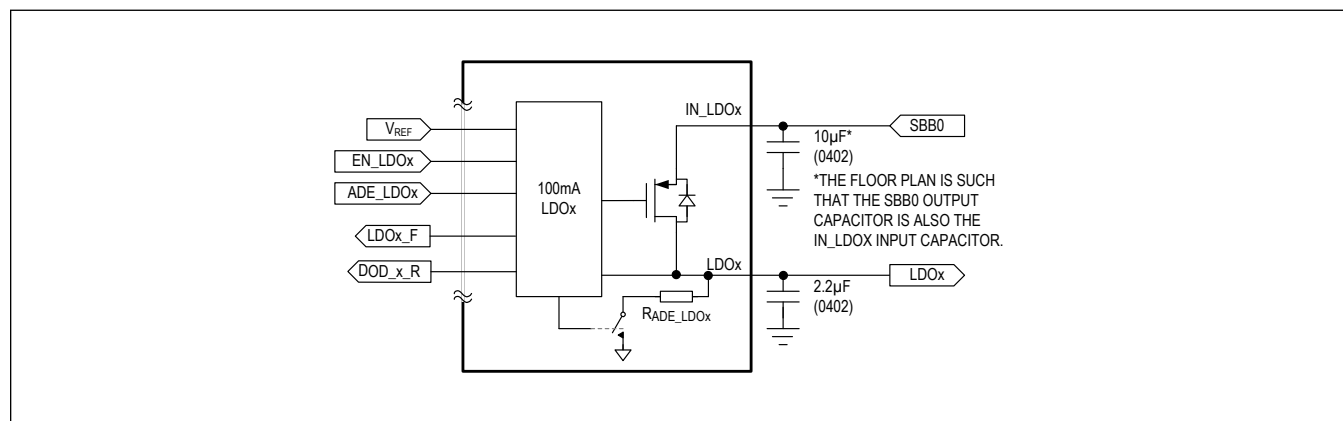


Figure 25. LDO Simplified Block Diagram

## LDO/LSW Active-Discharge Resistor

Each LDO/LSW block has an active-discharge resistor (R<sub>AD\_LDOx</sub>) that is enabled if CNFG\_LDO\_B.ADE\_LDOx = 1 and LDOx is disabled. Enabling the active discharge feature helps ensure a complete and timely power down of the resource. During power up, if V<sub>sys</sub> > V<sub>POR</sub> and CNFG\_LDO\_B.ADE\_LDOx = 1, the active-discharge resistor is enabled.

## LDO/LSW Soft-Start

The soft-start feature limits inrush current during startup, and is achieved by limiting the slew rate of the output voltage during startup (dV<sub>OUT\_LDOx</sub>/dt<sub>SS</sub>).

More output capacitance results in higher input current surges during startup. The equation and example describes the input current surge phenomenon during startup.

The input current (I<sub>IN\_LDOx</sub>) during soft-start is:

$$I_{IN\_LDOx} = C_{LDOx} \frac{dV_{OUT\_LDOx}}{dt_{SS}} + I_{OUT\_LDOx}$$

where:

- C<sub>LDOx</sub> is the capacitance on the output of the regulator
- dV<sub>OUT\_LDOx</sub>/dt<sub>SS</sub> is the voltage change rate of the output

For example, given the following conditions, the input current (I<sub>IN\_LDOx</sub>) during soft start is 13.08mA:

Given:

- C<sub>LDOx</sub> = 2.2µF
- dV<sub>OUT\_LDOx</sub>/dt<sub>SS</sub> = 1.4mV/µs
- LDOx programmed to 1.85V
- R<sub>LDOx</sub> = 185Ω (I<sub>OUT\_LDOx</sub> = 1.85V/185Ω = 10mA)

Calculation:

- I<sub>IN</sub> = 2.2µF × 1.4mV/µs + 10mA
- I<sub>IN</sub> = 13.08mA

## Load Switch Configuration

Both LDO0 and LDO1 can be configured as load switches with the CNFG\_LDOx\_B.LDOx\_MD bit. As shown in [Figure 26](#), the transition from LDO to LSW mode is controlled by a defined slew rate until dropout is detected. Once dropout is detected, the load switch is fully closed and the dropout interrupt flag (INT\_GLBL.DODx\_R) is set.

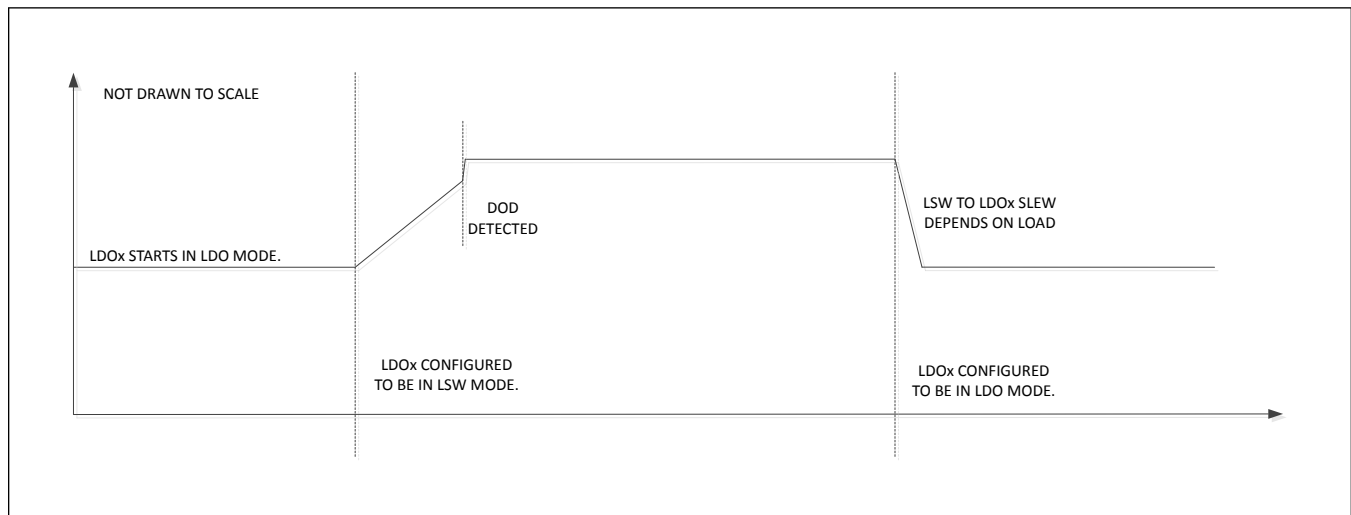


Figure 26. LDO to LSW Transition Waveform

## Applications Information

### Input Capacitor Selection

Make sure the input bypass capacitance ( $C_{IN\_LDOx}$ ) is at least  $2.2\mu F$ . Larger values of  $C_{IN\_LDOx}$  improve the decoupling for LDOx. The floor plan of the device is such that SBB0 is adjacent to IN\_LDOx and if the SIMO channel 0 output powers the input of LDOx, then its output capacitor ( $C_{SBB0}$ ) can also serve as  $C_{IN\_LDOx}$  such that only one capacitor is required.

$C_{IN\_LDOx}$  reduces the current peaks drawn from the battery or input power source during operation. The impedance of the input capacitor (ESR, ESL) should be very low (i.e.,  $ESR \leq 50m\Omega$  and  $ESL \leq 5nH$ ) for frequencies up to 0.5MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

### Output Capacitor Selection

For both LDO and LSW modes, choose the output bypass capacitance ( $C_{LDOx}$ ) to be  $1\mu F$ .

In LDO mode, larger values of  $C_{LDOx}$  improve output PSRR but increase input surge currents during soft-start and output voltage changes. The effective output capacitance should not exceed  $2.8\mu F$  to maintain stability.

While in LDO mode,  $C_{LDOx}$  is required to keep stability. The series inductance of the output capacitor and its series resistance should be low (i.e.,  $ESR \leq 10m\Omega$  and  $ESL \leq 1nH$ ) for frequencies up to 0.5MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with increased DC bias voltage. This effect is more pronounced with smaller capacitor case sizes. Due to this characteristic, 0603 case size capacitors tend to perform well while 0402 case size capacitors of the same value perform poorly.

## Detailed Description—I<sup>2</sup>C Serial Communication

### General Description

The IC features a revision 3.0 I<sup>2</sup>C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). This device acts as a slave-only device, relying on the master to generate a clock signal. SCL clock rates from 0Hz to 3.4MHz are supported.

I<sup>2</sup>C is an open-drain bus and therefore SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

[Figure 27](#) shows the functional diagram for the I<sup>2</sup>C based communications controller. For additional information on I<sup>2</sup>C, refer to the "I<sup>2</sup>C Bus Specification and User Manual" which is available for free through the internet.

### Features

- I<sup>2</sup>C Revision 3.0 Compatible Serial Communications Channel
- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast-Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)
- Does not utilize I<sup>2</sup>C Clock Stretching

### I<sup>2</sup>C Simplified Block Diagram

There are three pins (aside from GND) for the I<sup>2</sup>C-compatible interface. V<sub>IO</sub> determines the logic level, SCL is the clock line, and SDA is the data line. Note that the interface does **not** have the ability to drive the SCL line.

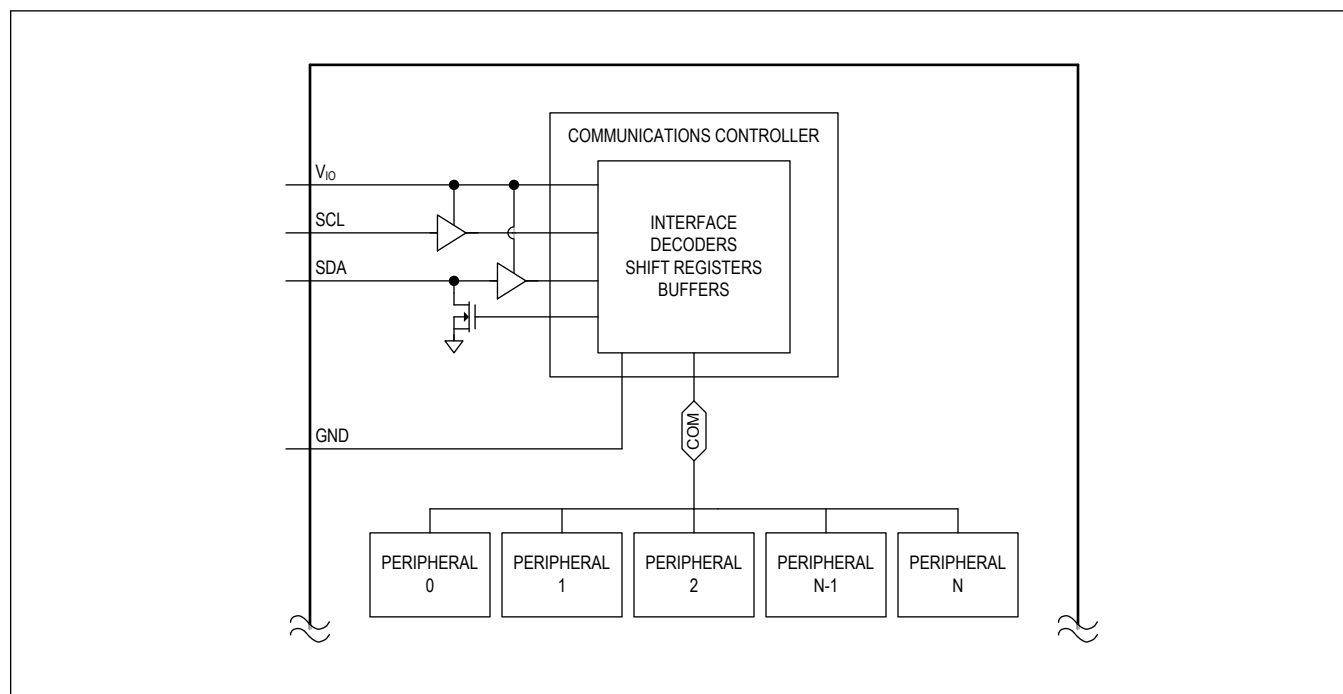


Figure 27. I<sup>2</sup>C Simplified Block Diagram



## I<sup>2</sup>C System Configuration

The I<sup>2</sup>C-compatible interface is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I<sup>2</sup>C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. The I<sup>2</sup>C-compatible interface operates as a slave on the I<sup>2</sup>C bus with transmit and receive capabilities.

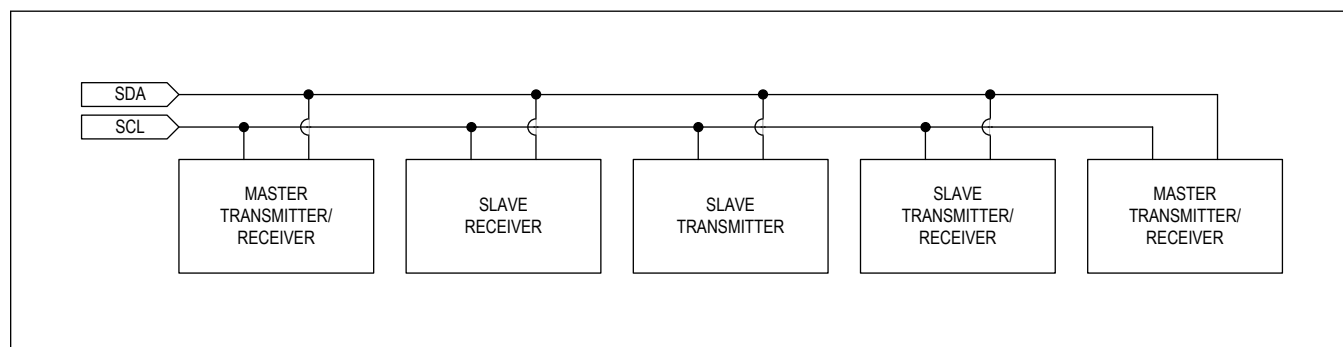


Figure 28. I<sup>2</sup>C System Configuration

## I<sup>2</sup>C Interface Power

The I<sup>2</sup>C interface derives its power from  $V_{IO}$ . Typically a power input such as  $V_{IO}$  would require a local 0.1 $\mu$ F ceramic bypass capacitor to ground. However, in highly integrated power distribution systems, a dedicated capacitor might not be necessary. If the impedance between  $V_{IO}$  and the next closest capacitor ( $\geq 0.1\mu$ F) is less than 100m $\Omega$  in series with 10nH, then a local capacitor is not needed. Otherwise, bypass  $V_{IO}$  to GND with a 0.1 $\mu$ F ceramic capacitor.

$V_{IO}$  accepts voltages from 1.7V to 3.6V ( $V_{IO}$ ). Cycling  $V_{IO}$  does not reset the I<sup>2</sup>C registers. When  $V_{IO}$  is less than  $V_{IOUVLO}$  and  $V_{SYS}$  is less than  $V_{SYSUVLO}$ , SDA and SCL are high-impedance.

## I<sup>2</sup>C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals. See the [I<sup>2</sup>C Start and Stop Conditions](#) section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

## I<sup>2</sup>C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See [Figure 29](#).

A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the [I<sup>2</sup>C Acknowledge Bit](#) section for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general a repeated start command is functionally equivalent to a regular start command.

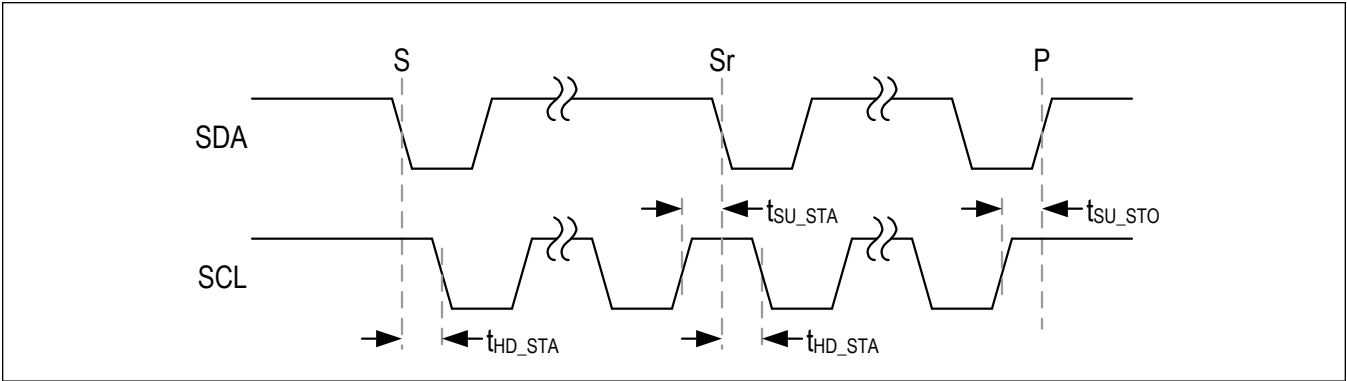


Figure 29. I<sup>2</sup>C Start and Stop Conditions

**I<sup>2</sup>C Acknowledge Bit**

Both the I<sup>2</sup>C bus master and slave devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See Figure 30. To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

This device issues an ACK for all register addresses in the possible address space even if the particular register does not exist.

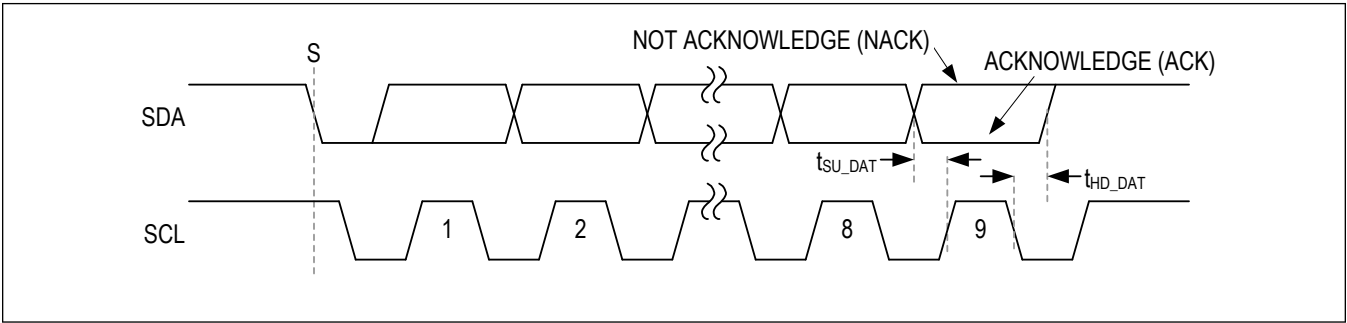


Figure 30. Acknowledge Bit

**I<sup>2</sup>C Slave Address**

The I<sup>2</sup>C controller implements 7-bit slave addressing. An I<sup>2</sup>C bus master initiates communication with the slave by issuing a START condition followed by the slave address. See Figure 31. The OTP address is factory-programmable for one of two options. See Table 20. All slave addresses not mentioned in Table 20 are not acknowledged.

**Table 20. I<sup>2</sup>C Slave Address Options**

| ADDRESS                  | 7-BIT SLAVE ADDRESS | 8-BIT WRITE ADDRESS | 8-BIT READ ADDRESS |
|--------------------------|---------------------|---------------------|--------------------|
| Main Address (ADDR = 1)* | 0x48, 0b 100 1000   | 0x90, 0b 1001 0000  | 0x91, 0b 1001 0001 |
| Main Address (ADDR = 0)* | 0x40, 0b 100 0000   | 0x80, 0b 1000 0000  | 0x81, 0b 1000 0001 |

Table 20. I<sup>2</sup>C Slave Address Options (continued)

| ADDRESS     | 7-BIT SLAVE ADDRESS | 8-BIT WRITE ADDRESS | 8-BIT READ ADDRESS |
|-------------|---------------------|---------------------|--------------------|
| Test Mode** | 0x49, 0b 100 1001   | 0x92, 0b 1001 0010  | 0x93, 0b 1001 0011 |

\*Perform all reads and writes on the main address. ADDR is a factory one-time programmable (OTP) option, allowing for address changes in the event of a bus conflict. [Contact Maxim](#) for more information.

\*\*When test mode is unlocked, the additional address is acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Maxim.

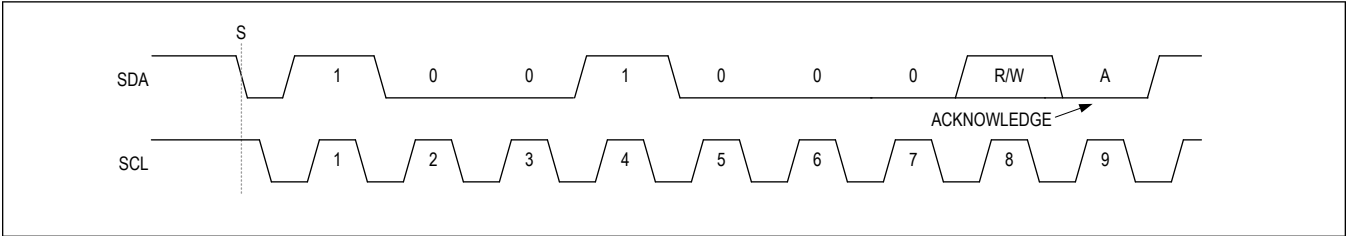


Figure 31. Slave Address Example

**I<sup>2</sup>C Clock Stretching**

In general, the clock signal generation for the I<sup>2</sup>C bus is the responsibility of the master device. The I<sup>2</sup>C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

**I<sup>2</sup>C General Call Address**

This device does not implement the I<sup>2</sup>C specifications general call address and does not acknowledge the general call address (0b0000\_0000).

**I<sup>2</sup>C Device ID**

This device does not support the I<sup>2</sup>C Device ID feature.

**I<sup>2</sup>C Communication Speed**

This device is compatible with all four communication speed ranges as defined by the Revision 3.0 I<sup>2</sup>C specification:

- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast-Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing bus speed through this range is the combination of the bus capacitance and pullup resistors. Larger values of bus capacitance and pullup resistance increase the time constant ( $C \times R$ ), slowing bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I<sup>2</sup>C bus specification and user manual (available for free on the internet) for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6k $\Omega$  pullup resistors, a 400kHz bus needs about 1.5k $\Omega$  pullup resistors, and a 1MHz bus needs 680 $\Omega$  pullup resistors. Remember that, while the open-drain bus is low, the pullup resistor is dissipating power, and lower value pullup resistors dissipate more power ( $V^2/R$ ).

Operating in high-speed mode requires some special considerations. For a full list of considerations, refer to the publicly available I<sup>2</sup>C bus specification and user manual. Major considerations with respect to this part are:

- The I<sup>2</sup>C bus master uses current source pullups to shorten the signal rise.
- The I<sup>2</sup>C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the bus input filters are set for standard mode, fast mode, and fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the [I<sup>2</sup>C Communication Protocols](#) section.

## I<sup>2</sup>C Communication Protocols

Both writing to and reading from registers are supported as described in the following subsections.

### Writing to a Single Register

[Figure 32](#) shows the protocol for the I<sup>2</sup>C master device to write one byte of data to this device. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data.
8. The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

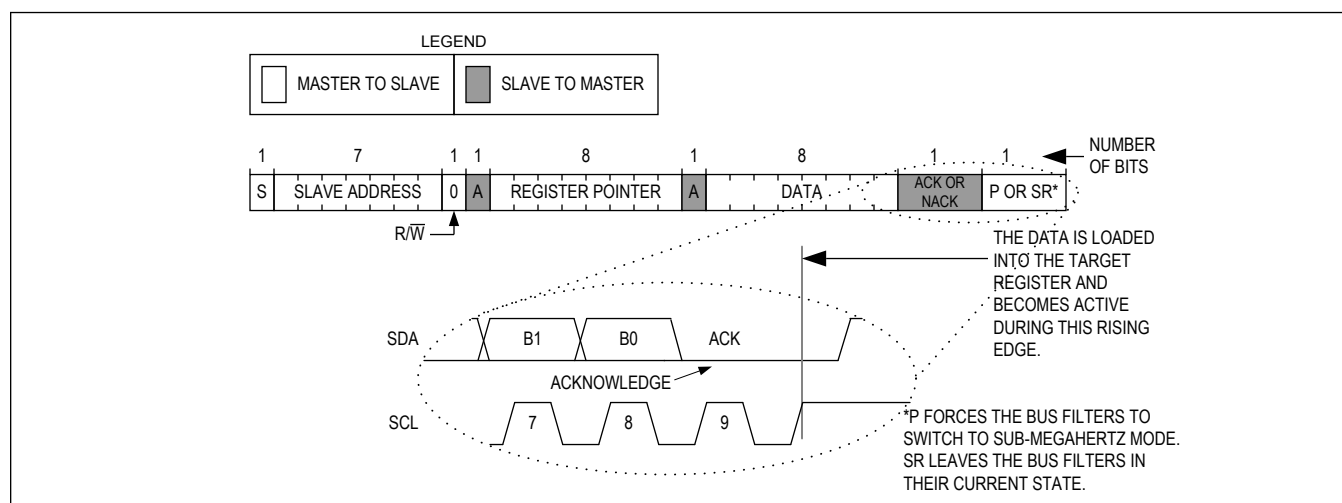


Figure 32. Writing to a Single Register with the Write Byte Protocol

## Writing Multiple Bytes to Sequential Registers

Figure 33 shows the protocol for writing to sequential registers. This protocol is similar to the write byte protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a stop or repeated start.

The writing to sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge related clock pulse, the master can issue an acknowledge or a not acknowledge.
10. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

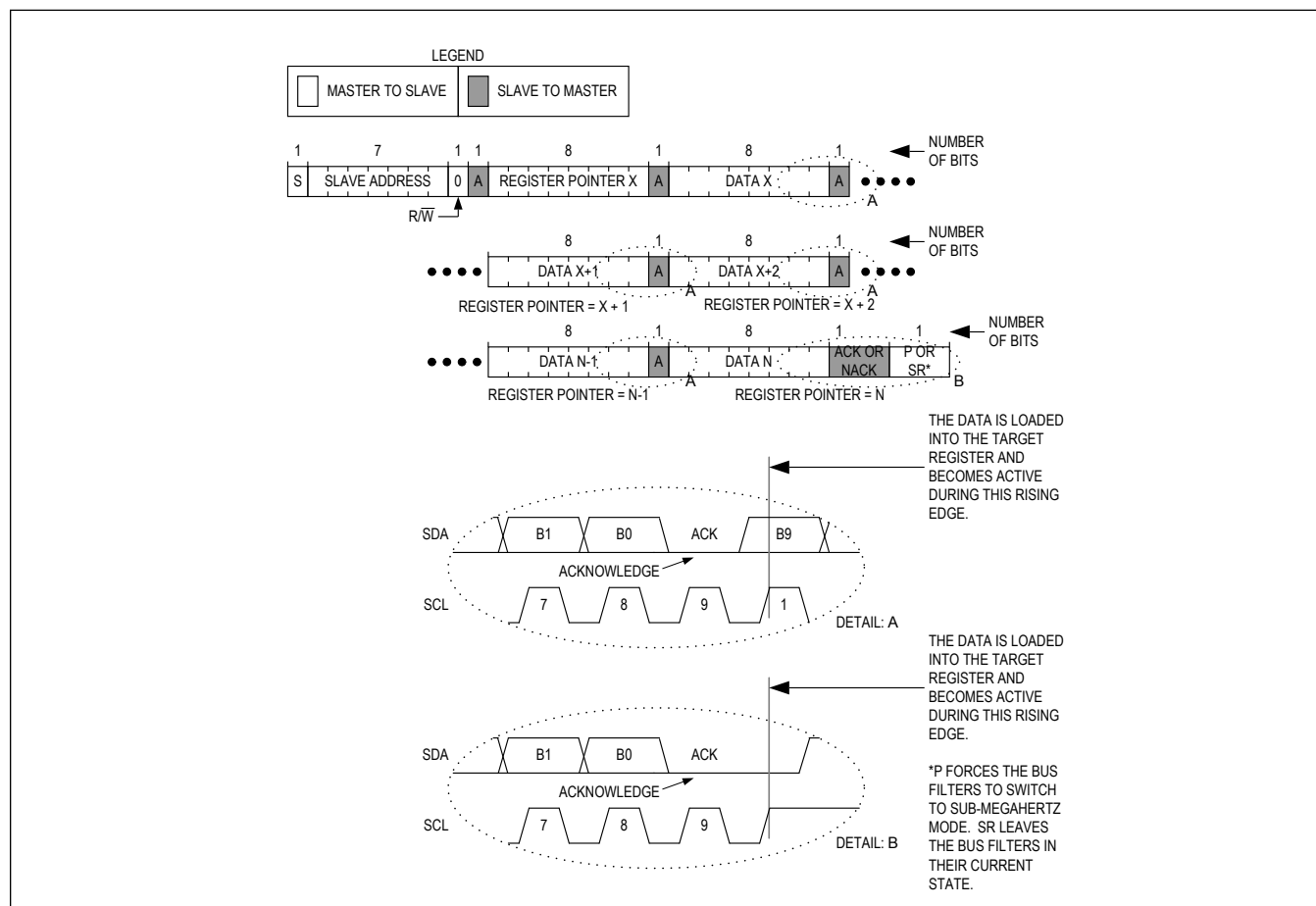


Figure 33. Writing to Sequential Registers X to N

### Reading from a Single Register

Figure 34 shows the protocol for the I<sup>2</sup>C master device to read one byte of data. This protocol is the same as the SMBus specification's read byte protocol.

The read byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a not acknowledge (nA).
11. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop, the register pointer is not modified. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

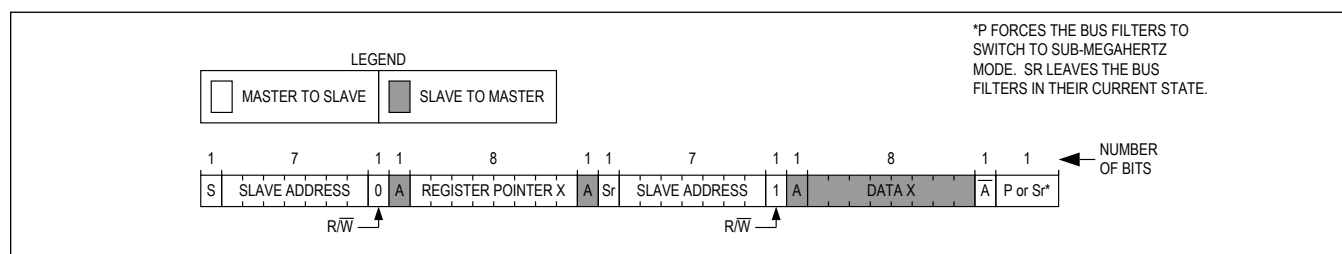


Figure 34. Reading from a Single Register with the Read Byte Protocol

### Reading from Sequential Registers

Figure 35 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data: when the master has all the data it requires it issues a not acknowledge (nA) and a stop (P) to end the transmission. The continuous read from sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
12. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop it does not modify its register pointer. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

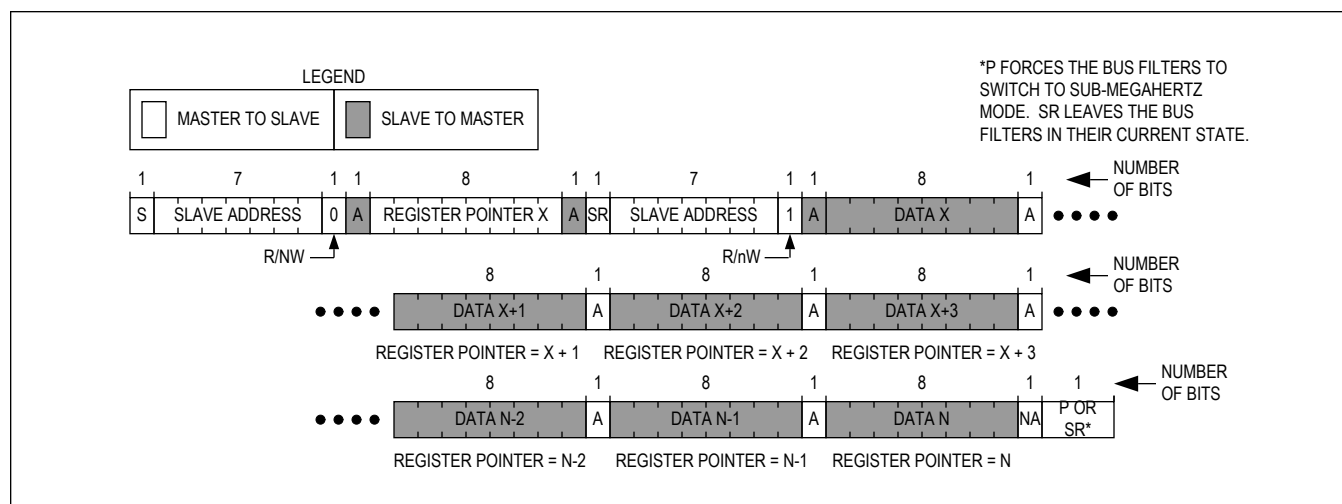


Figure 35. Reading Continuously from Sequential Registers X to N

## Engaging HS-Mode for Operation up to 3.4MHz

Figure 36 shows the protocol for engaging HS-mode operation. HS-mode operation allows for a bus operating speed up to 3.4MHz. The engaging HS-mode protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a start command (S).
3. The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't care bits.
4. The addressed slave issues a not acknowledge (nA).
5. The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a stop (P) is issued. To continue operations in high-speed mode, use repeated start (Sr)

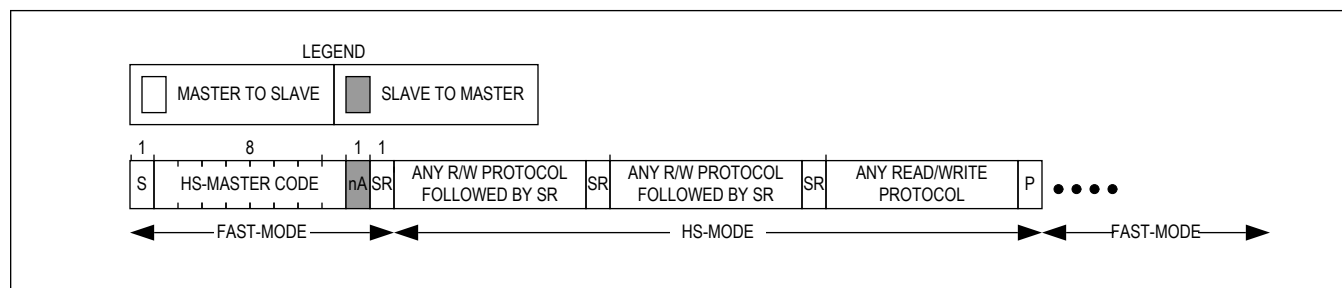


Figure 36. Engaging HS Mode

# MAX77654

## Ultra-Low Power PMIC Featuring Single-Inductor, 3-Output Buck-Boost, 2-LDOs, Power-Path Charger for Small Li+, and Ship Mode

### Register Map

#### MAX77654

| ADDRESS | NAME                            | MSB               |                 |                 |                 |                 |               |                 | LSB      |
|---------|---------------------------------|-------------------|-----------------|-----------------|-----------------|-----------------|---------------|-----------------|----------|
| Global  |                                 |                   |                 |                 |                 |                 |               |                 |          |
| 0x00    | <a href="#">INT_GLBL0[7:0]</a>  | DOD0_R            | DOD1_R          | TJAL2_R         | TJAL1_R         | nEN_R           | nEN_F         | GPI0_R          | GPI0_F   |
| 0x04    | <a href="#">INT_GLBL1[7:0]</a>  | RSVD              | LDO1_F          | LDO0_F          | SBB_TO          | GPI2_R          | GPI2_F        | GPI1_R          | GPI1_F   |
| 0x05    | <a href="#">ERCFLAG[7:0]</a>    | WDT_RST           | WDT_OFF         | SFT_CRST_F      | SFT_OFF_F       | MRST            | SYSUVO        | SYSOVL_O        | TOVLD    |
| 0x06    | <a href="#">STAT_GLBL[7:0]</a>  | DIDM              | BOK             | DOD0_S          | DOD1_S          | TJAL2_S         | TJAL1_S       | STAT_EN         | STAT_IRQ |
| 0x08    | <a href="#">INTM_GLBL1[7:0]</a> | RSVD              | LDO1_M          | LDO0_M          | SBB_TO_M        | GPI2_RM         | GPI2_FM       | GPI1_RM         | GPI1_FM  |
| 0x09    | <a href="#">INTM_GLBL0[7:0]</a> | DOD0_RM           | DOD1_RM         | TJAL2_RM        | TJAL1_RM        | nEN_RM          | nEN_FM        | GPI0_RM         | GPI0_FM  |
| 0x10    | <a href="#">CNFG_GLBL[7:0]</a>  | PU_DIS            | T_MRST          | SBIA_LPM        | SBIA_EN         | nEN_MODE        | DBEN_nEN      | SFT_CTRL[1:0]   |          |
| 0x11    | <a href="#">CNFG_GPIO0[7:0]</a> | RSVD              | –               | ALT_GPIO0       | DBEN_GPI        | DO              | DRV           | DI              | DIR      |
| 0x12    | <a href="#">CNFG_GPIO1[7:0]</a> | RSVD[1:0]         |                 | ALT_GPIO1       | DBEN_GPI        | DO              | DRV           | DI              | DIR      |
| 0x13    | <a href="#">CNFG_GPIO2[7:0]</a> | RSVD[1:0]         |                 | ALT_GPIO2       | DBEN_GPI        | DO              | DRV           | DI              | DIR      |
| 0x14    | <a href="#">CID[7:0]</a>        | CID               | –               | –               | –               | CID[3:0]        |               |                 |          |
| 0x17    | <a href="#">CNFG_WDT[7:0]</a>   | RSVD[1:0]         |                 | WDT_PER[1:0]    |                 | WDT_MODE        | WDT_CLR       | WDT_EN          | WDT_LOCK |
| OVERLAP |                                 |                   |                 |                 |                 |                 |               |                 |          |
| Charger |                                 |                   |                 |                 |                 |                 |               |                 |          |
| 0x01    | <a href="#">INT_CHG[7:0]</a>    | RSVD              | SYS_CFG_I       | SYS_CTL_I       | CHGIN_CTRL_I    | TJ_REG_I        | CHGIN_I       | CHG_I           | THM_I    |
| 0x02    | <a href="#">STAT_CHG_A[7:0]</a> | RSVD              | VCHGIN_MIN_STAT | ICHGIN_LIM_STAT | VSYS_MIN_STAT   | TJ_REG_STAT     | THM_DTLS[2:0] |                 |          |
| 0x03    | <a href="#">STAT_CHG_B[7:0]</a> | CHG_DTLS[3:0]     |                 |                 |                 | CHGIN_DTLS[1:0] |               | CHG             | TIME_SUS |
| 0x07    | <a href="#">INT_M_CHG[7:0]</a>  | RSVD              | SYS_CFG_M       | SYS_CTL_M       | CHGIN_CTRL_M    | TJ_REG_M        | CHGIN_M       | CHG_M           | THM_M    |
| 0x20    | <a href="#">CNFG_CHG_A[7:0]</a> | THM_HOT[1:0]      |                 | THM_WARM[1:0]   |                 | THM_COOL[1:0]   |               | THM_COLD[1:0]   |          |
| 0x21    | <a href="#">CNFG_CHG_B[7:0]</a> | VCHGIN_MIN[2:0]   |                 |                 | ICHGIN_LIM[2:0] |                 |               | I_PQ            | CHG_EN   |
| 0x22    | <a href="#">CNFG_CHG_C[7:0]</a> | CHG_PQ[2:0]       |                 |                 | I_TERM[1:0]     |                 | T_TOPOFF[2:0] |                 |          |
| 0x23    | <a href="#">CNFG_CHG_D[7:0]</a> | TJ_REG[2:0]       |                 |                 | VSYS_REG[4:0]   |                 |               |                 |          |
| 0x24    | <a href="#">CNFG_CHG_E[7:0]</a> | CHG_CC[5:0]       |                 |                 |                 |                 |               | T_FAST_CHG[1:0] |          |
| 0x25    | <a href="#">CNFG_CHG_F[7:0]</a> | CHG_CC_JEITA[5:0] |                 |                 |                 |                 |               | THM_EN          | –        |
| 0x26    | <a href="#">CNFG_CHG_G[7:0]</a> | CHG_CV[5:0]       |                 |                 |                 |                 |               | USBS            | RSVD     |
| 0x27    | <a href="#">CNFG_CHG_H[7:0]</a> | CHG_CV_JEITA[5:0] |                 |                 |                 |                 |               | RSVD[1:0]       |          |



# MAX77654

## Ultra-Low Power PMIC Featuring Single-Inductor, 3-Output Buck-Boost, 2-LDOs, Power-Path Charger for Small Li+, and Ship Mode

| ADDRESS | NAME                              | MSB                    |              |              |             |              |              |              | LSB |
|---------|-----------------------------------|------------------------|--------------|--------------|-------------|--------------|--------------|--------------|-----|
| 0x28    | <a href="#">CNFG_CHG_I[7:0]</a>   | IMON_DISCHG_SCALE[3:0] |              |              |             | MUX_SEL[3:0] |              |              |     |
| SBB     |                                   |                        |              |              |             |              |              |              |     |
| 0x29    | <a href="#">CNFG_SBB0_A[7:0]</a>  | –                      | TV_SBB0[6:0] |              |             |              |              |              |     |
| 0x2A    | <a href="#">CNFG_SBB0_B[7:0]</a>  | RSVD                   | OP_MO<br>DE  | IP_SBB0[1:0] |             | ADE_SB<br>B0 | EN_SBB0[2:0] |              |     |
| 0x2B    | <a href="#">CNFG_SBB1_A[7:0]</a>  | –                      | TV_SBB1[6:0] |              |             |              |              |              |     |
| 0x2C    | <a href="#">CNFG_SBB1_B[7:0]</a>  | RSVD                   | OP_MO<br>DE  | IP_SBB1[1:0] |             | ADE_SB<br>B1 | EN_SBB1[2:0] |              |     |
| 0x2D    | <a href="#">CNFG_SBB2_A[7:0]</a>  | –                      | TV_SBB2[6:0] |              |             |              |              |              |     |
| 0x2E    | <a href="#">CNFG_SBB2_B[7:0]</a>  | RSVD                   | OP_MO<br>DE  | IP_SBB2[1:0] |             | ADE_SB<br>B2 | EN_SBB2[2:0] |              |     |
| 0x2F    | <a href="#">CNFG_SBB_TOP[7:0]</a> | ICHGIN_<br>LIM_DE<br>F | –            | –            | –           | –            | –            | DRV_SBB[1:0] |     |
| LDO     |                                   |                        |              |              |             |              |              |              |     |
| 0x38    | <a href="#">CNFG_LDO0_A[7:0]</a>  | RSVD                   | TV_LDO0[6:0] |              |             |              |              |              |     |
| 0x39    | <a href="#">CNFG_LDO0_B[7:0]</a>  | –                      | –            | –            | LDO0_M<br>D | ADE_LD<br>O0 | EN_LDO0[2:0] |              |     |
| 0x3A    | <a href="#">CNFG_LDO1_A[7:0]</a>  | RSVD                   | TV_LDO1[6:0] |              |             |              |              |              |     |
| 0x3B    | <a href="#">CNFG_LDO1_B[7:0]</a>  | –                      | –            | –            | LDO1_M<br>D | ADE_LD<br>O1 | EN_LDO1[2:0] |              |     |

### Register Details

#### [INT\\_GLBL0 \(0x00\)](#)

| BIT         | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Field       | DOD0_R          | DOD1_R          | TJAL2_R         | TJAL1_R         | nEN_R           | nEN_F           | GPI0_R          | GPI0_F          |
| Reset       | 0b0             | 0b0             | 0b0             | 0b0             | 0b0             | 0b0             | 0b0             | 0b0             |
| Access Type | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All |

| BITFIELD | BITS | DESCRIPTION                           | DECODE                                                                                                                                                                                     |
|----------|------|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOD0_R   | 7    | LDO Dropout Detector Rising Interrupt | 0 = The LDO has not detected dropout since the last time this bit was read.<br>1 = The LDO has detected dropout since the last time this bit was read.                                     |
| DOD1_R   | 6    | LDO Dropout Detector Rising Interrupt | 0 = The LDO has not detected dropout since the last time this bit was read.<br>1 = The LDO has detected dropout since the last time this bit was read.                                     |
| TJAL2_R  | 5    | Thermal Alarm 2 Rising Interrupt      | 0 = The junction temperature has not risen above TJAL2 since the last time this bit was read.<br>1 = The junction temperature has risen above TJAL2 since the last time this bit was read. |
| TJAL1_R  | 4    | Thermal Alarm 1 Rising Interrupt      | 0 = The junction temperature has not risen above TJAL1 since the last time this bit was read.<br>1 = The junction temperature has risen above TJAL1 since the last time this bit was read. |

| BITFIELD | BITS | DESCRIPTION                                                                           | DECODE                                                                                                                                                      |
|----------|------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| nEN_R    | 3    | nEN Rising Interrupt                                                                  | 0 = No nEN rising edges have occurred since the last time this bit was read.<br>1 = A nEN rising edge has occurred since the last time this bit was read.   |
| nEN_F    | 2    | nEN Falling Interrupt                                                                 | 0 = No nEN falling edges have occurred since the last time this bit was read.<br>1 = A nEN falling edge occurred since the last time this bit was read.     |
| GPI0_R   | 1    | GPI Rising Interrupt<br>Note that "GPI" refers to the GPIO programmed to be an input. | 0 = No GPI rising edges have occurred since the last time this bit was read.<br>1 = A GPI rising edge has occurred since the last time this bit was read.   |
| GPI0_F   | 0    | GPI Falling Interrupt<br>Note that the GPI is the GPIO programmed to be an input.     | 0 = No GPI falling edges have occurred since the last time this bit was read.<br>1 = A GPI falling edge has occurred since the last time this bit was read. |

**INT\_GLBL1 (0x04)**

| BIT         | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Field       | RSVD            | LDO1_F          | LDO0_F          | SBB_TO          | GPI2_R          | GPI2_F          | GPI1_R          | GPI1_F          |
| Reset       | 0b000           | 0b0             | 0b0             | 0b0             | 0b0             | 0b0             | 0b0             | 0b0             |
| Access Type | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All |

| BITFIELD | BITS | DESCRIPTION                                                                           | DECODE                                                                                                                                                      |
|----------|------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSVD     | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care.                           |                                                                                                                                                             |
| LDO1_F   | 6    | LDO1 Fault Interrupt                                                                  | 0 = No fault has occurred on LDO1 since the last time this bit was read.<br>1 = LDO1 has fallen out of regulation since the last time this bit was read.    |
| LDO0_F   | 5    | LDO0 Fault Interrupt                                                                  | 0 = No fault has occurred on LDO0 since the last time this bit was read.<br>1 = LDO0 has fallen out of regulation since the last time this bit was read.    |
| SBB_TO   | 4    | SBB Timeout                                                                           | 0 = NO SBB timeout occurred since the last time this bit was read.<br>1 = SBB timeout occurred since the last time this bit was read.                       |
| GPI2_R   | 3    | GPI Rising Interrupt<br>Note that "GPI" refers to the GPIO programmed to be an input. | 0 = No GPI rising edges have occurred since the last time this bit was read.<br>1 = A GPI rising edge has occurred since the last time this bit was read.   |
| GPI2_F   | 2    | GPI Falling Interrupt<br>Note that the GPI is the GPIO programmed to be an input.     | 0 = No GPI falling edges have occurred since the last time this bit was read.<br>1 = A GPI falling edge has occurred since the last time this bit was read. |
| GPI1_R   | 1    | GPI Rising Interrupt<br>Note that "GPI" refers to the GPIO programmed to be an input. | 0 = No GPI rising edges have occurred since the last time this bit was read.<br>1 = A GPI rising edge has occurred since the last time this bit was read.   |

| BITFIELD | BITS | DESCRIPTION                                                                           | DECODE                                                                                                                                                      |
|----------|------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPI1_F   | 0    | GPI Falling Interrupt<br><br>Note that the GPI is the GPIO programmed to be an input. | 0 = No GPI falling edges have occurred since the last time this bit was read.<br>1 = A GPI falling edge has occurred since the last time this bit was read. |

**ERCFLAG (0x05)**

| BIT         | 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
|-------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Field       | WDT_RST            | WDT_OFF            | SFT_CRST_F         | SFT_OFF_F          | MRST               | SYSUVLO            | SYSOVLO            | TOVLD              |
| Reset       | 0b0                | 0b0                | 0b0                | 0b0                | 0b0                | 0b0                | 0b0                | 0b0                |
| Access Type | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All |

| BITFIELD   | BITS | DESCRIPTION                                                                                                       | DECODE                                                                                                                                                                                                                                                                          |
|------------|------|-------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WDT_RST    | 7    | Watchdog Timer Reset Flag. This bit sets when the watchdog timer expires and causes a power-reset (WDT_MODE = 1). | 0 = Watchdog timer has not caused a power-reset since the last time this bit was read.<br>1 = Watchdog timer has expired and caused a power-reset since the last time this bit was read.                                                                                        |
| WDT_OFF    | 6    | Watchdog Timer OFF Flag. This bit sets when the watchdog timer expires and causes a power-off (WDT_MODE = 0).     | 0 = Watchdog timer has not caused a power-off since the last time this bit was read.<br>1 = Watchdog timer has expired and caused a power-off since the last time this bit was read.                                                                                            |
| SFT_CRST_F | 5    | Software Cold Reset Flag                                                                                          | 0 = The software cold reset has not occurred since the last read of this register.<br>1 = The software cold reset has occurred since the last read of this register. This indicates that software has set SFT_CTRL[1:0] = 0b01.                                                 |
| SFT_OFF_F  | 4    | Software OFF Flag                                                                                                 | 0 = The SFT_OFF function has not occurred since the last read of this register.<br>1 = The SFT_OFF function has occurred since the last read of this register. This indicates that software has set SFT_CTRL[1:0] = 0b10.                                                       |
| MRST       | 3    | Manual Reset Timer                                                                                                | 0 = A manual reset has not occurred since the last read of this register.<br>1 = A manual reset has occurred since the last read of this register.                                                                                                                              |
| SYSUVLO    | 2    | SYS Domain Undervoltage Lockout                                                                                   | 0 = The SYS domain undervoltage lockout has not occurred since the last read of this register.<br>1 = The SYS domain undervoltage lockout has occurred since the last read of this register. This indicates that the SYS domain voltage fell below V <sub>SYSUVLO</sub> (~2.4V) |
| SYSOVLO    | 1    | SYS Domain Overvoltage Lockout                                                                                    | 0 = The SYS domain overvoltage lockout has not occurred since the last read of this register.<br>1 = The SYS domain overvoltage lockout has occurred since the last read of this register. This indicates that the SYS domain voltage rose below V <sub>SYSOVLO</sub> (~5.85V)  |

## MAX77654

Ultra-Low Power PMIC Featuring Single-Inductor,  
3-Output Buck-Boost, 2-LDOs, Power-Path  
Charger for Small Li+, and Ship Mode

| BITFIELD | BITS | DESCRIPTION      | DECODE                                                                                                                                                                                                                  |
|----------|------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TOVLD    | 0    | Thermal Overload | 0 = Thermal overload has not occurred since the last read of this register.<br>1 = Thermal overload has occurred since the last read of this register. This indicates that the junction temperature has exceeded 165°C. |

**STAT\_GLBL (0x06)**

| BIT         | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Field       | DIDM      | BOK       | DOD0_S    | DOD1_S    | TJAL2_S   | TJAL1_S   | STAT_EN   | STAT_IRQ  |
| Reset       | OTP       | 0b1       | 0b0       | 0b0       | 0b0       | 0b0       | 0b0       | 0b0       |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION                                    | DECODE                                                                                                  |
|----------|------|------------------------------------------------|---------------------------------------------------------------------------------------------------------|
| DIDM     | 7    | Device Identification Bits for Metal Options   | 0 = MAX77654<br>1 = Reserved                                                                            |
| BOK      | 6    | BOK Interrupt Status                           | 0 = Main bias is not ready.<br>1 = Main bias enabled and ready.                                         |
| DOD0_S   | 5    | LDO0 Dropout Detector Rising Status            | 0 = LDO0 is not in dropout.<br>1 = LDO0 is in dropout.                                                  |
| DOD1_S   | 4    | LDO1 Dropout Detector Rising Status            | 0 = LDO1 is not in dropout.<br>1 = LDO1 is in dropout.                                                  |
| TJAL2_S  | 3    | Thermal Alarm 2 Status                         | 0 = The junction temperature is less than TJA2.<br>1 = The junction temperature is greater than TJAL2.  |
| TJAL1_S  | 2    | Thermal Alarm 1 Status                         | 0 = The junction temperature is less than TJAL1.<br>1 = The junction temperature is greater than TJAL1. |
| STAT_EN  | 1    | Debounced Status for the nEN Input             | 0 = nEN is not active (logic high).<br>1 = nEN is active (logic low).                                   |
| STAT_IRQ | 0    | Software Version of the nIRQ MOSFET Gate Drive | 0 = Unmasked gate drive is logic low.<br>1 = Unmasked gate drive is logic high.                         |

**INTM\_GLBL1 (0x08)**

| BIT         | 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Field       | RSVD        | LDO1_M      | LDO0_M      | SBB_TO_M    | GPI2_RM     | GPI2_FM     | GPI1_RM     | GPI1_FM     |
| Reset       | 0b0         | 0b1         | 0b1         | 0b1         | 0b1         | 0b1         | 0b1         | 0b1         |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                 | DECODE                                                                                                                                                               |
|----------|------|-------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSVD     | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care. |                                                                                                                                                                      |
| LDO1_M   | 6    | LDO1 Fault Interrupt Mask                                   | 0 = Unmasked. If LDO1_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to LDO1_F. |

| BITFIELD | BITS | DESCRIPTION                | DECODE                                                                                                                                                               |
|----------|------|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO0_M   | 5    | LDO0 Fault Interrupt Mask  | 0 = Unmasked. If LDO0_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to LDO0_F. |
| SBB_TO_M | 4    | SBB Timeout Mask           | 0 = Unmasked. If SBB_TO goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to SBB_TO. |
| GPI2_RM  | 3    | GPI Rising Interrupt Mask  | 0 = Unmasked. If GPI_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to GPI_R.   |
| GPI2_FM  | 2    | GPI Falling Interrupt Mask | 0 = Unmasked. If GPI_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to GPI_F.   |
| GPI1_RM  | 1    | GPI Rising Interrupt Mask  | 0 = Unmasked. If GPI_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to GPI_R.   |
| GPI1_FM  | 0    | GPI Falling Interrupt Mask | 0 = Unmasked. If GPI_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to GPI_F.   |

#### INTM\_GLBL0 (0x09)

| BIT         | 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Field       | DOD0_RM     | DOD1_RM     | TJAL2_RM    | TJAL1_RM    | nEN_RM      | nEN_FM      | GPI0_RM     | GPI0_FM     |
| Reset       | 0b1         | 0b1         | 0b1         | 0b1         | 0b1         | 0b1         | 0b1         | 0b1         |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                | DECODE                                                                                                                                                                 |
|----------|------|--------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOD0_RM  | 7    | LDO Dropout Detector Rising Interrupt Mask | 0 = Unmasked. If DOD0_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to DOD0_R.   |
| DOD1_RM  | 6    | LDO Dropout Detector Rising Interrupt Mask | 0 = Unmasked. If DOD1_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to DOD1_R.   |
| TJAL2_RM | 5    | Thermal Alarm 2 Rising Interrupt Mask      | 0 = Unmasked. If TJAL2_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to TJAL2_R. |

| BITFIELD | BITS | DESCRIPTION                           | DECODE                                                                                                                                                                 |
|----------|------|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TJAL1_RM | 4    | Thermal Alarm 1 Rising Interrupt Mask | 0 = Unmasked. If TJAL1_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to TJAL1_R. |
| nEN_RM   | 3    | nEN Rising Interrupt Mask             | 0 = Unmasked. If nEN_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to nEN_R.     |
| nEN_FM   | 2    | nEN Falling Interrupt Mask            | 0 = Unmasked. If nEN_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to nEN_F.     |
| GPI0_RM  | 1    | GPI Rising Interrupt Mask             | 0 = Unmasked. If GPI_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to GPI_R.     |
| GPI0_FM  | 0    | GPI Falling Interrupt Mask            | 0 = Unmasked. If GPI_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared.<br>1 = Masked. nIRQ does not go low due to GPI_F.     |

## CNFG\_GLBL (0x10)

| BIT         | 7           | 6           | 5           | 4           | 3           | 2           | 1             | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------|---|
| Field       | PU_DIS      | T_MRST      | SBIA_LPM    | SBIA_EN     | nEN_MODE    | DBEN_nEN    | SFT_CTRL[1:0] |   |
| Reset       | 0b0         | OTP         | OTP         | 0b0         | OTP         | OTP         | 0b00          |   |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read   |   |

| BITFIELD | BITS | DESCRIPTION                                     | DECODE                                                                                                                                              |
|----------|------|-------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| PU_DIS   | 7    | nEN Internal Pullup Resistor                    | 0 = Strong internal nEN pullup (200kΩ)<br>1 = Weak internal nEN pullup (10MΩ)                                                                       |
| T_MRST   | 6    | Sets the Manual Reset Time (t <sub>MRST</sub> ) | 0 = 8s<br>1 = 16s                                                                                                                                   |
| SBIA_LPM | 5    | Main Bias Low-Power Mode Software Request       | 0 = Main bias requested to be in normal-power mode by software.<br>1 = Main bias request to be in low-power mode by software.                       |
| SBIA_EN  | 4    | Main Bias Enable Software Request               | 0 = Main bias not enabled by software. Note that the main bias can be enabled by the on/off controller.<br>1 = Main bias force enabled by software. |
| nEN_MODE | 3    | nEN Input (ON-KEY) Default Configuration Mode   | 0 = Push-button mode<br>1 = Slide-switch mode                                                                                                       |
| DBEN_nEN | 2    | Debounce Timer Enable for the nEN Pin           | 0 = 500μs Debounce<br>1 = 30ms Debounce                                                                                                             |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SFT_CTRL | 1:0  | <p>Software Reset Functions</p> <p>Note that the SFT_CRST and SFT_OFF commands initiate the power-down sequence flow as described in the data sheet. This power-down sequence flow has delay elements that add up to 205.24ms (60ms delay + 10.24ms nRST assert delay + 4x2.56ms power-down slot delays + 125ms output discharge delay). If issuing the SFT_CRST and/or SFT_OFF functions in software, wait for more than 300ms before trying to issue any additional commands through I<sup>2</sup>C.</p> | <p>0b00 = No action</p> <p>0b01 = Software cold reset (SFT_CRST). The device powers down, resets, and then powers up again.</p> <p>0b10 = Software off (SFT_OFF). The device powers down, resets, and then remains off and waiting for a wake-up event.</p> <p>0b11 = Factory-ship mode enter (FSM). The IC powers down, configuration registers reset, and the internal BATT to SYS switch opens. The device remains this way until a factory-ship mode exit event occurs.</p> |

## CNFG\_GPIO0 (0x11)

| BIT         | 7           | 6 | 5           | 4           | 3           | 2           | 1         | 0           |
|-------------|-------------|---|-------------|-------------|-------------|-------------|-----------|-------------|
| Field       | RSVD        | – | ALT_GPIO0   | DBEN_GPI    | DO          | DRV         | DI        | DIR         |
| Reset       | 0b0         | – | OTP         | 0b0         | 0b0         | 0b0         | 0b0       | 0b1         |
| Access Type | Write, Read | – | Write, Read | Write, Read | Write, Read | Write, Read | Read Only | Write, Read |

| BITFIELD  | BITS | DESCRIPTION                                                                                                                              | DECODE                                                                                                                                                                                                                                                                                      |
|-----------|------|------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSVD      | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care.                                                                              |                                                                                                                                                                                                                                                                                             |
| ALT_GPIO0 | 5    | Alternate Mode Enable for GPIO0                                                                                                          | <p>0 = Standard GPIO.</p> <p>1 = Flexible power sequencer active-high output for SBB2.</p>                                                                                                                                                                                                  |
| DBEN_GPI  | 4    | General Purpose Input Debounce Timer Enable                                                                                              | <p>0 = No debounce</p> <p>1 = 30ms Debounce</p>                                                                                                                                                                                                                                             |
| DO        | 3    | General Purpose Output Data Output                                                                                                       | <p>This bit is a don't care when DIR = 1 (configured as input).</p> <p>When set for GPO (DIR = 0):</p> <p>0 = GPIO is output logic low.</p> <p>1 = GPIO is output logic high when set as push-pull output (DRV = 1). GPIO is high-impedance when set as an open-drain output (DRV = 0).</p> |
| DRV       | 2    | General Purpose Output Driver Type                                                                                                       | <p>This bit is a don't care when DIR = 1 (configured as input).</p> <p>When set for GPO (DIR = 0):</p> <p>0 = Open-drain</p> <p>1 = Push-pull</p>                                                                                                                                           |
| DI        | 1    | GPIO Digital Input Value. Irrespective of whether the GPIO is set for GPI (DIR = 1) or GPO (DIR = 0), DI reflects the state of the GPIO. | <p>0 = Input logic low</p> <p>1 = Input logic high</p>                                                                                                                                                                                                                                      |
| DIR       | 0    | GPIO Direction                                                                                                                           | <p>0 = General purpose output (GPO)</p> <p>1 = General purpose input (GPI)</p>                                                                                                                                                                                                              |

**CNFG\_GPIO1 (0x12)**

| BIT         | 7           | 6 | 5           | 4           | 3           | 2           | 1         | 0           |
|-------------|-------------|---|-------------|-------------|-------------|-------------|-----------|-------------|
| Field       | RSVD[1:0]   |   | ALT_GPIO1   | DBEN_GPI    | DO          | DRV         | DI        | DIR         |
| Reset       | 0b00        |   | OTP         | 0b0         | 0b0         | 0b0         | 0b0       | 0b1         |
| Access Type | Write, Read |   | Write, Read | Write, Read | Write, Read | Write, Read | Read Only | Write, Read |

| BITFIELD  | BITS | DESCRIPTION                                                                                                                              | DECODE                                                                                                                                                                                                                                                                       |
|-----------|------|------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSVD      | 7:6  | Reserved. Unutilized bit. Write to 0. Reads are don't care.                                                                              |                                                                                                                                                                                                                                                                              |
| ALT_GPIO1 | 5    | Alternate Mode Enable for GPIO1                                                                                                          | 0 = Standard GPIO<br>1 = SBB2 Enable                                                                                                                                                                                                                                         |
| DBEN_GPI  | 4    | General Purpose Input Debounce Timer Enable                                                                                              | 0 = No debounce<br>1 = 30ms Debounce                                                                                                                                                                                                                                         |
| DO        | 3    | General Purpose Output Data Output                                                                                                       | This bit is a don't care when DIR = 1 (configured as input).<br><br>When set for GPO (DIR = 0):<br>0 = GPIO is output logic low.<br>1 = GPIO is output logic high when set as push-pull output (DRV = 1). GPIO is high-impedance when set as an open-drain output (DRV = 0). |
| DRV       | 2    | General Purpose Output Driver Type                                                                                                       | This bit is a don't care when DIR = 1 (configured as input).<br><br>When set for GPO (DIR = 0):<br>0 = Open-drain<br>1 = Push-pull                                                                                                                                           |
| DI        | 1    | GPIO Digital Input Value. Irrespective of whether the GPIO is set for GPI (DIR = 1) or GPO (DIR = 0), DI reflects the state of the GPIO. | 0 = Input logic low<br>1 = Input logic high                                                                                                                                                                                                                                  |
| DIR       | 0    | GPIO Direction                                                                                                                           | 0 = General purpose output (GPO)<br>1 = General purpose input (GPI)                                                                                                                                                                                                          |

**CNFG\_GPIO2 (0x13)**

| BIT         | 7           | 6 | 5           | 4           | 3           | 2           | 1         | 0           |
|-------------|-------------|---|-------------|-------------|-------------|-------------|-----------|-------------|
| Field       | RSVD[1:0]   |   | ALT_GPIO2   | DBEN_GPI    | DO          | DRV         | DI        | DIR         |
| Reset       | 0b00        |   | OTP         | 0b0         | 0b0         | 0b0         | 0b0       | 0b1         |
| Access Type | Write, Read |   | Write, Read | Write, Read | Write, Read | Write, Read | Read Only | Write, Read |

| BITFIELD  | BITS | DESCRIPTION                                                 | DECODE                                        |
|-----------|------|-------------------------------------------------------------|-----------------------------------------------|
| RSVD      | 7:6  | Reserved. Unutilized bit. Write to 0. Reads are don't care. |                                               |
| ALT_GPIO2 | 5    | Alternate Mode Enable for GPIO2.                            | 0 = Standard GPIO<br>1 = Bias LPM mode enable |
| DBEN_GPI  | 4    | General Purpose Input Debounce Timer Enable                 | 0 = No debounce<br>1 = 30ms Debounce          |



| BITFIELD | BITS | DESCRIPTION                                                                                                                              | DECODE                                                                                                                                                                                                                                                                       |
|----------|------|------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DO       | 3    | General Purpose Output Data Output                                                                                                       | This bit is a don't care when DIR = 1 (configured as input).<br><br>When set for GPO (DIR = 0):<br>0 = GPIO is output logic low.<br>1 = GPIO is output logic high when set as push-pull output (DRV = 1). GPIO is high-impedance when set as an open-drain output (DRV = 0). |
| DRV      | 2    | General Purpose Output Driver Type                                                                                                       | This bit is a don't care when DIR = 1 (configured as input).<br><br>When set for GPO (DIR = 0):<br>0 = Open-drain<br>1 = Push-pull                                                                                                                                           |
| DI       | 1    | GPIO Digital Input Value. Irrespective of whether the GPIO is set for GPI (DIR = 1) or GPO (DIR = 0), DI reflects the state of the GPIO. | 0 = Input logic low<br>1 = Input logic high                                                                                                                                                                                                                                  |
| DIR      | 0    | GPIO Direction                                                                                                                           | 0 = General purpose output (GPO)<br>1 = General purpose input (GPI)                                                                                                                                                                                                          |

**CID (0x14)**

| BIT         | 7         | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
|-------------|-----------|---|---|---|-----------|---|---|---|
| Field       | CID       | – | – | – | CID[3:0]  |   |   |   |
| Reset       | OTP       | – | – | – | OTP       |   |   |   |
| Access Type | Read Only | – | – | – | Read Only |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                  |
|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CID      | 7    | Bit 4 of the Chip Identification Code<br>The chip identification code refers to a set of reset values in the register map, or the "OTP configuration."       |
| CID      | 3:0  | Bits 0 to 3 of the Chip Identification Code<br>The chip identification code refers to a set of reset values in the register map, or the "OTP configuration." |

**CNFG\_WDT (0x17)**

| BIT         | 7           | 6 | 5            | 4 | 3           | 2           | 1           | 0         |
|-------------|-------------|---|--------------|---|-------------|-------------|-------------|-----------|
| Field       | RSVD[1:0]   |   | WDT_PER[1:0] |   | WDT_MOD_E   | WDT_CLR     | WDT_EN      | WDT_LOCK  |
| Reset       | 0b00        |   | 0b11         |   | 0b0         | 0b0         | OTP         | OTP       |
| Access Type | Write, Read |   | Write, Read  |   | Write, Read | Write, Read | Write, Read | Read Only |

| BITFIELD | BITS | DESCRIPTION                                                                                                                 | DECODE                                                                            |
|----------|------|-----------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|
| RSVD     | 7:6  | Reserved. Unutilized bit. Write to 0. Reads are don't care.                                                                 |                                                                                   |
| WDT_PER  | 5:4  | Watchdog Timer Period. Sets $t_{WD}$ . Watchdog timer is reset to the programmed value as soon as this bitfield is changed. | 0b00 = 16 seconds<br>0b01 = 32 seconds<br>0b10 = 64 seconds<br>0b11 = 128 seconds |

| BITFIELD | BITS | DESCRIPTION                                                                                                   | DECODE                                                                                                                                                                             |
|----------|------|---------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WDT_MODE | 3    | Watchdog Timer Expired Action. Determines what the IC does after the watchdog timer expires.                  | 0 = Watchdog timer expire causes power-off.<br>1 = Watchdog timer expire causes power-reset.                                                                                       |
| WDT_CLR  | 2    | Watchdog Timer Clear Control. Set this bit to feed (reset) the watchdog timer.                                | 0 = Watchdog timer period is not reset.<br>1 = Watchdog timer is reset back to $t_{WD}$ .                                                                                          |
| WDT_EN   | 1    | Watchdog Timer Enable. Write protected depending on WDT_LOCK.                                                 | 0 = Watchdog timer is not enabled.<br>1 = Watchdog timer is enabled. The timer expires if not reset by setting WDT_CLR.                                                            |
| WDT_LOCK | 0    | Factory-Set Safety Bit for the Watchdog Timer. Determines if the timer can be disabled through WDT_EN or not. | 0 = Watchdog timer can be enabled and disabled with WDT_EN.<br>1 = Watchdog timer can not be disabled with WDT_EN. However, WDT_EN can still be used to enable the watchdog timer. |

## INT\_CHG (0x01)

| BIT         | 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
|-------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Field       | RSVD               | SYS_CNFG_I         | SYS_CTRL_I         | CHGIN_CTL_I        | TJ_REG_I           | CHGIN_I            | CHG_I              | THM_I              |
| Reset       | 0b0                | 0b0                | 0b0                | 0b0                | 0b0                | 0b0                | 0b0                | 0b0                |
| Access Type | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All | Read<br>Clears All |

| BITFIELD    | BITS | DESCRIPTION                                                                                                                                                                             | DECODE                                                                                                                                                                                                                                                      |
|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSVD        | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care.                                                                                                                             |                                                                                                                                                                                                                                                             |
| SYS_CNFG_I  | 6    | System Voltage Configuration Error Interrupt                                                                                                                                            | 0 = The bit combination in CHG_CV has not been forced to change since the last time this bit was read.<br>1 = The bit combination in CHG_CV has been forced to change to ensure $V_{SYS-REG} = V_{FAST-CHG} + 200mV$ since the last time this bit was read. |
| SYS_CTRL_I  | 5    | Minimum System Voltage Regulation-Loop Related Interrupt. This interrupt signals a change in the status bit VSYS_MIN_STAT.                                                              | 0 = The minimum system voltage regulation loop has not engaged since the last time this bit was read.<br>1 = The minimum system voltage regulation loop has engaged since the last time this bit was read.                                                  |
| CHGIN_CTL_I | 4    | CHGIN Control-Loop Related Interrupt. This bit asserts when the input reaches current limit ( $I_{CHGIN-LIM}$ ) or $V_{CHGIN}$ falls below $V_{CHGIN-MIN}$ .                            | 0 = Neither the VCHGIN_MIN_STAT nor the ICHGIN_LIM_STAT bits have changed since the last time this bit was read.<br>1 = The VCHGIN_MIN_STAT or ICHGIN_LIM_STAT bits have changed since the last time this bit was read.                                     |
| TJ_REG_I    | 3    | Die Junction Temperature Regulation Interrupt. This bit asserts when the die temperature ( $T_J$ ) exceeds $T_{J-REG}$ . This interrupt signals a change in the status bit TJ_REG_STAT. | 0 = The die temperature has not exceeded $T_{J-REG}$ since the last time this bit was read.<br>1 = The die temperature has exceeded $T_{J-REG}$ since the last time this bit was read.                                                                      |
| CHGIN_I     | 2    | CHGIN Related Interrupt                                                                                                                                                                 | 0 = The bits in CHGIN_DTLS[1:0] have not changed since the last time this bit was read.<br>1 = The bits in CHGIN_DTLS[1:0] have changed since the last time this bit was read.                                                                              |

| BITFIELD | BITS | DESCRIPTION                  | DECODE                                                                                                                                                                     |
|----------|------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CHG_I    | 1    | Charger Related Interrupt    | 0 = The bits in CHG_DTLS[3:0] have not changed since the last time this bit was read.<br>1 = The bits in CHG_DTLS[3:0] have changed since the last time this bit was read. |
| THM_I    | 0    | Thermistor Related Interrupt | 0 = The bits in THM_DTLS[2:0] have not changed since the last time this bit was read.<br>1 = The bits in THM_DTLS[2:0] have changed since the last time this bit was read. |

## STAT\_CHG\_A (0x02)

| BIT         | 7         | 6               | 5               | 4             | 3           | 2             | 1 | 0 |
|-------------|-----------|-----------------|-----------------|---------------|-------------|---------------|---|---|
| Field       | RSVD      | VCHGIN_MIN_STAT | ICHGIN_LIM_STAT | VSYS_MIN_STAT | TJ_REG_STAT | THM_DTLS[2:0] |   |   |
| Reset       | 0b0       | 0b0             | 0b0             | 0b0           | 0b0         | 0b000         |   |   |
| Access Type | Read Only | Read Only       | Read Only       | Read Only     | Read Only   | Read Only     |   |   |

| BITFIELD        | BITS | DESCRIPTION                                                          | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------------|------|----------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSVD            | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care.          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| VCHGIN_MIN_STAT | 6    | Minimum Input Voltage Regulation Loop Status                         | 0 = The minimum CHGIN voltage regulation loop is not engaged.<br>1 = The minimum CHGIN voltage regulation loop has engaged to regulate $V_{CHGIN} \geq V_{CHGIN-MIN}$ .                                                                                                                                                                                                                                                                                                                                                                                                               |
| ICHGIN_LIM_STAT | 5    | Input Current Limit Loop Status                                      | 0 = The CHGIN current limit loop is not engaged.<br>1 = The CHGIN current limit loop has engaged to regulate $I_{CHGIN} \leq I_{CHGIN-LIM}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| VSYS_MIN_STAT   | 4    | Minimum System Voltage Regulation Loop Status                        | 0 = The minimum system voltage regulation loop is not engaged.<br>1 = The minimum system voltage regulation loop is engaged to regulate $V_{SYS} \geq V_{SYS-MIN}$ .                                                                                                                                                                                                                                                                                                                                                                                                                  |
| TJ_REG_STAT     | 3    | Maximum Junction Temperature Regulation Loop Status                  | 0 = The maximum junction temperature regulation loop is not engaged.<br>1 = The maximum junction temperature regulation loop has engaged to regulate the junction temperature to less than $T_{J-REG}$ .                                                                                                                                                                                                                                                                                                                                                                              |
| THM_DTLS        | 2:0  | Battery Temperature Details. Valid only when CHGIN_DTLS[1:0] = 0b11. | 0b000 = Thermistor is disabled (THM_EN = 0).<br>0b001 = Battery is cold as programmed by THM_COLD[1:0]. If thermistor and charger are enabled while the battery is cold, a battery temperature fault occurs.<br>0b010 = Battery is cool as programmed by THM_COOL[1:0].<br>0b011 = Battery is warm as programmed by THM_WARM[1:0].<br>0b100 = Battery is hot as programmed by THM_HOT[1:0]. If thermistor and charger are enabled while the battery is hot, a battery temperature fault occurs.<br>0b101 = Battery is in the normal temperature region.<br>0b110 to 0b111 = Reserved. |

STAT\_CHG\_B (0x03)

| BIT         | 7             | 6 | 5 | 4 | 3               | 2 | 1         | 0         |
|-------------|---------------|---|---|---|-----------------|---|-----------|-----------|
| Field       | CHG_DTLS[3:0] |   |   |   | CHGIN_DTLS[1:0] |   | CHG       | TIME_SUS  |
| Reset       | 0x0           |   |   |   | 0b00            |   | 0b0       | 0b0       |
| Access Type | Read Only     |   |   |   | Read Only       |   | Read Only | Read Only |

| BITFIELD   | BITS | DESCRIPTION            | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------------|------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CHG_DTLS   | 7:4  | Charger Details        | 0b0000 = Off<br>0b0001 = Prequalification mode.<br>0b0010 = Fast-charge constant-current (CC) mode.<br>0b0011 = JEITA modified fast-charge constant-current mode.<br>0b0100 = Fast-charge constant-voltage (CV) mode.<br>0b0101 = JEITA modified fast-charge constant-voltage mode.<br>0b0110 = Top-off mode.<br>0b0111 = JEITA modified top-off mode.<br>0b1000 = Done<br>0b1001 = JEITA modified done (done was entered through the JEITA-modified fast-charge states).<br>0b1010 = Prequalification timer fault.<br>0b1011 = Fast-charge timer fault.<br>0b1100 = Battery temperature fault.<br>0b1101 to 0b1111 = Reserved. |
| CHGIN_DTLS | 3:2  | CHGIN Status Detail    | 0b00 = The CHGIN input voltage is below the UVLO threshold ( $V_{CHGIN} < V_{UVLO}$ ).<br>0b01 = The CHGIN input voltage is above the OVP threshold ( $V_{CHGIN} > V_{OVP}$ ).<br>0b10 = The CHGIN input is being debounced (no power accepted from CHGIN during debounce).<br>0b11 = The CHGIN input is okay and debounced.                                                                                                                                                                                                                                                                                                    |
| CHG        | 1    | Quick Charger Status   | 0 = Charging is not happening.<br>1 = Charging is happening.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| TIME_SUS   | 0    | Time Suspend Indicator | 0 = The charger's timers are either not active, or not suspended.<br>1 = The charger's active timer is suspended due to one of three reasons: charge current dropped below 20% of $I_{FAST-CHG}$ while the charger state machine is in FAST CHARGE CC mode, the charger is in SUPPLEMENT mode, or the charger state machine is in BATTERY TEMPERATURE FAULT mode.                                                                                                                                                                                                                                                               |

INT\_M\_CHG (0x07)

| BIT         | 7           | 6           | 5           | 4            | 3           | 2           | 1           | 0           |
|-------------|-------------|-------------|-------------|--------------|-------------|-------------|-------------|-------------|
| Field       | RSVD        | SYS_CNFG_M  | SYS_CTRL_M  | CHGIN_CTRL_M | TJ_REG_M    | CHGIN_M     | CHG_M       | THM_M       |
| Reset       | 0b1         | 0b1         | 0b1         | 0b1          | 0b1         | 0b1         | 0b1         | 0b1         |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read  | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD     | BITS | DESCRIPTION                                                                | DECODE                                                         |
|--------------|------|----------------------------------------------------------------------------|----------------------------------------------------------------|
| RSVD         | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care.                |                                                                |
| SYS_CNFG_M   | 6    | Setting this bit prevents the SYS_CNFG_I bit from causing hardware IRQs.   | 0 = SYS_CNFG_I is not masked.<br>1 = SYS_CNFG_I is masked.     |
| SYS_CTRL_M   | 5    | Setting this bit prevents the SYS_CTRL_I bit from causing hardware IRQs.   | 0 = SYS_CTRL_I is not masked.<br>1 = SYS_CTRL_I is masked.     |
| CHGIN_CTRL_M | 4    | Setting this bit prevents the CHGIN_CTRL_I bit from causing hardware IRQs. | 0 = CHGIN_CTRL_I is not masked.<br>1 = CHGIN_CTRL_I is masked. |
| TJ_REG_M     | 3    | Setting this bit prevents the TJREG_I bit from causing hardware IRQs.      | 0 = TJREG_I is not masked.<br>1 = TJREG_I is masked.           |
| CHGIN_M      | 2    | Setting this bit prevents the CHGIN_I bit from causing hardware IRQs.      | 0 = CHGIN_I is not masked.<br>1 = CHGIN_I is masked.           |
| CHG_M        | 1    | Setting this bit prevents the CHG_I bit from causing hardware IRQs.        | 0 = CHG_I is not masked.<br>1 = CHG_I is masked.               |
| THM_M        | 0    | Setting this bit prevents the THM_I bit from causing hardware IRQs.        | 0 = THM_I is not masked.<br>1 = THM_I is masked.               |

## CNFG\_CHG\_A (0x20)

| BIT         | 7            | 6 | 5             | 4 | 3             | 2 | 1             | 0 |
|-------------|--------------|---|---------------|---|---------------|---|---------------|---|
| Field       | THM_HOT[1:0] |   | THM_WARM[1:0] |   | THM_COOL[1:0] |   | THM_COLD[1:0] |   |
| Reset       | 0b00         |   | 0b00          |   | 0b11          |   | 0b11          |   |
| Access Type | Write, Read  |   | Write, Read   |   | Write, Read   |   | Write, Read   |   |

| BITFIELD | BITS | DESCRIPTION                                     | DECODE                                                                                                                                                                                                                           |
|----------|------|-------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| THM_HOT  | 7:6  | Sets the $V_{HOT}$ JEITA Temperature Threshold  | 0b00 = $V_{HOT}$ = 0.411V (45°C for $\beta$ = 3380K)<br>0b01 = $V_{HOT}$ = 0.367V (50°C for $\beta$ = 3380K)<br>0b10 = $V_{HOT}$ = 0.327V (55°C for $\beta$ = 3380K)<br>0b11 = $V_{HOT}$ = 0.291V (60°C for $\beta$ = 3380K)     |
| THM_WARM | 5:4  | Sets the $V_{WARM}$ JEITA Temperature Threshold | 0b00 = $V_{WARM}$ = 0.511V (35°C for $\beta$ = 3380K)<br>0b01 = $V_{WARM}$ = 0.459V (40°C for $\beta$ = 3380K)<br>0b10 = $V_{WARM}$ = 0.411V (45°C for $\beta$ = 3380K)<br>0b11 = $V_{WARM}$ = 0.367V (50°C for $\beta$ = 3380K) |
| THM_COOL | 3:2  | Sets the $V_{COOL}$ JEITA Temperature Threshold | 0b00 = $V_{COOL}$ = 0.923V (0°C for $\beta$ = 3380K)<br>0b01 = $V_{COOL}$ = 0.867V (5°C for $\beta$ = 3380K)<br>0b10 = $V_{COOL}$ = 0.807V (10°C for $\beta$ = 3380K)<br>0b11 = $V_{COOL}$ = 0.747V (15°C for $\beta$ = 3380K)   |
| THM_COLD | 1:0  | Sets the $V_{COLD}$ JEITA Temperature Threshold | 0b00 = $V_{COLD}$ = 1.024V (-10°C for $\beta$ = 3380K)<br>0b01 = $V_{COLD}$ = 0.976V (-5°C for $\beta$ = 3380K)<br>0b10 = $V_{COLD}$ = 0.923V (0°C for $\beta$ = 3380K)<br>0b11 = $V_{COLD}$ = 0.867V (5°C for $\beta$ = 3380K)  |

## CNFG\_CHG\_B (0x21)

| BIT         | 7               | 6 | 5 | 4               | 3 | 2 | 1           | 0           |
|-------------|-----------------|---|---|-----------------|---|---|-------------|-------------|
| Field       | VCHGIN_MIN[2:0] |   |   | ICHGIN_LIM[2:0] |   |   | I_PQ        | CHG_EN      |
| Reset       | 0b000           |   |   | 0b000           |   |   | 0b0         | OTP         |
| Access Type | Write, Read     |   |   | Write, Read     |   |   | Write, Read | Write, Read |

| BITFIELD   | BITS | DESCRIPTION                                                                                            | DECODE                                                                                                                                                                                                                                                 |
|------------|------|--------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VCHGIN_MIN | 7:5  | Minimum CHGIN Regulation Voltage (V <sub>CHGIN-MIN</sub> )                                             | 0b000 = 4.0V<br>0b001 = 4.1V<br>0b010 = 4.2V<br>0b011 = 4.3V<br>0b100 = 4.4V<br>0b101 = 4.5V<br>0b110 = 4.6V<br>0b111 = 4.7V                                                                                                                           |
| ICHGIN_LIM | 4:2  | CHGIN Input Current Limit (I <sub>CHGIN-LIM</sub> )                                                    | When CNFG_SBB_TOP.ICHGIN_LIM_DEF = 0:<br>0b000 = 95mA<br>0b001 = 190mA<br>0b010 = 285mA<br>0b011 = 380mA<br>0b100 = 475mA<br>0b101 to 0b111 = Reserved. Defaults to 0b100.<br><br>When CNFG_SBB_TOP.ICHGIN_LIM_DEF = 1,<br>the above list is reversed. |
| I_PQ       | 1    | Sets the prequalification charge current (I <sub>PQ</sub> ) as a percentage of I <sub>FAST-CHG</sub> . | 0 = 10%<br>1 = 20%                                                                                                                                                                                                                                     |
| CHG_EN     | 0    | Charger Enable                                                                                         | 0 = The battery charger is disabled.<br>1 = The battery charger is enabled.                                                                                                                                                                            |

**CNFG\_CHG\_C (0x22)**

| BIT         | 7           | 6 | 5 | 4           | 3 | 2             | 1 | 0 |
|-------------|-------------|---|---|-------------|---|---------------|---|---|
| Field       | CHG_PQ[2:0] |   |   | I_TERM[1:0] |   | T_TOPOFF[2:0] |   |   |
| Reset       | 0b111       |   |   | 0b11        |   | 0b000         |   |   |
| Access Type | Write, Read |   |   | Write, Read |   | Write, Read   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                           | DECODE                                                                                                                                                                     |
|----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CHG_PQ   | 7:5  | Battery Prequalification Voltage Threshold (V <sub>PQ</sub> )                                                                                                         | 0b000 = 2.3V<br>0b001 = 2.4V<br>0b010 = 2.5V<br>0b011 = 2.6V<br>0b100 = 2.7V<br>0b101 = 2.8V<br>0b110 = 2.9V<br>0b111 = 3.0V                                               |
| I_TERM   | 4:3  | Charger Termination Current (I <sub>TERM</sub> ). I_TERM[1:0] sets the charger termination current as a percentage of the fast-charge current I <sub>FAST-CHG</sub> . | 00 = 5%<br>01 = 7.5%<br>10 = 10%<br>11 = 15%                                                                                                                               |
| T_TOPOFF | 2:0  | Top-Off Timer Value (t <sub>TO</sub> )                                                                                                                                | 0b000 = 0 minutes<br>0b001 = 5 minutes<br>0b010 = 10 minutes<br>0b011 = 15 minutes<br>0b100 = 20 minutes<br>0b101 = 25 minutes<br>0b110 = 30 minutes<br>0b111 = 35 minutes |

**CNFG\_CHG\_D (0x23)**

| BIT         | 7           | 6 | 5 | 4           | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|-------------|---|---|---|---|
| Field       | TJ_REG[2:0] |   |   | VSYREG[4:0] |   |   |   |   |
| Reset       | 0b000       |   |   | 0b10000     |   |   |   |   |
| Access Type | Write, Read |   |   | Write, Read |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                             | DECODE                                                                                               |
|----------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| TJ_REG   | 7:5  | Sets the die junction temperature regulation point, TJ-REG.                                                                                                                                                                                             | 0b000 = 60°C<br>0b001 = 70°C<br>0b010 = 80°C<br>0b011 = 90°C<br>0b100 to 0b111 = 100°C               |
| VSYREG   | 4:0  | System Voltage Regulation (VSYREG)<br><br>This 5-bit configuration is a linear transfer function that starts at 4.1V and ends at 4.8V, with 25mV increments.<br><br>Program VSYREG to at least 200mV above the higher of VFAST-CHG and VFAST-CHG-JEITA. | 0x0 = 4.100V<br>0x1 = 4.125V<br>0x2 = 4.150V<br><br>...<br><br>0x1B = 4.775V<br>0x1C - 0x1F = 4.800V |

**CNFG\_CHG\_E (0x24)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1               | 0 |
|-------------|-------------|---|---|---|---|---|-----------------|---|
| Field       | CHG_CC[5:0] |   |   |   |   |   | T_FAST_CHG[1:0] |   |
| Reset       | 0b000001    |   |   |   |   |   | 0b01            |   |
| Access Type | Write, Read |   |   |   |   |   | Write, Read     |   |

| BITFIELD   | BITS | DESCRIPTION                                                                                                                                                                          | DECODE                                                                                                 |
|------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| CHG_CC     | 7:2  | Sets the fast-charge constant current value, IFAST-CHG.<br><br>This 6-bit configuration is a linear transfer function that starts at 7.5mA and ends at 300mA, with 7.5mA increments. | 0x0 = 7.5mA<br>0x1 = 15.0mA<br>0x2 = 22.5mA<br><br>...<br><br>0x26 = 292.5mA<br>0x27 to 0x3F = 300.0mA |
| T_FAST_CHG | 1:0  | Sets the fast-charge safety timer, tFC.                                                                                                                                              | 0b00 = Timer disabled<br>0b01 = 3 hours<br>0b10 = 5 hours<br>0b11 = 7 hours                            |

**CNFG\_CHG\_F (0x25)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1           | 0 |
|-------------|-------------------|---|---|---|---|---|-------------|---|
| Field       | CHG_CC_JEITA[5:0] |   |   |   |   |   | THM_EN      | – |
| Reset       | 0b000001          |   |   |   |   |   | 0b0         | – |
| Access Type | Write, Read       |   |   |   |   |   | Write, Read | – |

| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                         | DECODE                                                                                                                             |
|--------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|
| CHG_CC_JEITA | 7:2  | <p>Sets I<sub>FAST-CHG-JEITA</sub> for when the battery is either cool or warm as defined by the V<sub>COOL</sub> and V<sub>WARM</sub> temperature thresholds. This register is a don't care if the battery temperature is normal.</p> <p>This 6-bit configuration is a linear transfer function that starts at 7.5mA and ends at 300mA, with 7.5mA increments.</p> | <p>0x0 = 7.5mA<br/>0x1 = 15.0mA<br/>0x2 = 22.5mA<br/>...<br/>0x26 = 292.5mA<br/>0x27 to 0x3F = 300.0mA</p>                         |
| THM_EN       | 1    | Thermistor Enable Bit                                                                                                                                                                                                                                                                                                                                               | <p>0 = Thermistor is disabled.<br/>1 = Thermistor is enabled.</p> <p>Note that the thermistor is powered by the charger input.</p> |

## CNFG\_CHG\_G (0x26)

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1           | 0           |
|-------------|-------------|---|---|---|---|---|-------------|-------------|
| Field       | CHG_CV[5:0] |   |   |   |   |   | USBS        | RSVD        |
| Reset       | 0b000000    |   |   |   |   |   | 0b0         | 0b0         |
| Access Type | Write, Read |   |   |   |   |   | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                       | DECODE                                                                                                                                                                                                                                           |
|----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CHG_CV   | 7:2  | <p>Sets fast-charge battery regulation voltage, V<sub>FAST-CHG</sub>.</p> <p>This 6-bit configuration is a linear transfer function that starts at 3.6V and ends at 4.6V, with 25mV increments.</p> <p>Program V<sub>SYS_REG</sub> to at least 200mV above the higher of V<sub>FAST-CHG</sub> and V<sub>FAST-CHG-JEITA</sub>.</p> | <p>0x0 = 3.600V<br/>0x1 = 3.625V<br/>0x2 = 3.650V<br/>...<br/>0x27 = 4.575V<br/>0x28 to 0x3F = 4.600V</p>                                                                                                                                        |
| USBS     | 1    | Setting this bit places CHGIN in USB suspend mode.                                                                                                                                                                                                                                                                                | <p>0 = CHGIN is not suspended and may draw current from an adapter source.<br/>1 = CHGIN is suspended and may not draw current from an adapter source.</p> <p><b>Note:</b> USBS = 1 results in CHGIN_I interrupt AND CHGIN_DTLS[1:0] = 0b00.</p> |
| RSVD     | 0    | Reserved. Unutilized bit. Write to 0. Reads are don't care.                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                  |

## CNFG\_CHG\_H (0x27)

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1           | 0 |
|-------------|-------------------|---|---|---|---|---|-------------|---|
| Field       | CHG_CV_JEITA[5:0] |   |   |   |   |   | RSVD[1:0]   |   |
| Reset       | 0b000000          |   |   |   |   |   | 0b00        |   |
| Access Type | Write, Read       |   |   |   |   |   | Write, Read |   |



| BITFIELD     | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | DECODE                                                                                                    |
|--------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|
| CHG_CV_JEITA | 7:2  | <p>Sets the modified <math>V_{\text{FAST-CHG-JEITA}}</math> for when the battery is either cool or warm as defined by the <math>V_{\text{COOL}}</math> and <math>V_{\text{WARM}}</math> temperature thresholds. This register is a don't care if the battery temperature is normal.</p> <p>This 6-bit configuration is a linear transfer function that starts at 3.6V and ends at 4.6V, with 25mV increments.</p> <p>Program <math>V_{\text{SYS\_REG}}</math> to at least 200mV above the higher of <math>V_{\text{FAST-CHG}}</math> and <math>V_{\text{FAST-CHG-JEITA}}</math>.</p> | <p>0x0 = 3.600V<br/>0x1 = 3.625V<br/>0x2 = 3.650V<br/>...<br/>0x27 = 4.575V<br/>0x28 to 0x3F = 4.600V</p> |
| RSVD         | 1:0  | Reserved. Unutilized bit. Write to 0. Reads are don't care.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                           |

## CNFG\_CHG\_I (0x28)

| BIT         | 7                      | 6 | 5 | 4 | 3            | 2 | 1 | 0 |
|-------------|------------------------|---|---|---|--------------|---|---|---|
| Field       | IMON_DISCHG_SCALE[3:0] |   |   |   | MUX_SEL[3:0] |   |   |   |
| Reset       | 0xF                    |   |   |   | 0x0          |   |   |   |
| Access Type | Write, Read            |   |   |   | Write, Read  |   |   |   |

| BITFIELD          | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                           | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IMON_DISCHG_SCALE | 7:4  | Selects the battery discharge current full-scale current value.                                                                                                                                                                                                                                                                       | <p>0x0 = 8.2mA<br/>0x1 = 40.5mA<br/>0x2 = 72.3mA<br/>0x3 = 103.4mA<br/>0x4 = 134.1mA<br/>0x5 = 164.1mA<br/>0x6 = 193.7mA<br/>0x7 = 222.7mA<br/>0x8 = 251.2mA<br/>0x9 = 279.3mA<br/>0xA to 0xF = 300.0mA</p>                                                                                                                                                                                                                                                                                                                                                                                               |
| MUX_SEL           | 3:0  | <p>Selects the analog channel to connect to AMUX:</p> <p>Note that the multiplexer consumes current unless it is in the 0b0000 state. When measurements are not needed, make sure to configure <math>MUX\_SEL[3:0] = 0b0000</math>. Also note that for AMUX to operate, the on/off controller must be in the "Resource On" state.</p> | <p>0b0000 = Multiplexer is disabled and AMUX is high-impedance.<br/>0b0001 = CHGIN voltage monitor.<br/>0b0010 = CHGIN current monitor.<br/>0b0011 = BATT voltage monitor.<br/>0b0100 = BATT charge current monitor. Valid only while battery charging is happening (CHG = 1).<br/>0b0101 = BATT discharge current monitor normal measurement.<br/>0b0110 = BATT discharge current monitor nulling measurement.<br/>0b0111 = THM voltage monitor.<br/>0b1000 = TBIAS voltage monitor.<br/>0b1001 = AGND voltage monitor (through 100Ω pulldown resistor).<br/>0b1010 to 0b1111 = SYS voltage monitor.</p> |

**CNFG\_SBB0\_A (0x29)**

| BIT         | 7 | 6            | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|--------------|---|---|---|---|---|---|
| Field       | – | TV_SBB0[6:0] |   |   |   |   |   |   |
| Reset       | – | OTP          |   |   |   |   |   |   |
| Access Type | – | Write, Read  |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                        | DECODE                                                                                                                                                                    |
|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TV_SBB0  | 6:0  | SIMO Buck-Boost Channel 0 Target Output Voltage<br>This 7-bit configuration is a linear transfer function that starts at 0.8V, ends at 5.5V, with 50mV increments. | 0x00 = 0.800V 0x01 = 0.850V 0x02 = 0.900V<br>0x03 = 0.950V 0x04 = 1.000V 0x05 = 1.050V<br>0x06 = 1.100V<br>...<br>0x5C = 5.400V<br>0x5D = 5.450V<br>0x5E to 0x7F = 5.500V |

**CNFG\_SBB0\_B (0x2A)**

| BIT         | 7           | 6           | 5            | 4 | 3           | 2            | 1 | 0 |
|-------------|-------------|-------------|--------------|---|-------------|--------------|---|---|
| Field       | RSVD        | OP_MODE     | IP_SBB0[1:0] |   | ADE_SBB0    | EN_SBB0[2:0] |   |   |
| Reset       | 0b0         | OTP         | OTP          |   | OTP         | OTP          |   |   |
| Access Type | Write, Read | Write, Read | Write, Read  |   | Write, Read | Write, Read  |   |   |

| BITFIELD | BITS | DESCRIPTION                                                 | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------|------|-------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSVD     | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care. |                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| OP_MODE  | 6    | Operation Mode of SBB0                                      | 0 = Buck-boost mode<br>1 = Buck mode                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| IP_SBB0  | 5:4  | SIMO Buck-Boost Channel 0 Peak Current Limit                | 0b00 = 1.000A<br>0b01 = 0.750A<br>0b10 = 0.500A<br>0b11 = 0.333A                                                                                                                                                                                                                                                                                                                                                                                                      |
| ADE_SBB0 | 3    | SIMO Buck-Boost Channel 0 Active-Discharge Enable           | 0 = The active discharge function is disabled. When SBB0 is disabled, its discharge rate is a function of the output capacitance and the external load.<br>1 = The active discharge function is enabled. When SBB0 is disabled, an internal resistor (RAD_SBB0) is activated from SBB0 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal RAD_SBB0 load. |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                  | DECODE                                                                                                                                                                                                                           |
|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EN_SBB0  | 2:0  | <p>Enable Control for SIMO Buck-Boost Channel 0, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off.</p> <p>Prior to enabling the SIMO, program the bias circuits to normal-power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits may be programmed back to low-power mode (SBIA_LPM = 1) to decrease quiescent current.</p> | <p>0b000 = FPS slot 0<br/> 0b001 = FPS slot 1<br/> 0b010 = FPS slot 2<br/> 0b011 = FPS slot 3<br/> 0b100 = Off irrespective of FPS<br/> 0b101 = Same as 0b100<br/> 0b110 = On irrespective of FPS<br/> 0b111 = Same as 0b110</p> |

**CNFG\_SBB1\_A (0x2B)**

| BIT         | 7 | 6            | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|--------------|---|---|---|---|---|---|
| Field       | – | TV_SBB1[6:0] |   |   |   |   |   |   |
| Reset       | – | OTP          |   |   |   |   |   |   |
| Access Type | – | Write, Read  |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                   | DECODE                                                                                                                                                                                       |
|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TV_SBB1  | 6:0  | <p>SIMO Buck-Boost Channel 1 Target Output Voltage</p> <p>This 7-bit configuration is a linear transfer function that starts at 0.8V, ends at 5.5V, with 50mV increments.</p> | <p>0x00 = 0.800V 0x01 = 0.850V 0x02 = 0.900V<br/> 0x03 = 0.950V 0x04 = 1.000V 0x05 = 1.050V<br/> 0x06 = 1.100V<br/> ...<br/> 0x5C = 5.400V<br/> 0x5D = 5.450V<br/> 0x5E to 0x7F = 5.500V</p> |

**CNFG\_SBB1\_B (0x2C)**

| BIT         | 7           | 6           | 5            | 4 | 3           | 2            | 1 | 0 |
|-------------|-------------|-------------|--------------|---|-------------|--------------|---|---|
| Field       | RSVD        | OP_MODE     | IP_SBB1[1:0] |   | ADE_SBB1    | EN_SBB1[2:0] |   |   |
| Reset       | 0b0         | OTP         | OTP          |   | OTP         | OTP          |   |   |
| Access Type | Write, Read | Write, Read | Write, Read  |   | Write, Read | Write, Read  |   |   |

| BITFIELD | BITS | DESCRIPTION                                                 | DECODE                                                                        |
|----------|------|-------------------------------------------------------------|-------------------------------------------------------------------------------|
| RSVD     | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care. |                                                                               |
| OP_MODE  | 6    | Operation Mode of SBB1                                      | <p>0 = Buck-boost mode<br/> 1 = Buck mode</p>                                 |
| IP_SBB1  | 5:4  | SIMO Buck-Boost Channel 1 Peak Current Limit                | <p>0b00 = 1.000A<br/> 0b01 = 0.750A<br/> 0b10 = 0.500A<br/> 0b11 = 0.333A</p> |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                           | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADE_SBB1 | 3    | SIMO Buck-Boost Channel 1 Active-Discharge Enable                                                                                                                                                                                                                                                                                                                                                     | 0 = The active discharge function is disabled. When SBB1 is disabled, its discharge rate is a function of the output capacitance and the external load.<br>1 = The active discharge function is enabled. When SBB1 is disabled, an internal resistor (RAD_SBB1) is activated from SBB1 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal RAD_SBB1 load. |
| EN_SBB1  | 2:0  | Enable control for SIMO buck-boost channel 1, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off.<br><br>Prior to enabling the SIMO, program the bias circuits to normal-power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits may be programmed back to low-power mode (SBIA_LPM = 1) to decrease quiescent current. | 0b000 = FPS slot 0<br>0b001 = FPS slot 1<br>0b010 = FPS slot 2<br>0b011 = FPS slot 3<br>0b100 = Off irrespective of FPS<br>0b101 = Same as 0b100<br>0b110 = On irrespective of FPS<br>0b111 = Same as 0b110                                                                                                                                                                                                                                                           |

## CNFG\_SBB2\_A (0x2D)

| BIT         | 7 | 6            | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|--------------|---|---|---|---|---|---|
| Field       | — | TV_SBB2[6:0] |   |   |   |   |   |   |
| Reset       | — | OTP          |   |   |   |   |   |   |
| Access Type | — | Write, Read  |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                        | DECODE                                                                                                                                                                        |
|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TV_SBB2  | 6:0  | SIMO Buck-Boost Channel 2 Target Output Voltage<br>This 7-bit configuration is a linear transfer function that starts at 0.8V, ends at 5.5V, with 50mV increments. | 0x00 = 0.800V 0x01 = 0.850V 0x02 = 0.900V<br>0x03 = 0.950V 0x04 = 1.000V 0x05 = 1.050V<br>0x06 = 1.100V<br><br>...<br>0x5C = 5.400V<br>0x5D = 5.450V<br>0x5E to 0x7F = 5.500V |

## CNFG\_SBB2\_B (0x2E)

| BIT         | 7           | 6                                                           | 5            | 4 | 3           | 2            | 1 | 0 |
|-------------|-------------|-------------------------------------------------------------|--------------|---|-------------|--------------|---|---|
| Field       | RSVD        | OP_MODE                                                     | IP_SBB2[1:0] |   | ADE_SBB2    | EN_SBB2[2:0] |   |   |
| Reset       | 0b0         | OTP                                                         | OTP          |   | OTP         | OTP          |   |   |
| Access Type | Write, Read | Write, Read                                                 | Write, Read  |   | Write, Read | Write, Read  |   |   |
| BITFIELD    | BITS        | DESCRIPTION                                                 |              |   | DECODE      |              |   |   |
| RSVD        | 7           | Reserved. Unutilized bit. Write to 0. Reads are don't care. |              |   |             |              |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                           | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OP_MODE  | 6    | Operation Mode of SBB2                                                                                                                                                                                                                                                                                                                                                                                | 0 = Buck-boost mode<br>1 = Buck mode                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| IP_SBB2  | 5:4  | SIMO Buck-Boost Channel 2 Peak Current Limit                                                                                                                                                                                                                                                                                                                                                          | 0b00 = 1.000A<br>0b01 = 0.750A<br>0b10 = 0.500A<br>0b11 = 0.333A                                                                                                                                                                                                                                                                                                                                                                                                      |
| ADE_SBB2 | 3    | SIMO Buck-Boost Channel 2 Active-Discharge Enable                                                                                                                                                                                                                                                                                                                                                     | 0 = The active discharge function is disabled. When SBB2 is disabled, its discharge rate is a function of the output capacitance and the external load.<br>1 = The active discharge function is enabled. When SBB2 is disabled, an internal resistor (RAD_SBB2) is activated from SBB2 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal RAD_SBB2 load. |
| EN_SBB2  | 2:0  | Enable control for SIMO buck-boost channel 2, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off.<br><br>Prior to enabling the SIMO, program the bias circuits to normal power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits may be programmed back to low power mode (SBIA_LPM = 1) to decrease quiescent current. | 0b000 = FPS slot 0<br>0b001 = FPS slot 1<br>0b010 = FPS slot 2<br>0b011 = FPS slot 3<br>0b100 = Off irrespective of FPS<br>0b101 = Same as 0b100<br>0b110 = On irrespective of FPS<br>0b111 = Same as 0b110                                                                                                                                                                                                                                                           |

## CNFG\_SBB\_TOP (0x2F)

| BIT         | 7              | 6 | 5 | 4 | 3 | 2 | 1            | 0 |
|-------------|----------------|---|---|---|---|---|--------------|---|
| Field       | ICHGIN_LIM_DEF | – | – | – | – | – | DRV_SBB[1:0] |   |
| Reset       | OTP            | – | – | – | – | – | OTP          |   |
| Access Type | Write, Read    | – | – | – | – | – | Write, Read  |   |

| BITFIELD       | BITS | DESCRIPTION                                                                                                 | DECODE                                                                                                                                     |
|----------------|------|-------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| ICHGIN_LIM_DEF | 7    | Changes how CNFG_CHG_B.ICHGIN_LIM is interpreted.                                                           | See CNFG_CHG_B.ICHGIN_LIM for more details.                                                                                                |
| DRV_SBB        | 1:0  | SIMO Buck-Boost (all channels) Drive Strength Trim. See the <i>Drive Strength</i> section for more details. | 0b00 = Fastest transition time<br>0b01 = A little slower than 0b00<br>0b10 = A little slower than 0b01<br>0b11 = A little slower than 0b10 |

## CNFG\_LDO0\_A (0x38)

| BIT         | 7           | 6            | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|--------------|---|---|---|---|---|---|
| Field       | RSVD        | TV_LDO0[6:0] |   |   |   |   |   |   |
| Reset       | 0b0         | OTP          |   |   |   |   |   |   |
| Access Type | Write, Read | Write, Read  |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                       | DECODE                                                                                                                                                            |
|----------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSVD     | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care.                                                                                       |                                                                                                                                                                   |
| TV_LDO0  | 6:0  | LDO Target Output Voltage<br>This 7-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.975V, with 25mV increments. | 0x00 = 0.800V 0x01 = 0.825V 0x02 = 0.850V<br>0x03 = 0.875V 0x04 = 0.900V 0x05 = 0.925V<br>0x06 = 0.950V<br>...<br>0x7D = 3.925V<br>0x7E = 3.950V<br>0x7F = 3.975V |

**CNFG\_LDO0\_B (0x39)**

| BIT         | 7 | 6 | 5 | 4           | 3           | 2            | 1 | 0 |
|-------------|---|---|---|-------------|-------------|--------------|---|---|
| Field       | – | – | – | LDO0_MD     | ADE_LDO0    | EN_LDO0[2:0] |   |   |
| Reset       | – | – | – | OTP         | OTP         | OTP          |   |   |
| Access Type | – | – | – | Write, Read | Write, Read | Write, Read  |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO0_MD  | 4    | Operation Mode of LDO0                                                                                                                     | 0 = Low dropout linear regulator (LDO) mode<br>1 = Load switch (LSW) mode                                                                                                                                                                                                                                                                                                                                                                                                  |
| ADE_LDO0 | 3    | LDO0 Active-Discharge Enable                                                                                                               | 0 = The active discharge function is disabled.<br>When LDO0 is disabled, its discharge rate is a function of the output capacitance and the external load.<br>1 = The active discharge function is enabled.<br>When LDO0 is disabled, an internal resistor (RAD_LDO0) is activated from LDO0 to GND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal RAD_LDO0 load. |
| EN_LDO0  | 2:0  | Enable Control for LDO0, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off. | 0b000 = FPS slot 0<br>0b001 = FPS slot 1<br>0b010 = FPS slot 2<br>0b011 = FPS slot 3<br>0b100 = Off irrespective of FPS<br>0b101 = Same as 0b100<br>0b110 = On irrespective of FPS<br>0b111 = Same as 0b110                                                                                                                                                                                                                                                                |

**CNFG\_LDO1\_A (0x3A)**

| BIT         | 7           | 6            | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|--------------|---|---|---|---|---|---|
| Field       | RSVD        | TV_LDO1[6:0] |   |   |   |   |   |   |
| Reset       | 0b0         | OTP          |   |   |   |   |   |   |
| Access Type | Write, Read | Write, Read  |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                       | DECODE                                                                                                                                                            |
|----------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSVD     | 7    | Reserved. Unutilized bit. Write to 0. Reads are don't care.                                                                                       |                                                                                                                                                                   |
| TV_LDO1  | 6:0  | LDO Target Output Voltage<br>This 7-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.975V, with 25mV increments. | 0x00 = 0.800V 0x01 = 0.825V 0x02 = 0.850V<br>0x03 = 0.875V 0x04 = 0.900V 0x05 = 0.925V<br>0x06 = 0.950V<br>...<br>0x7D = 3.925V<br>0x7E = 3.950V<br>0x7F = 3.975V |

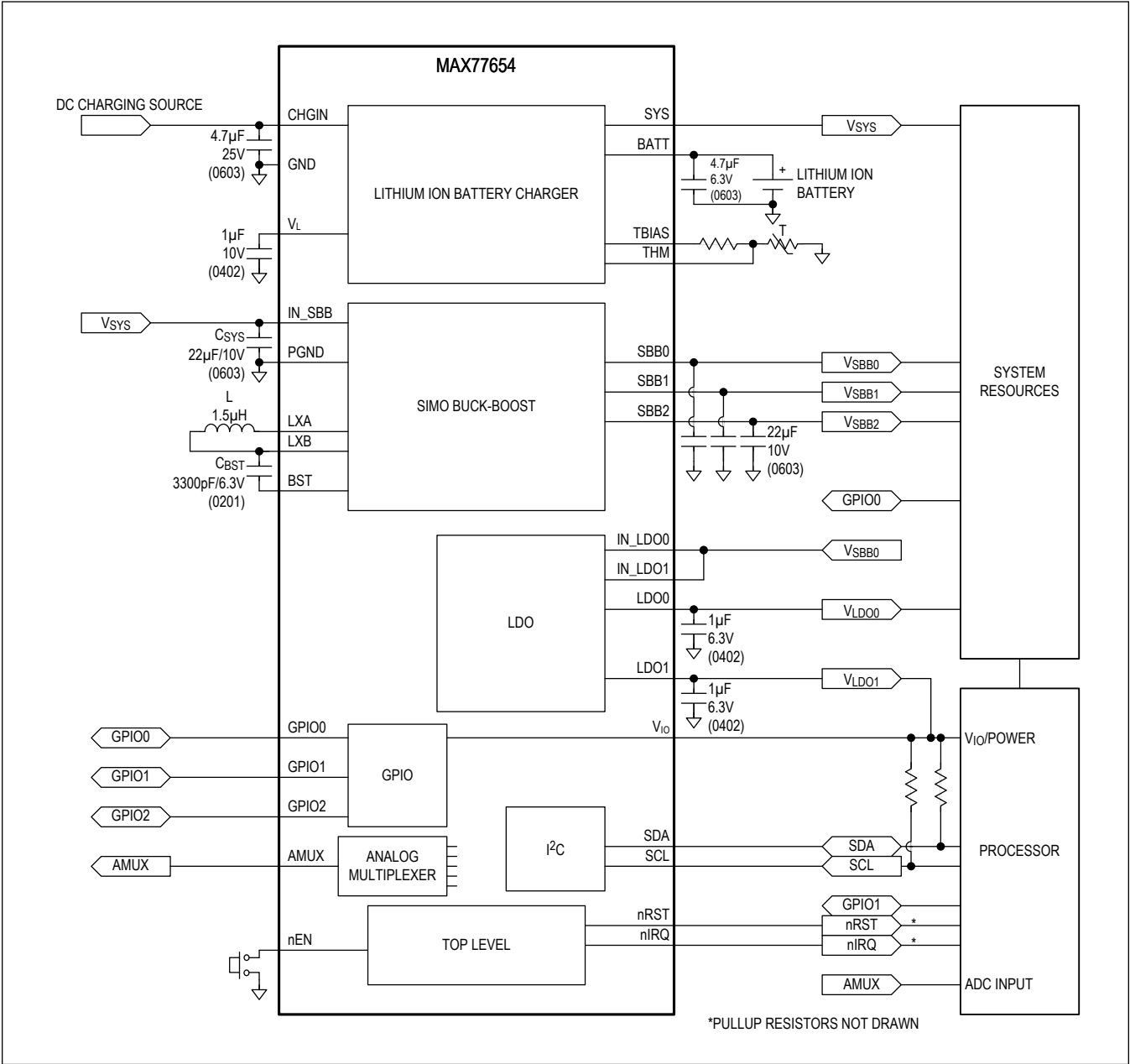
#### CNFG\_LDO1\_B (0x3B)

| BIT         | 7 | 6 | 5 | 4           | 3           | 2            | 1 | 0 |
|-------------|---|---|---|-------------|-------------|--------------|---|---|
| Field       | – | – | – | LDO1_MD     | ADE_LDO1    | EN_LDO1[2:0] |   |   |
| Reset       | – | – | – | OTP         | OTP         | OTP          |   |   |
| Access Type | – | – | – | Write, Read | Write, Read | Write, Read  |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO1_MD  | 4    | Operation Mode of LDO1                                                                                                                     | 0 = Low dropout linear regulator (LDO) mode<br>1 = Load switch (LSW) mode                                                                                                                                                                                                                                                                                                                                                                                                                           |
| ADE_LDO1 | 3    | LDO1 Active-Discharge Enable                                                                                                               | 0 = The active discharge function is disabled.<br>When LDO1 is disabled, its discharge rate is a function of the output capacitance and the external load.<br>1 = The active discharge function is enabled.<br>When LDO1 is disabled, an internal resistor (R <sub>AD_LDO1</sub> ) is activated from LDO1 to GND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R <sub>AD_LDO1</sub> load. |
| EN_LDO1  | 2:0  | Enable control for LDO1, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off. | 0b000 = FPS slot 0<br>0b001 = FPS slot 1<br>0b010 = FPS slot 2<br>0b011 = FPS slot 3<br>0b100 = Off irrespective of FPS<br>0b101 = Same as 0b100<br>0b110 = On irrespective of FPS<br>0b111 = Same as 0b110                                                                                                                                                                                                                                                                                         |

Typical Application Circuits

Typical Applications Circuit





## MAX77654

Ultra-Low Power PMIC Featuring Single-Inductor,  
3-Output Buck-Boost, 2-LDOs, Power-Path  
Charger for Small Li+, and Ship Mode

### Ordering Information

| PART             | TEMP RANGE     | PIN-PACKAGE | OPTIONS                 |
|------------------|----------------|-------------|-------------------------|
| MAX77654ENV+T*   | -40°C to +85°C | 30 WLP      |                         |
| MAX77654AENV+T   | -40°C to +85°C | 30 WLP      | <a href="#">Table 3</a> |
| MAX77654BENV+T   | -40°C to +85°C | 30 WLP      | <a href="#">Table 3</a> |
| MAX77654CENV+T** | -40°C to +85°C | 30 WLP      | <a href="#">Table 3</a> |
| MAX77654DENV+T   | -40°C to +85°C | 30 WLP      | <a href="#">Table 3</a> |
| MAX77654MENV+T   | -40°C to +85°C | 30 WLP      | <a href="#">Table 3</a> |
| MAX77654ENVN+T*  | -40°C to +85°C | 30 WLP      |                         |
| MAX77654AENVN+T  | -40°C to +85°C | 30 WLP      | <a href="#">Table 3</a> |

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

\*Custom samples only. Not for production or stock. Contact factory for more information.

\*\*Future product—[contact factory](#) for availability.

MAX77654

Ultra-Low Power PMIC Featuring Single-Inductor,  
3-Output Buck-Boost, 2-LDOs, Power-Path  
Charger for Small Li+, and Ship Mode

## Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | PAGES<br>CHANGED                                                                        |
|--------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 0                  | 5/19             | Initial release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | —                                                                                       |
| 1                  | 7/19             | Updated part decode in Table 3 and <i>Ordering Information</i> table                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 34, 35, 114                                                                             |
| 2                  | 2/20             | Fixed typographical errors, updated <i>Absolute Maximum Ratings</i> , <i>Electrical Characteristics</i> tables, <i>Typical Operating Characteristics</i> 6, 32, 42, 45, <i>Pin Description</i> table, Table 3, <i>Support Material</i> section, Figure 2, <i>Detailed Description—Global Resources</i> section, Figure 3, <i>nEN Internal Pullup Resistors to V<sub>CCINT</sub></i> section, Figure 4, <i>SIMO Features and Benefits</i> section, <i>SIMO Buck Mode</i> section, Table 15, <i>Inductor Selection</i> section, Figures 21, 22, and 23, <i>Summary</i> section, and <i>Ordering Information</i> table | 9-14, 19,<br>21-23, 26,<br>27, 30, 31,<br>34-39, 66,<br>68-70,<br>72-74, 76,<br>81, 113 |

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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