Click here for production status of specific part numbers.

MAX15162

8V to 60V Smart Dual 1.5A Circuit Breaker with Accurate Current Monitoring

General Description

The MAX15162/MAX15162A devices are dual-channel, circuit-breaker ICs. The devices integrate a dual-channel controller with dual 140mΩ (in WLP, 180mΩ in TQFN) power MOSFETs and electronic circuit-breaker protection in a single package.

These devices feature constant power control during start-up to keep the MOSFET operating under Safe Operating Area (SOA). The devices provide robust overcurrent protection with programmable current-limit level, and adjustable overcurrent shutdown delay for better immunity against system noises and load transient. The current monitoring pins provide a current sense accuracy of ±3% for each channel. When there is short-circuit at the output, a fast current limit comparator turns off MOSFETs within 200ns to isolate the load from the input. During a fault condition, the MAX15162A enters auto-retry mode and the MAX15162 enters latch off mode. For both devices, the ALRT pin asserts a fault indication. The MAX15162/MAX15162A can be configured as two independent channels or two parallel channels for one common output.

The devices feature a number of protection features including; IN-to-OUT short-circuit protection, output short-circuit protection, startup watchdog timer, input undervoltage lockout and internal overtemperature protection.

The MAX15162/MAX15162A are available in a 24-pin, 4mm x 4mm TQFN package and 16-bump, 2mm x 2mm WLP package and are rated over the -40°C to +105°C operation temperature range.

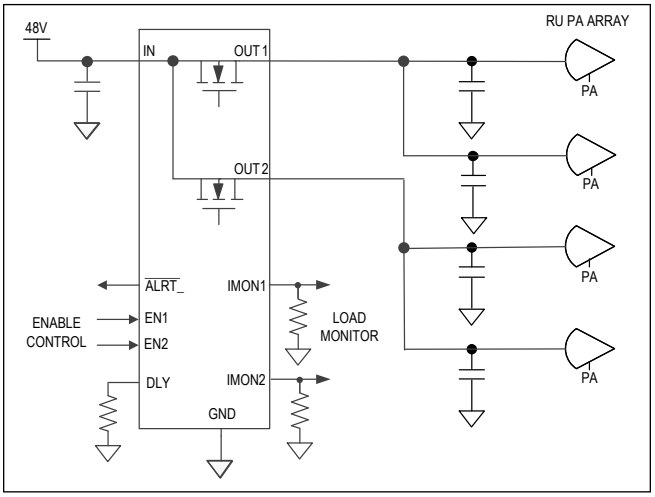
Applications

- Radio Access Point System
- Communication
- Industrial

Benefits and Features

- 8V to 60V Wide Input Voltage Range
- Integrated Dual-Power MOSFET
- Turn-On Resistance 140mΩ (WLP), 180mΩ (TQFN) MOSFET
- Dual-Channel Independent or Parallel Mode Configuration
- ± 3% Accuracy Current Reporting on Individual Channel
- Enable Inputs for Individual Channels
- Constant Power Control at Startup
- Startup Watchdog Timer
- Startup IN-to-OUT Short Protection
- Undervoltage-Lockout
- Overcurrent and Overtemperature Fault Status indication
- Multilevel Overcurrent Limit Protection
- Built in Thermal Shutdown Protection
- Programmable Current Limiting Level
- Programmable Overcurrent Shut-down Delay time
- Programmable Auto-Retry Time (MAX15162A)
- Latch Off in a Fault Event (MAX15162)
- Auto-retry in a Fault Event (MAX15162A)
- 24-pin, 4mm x 4mm TQFN or 16-bump, 2mm x 2mm WLP

Simplified Block Diagram



maxim integrated™

Absolute Maximum Ratings

IN_ to GND ..... -0.3V to +65V
OUT_ to GND ..... -0.3 V to (IN_+ 0.3)V
EN_, ALRT_, IMON_, DLY to GND ..... -0.3 V to +6V
Operating Junction Temperature Range ..... -40°C to +125°C
TQFN (Derate 25.6 mW/°C above +70°C) 2000mW
WLP (Derate 20.4mW/°C above +70°C) 1632mW
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W161M1+1
Outline Number	21-100353
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49°C/W
Junction to Case (θ_{JC})	9.45°C/W

24 TQFN

Package Code	T2444+2C
Outline Number	21-0139
Land Pattern Number	90-0020
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	39°C/W
Junction to Case (θ_{JC})	6°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 8V to 60V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{IN} = 48V, C_{OUT} = 22µF, T_A = +25°C, R_{IMON1} = 3.01kΩ, R_{IMON2} = 3.01kΩ, R_{DLY} = 68kΩ (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
IN Voltage Range	V_{IN}		8		60	V
Shutdown Input Current	I_{SHDN}	V_{EN1} = 0V, V_{EN2} = 0V, V_{IN} = 48V		32	90	µA
Shutdown OUT Current	I_{OFF}	V_{EN1} = V_{EN2} = 0V; V_{OUT} = 0.1V; T_A = +25°C	-2			µA
Supply Current	I_{IN}	V_{IN} = V_{OUT} = 48V,		0.88	1.5	mA
UVLO						
UVLO Trip Level	V_{UVLO}	V_{IN} falling, UVLO trip point		7.1		
		V_{IN} rising		7.58	7.9	V
UVLO Hysteresis				500		mV
EN_						
EN_ Input Logic-High	V_{EN_IH}		1.4			V
EN_ Input Logic-Low	V_{EN_IL}				0.4	V
EN_ Pullup Voltage	V_{EN_PUP}	EN_ pin unconnected, V_{IN} = 60V			2.35	V
EN_ Input Current	I_{EN_IN}	$V_{EN_}$ = 5.5V	-1		+1	µA
EN_ Pullup Current	I_{EN_PUP}	$V_{EN_}$ = 0.4V	1	4.5	12	µA
INTERNAL FETs						
Internal FETs On-Resistance	R_{DSON}	V_{IN} ≥ 10V, I_{OUT} = 100mA, T_A = +25ºC, TQFN Package		180		mΩ
		V_{IN} ≥ 10V, I_{OUT} = 100mA, T_A = +25ºC, WLP Package		140		
CURRENT LIMIT						
Current Limit Range	I_{LIM}		0.5		1.5	A
Current Limit Accuracy	I_{LIM_ACC}	T_A = -40°C to 105°C, 0.5A ≤ I_{LIM_ACC} ≤ 1.5A	-5		+5	%
Fast Current Limit Range	I_{LIM_F}	133% x I_{LIM}	0.66		2	A
Fast Current Limit Accuracy		0.66A ≤ I_{LIM_F} ≤ 2A	-10		+10	%
Fast Current Limit Shut Down Time	T_{LIM_F}			200		ns
Average Inrush Current	I_{INRUSH}	During initial turn-on period, V_{IN} - V_{OUT} > 0.7V		28		mA
IMON_						
IMON_ Reference	V_{REF}			1.125		V
Current-Mirror Output Ratio	C_{IRATIO}	0.05A ≤ I_{OUT} ≤ 1.5A		4000		A/A

Electrical Characteristics (continued)

(V_{IN} = 8V to 60V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{IN} = 48V, C_{OUT} = 22µF, T_A = +25°C, R_{IMON1} = 3.01kΩ, R_{IMON2} = 3.01kΩ, R_{DLY} = 68kΩ (Note 1))

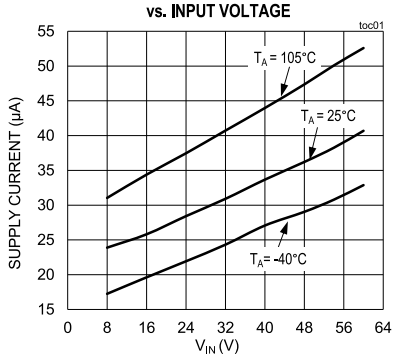
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Sense Accuracy	I_{SENS_ACC}	T_A = -40°C to +105°C	0.05A ≤ I_{SENS_ACC} < 0.5A	-12.5		+12.5	%
			0.5A ≤ I_{SENS_ACC} ≤ 1.5A	-3		+3	
IMON_ Leakage Current	I_{IMON_L}	V_{EN1} = V_{EN2} = 0V		-1		+1	µA
TIMING							
Startup Watchdog Timeout	T_{SU}				250		ms
Switch Turn-On Time	T_{ON_SWITCH}	V_{IN} = 48V, C_{OUT} = 22µF			37		ms
IN Debounce Time	T_{DEB}	V_{IN} > V_{IN_UVLO} and EN = High			16		ms
Current Limit Delay Time	T_{DELAY}	R_{DLY} = 0		7	12	17	µs
		R_{DLY} = 28kΩ		80	110	130	
		R_{DLY} = 47.5kΩ		0.8	1	1.2	ms
		R_{DLY} = 68.1kΩ		8	10	12	
Auto-retry Time	T_{RETRY}				60 X T_{DELAY}		ms
$\overline{ALRT}$							
$\overline{ALRT}$ De-assertion Threshold	$V_{\overline{ALRT}}$	Measured V_{IN} - V_{OUT}			2.1		V
$\overline{ALRT}$ Assertion Delay	$T_{\overline{ALRT}}$	I_{OUT} reaches Current Limit			6		us
$\overline{ALRT}$ Output Low Voltage	$V_{\overline{ALRT}_OL}$	Low-Impedance State, $I_{\overline{ALRT}}$ = 1mA				0.4	V
$\overline{ALRT}$ Output High Leakage Current	$I_{\overline{ALRT}_OH}$	High-Impedance State, $V_{\overline{ALRT}}$ = 5.5V			1		uA
THERMAL PROTECTION							
Thermal Shutdown	T_{J_MAX}				156		°C
Thermal-Shutdown Hysteresis					20		°C

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating-temperature range are guaranteed by design; not production tested.

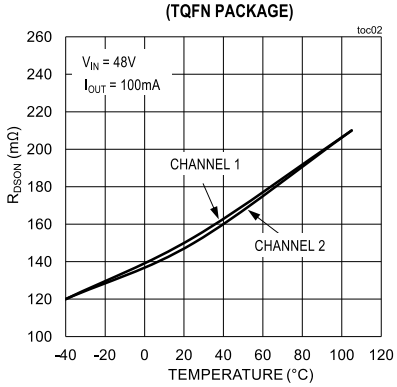
Typical Operating Characteristics

(V_{IN} = 8V to 60V, T_A = -40°C to +105°C, C_{OUT} = 4 x 4.7µF per channel, V_{EN1} = 3.3V, V_{EN2} = 3.3V, ALRT = OPEN, R_{IMON1} = 3.01kΩ, R_{IMON2} = 3.01kΩ, R_{DLY} = 68kΩ. Unless otherwise noted.)

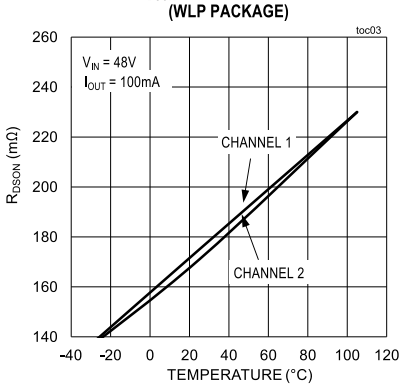
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



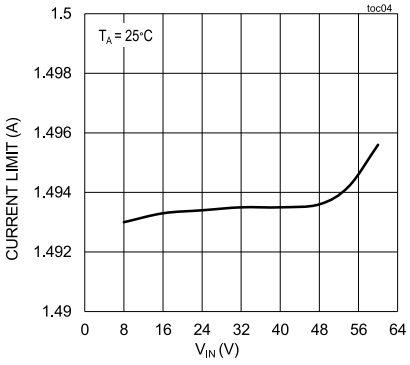
RDSON vs. TEMPERATURE (TQFN PACKAGE)



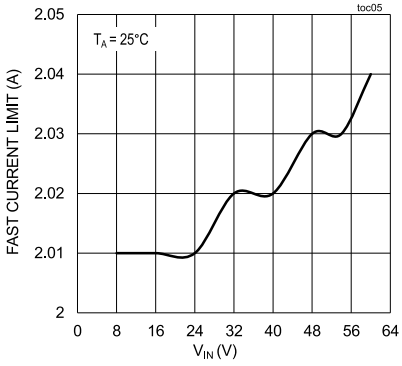
RDSON vs. TEMPERATURE (WLP PACKAGE)



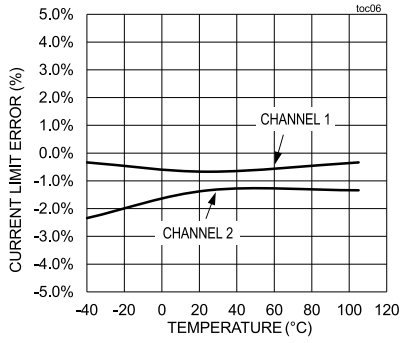
CURRENT LIMIT vs. INPUT VOLTAGE ($R_{IMON_}$ = 3.01kΩ, INDEPENDENT MODE)



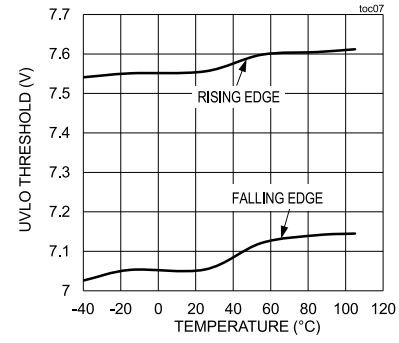
FAST CURRENT LIMIT vs. INPUT VOLTAGE ($R_{IMON_}$ = 3.01kΩ, INDEPENDENT MODE)



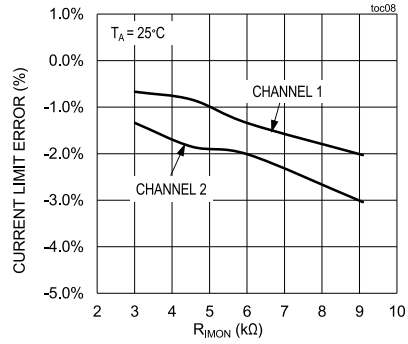
CURRENT LIMIT ERROR vs. TEMPERATURE (at V_{IN} = 48V, R_{IMON1} = R_{IMON2} = 3.01kΩ)



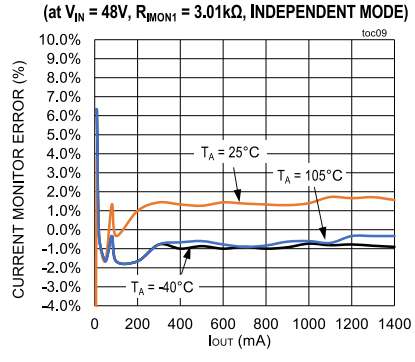
UVLO THRESHOLD vs. TEMPERATURE



CURRENT LIMIT ERROR vs. R_{IMON} (at VIN = 48V, INDEPENDENT MODE)



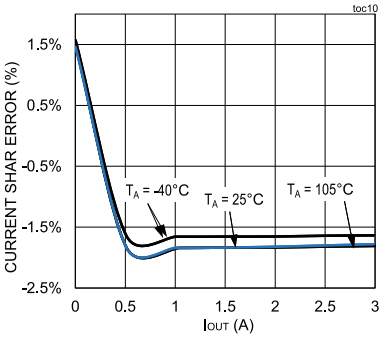
IMON1 PIN CURRENT MONITOR ERROR vs. I_{OUT} (at V_{IN} = 48V, R_{IMON1} = 3.01kΩ, INDEPENDENT MODE)



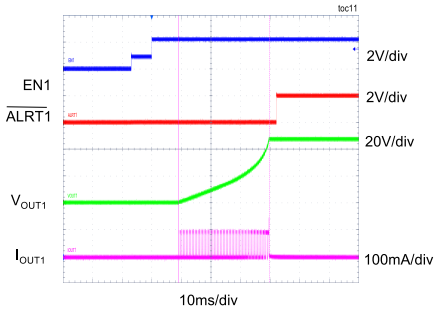
Typical Operating Characteristics (continued)

(V_{IN} = 8V to 60V, T_A = -40°C to +105°C, C_{OUT} = 4 x 4.7µF per channel, V_{EN1} = 3.3V, V_{EN2} = 3.3V, ALRT = OPEN, R_{IMON1} = 3.01kΩ, R_{IMON2} = 3.01kΩ, R_{DLY} = 68kΩ. Unless otherwise noted.)

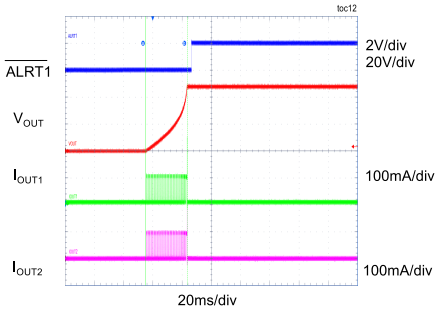
CURRENT SHARE ERROR vs. I_{OUT}
(at V_{IN} = 48V, $R_{IMON1/2}$ = 3.01kΩ, PARALLEL MODE)



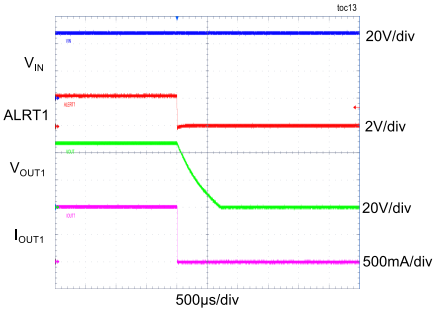
POWER-UP RESPONSE
IN INDEPENDENT MODE



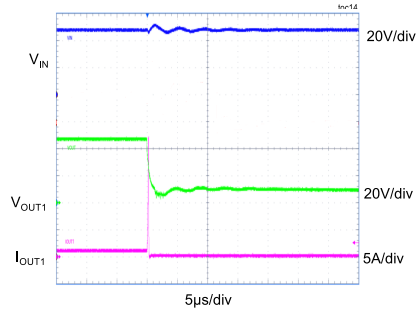
POWER-UP RESPONSE
IN PARALLEL MODE



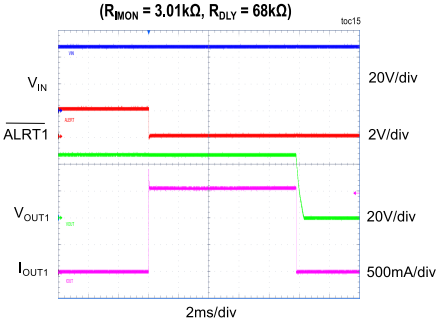
THERMAL SHUTDOWN



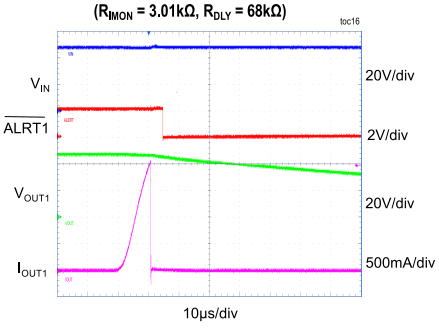
OUTPUT SHORT-CIRCUIT RESPONSE



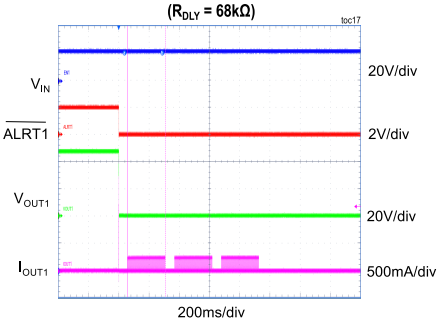
CURRENT LIMIT RESPONSE
(R_{IMON} = 3.01kΩ, R_{DLY} = 68kΩ)



FAST CURRENT LIMIT RESPONSE
(R_{IMON} = 3.01kΩ, R_{DLY} = 68kΩ)

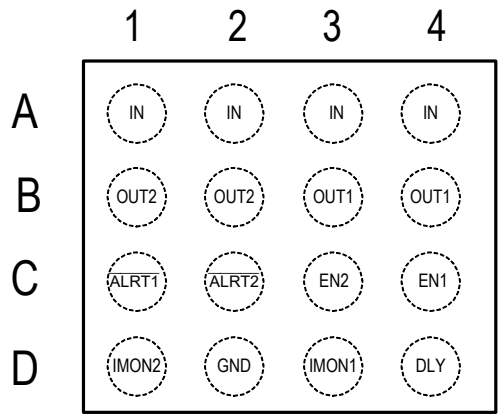


AUTO-RETRY
AFTER FAST OCP SHUT DOWN
(R_{DLY} = 68kΩ)



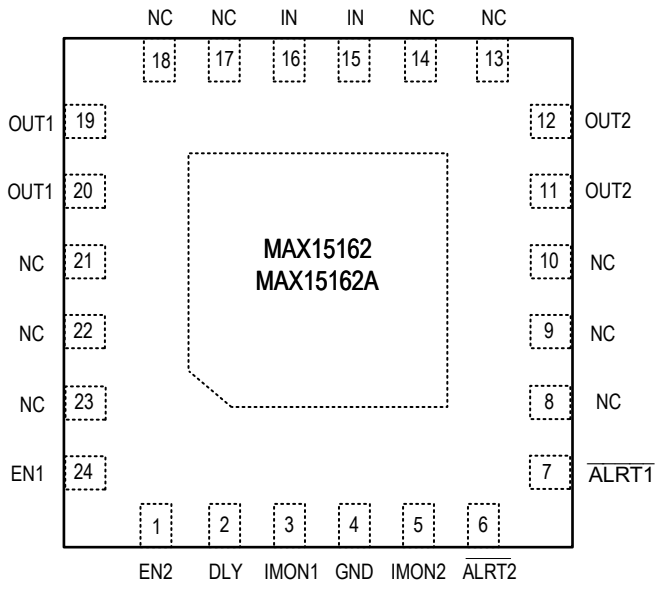
Pin Configurations

16 WLP



MAX15162/MAX15162A
(2mm x 2mm)
Top View

24 TQFN



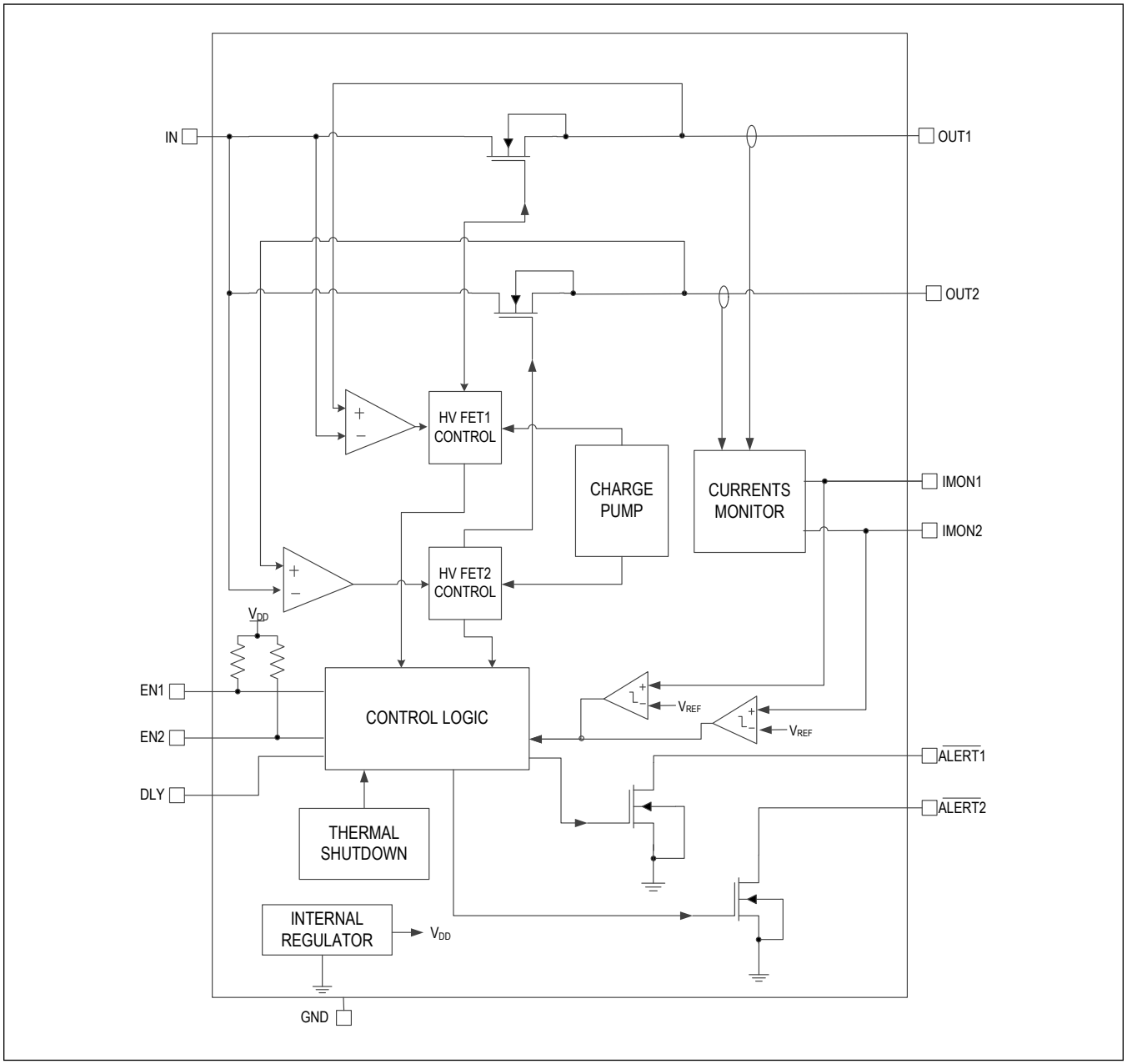
(4mm x 4mm)
Top View

Pin Description

PIN		NAME	FUNCTION
16 WLP	24 TQFN		
A1, A2, A3, A4	15,16	IN	Supply Voltage Input. IN is connected to the drain of internal MOSFET. Apply at least 1µF capacitor at IN. Bypass IN with a transient voltage-suppressor diode to GND for clamping inductive transients in the case of fast output short event.
B3, B4	19, 20	OUT1	Power Output 1. Source of the internal power MOSFET1. In parallel mode It shall be connected to OUT2 to scale the current capability.
B1, B2	11, 12	OUT2	Power Output 2. Source of the internal power MOSFET2. In parallel mode, it should be connected to OUT1 to scale the current capability.
D3	3	IMON1	Current Limit Threshold Setting and Current Monitor Output for Channel 1. This pin sources a scaled-down internal MOSFET current. Connect a resistor to GND to set current limit threshold between 0.5A and 1.5A, and convert current to voltage for current motoring. This pin can not be floating.
D1	5	IMON2	Current Limit Threshold Setting and Current Monitor Output for Channel 2. This pin sources a scaled-down internal MOSFET current. Connect a resistor to GND to set current limit threshold between 0.5A and 1.5A, and convert current to voltage for current motoring. This pin can not be floating.
C4	24	EN1	Active-High Enable Input 1. Internally pulled up to 2V. The pin can be also externally pulled up to logic-high state to enable the output 1.
C3	1	EN2	Active-High Enable Input 2. Internally pulled up to 2V. The pin can be also externally pulled up to logic-high state to enable the output 2.
C1	7	$\overline{\text{ALRT1}}$	$\overline{\text{ALRT1}}$ Status Output for Channel 1. Open-drain output. $\overline{\text{ALRT1}}$ pin de-asserts when the channel 1 MOSFET is fully turned on. $\overline{\text{ALRT1}}$ pin asserts when these events occur—output 1 is disabled, current limit event, overtemperature event, startup watchdog timer times out, startup configuration fault. Leave $\overline{\text{ALRT1}}$ unconnected if unused.
C2	6	$\overline{\text{ALRT2}}$	$\overline{\text{ALRT2}}$ Status Output for Channel 2. Open-drain output. $\overline{\text{ALRT2}}$ pin de-asserts when the channel 2 MOSFET is fully turned on. $\overline{\text{ALRT2}}$ pin asserts when these events occur—output 2 is disabled, current limit event, overtemperature event, startup watchdog timer times out, startup configuration fault. Leave $\overline{\text{ALRT2}}$ unconnected if unused.
D4	2	DLY	Overcurrent Shutdown Delay Setting. Connect a resistor to GND to configure shut down delay to be 12µs, 100µs, 1ms, 10ms in current limit event.
D2	4	GND	Ground.
—	—	EP	Exposed Pad. Connect EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX15162 EV kit data sheet for a reference layout design.

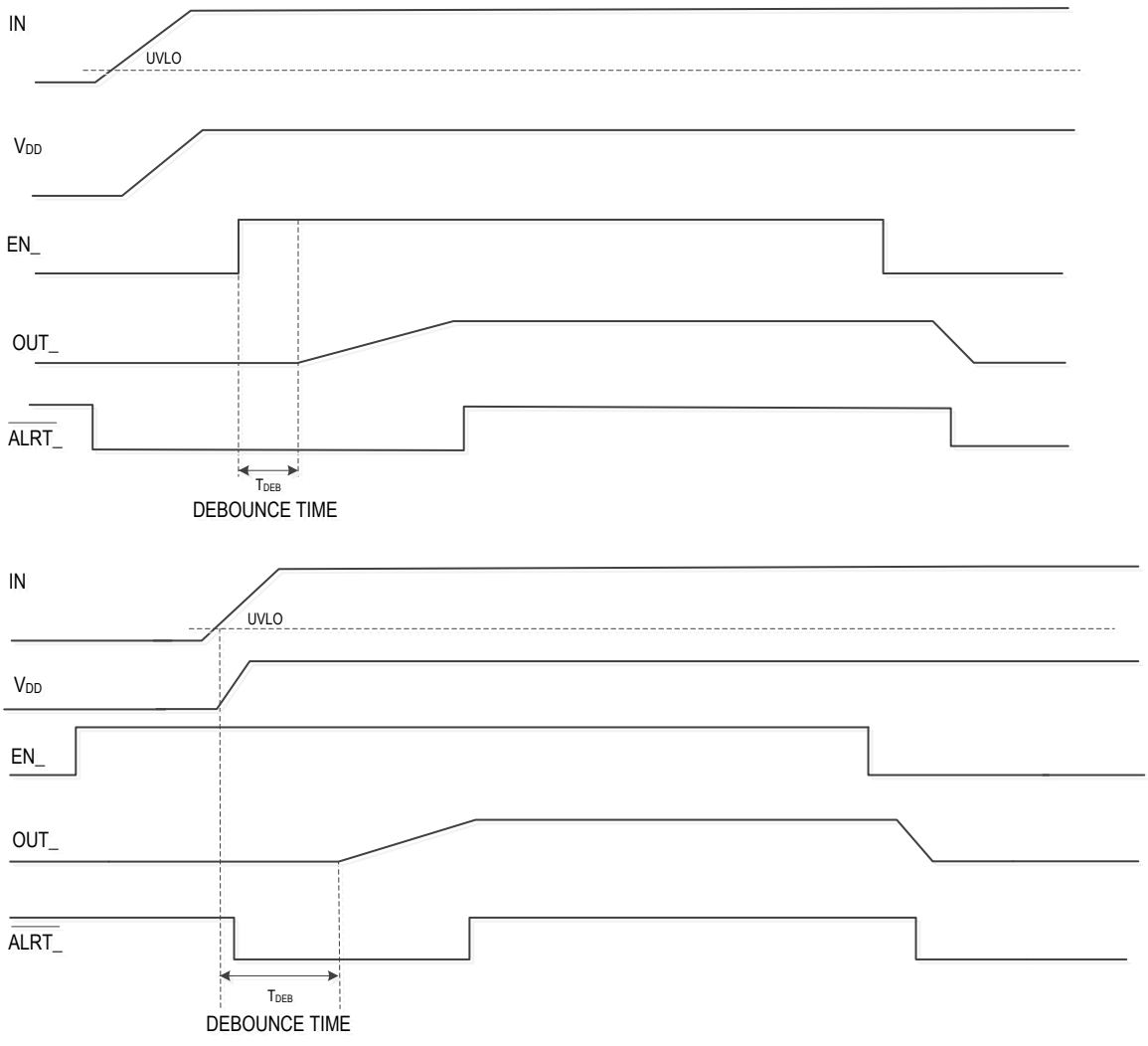
Functional Diagrams

Block Diagram



Functional Diagrams (continued)

Timing Diagram



NOTE: V_{DD} IS INTERNAL REGULATOR VOLTAGE.

Detailed Description

Overview

The MAX15162/MAX15162A are 8V to 60V integrated, dual-channel circuit breaker devices. The dual channels can be configured as independent mode, or parallel mode to scale up the current capability. The devices feature constant power control during startup process to ensure MOSFETs operating under Safe Operating Area (SOA). The programmable current limit and adjustable shutdown time for current limit event provide flexibility for various applications with different power levels. The fast overcurrent protection can shut down the MOSFET within 200ns when a larger current or short-circuit occurs at the output. The ±3% current monitoring over the input and temperature change can provide accurate current information to the system. The $\overline{ALRT}$ response indicates the output and fault status, and it asserts when

- The output is disabled
- Current limit occurs
- Overtemperature occurs
- Startup watchdog times out
- Configuration fault occurs.

The active-high EN pin functions make enable/disable easy to control. The input and EN debounce protection prevent the MOSFET turning on from noisy or transitioning input or EN signals. The IN-to-OUT short-circuit protection prevents the MOSFET from turning on when the MOSFET is shorted or the input and output are in shorted condition. The devices provide a choice of auto-retry or latch-off mode during fault events based on MAX15162A or MAX15162.

Startup

The devices are designed to power-up the output with constant power control by actively monitoring the MOSFET power and limiting the startup current. The startup current is a series of pulsating current whose duty cycles are controlled by constant power limit circuit. The averaged startup current with constant power control is approximately 28mA. This scheme is to ensure the internal MOSFET operate within SOA during the startup. Once the output ramps up to be within 700mV of the input voltage, the MOSFET is switched to constant current control to expedite the startup process. When the MOSFET is fully turned on, the current limit is switched to programmable normal operation current limit threshold.

An internal watchdog timer starts counting when the devices enter the startup phase. The devices complete the startup phase, de-assert $\overline{ALRT}$ pin and enter normal operation mode once V_{IN} - V_{OUT} < 700mV. If the watchdog timer elapses and V_{IN} - V_{OUT} is still greater than 700mV, the MOSFET will be turned off and the devices enter auto-retry mode in the MAX15162A or latch mode in the MAX15162. When the auto-retry time elapses the part will restart the power-up process. The thermal-protection circuit is always active and the MOSFET will be immediately turned off when the thermal-shutdown threshold is reached.

Startup in Overload or Short-Circuit Condition

When the device powers up the MOSFET with a very large load or short circuit at the output, the duty cycles of the pulsating startup current is limited to initial values to ensure the power dissipation is not overheating the device . While the output is shorted to GND, the MOSFET will be turned off once the startup watchdog timer times out in 250ms. The device then restarts the power-up process in auto-retry mode (MAX15162A), or latches off the MOSFET until EN is toggled or the input is cycled to cross UVLO (MAX15162).

Undervoltage Lockout (UVLO)

The devices feature an undervoltage lockout functionality. When the input voltage falls below V_{UVLO} the internal MOSFET is turned off immediately and $\overline{ALRT}$ pin asserts to indicate the fault condition. The UVLO comparator has a hysteresis of 500mV (typ).

Input Debounce Protection

The devices feature an input debounce protection in startup process to prevent the MOSFET from turning on from noisy and transitioning input. The devices start to ramp up the output (turn on the internal MOSFETs) only when the input voltage is higher than UVLO threshold and EN is pulled high for a period that is greater than the debounce time (T_{DEB}). The T_{DEB} time elapses only at startup process.

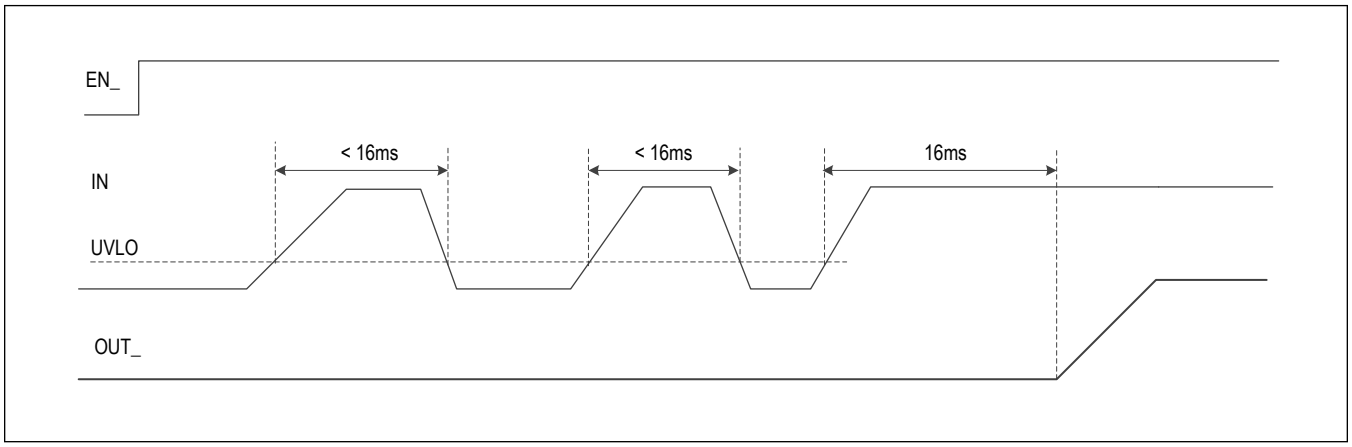


Figure 1. Input Debounce Protection

Enable

The dual MOSFETs can be individually enabled or disabled through EN_ pin by externally driving it above or below the EN_ threshold voltage. To enable the device EN_ pins must be pulled up to at least 1.4V or left floating. The external driving voltage can be as high as 5V. EN_ pins are default active-high with internal 2V pullup circuit, even when they are floated. The EN pins also have debounce protection to prevent the MOSFET from turning on by noise glitches on EN_ pins. If the device is configured to be parallel mode, two EN pins are required to tie together externally. When both EN_ pins are pulled to below 0.4V, externally the device shutdown current reduces to 32µA in low current shutdown mode.

IN-to-OUT Short-Circuit Protection

At startup, after the MOSFET is enabled without any faults, the device immediately checks for an IN-to-OUT short-circuit fault. If V_{IN} - V_{OUT} is less than a threshold (700mV), the internal MOSFET turns off and the device enters latch off mode (MAX15162) or auto-retry mode (MAX15162A). This is to prevent the MOSFET from turning on in shorted V_{IN} to V_{OUT} or shorted MOSFET condition.

Overcurrent and Short-Circuit Protection

Overcurrent fault protection is enabled in normal operation after the startup process with comparators for normal current limit threshold and fast current limit threshold. Overcurrent limit level can be configured through IMON_ pins for each MOSFET. The current limit comparator is designed so the load current can exceed the threshold for a programmable delay time prior to shut down the MOSFET. The delay time can be configured through DLY pin by connecting a resistor to GND (see Table 3).

During an overcurrent event, the $\overline{ALRT}$ pin asserts once the current limit threshold is tripped. The device turns off the internal MOSFET and disconnects the output from the input once the delay time elapses (see Figure 2). The device then operates in either auto-retry mode and restarts the output after a T_{RETRY} delay elapses (MAX15162A) or enters latch mode and latches off the output until EN is re-enabled or the input is cycled to cross UVLO threshold (MAX15162).

The devices also feature catastrophic fast overcurrent protection for large load event or short circuit condition. During normal operation, if the output is shorted to the ground or a very large current with high slope rate (di/dt) occurs, once the current reaches fast current limit comparator threshold (133% of normal current limit), a fast protection circuit forces

the gate of the MOSFET to discharge rapidly and disconnect the output from the input in 200ns (see Figure 3).

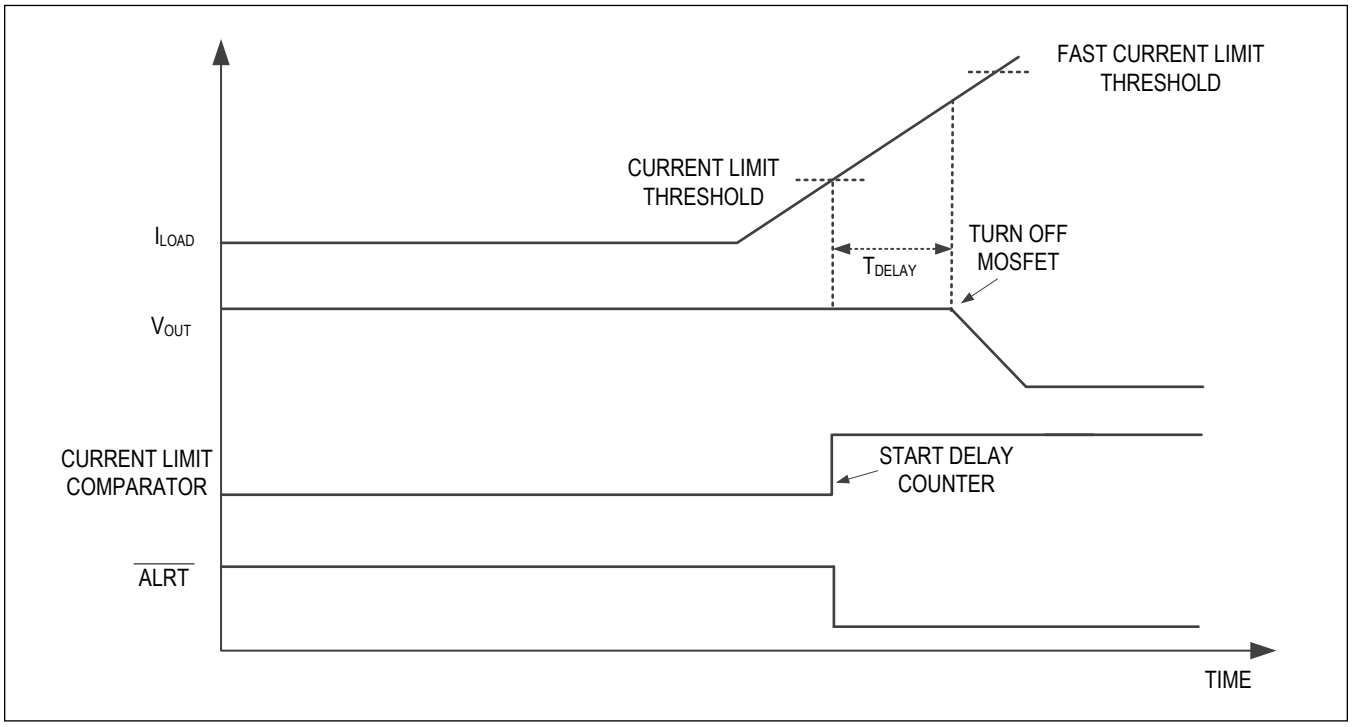


Figure 2. Overcurrent Event

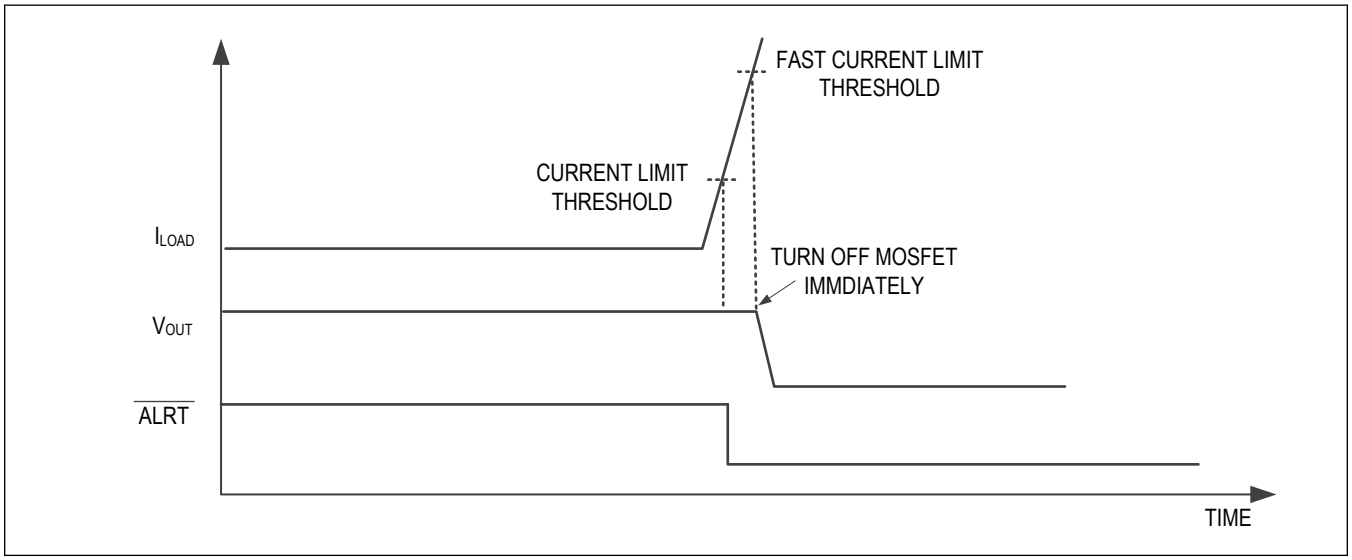


Figure 3. Fast Overcurrent Event

Current-Limit Threshold and Current Monitor (IMON_)

Connect a resistor between IMON_ and GND to program the current limit thresholds of the devices. Use the following equation to calculate current limit setting resistor $R_{IMON_}$ for independent mode:

$R_{IMON_}$ (Ω) = 1.125 x C_{IRATIO}/I_{LIM} (A)

In parallel mode, connect IMON1 and IMON2 pins together with one resistor to GND, and use the following equation to calculate current limit setting resistor $R_{IMON_}$:

$R_{IMON_}$ (Ω) = 1.125 x C_{IRATIO}/I_{LIM} (A)/2

Where I_{LIM} is the desired current limit in A, and C_{IRATIO} is current sensing ratio (4000, typ). Table 1 and Table 2 show $R_{IMON_}$ resistor settings for normal overcurrent limits and fast overcurrent limits for in independent and parallel mode respectively.

Table 1. R_{IMON} Settings for Overcurrent Limit in Independent Mode

$R_{IMON_}$ (KΩ) IN INDEPENDENT MODE	CURRENT LIMIT/CHANNEL (A)	FAST OCP LIMIT/CHANNEL (A)
9.09	0.50	0.66
6.04	0.75	0.99
4.53	0.99	1.32
3.01	1.50	1.99

Table 2. R_{IMON} Settings for Overcurrent Limit in Parallel Mode

$R_{IMON_}$ (KΩ) IN PARALLEL MODE	CURRENT LIMIT/ CHANNEL (A)	FAST OCP LIMIT/CHANNEL (A)
4.53	0.50	0.66
3.01	0.75	1.00
2.26	1.00	1.33
1.50	1.50	2.00

The devices feature a precise analog read-out of the current. The mirrored current flows out through IMON_ pins into external current-limit resistor R_{IMON}. The voltage on IMON_ pin V_{IMON} provides information about the current with the following relationship:

I_{OUT} (A) = V_{IMON} (V) x C_{IRATIO}/R_{IMON} (Ω)

In independent mode, I_{OUT} in above equation represents the current from individual channel. In parallel mode, while connect IMON1 and IMON2 pins together, I_{OUT} represents the summed current of two channels.

IMON_ pins must not be left floating.

Overcurrent Response and Shutdown Delay (DLY)

When the current flowing through the MOSFET reaches current limit threshold, T_{DELAY} timer begins to count up, and ALRT pin is asserted. If the current drops back to below current limit threshold then the T_{DELAY} timer begins to count down, as shown in Figure 4. The timer counting-down speed is slower than counting-up speed. Once the configured T_{DELAY} time is reached by the timer, the MOSFET is turned off. This mechanism is to prevent the MOSFET from turning off due to high-frequency current ripples or noises through the device.

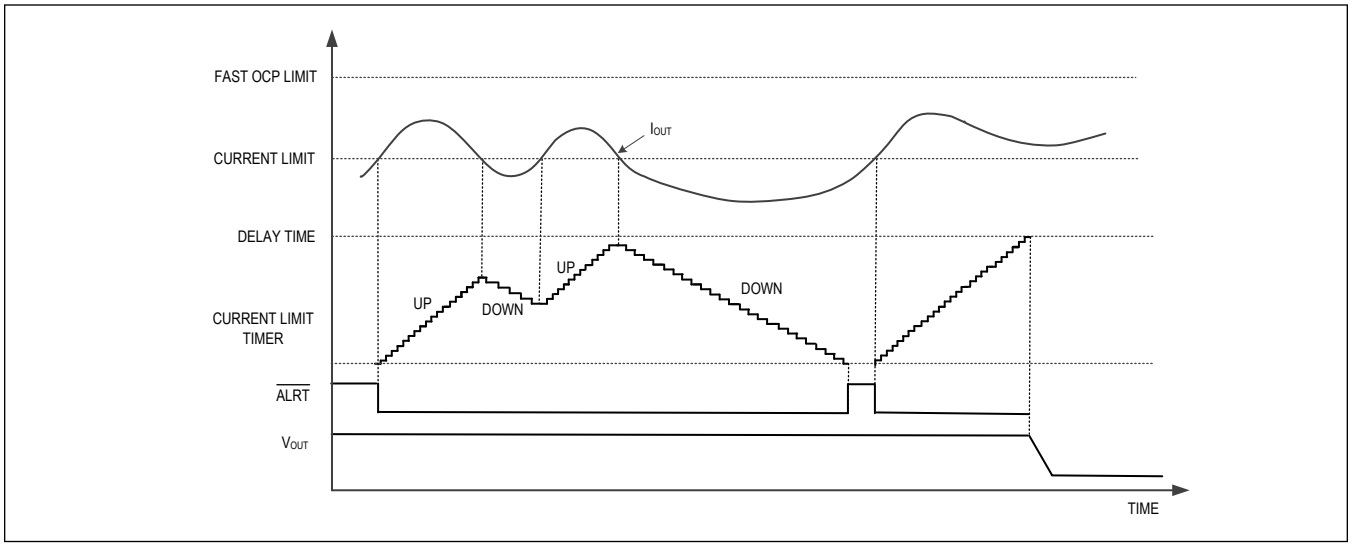


Figure 4. Overcurrent Response and Shutdown Delay

In the MAX15162A, in an overcurrent event, a auto-retry time delay (T_{RETRY}) starts immediately after T_{DELAY} elapses. During T_{RETRY} time the MOSFET remains off. Once T_{RETRY} elapses the MOSFET is turned on again. If the fault still exists then the cycle is repeated and ALRT pin remains asserted. If the overcurrent condition is resolved within T_{DELAY}, the switch stays on. By connecting a resistor to GND on DLY pin to set T_{DELAY} time and T_{RETRY} time, as shown in Table 3:

Table 3. R_{DLY} Settings for Delay Time and Auto-Retry Time—MAX15162A

RDLY (KΩ)	DELAY TIME T_{DELAY}	AUTO-RETRY TIME T_{RETRY} (ms)
0	12µs	0.6
28	100µs	6
47.5	1ms	60
68.1	10ms	600

In the MAX15162, in an overcurrent event after T_{DELAY} elapses, the MOSFET is turned off and enters latch off mode until EN pin is re-enabled or the input is cycled to cross UVLO.

$\overline{\text{ALRT_}}$ Response

The devices feature an open-drain, $\overline{\text{ALRT_}}$ output as indication of MOSFET fully turning on and fault events. Once the MOSFET is fully enhanced without any faults $\overline{\text{ALERT_}}$ pin will be de-asserted and remain de-asserted in MOSFET normal operation. $\overline{\text{ALERT_}}$ pin will be asserted when

- MOSFET V_{DS} voltage is greater than 2V.
- Input voltage drops to UVLO level.
- Overcurrent limit threshold is tripped.
- Overtemperature threshold is tripped.
- Startup watchdog timer times out.
- Startup configuration fault occurs.

In Parallel mode, $\overline{\text{ALERT_}}$ pins are driven by status of both MOSFETs. Fault from either channel will assert both $\overline{\text{ALERT_}}$ pins.

Independent and Parallel Mode

The devices can be configured as two independent channels or parallel channels for one common output. The device is configured as independent mode if IMON_pins are separately connecting to two resistors. To configure as parallel mode, two IMON_ pins are required to tie together and connect to one resistor across IMON_ to GND, EN1 and EN2 pins are required to tie together, and OUT1 and OUT2 are to be connected together. The device detects IMON_ pins connection during initialization process and determines independent or parallel channel configuration mode. IMON_ pins must not be left floating; otherwise, a startup configuration fault occurs.

Fault Auto-Retry and Latch Off

In a fault condition, the MAX15162A supports auto-retry mode and the MAX15162 supports latch-off mode. When the device turns off the MOSFET due to below fault conditions:

- Overcurrent event after delay time elapses.
- Fast overcurrent threshold is tripped.
- Output hard short event.
- Startup watchdog timer times out.

After the MOSFET is turned off, the MAX15162A enters auto-retry mode and restarts the power-up process after auto-retry delay time elapses. If the power-up is not successful in 250ms watchdog timeout, it stops and waits till the delay time elapses and starts next power-up. The auto-retry attempts totally 3 times. After three time auto-retries if the power-up is still not successfully the device stops retrying and latches off. In auto-retry mode, the delay time is configured by DLY pin.

The MAX15162 enters latch off mode once the fault events occur and the MOSFET is turned off, and it restarts the power-up process once EN_ is re-enabled or the input is cycled to cross UVLO.

Thermal Protection

The devices enter a thermal-shutdown mode in the event of overheating caused by excessive power dissipation or high ambient temperature. When the junction temperature exceeds thermal shutdown threshold, the internal thermal-protection circuitry turns off the MOSFET and $\overline{\text{ALRT_}}$ asserts to indicate the fault event. When the junction temperature falls below thermal-shutdown threshold hysteresis level, the device restarts the MOSFET power-up process.

Applications Information

IN Capacitor

Place at least a 1µF capacitor from the IN pin to GND to hold input voltage during any transients. If the upstream converter is too far away from the MAX15162, more input capacitors are recommended to be added to stabilize input voltage due to sudden load-current changes or MOSFET fast turn-off.

OUT Capacitor

The maximum capacitive load (C_{MAX}) that can be connected is a function of average startup current (I_{INRUSH}), the watchdog time (T_{SU}) and the input voltage (V_{IN}). C_{MAX} can be calculated using the following relationship:

$$C_{MAX}(\mu F) = \frac{I_{INRUSH}(mA) \times T_{SU}(ms)}{V_{IN}(V)}$$

Equation 1: Maximum Output Capacitor

For example, for V_{IN} = 48V, T_{SU} = 250ms, and I_{INRUSH} = 28mA, C_{MAX} is 146µF.

Output capacitor values in excess of C_{MAX} can result in a longer charging period and startup time, hence the possibility of watchdog timeout fault. Since the startup process is constant power limited, excessive capacitors will not cause more power dissipation or thermally stress the device.

Output Diode for Inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, a diode between the OUT terminal and ground is recommended. This is to prevent a negative spike on the OUT due to the inductive kickback during a short-circuit event.

Layout and Thermal Dissipation

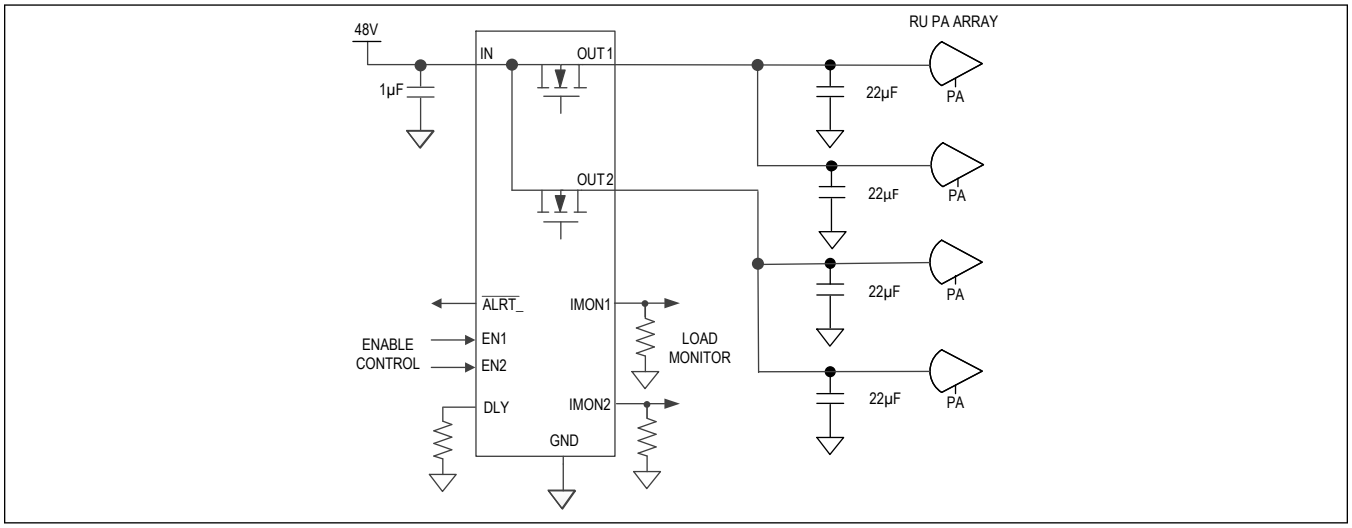
To optimize the switch response time to turn off the output fast during short-circuit conditions, it is very important to keep all traces as short as possible to reduce the effect of undesirable parasitic inductance. Place the device close to the input supply to avoid too much parasitic inductance. Place input capacitors as close as possible to the device (no more than 5mm). Place output capacitors close to the load. If there are protection devices such as TVS, or diodes, they must be placed close to the part with short traces to reduce inductance. IN and OUT must be connected with wide short traces to the power bus.

To allow for the best cooling ability of the TQFN package, the EP (exposed pad) must be soldered directly to the board GND plane. It is highly recommended to apply four 20mil thermal vias on EP to help power dissipation, and reduce thermal resistance to the ambient. On the PCB board, the second layer from top and bottom should be continuous GND plane for electrical and thermal optimization. Place all support components close to connection pins. Connect the components to the GND with shortest trace length. The trace for IMON_ pin resistor $R_{IMON1/2}$ to the device must be as short as possible to reduce parasitic effects on the current limit and current reporting accuracy. Avoid any coupling of switching signals from the board to R_{IMON} traces.

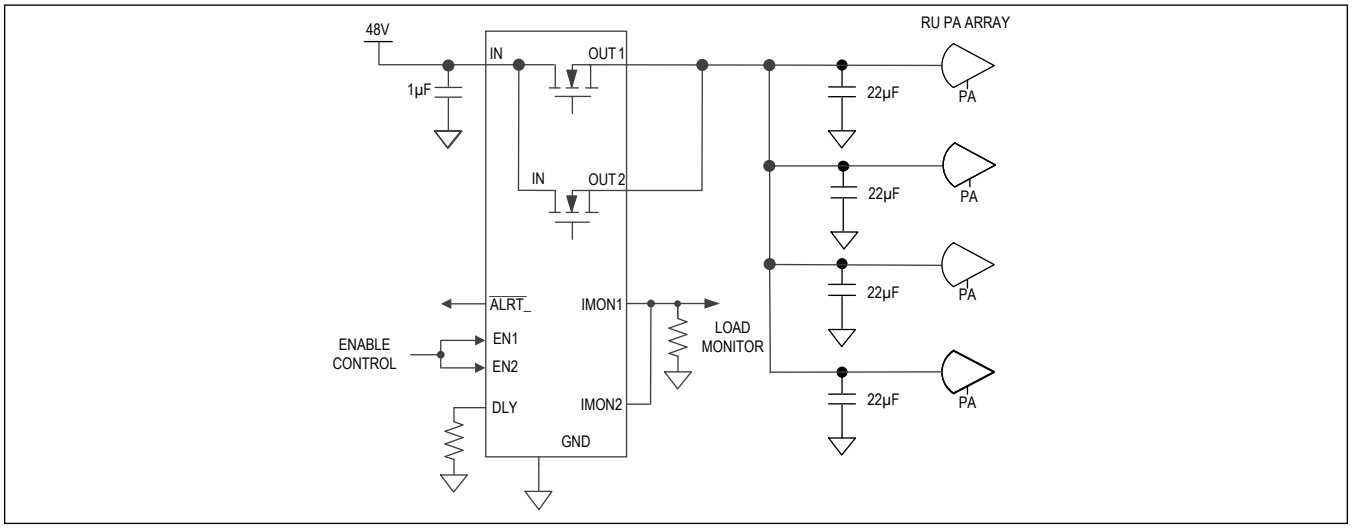
Refer to the MAX15162 EV kit data sheet for a reference layout design.

Typical Application Circuits

Typical Application Circuit—Independent Mode



Typical Application Circuit—Parallel Mode



Ordering Information

PART NUMBER	FAULT RESPONSE	PIN-PACKAGE
MAX15162AAWE+	Auto-Retry	16 WLP
MAX15162AWE+	Latch Off	16 WLP
MAX15162AATG+	Auto-Retry	24 TQFN
MAX15162ATG+	Latch Off	24 TQFN

+ Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/19	Initial release	—
1	2/20	Updated *Benefits and Features*, *Thermal Protection*, and *Ordering Information*	1, 16, 23

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