Reference Design:

HFRD-04.0

Rev. 7: 11/08

As of July, 2008 this reference design board is no longer available.

Gerber files and schematics are available upon request.

REFERENCE DESIGN
2.7Gbps, 1310nm Small Form Factor Pluggable (SFP) Transceiver

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Table of Contents

1 Overview

High Frequency Reference Design (HFRD) 4.0 is a complete optical transceiver targeted for the Small Form Factor Pluggable (SFP) Multisource Agreement (MSA) market and other high-speed optical transceiver applications.

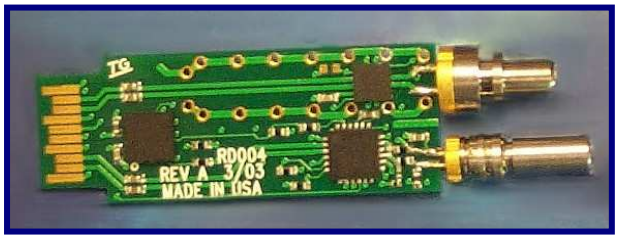
Data rates up to 2.7Gbps are attainable with the high-speed Fabry Perot laser, the high-speed MAX3735A direct modulation laser driver, the MAX3744 transimpedance amplifier (TIA), the high-speed PIN photodiode and the MAX3748 limiting amplifier. Average power and extinction ratio are held constant over the full –40°C to +85°C temperature range using the APC loop of the MAX3735A and the Dallas Semiconductor DS1859 dual temperature-controlled digital resistors.

The DS1859 provides digital monitors for bias current, monitor diode current, received power, VCC and temperature. The device is compatible with SFF 8472 digital diagnostic requirements and has the capability of performing internal calibration and monitor scaling/offsets.

The HFRD-4.0 transceiver reduces design time for SFP and other optical transmitters by providing the schematics, PC board layout, Gerber files and bill of materials for a complete SFP transceiver. Test data and typical performance from an assembled board are also given to aid in the evaluation of this reference design.

1.1 Features

- Schematics and Bill of Materials Provided
- Gerber Plot Files Available
- Multi-Rate (up to 2.7Gbps)
- Single +3.3V Power Supply
- SFP Multisource Footprint
- Digital Diagnostic Monitors and Internal Calibration.
- -40° C to +85° C Operating Range
- Temperature Compensation using Variable Digital Resistors with Look-Up Table and Digital Diagnostics
- Assembled SFP transceiver Board (RD004-1) and SFP Host Board (RD003-2) are Available for Evaluation



2 Obtaining Additional Information

Limited quantities of the RD004-1 SFP transceiver board and RD003-2 SFP host board are available. For more information about the reference design or to obtain an SFP transceiver and/or host board please email to: https://support.maxim-ic.com/ .

3 Reference Design Details

The HFRD-4.0 SFP transceiver reference design (Figure 1) is implemented using a high-speed laser driver (MAX3735A), a dual temperature-controlled variable resistor (DS1859) with monitors and internal calibration, a Fabry-Perot laser (ExceLight SLT2170-LN), a high-speed limiting amplifier with RSSI output (MAX3748), a Receiver Optical Sub-Assembly (the ROSA includes a MAX3744 and a PIN photodiode), and an SFP module board (RD004-1). The design is SFP and SFF 8472 MSA compatible and incorporates optional safety features and internal calibration.

The transmitter section is multi-rate compatible and can be operated at data rates from 155Mbps to 2.7Gbps using long pseudo-random bit stream (PRBS) patterns. The receiver section of the design may also be operated at 155Mbps to 2.7Gbps; however, overload of the MAX3744 TIA is reduced at data rates below 2.5Gbps. See section 8.7, *Operating at Lower Data Rates* for additional information.

3.1 Transmitter Components

3.1.1 MAX3735A Laser Driver

The MAX3735A is designed for direct modulation of DC-coupled laser diodes at data rates up to 2.7Gbps. An automatic power control (APC) loop is used to maintain average power over temperature.

The MAX3735A can modulate laser diodes at amplitudes up to 60mAp-p (85mAp-p AC-coupled) and supply bias currents up to 100mA. Typical edge speeds are 50ps.

The MAX3735A features current monitors and safety features in compliance with the SFP MSA. A TX_FAULT output is provided to indicate when the APC loop is unable to maintain the average optical power or when a safety fault has occurred.

For additional information see the MAX3735 data sheet available on the web at www.maxim-ic.com.

3.1.2 DS1859 Digital Potentiometer

The DS1859 Dual Temperature-Controlled NV Variable Resistor consists of two 50kΩ 256-position variable resistors, a "direct-to-digital" temperature sensor, three external voltage monitors, and one internal voltage monitor for V_{CC}. The DS1859 is compliant with SFF-8472 requirements and provides internal calibration. The device provides temperature compensation to the bias and modulation currents by changing the resistance seen by the current-setting pins of the MAX3735A.

The variable resistors' settings are stored in EEPROM memory and can be accessed over the industry standard 2-wire serial bus. The value of each variable resistor is determined by a temperature-addressed look-up table, which can assign a unique value to each resistor for every 2°C increment over the –40°C to +102°C range.

The output of temperature, supply voltage and the three monitors is available as a 12bit value (left justified) over the serial bus. Flags for supply voltage and the monitors can be set and read from the device as well.

For additional information see the DS1859 data sheet available on the web at www.maxim-ic.com.

3.1.3 ExceLight Laser

The SLT2170-LN, manufactured by ExceLight, is a 1.3um InGaAsP/lnP MQW-FP laser diode suited for LC connector fiber optic transmitters up to 2.5Gbps.

For additional information see the SLT2170-xN series data sheet available on the web at www.excelight.com.

3.2 Receiver Components

3.2.1 MAX3748 Limiting Amplifier

The MAX3748 multi-rate limiting amplifier functions as a data quantizer for SONET, Fibre Channel and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input

voltages and provides constant-level current-mode logic (CML) output voltages with controlled edge speeds.

A received-signal-strength indicator (RSSI) is available when the MAX3748 is combined with the MAX3744 SFP transimpedance amplifier (TIA) that can provide up to 19dB RSSI dynamic range. Additional features include a programmable loss-of-signal (LOS) detect, an optional polarity reversal and an output disable which can be used to implement a squelch of the outputs.

The combination of the MAX3748 and the MAX3744 allows for the simple implementation of the small-form-factor SFF-8472 digital diagnostics specifications using a standard 4-pin TO-46 header using a Maxim-proprietary interface technique (patent pending).

For additional information see the MAX3748 data sheet available on the web at www.maxim-ic.com.

3.2.2 MAX3744 Transimpedance Amplifier

The MAX3744 transimpedance amplifier provides a compact, low-power solution for communication up to 2.7Gbps. It features a 330nA input-referred noise at 2.1GHz bandwidth (BW) with 0.85pF input capacitance.

The MAX3744 operates from a single +3.3V supply and consumes 93mW. The MAX3744 die measures 30-mil x 50-mil and requires no external compensation capacitor. A space-saving filter connection is provided for positive bias to the photodiode through an on-chip 580Ω resistor to V_{CC}.

For additional information see the MAX3744 data sheet available on the web at www.maxim-ic.com.

3.2.3 Receiver Optical Sub-Assembly (ROSA)

The TO-46 receiver optical sub-assembly (ROSA), which includes the MAX3744 transimpedance amplifier (TIA), is assembled by Tyco Electronics. The ROSA is a metal ADM receiver utilizing a 1310nm InGaAs PIN designed for high bandwidth applications. The Tyco part number for this ROSA is 1382783-1. For information concerning this ROSA, please contact Tyco Electronics, Harrisburg, PA, www.tycoelectronics.com/fiberoptics.

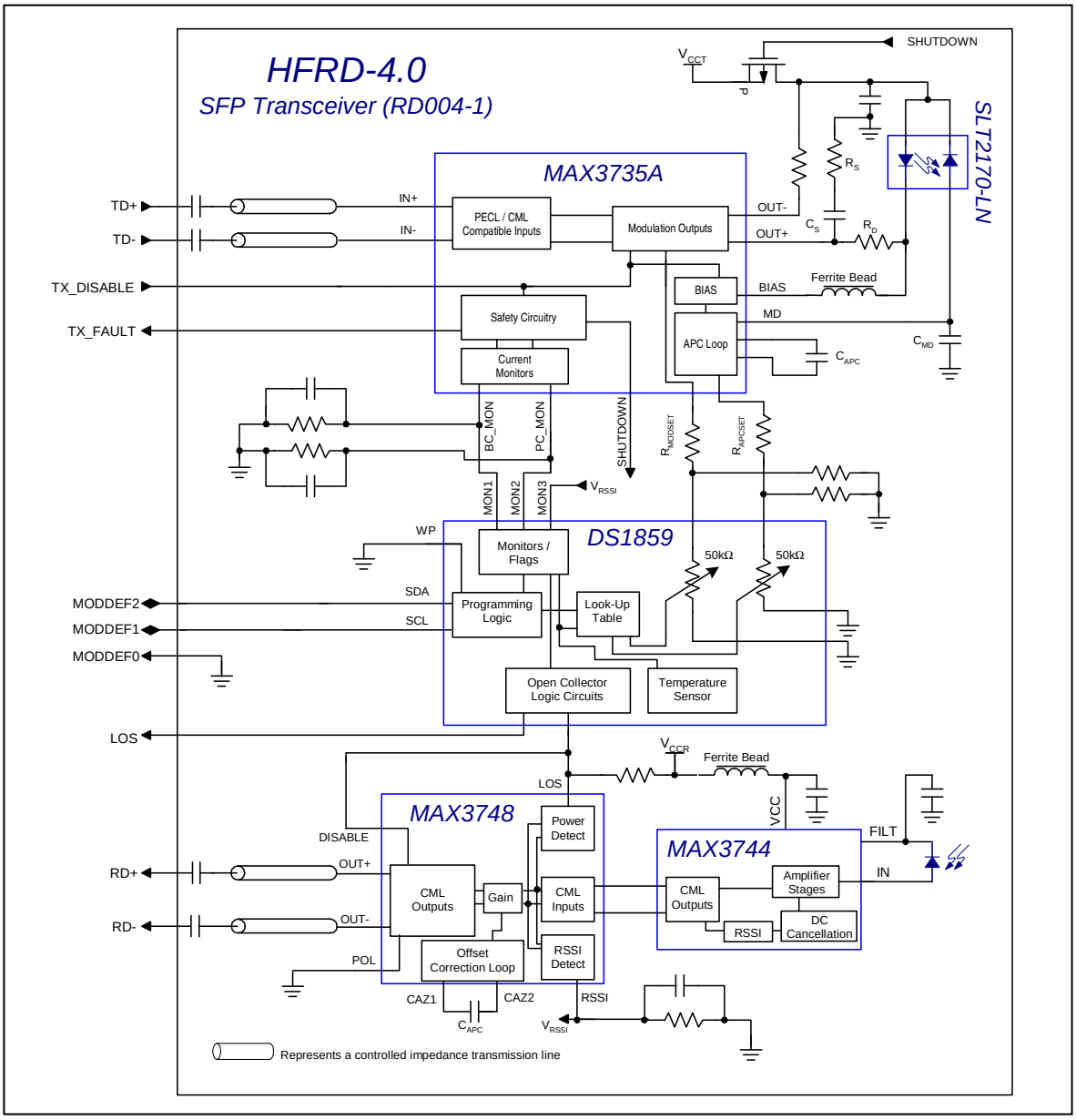


Figure 1. Functional Diagram

4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Ambient Temperature	T_A		-40		85	^oC
Supply Voltage	V_{CC}		3.0	3.3	3.63	V
Data Rate (Note 1)		Transmitter Section (2^{23}-1 Patterns)	.155		2.7	Gbps
		Receiver Section (2^{23}-1 Patterns)		2.5	2.7	Gbps
Differential Input Voltage	V_{ID}		200		2400	mV_{p-p}
TTL Input Voltage (Low)	V_{IL}				1.1	V
TTL Input Voltage (High)	V_{IH}		2.6			V

Note 1: Refer to section 8.7, *Operating at Lower Data Rates* for additional information.

5 Typical Reference Design Performance

5.1 Transmitter Performance Data

(Typical values are measured at T_A = +25°C, V_{CC} = +3.3V, Average Power = -4dBm, Extinction Ratio = 10dB unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Power Supply Current			65	mA
Average Optical Power	P_{AVG}		-4.0 to –4.5	dBm
		With TX_DISABLE Asserted	< -60	dBm
Extinction Ratio	E_R	-40°C to +85°C (Note 1)	10	dB
Extinction Ratio Variation		-40°C to +85°C (Note 1, 2)	0.2	dB
Optical Rise Time	t_R	20% to 80% (Notes 3, 4)	51	ps
Optical Fall Time	t_F	80% to 20% (Notes 3, 4)	150	ps
Jitter Generation	TJ	Total Jitter Peak to Peak Measured after acquiring 3000 Waveforms (Notes 1, 5)	37	ps_{P-P}
	RJ	RMS Random Jitter (Note 3)	1.7	ps_{RMS}
Eye Mask Margin		(Notes 1, 6)	25	%
Center Wavelength			1310	nm

Note 1: Measured using a 2.488Gbps with a 2^{23}-1 PRBS input data pattern.
Note 2: Extinction ratio variation refers to the obtainable variation using multiple calibration points.
Note 3: Measured using a 2.488Gbps repeating 00000 11111 pattern.
Note 4: Measured using an unfiltered optical output.
Note 5: Includes approximately 17ps of total jitter from the test equipment.
Note 6: Mask margin is measured after acquiring 3000 waveforms using standard mask limits and filters.

5.2 Receiver Performance Data

(Typical values are measured at T_A = +25°C, V_{CC} = +3.3V, Optical Source is HFRD 4.0 Transmitter)

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Power Supply Current		Receiver Only	83	mA
Average Optical Input Power Overload	P_{AVGMAX}	(Note 1)	-5	dBm
Receiver Sensitivity (Note 2)	P_{AVGMIN}	Data Rate = OC-24 (1.24416Gbps)	-24.8	dBm
		Data Rate = OC-48 (2.48832Gbps)	-23.7	
		Data Rate = OC-48 FEC (2.6660571Gbps)	-23.4	

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Transceiver Sensitivity (Note 2,3)	P_{AVGMIN}	Data Rate = OC-24 (1.24416Gbps)	-24.3	dBm
		Data Rate = OC-48 (2.48832Gbps)	-23.4	
		Data Rate = OC-48 FEC (2.6660571Gbps)	-22.6	
Loss of Signal (Note 4)	LOS	Assert	-26.3	dBm
		De-Assert	-24.0	
Loss of Signal Hysteresis			2.3	dB

Note 1: Optical overload at OC-48 data rates is dominated by the design of the ROSA. The AC overload of the MAX3744 is >2mAp-p. This would equate to an optical overload of approximately 0dBm. Overload is specified at 2.48832Gbps operation using a 2^{23}-1PRBS test pattern. Operating at a data rates less than OC-48 will reduce the overload specification due to limitations within the MAX3744 TIA.
Note 2: Sensitivity is measured using a 2^{23}-1 PRBS test pattern to a BER of approximately 10^{-10}. An isolated HFRD-04.0 transmitter is used as the optical source for the BER testing.
Note 3: Transceiver sensitivity is measured with data present on the transmitter with the transmitter enabled.
Note 4: Loss of Signal (LOS) is measured using at OC-48 with a 2^{23}-1 PRBS test pattern.

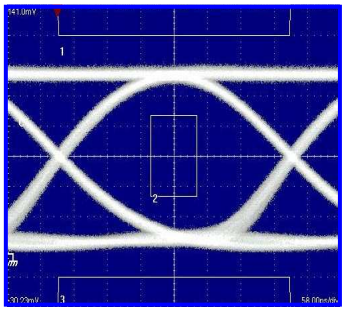
5.3 Transceiver Timing Data

TX_DISABLE Assert Time	t_{OFF}	Time from rising edge of TX_DISABLE to optical power at 5% of steady state.	180	µs
TX_DISABLE Negate Time	t_{ON}	Time from falling edge of T_{DIS} to optical power at 95% of steady state when TX_FAULT = 0 before reset.	184	µs
TX_FAULT Reset Time or Power on Time	t_{INIT}	From power on or negation of TX_FAULT using TX_DISABLE.	64	ms
TX_FAULT Assert Time	t_{FAULT}	Time from fault occurrence to TX_FAULT on, C_{FAULT} < 20pF, R_{FAULT} = 4.7kΩ.	64	µs
TX_FAULT Delay Time	t_{FLTDLY}	Time from fault to bias and modulation current at off state limits.	2	µs
LOS Assert Time	T_{LOS}	Time from LOS state to LOS Assert.	< 50	µs
LOS De-Assert Time	T_{LOS}	Time from non-LOS state to LOS De-Assert.	< 50	µs
TX_DISABLE to Reset		Time TX_DISABLE must be held high to reset TX_FAULT.	<0.5	µs

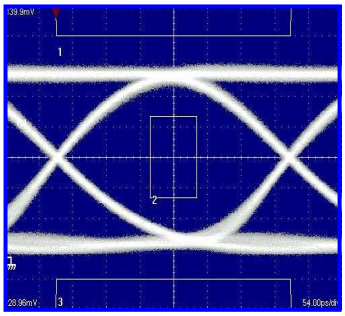
6 Transmitter Characteristic Graphs

(Optical eye diagrams filtered at ≈ 0.75 x data rate, T_A = +25°C, V_{CC} = +3.3V, 2.488Gbps, -4dBm average power unless otherwise noted)

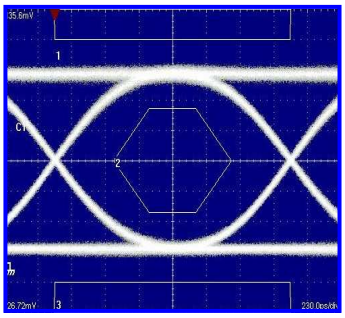
OPTICAL EYE DIAGRAM
(E_R = 10.2dB, 2.488Gbps, 25% Margin, 2^{23}-1 PRBS)



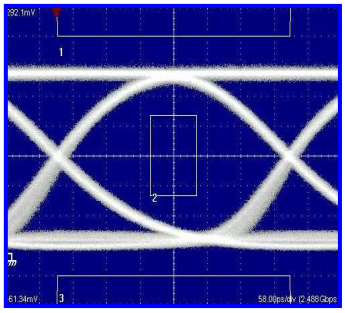
OPTICAL EYE DIAGRAM
(E_R = 9.9dB, 2.666Gbps, 24% Margin, 2^{23}-1 PRBS)



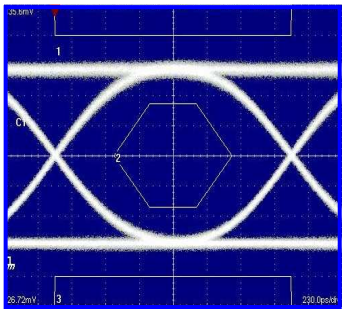
OPTICAL EYE DIAGRAM
(E_R = 10.7dB, 1.244Gbps, 44% Margin, 2^{23}-1 PRBS)



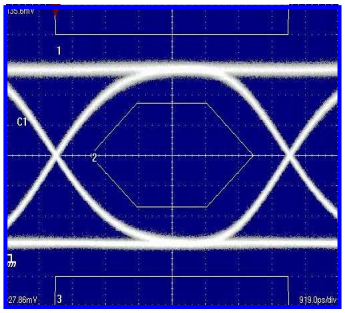
OPTICAL EYE DIAGRAM
(E_R = 10.0dB, 2.488Mbps, 2^{23}-1 PRBS, T_A = +85C)



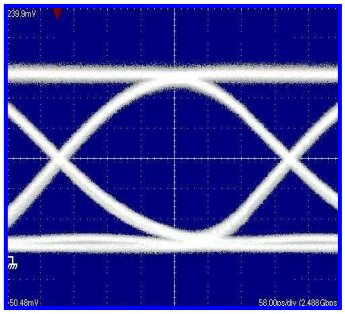
OPTICAL EYE DIAGRAM
(E_R = 11.0dB, 622Mbps, 2^{23}-1 PRBS)



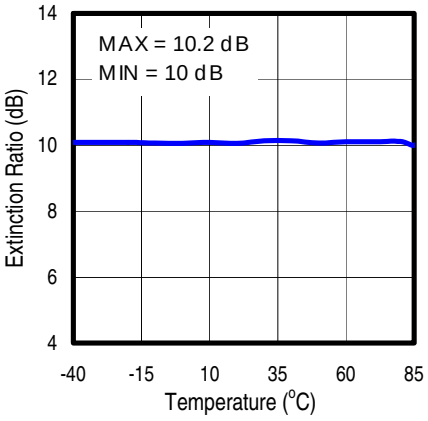
OPTICAL EYE DIAGRAM
(E_R = 11.7dB, 155Mbps, 2^{23}-1 PRBS)



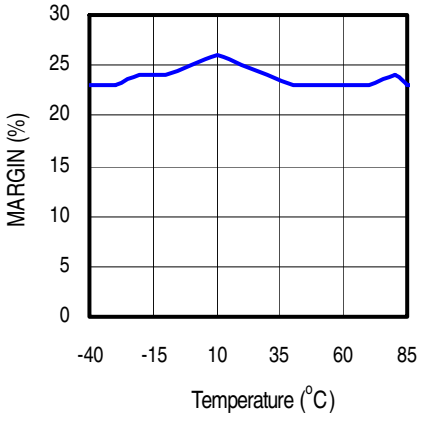
OPTICAL EYE DIAGRAM
(E_R = 10.1dB, 2.488Mbps, 2^{23}-1 PRBS, T_A = -40C)



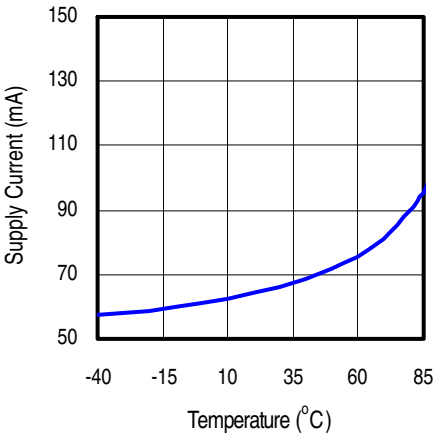
EXTINCTION RATIO vs. TEMPERATURE



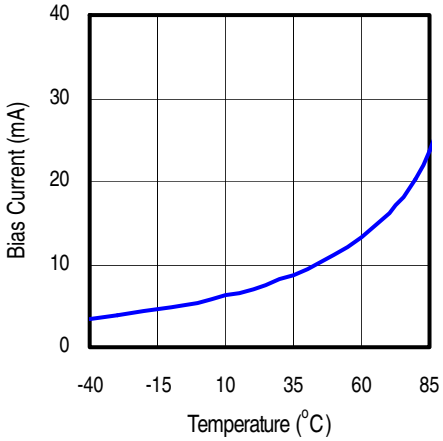
OC48 MASK MARGIN vs. TEMPERATURE



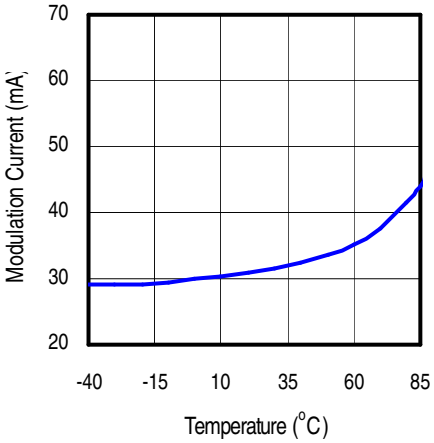
SUPPLY CURRENT vs. TEMPERATURE



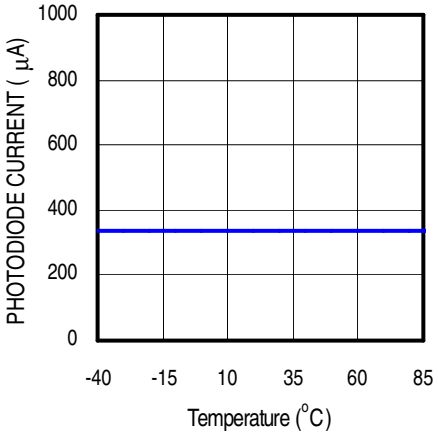
BIAS CURRENT vs. TEMPERATURE



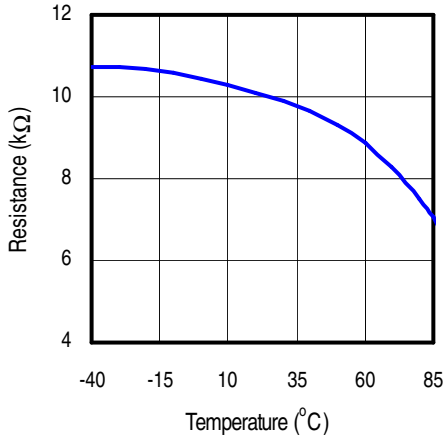
MODULATION CURRENT vs. TEMPERATURE



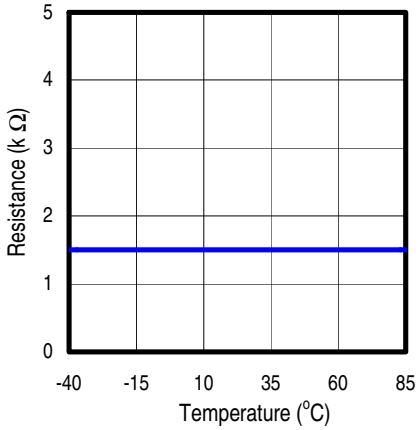
PHOTODIODE CURRENT vs. TEMPERATURE



R_{MODSET} vs. TEMPERATURE



R_{APCSET} vs. TEMPERATURE

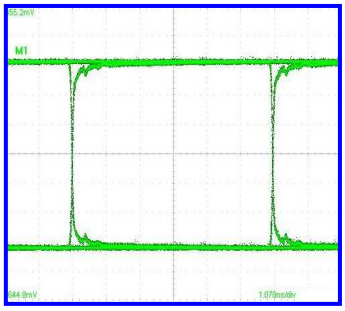


Temperature	Digital Change in Rmodset	Temperature	Digital Change in Rmodset	Temperature	Digital Change in Rmodset
-40	12	4	6	48	-10
-38	12	6	5	50	-12
-36	12	8	5	52	-12
-34	12	10	4	54	-13
-32	11	12	4	56	-15
-30	11	14	3	58	-16
-28	11	16	3	60	-17
-26	11	18	2	62	-18
-24	10	20	1	64	-19
-22	10	22	1	66	-20
-20	10	24	0	68	-21
-18	10	26	-1	70	-22
-16	10	28	-1	72	-23
-14	9	30	-2	74	-24
-12	9	32	-3	76	-25
-10	9	34	-4	78	-26
-8	8	36	-5	80	-27
-6	8	38	-6	82	-28
-4	8	40	-7	84	-29
-2	7	42	-8	86	-30
0	7	44	-9	88	-31
2	6	46	-9	90	-32

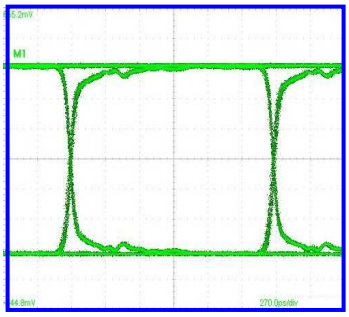
7 Receiver Characteristic Graphs

(T_A = +25°C, V_{CC} = +3.3V, OC48, 2^{23}-1 PRBS, Diagrams taken at received data output SMA connectors of RD003-2 host board.)

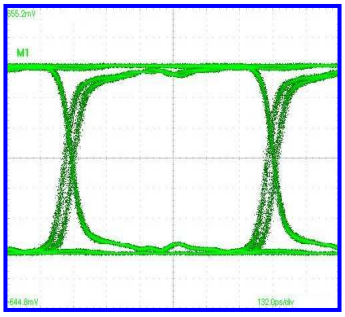
OUTPUT EYE DIAGRAM
(OC-3, -18dBm Optical Input)



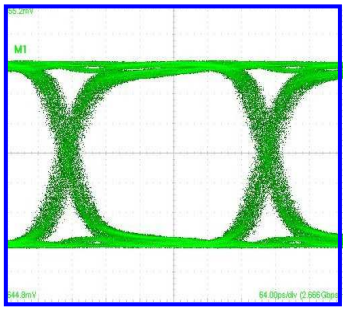
OUTPUT EYE DIAGRAM
(OC-12, -18dBm Optical Input)



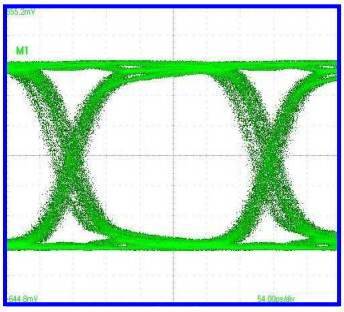
OUTPUT EYE DIAGRAM
(OC-24, -18dBm Optical Input)



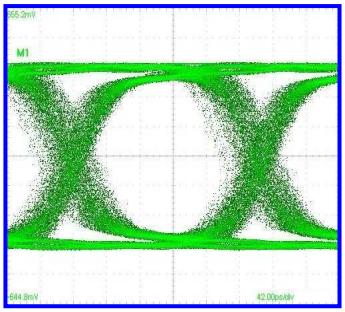
OUTPUT EYE DIAGRAM
(OC-48 FEC, -18dBm Optical Input)



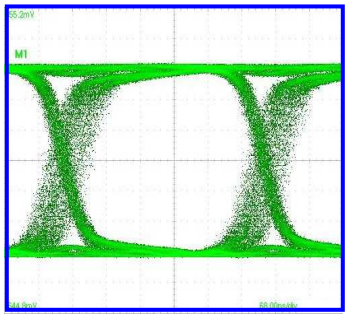
OUTPUT EYE DIAGRAM
(3.125 Gbps, -18dBm, 2^7-1 PRBS)



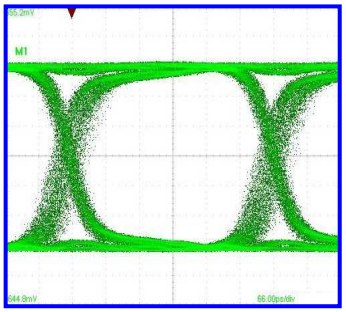
OUTPUT EYE DIAGRAM
(4.25 Gbps, -18dBm, 2^7-1 PRBS)



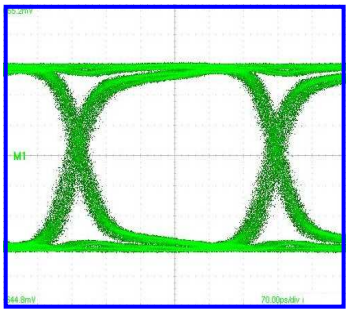
OUTPUT EYE DIAGRAM
(OC-48, -18 Optical Input, Temperature = -40°C)

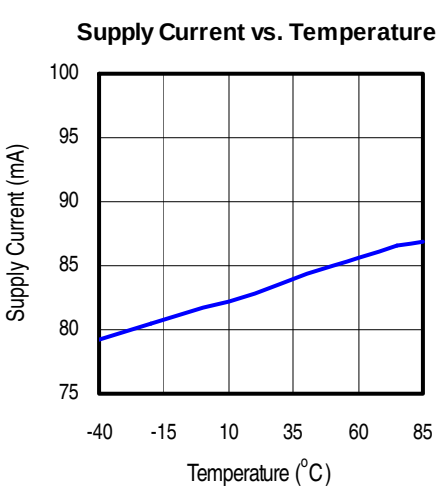


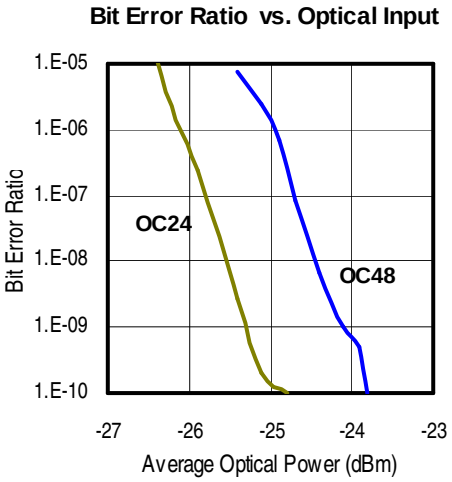
OUTPUT EYE DIAGRAM
(OC-48, -18 Optical Input, Temperature = 25°C)

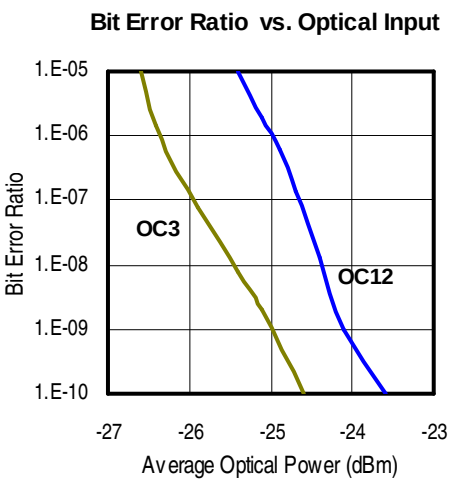


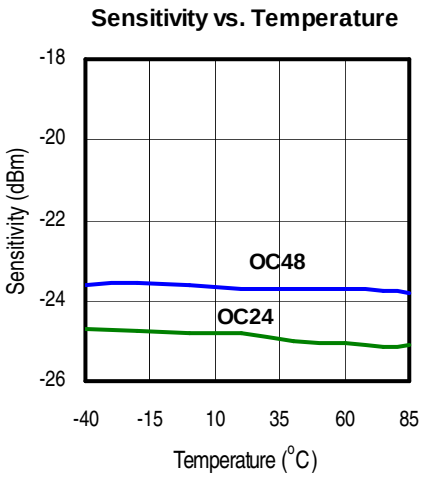
OUTPUT EYE DIAGRAM
(OC-48, -18 Optical Input, Temperature = 85°C)

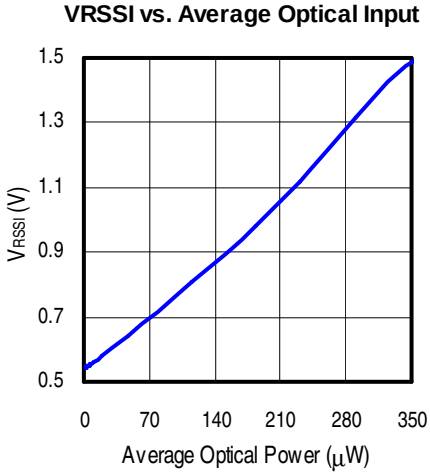


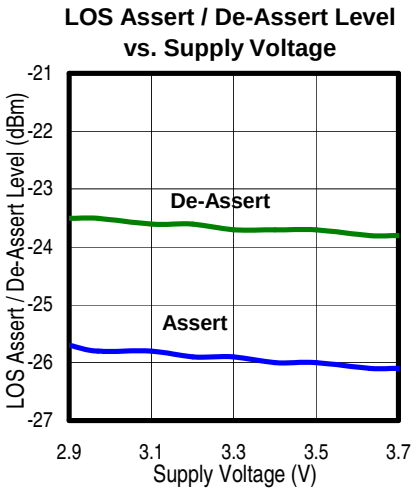

Supply Current vs. Temperature
Supply Current (mA)
100
95
90
85
80
75
-40
-15
10
35
60
85
Temperature (°C)


Bit Error Ratio vs. Optical Input
Bit Error Ratio
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
OC24
OC48
-27
-26
-25
-24
-23
Average Optical Power (dBm)


Bit Error Ratio vs. Optical Input
Bit Error Ratio
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
OC3
OC12
-27
-26
-25
-24
-23
Average Optical Power (dBm)


Sensitivity vs. Temperature
Sensitivity (dBm)
-18
-20
-22
-24
-26
OC48
OC24
-40
-15
10
35
60
85
Temperature (°C)


VRSSI vs. Average Optical Input
VRSSI (V)
1.5
1.3
1.1
0.9
0.7
0.5
0
70
140
210
280
350
Average Optical Power (µW)


LOS Assert / De-Assert Level vs. Supply Voltage
LOS Assert / De-Assert Level (dBm)
-21
-22
-23
-24
-25
-26
-27
De-Assert
Assert
2.9
3.1
3.3
3.5
3.7
Supply Voltage (V)

8 Application Information

8.1 Small Form Factor Pluggable (SFP) Transceivers

The RD004-1 transmitter design was specifically engineered to meet the requirements of the Small Form Factor Pluggable (SFP) Transceiver Multisource Agreement (MSA) and the SFF-8472 MSA. These MSAs set guidelines for the package outline, pin function and other aspects of the module design. By complying with the standard, modules are mechanically and functionally interchangeable.

8.2 Monitor Outputs

The MAX3735A and MAX3748 have on-chip current monitors for bias, and monitor diode current of the laser (MAX3735A) as well as the received signal strength of the photodiode (MAX3748).

The MAX3735A current monitors generate a ground-referenced voltage across external resistors connected from the monitor pins to ground. The relations are given mathematically as:

$$I_{BIAS} = \frac{76 \cdot V_{BC\_MON}}{2.5k\Omega}$$

$$I_{MD} = \frac{V_{PC\_MON}}{2k\Omega}$$

The received signal monitor (RSSI of the MAX3748) generates a ground-referenced voltage across an external resistor that is proportional to both the DC photodiode current (I_{PD}) and the average optical input power. See page 11 for a graph of the typical response.

The voltages at the monitor pins ($V_{BIASMON}$, V_{PWRMON} and V_{RSSI}) are sampled by the DS1859 and stored in memory. The values can then be read over the 2-wire bus as a 12bit digitized number. If the voltage at the BC_MON or PC_MON pin of the MAX3735A exceeds 1.32V (Typical), a fault condition will be latched.

8.3 Programming the DS1859

The DS1859 dual variable resistor is programmed with an industry standard 2-wire interface. The interface I/O pins consist of SDA and SCL (see the DS1859 data sheet for more information). These control lines are connected to pad 4 (MOD-DEF2, SDA) and pad 5 (MOD-DEF1, SCL) of the transmitter board. The data can then be programmed into the device through these pins using the connections of a standard SFP evaluation board.

To facilitate the programming of the DS1859 additional materials such as software, DS3900 serial port adapter, cable, and RD003-2 host board can be used. These materials allow easy adjustments to be made to the DS1859 through the 2-wire interface. See 18 *Additional Evaluation Materials* on page 21 for more information.

8.4 Layout Considerations

Differential and single-ended transmission lines are designed in the RD004-1 board. Changing the PCB layer profile (see details on page 21) can affect the impedance of these transmission lines and the performance of the reference design. If the layer profile is changed, the transmission line dimensions should be recalculated.

8.5 Host Board Requirements

Controlled-impedance transmission lines and good high-frequency design techniques should be used when interfacing to the RD004-1 SFP transceiver board. The host board should provide the necessary power supply filtering. The recommended SFP MSA power supply filter for the transmitter is shown in Figure 2.

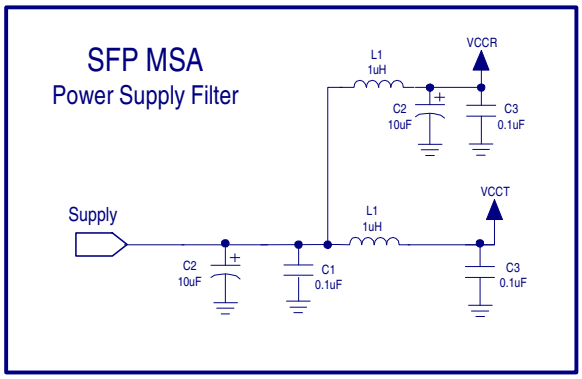


Figure 2. Power Supply Filter

8.6 MSA Compliance, EMI and Safety Issues

Full compliance to the SFP MSA and other performance specifications cannot be guaranteed by Maxim and are therefore the responsibility of the user of this reference design. This reference design is intended to aide SFP module designers and is not intended to take the place of the entire design process. The SFP module designer should evaluate the reference design and modify it as necessary to meet the specification for each particular project. The designer should also carefully consider safety and EMI issues related to the particular application.

8.7 Operation at Lower data rates

Transmitter Section: Due to the low frequency cutoff of the APC loop and AC-coupling capacitors on the data inputs, the optical performance for data rates less than 155Mbps is degraded due to baseline wander. This will occur when using long patterns with low frequency content such as a 2^{23}-1 PRBS. If a short test pattern is used such as 2^{7}-1 or K28.5, acceptable optical performance can be obtained at data rates as low as 10Mbps. See the Maxim design note HFDN 23.0 – "Choosing the APC loop capacitors used with MAX3735/MAX3735A SFP module designs" for more information.

Receiver Section: The MAX3748 limiting amplifier is specified for 155Mbps to 3.2Gbps operation. The MAX3744 is specified for 2.5 to 2.7Gbps applications. Operating at data rates less than 2.5Gbps will reduce the optical overload performance due to restrictions in the MAX3744 TIA. This will occur when using long patterns with low frequency content such as a 2^{23}-1 PRBS. Using a short test pattern such as 2^{7}-1 or K28.5 will improve the overload limit at lower data rates.

8.8 Improving Receiver Sensitivity

Improved receiver sensitivity can be obtained by providing high frequency isolation between the MAX3748 limiting amplifier and the MAX3744 TIA. By placing a small inductor (3.3nH to 6.8nH) between each of the TIA outputs and the MAX3748 inputs, the sensitivity can be improved by 1 to 1.5dBm. Using inductors larger than 6.8nH will improve the sensitivity further, but at the cost of increased jitter at the limiting amplifier output.

The RD004-1 PCB can be modified to incorporate these changes by cutting the data traces and placing 0402 size inductors as shown in Figure 3. Multi-layer inductors, that have a small DC resistance, are suggested for this use.

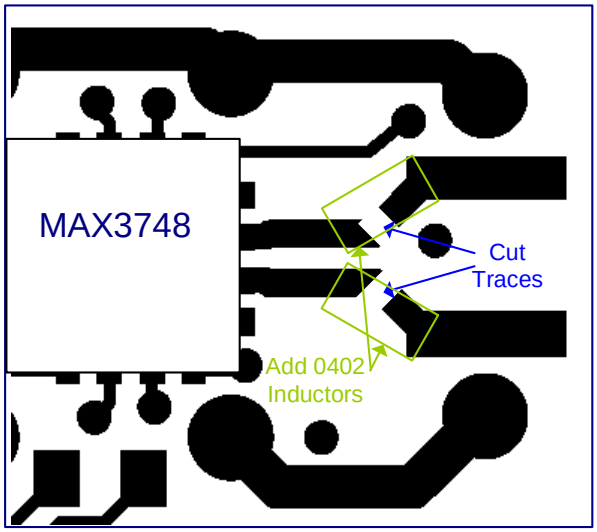


Figure 3. Board Modification

8.9 Gerber Files

The Gerber files for this reference design are available. Email to:https://support.maxim-ic.com/
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9 Quick Start

RD004-1 can be evaluated in any standard SFP host board. Changes to the settings of the DS1859 can be done through the MOD-DEF2 and MOD-DEF1 pads. The module has been pre-programmed prior to shipment to provide an extinction ratio of 10dB and an average power of –4dBm at 25°C. A typical curve has also been loaded into the memory table for temperature compensation. The temperature compensation table is generated using typical data. The extinction ratio variation may be larger than that shown in the Reference Design Characteristic Graphs unless it is adjusted using the Dallas DS1859 software.

Precautions must be taken in order to insure safe operation when using a device with a laser diode. Laser light emissions can be harmful and may cause eye damage. Maxim assumes no responsibility for harm or injury as a result of the use of this reference design. The safe operation of this design is the sole responsibility of the user.

To evaluate the RD004-1 transmitter in a standard SFP host board:

1) Connect the RD004-1 to an SFP host board.
2) Attach a 155Mbps to 2.5Gbps differential source (refer to section 8.7, *Operation at Lower Data Rates*) to the host board so that data is applied to pads 18 and 19 of the SFP board. Each source should have a peak-to-peak amplitude between 100mV and 1200mV (200mV and 2400mV differential).
3) Connect a single mode fiber with an LC-type ferrule to the laser. Do not place mechanical stress on the laser with the fiber cable. Stress by the fiber cable or other sources could damage the laser.
4) Connect the other end of the fiber to a high-speed oscilloscope through an optical-to-electrical converter or an optical plug-in module. The optical-to-electrical conversion device should have a bandwidth of at least 1870MHz and be able to detect 1310nm wavelengths. **Note: The laser supplied with the reference design has a maximum power rating of 0.8mW. Attenuation may be required if 0.8mW of optical power exceeds the optical-to-electrical device's input power rating.**
5) Apply a +3.3V power supply to the host board. Set the current limit to 200mA.
6) Verify that TX_DISABLE is deasserted so that the SFP transmitter may operate.

To evaluate the RD004-1 receiver in a standard SFP host board:

7) Connect the RD004-1 to an SFP host board.
8) Attach high-speed SMA coaxial cables to the differential outputs from the host board to the oscilloscope.
9) Connect a single mode fiber with an LC-type ferrule to the ROSA. Do not place mechanical stress on the ROSA with the fiber cable. Stress by the fiber cable or other sources could damage the ROSA.
10) Connect the other end of the fiber to a high-speed 1310nm optical source through an optical attenuator. If using the transmitter portion of the reference design as the optical source, follow steps 1-7 to setup the transmitter. The average output power of the optical source should be less than -6dBm.
11) Apply a +3.3V power supply to the host board. Set the current limit to 200mA.

10 Pad Description

PAD	NAME	FUNCTION
1,17,20	$V_{EE}T$	Transmitter Ground
2	TX_FAULT	Transmitter Fault Indication (open collector)
3	TX_DISABLE	Transmitter Disable
4	MOD-DEF2	Module Definition 2, 2 wire serial ID interface (SDA of the DS1859).
5	MOD-DEF1	Module Definition 1, 2 wire serial ID interface (SCL of the DS1859).
6	MOD-DEF0	Module Definition 0, Connected to $V_{EE}T$.
7	RATE SELECT	N.A. - No Connection
8	LOS	Loss of Signal
9, 10, 11, 14	$V_{EE}R$	Receiver Ground
12	RD-	Inv. Receiver Data Out
13	RD+	Receiver Data Out
15	$V_{CC}R$	Receiver Power, +3.3V Supply ±5%
16	$V_{CC}T$	Transmitter Power, +3.3V Supply ±5%
18	TD+	Transmitter Data In
19	TD-	Inv. Transmitter Data In

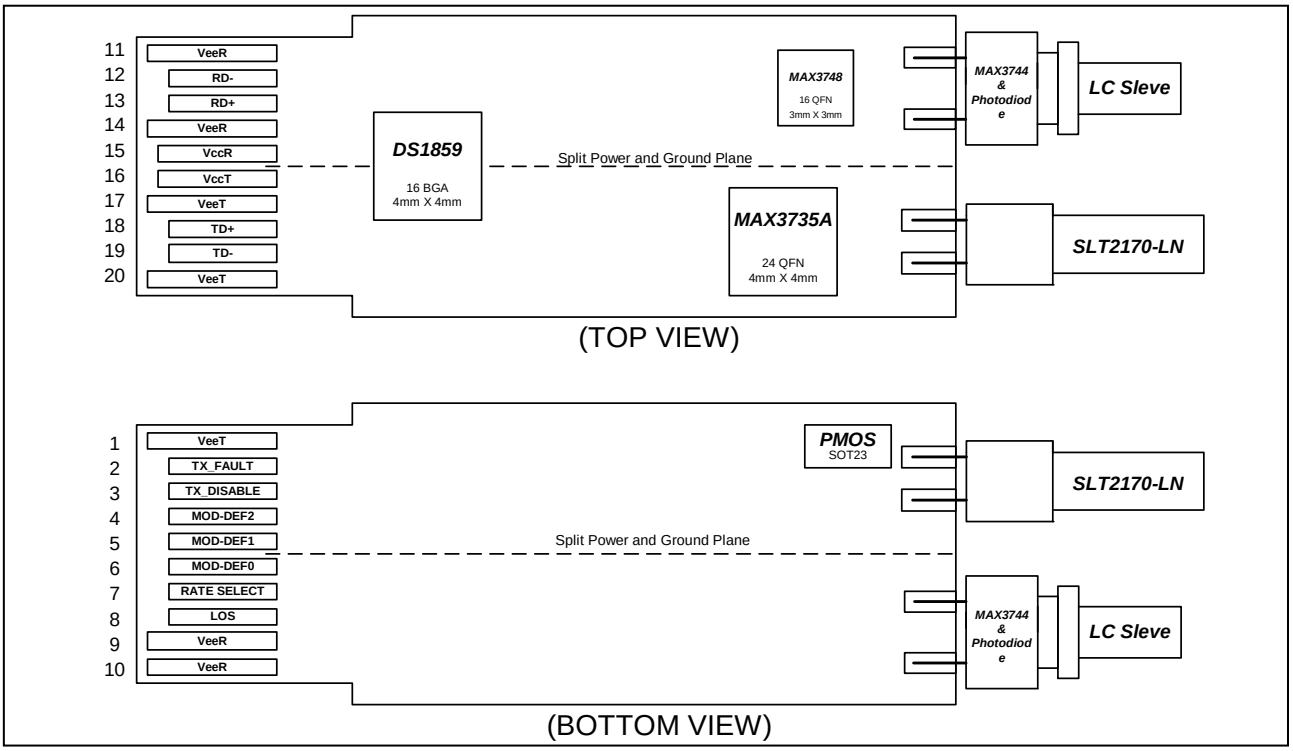


Figure 4. RD004-1 SFP Board Pad Diagram

11 Component List (RD004-1)

DESIGNATION	QTY	DESCRIPTION
C1, C2, C22, C23	4	1µF ± 10% Ceramic Capacitor (0402)
C3-C8, C13, C15, C16, C20, C24	11	0.01µF ± 10% Ceramic Capacitor (0402)
C9	1	0.47µF ± 10% Ceramic Capacitor (0402)
C10, C17	2	680pF ± 10% Ceramic Capacitor (0402)
C11, C18, C19, C21	4	0.1µF ± 10% Ceramic Capacitor (0402)
C12	1	0.068µF ± 10% Ceramic Capacitor (0402)
C14	1	Open (0201)
C25	1	4.7pF ± 10% Ceramic Capacitor (0201)
D1	1	FP Laser Diode ExceLight SLT2170-LN
L1-L3	3	600Ω Ferrite Beads (0402) TDK MMZ1005Y-601
Q1	1	MOSFET Transistor (SOT-23) Fairchild FDN306P or FDN302P
R1, R11	2	2.0kΩ ±1% Resistor (0402)
R2	1	18.2kΩ ±1% Resistor (0402)
R3	1	1.0kΩ ±1% Resistor (0402)
R4	1	182Ω ±1% Resistor (0402)
R5	1	3.01kΩ ±1% Resistor (0402)
R6	1	Open (0402)
R7	1	51Ω 5% Resistor (0201)
R8, R15, R16	3	0Ω 5% Resistor (0402)
R9, R10	2	10Ω ±5% Resistor (0402)
R12	1	2.49kΩ ±1% Resistor (0402)
R13	1	10kΩ ±5% Resistor (0402)
R14	1	270Ω ±5% Resistor (0402)
U1	1	MAX3735AETG 24 Pin QFN (Exposed Pad)
U2	1	DS1859B-050 16 Ball BGA
U3	1	MAX3748ETE 16 Pin QFN (Exposed Pad)
None	1	SFP Transmitter Board (RD004-1)

12 Component List (RD003-2)

DESIGNATION	QTY	DESCRIPTION
C6, C7, C11, C31	4	10µF ±10% Ceramic Capacitor AVX TAJC106K010R
C5	1	Open
C8, C53	2	0.1µF ± 10% Ceramic Capacitor (0603)
C9, C10, C54	3	0.1µF ± 10% Ceramic Capacitor (0402)
D1 – D6	6	LED, red T1 package
J1	1	20 Pin, Right Angle Connector AMP 1367073-1
J2 – J5	4	SMA Edge-Mount Connectors
J6	1	6 Pin, Phone Jack Connector AMP 555077-1
JP1, JP2	2	2x8 Pin Headers, 0.1in centers
JU1, JU2	2	1x2 Pin Headers, 0.1in centers
JU3, JU4	2	1x3 Pin Headers, 0.1in centers
L1, L2, L3, L13	4	1µH Inductor (1008CS) Coilcraft 1008CS-102XKBC
R3 – R7	5	4.7kΩ ±1% Resistor (0603)
R8 – R13	6	300Ω ±5% Resistor (0603)
TP1 – TP7, J9, J10, J37, J38	11	Test Points
U1, U2	2	Dual Inverters Fairchild NC7WZ04P6X
None	1	SFP Host Board (RD003-2)

13 Schematic (RD004-1)

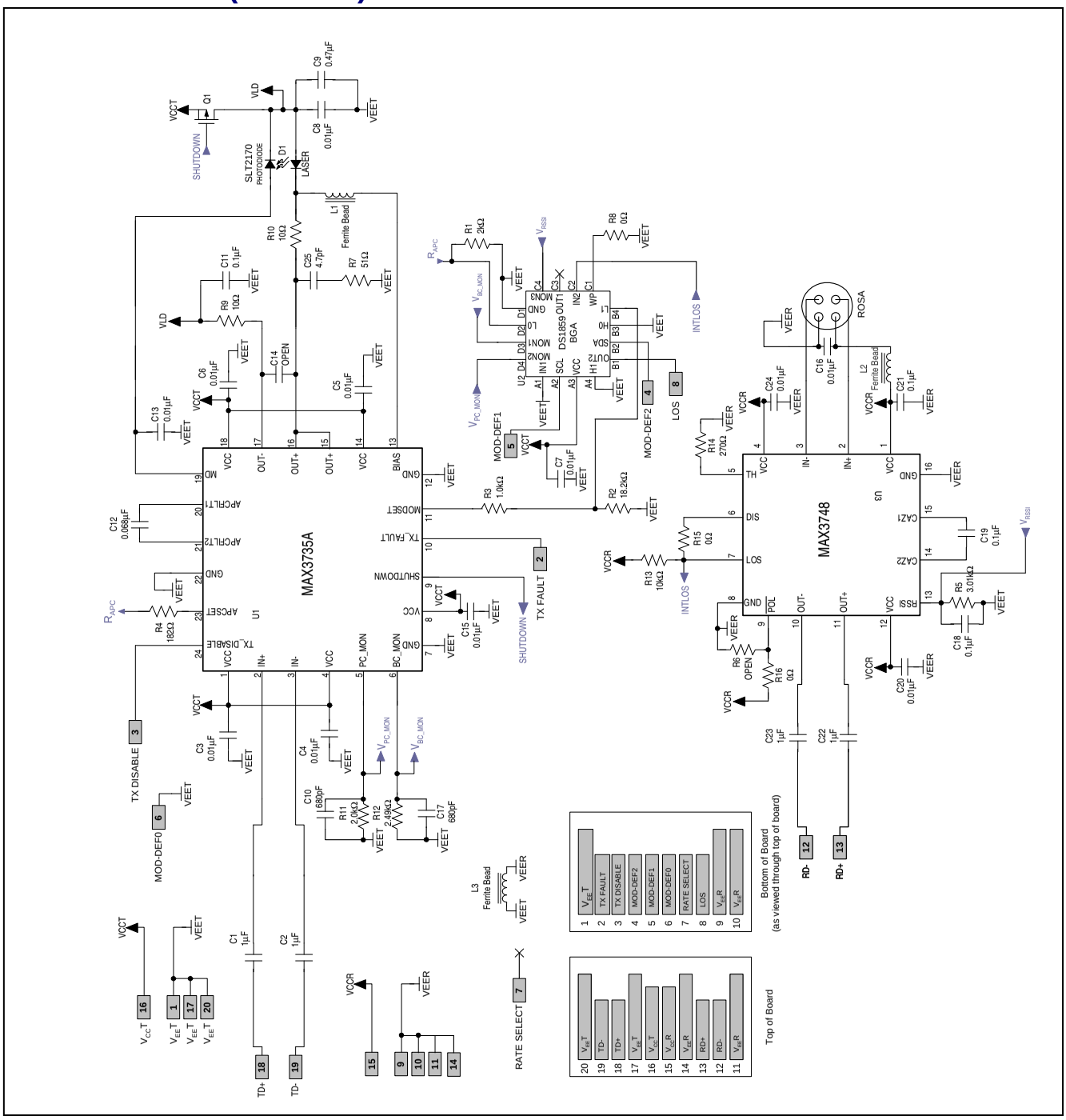


Figure 5. RD004-1 SFP Transmitter Schematic

14 Schematic (RD003-2)

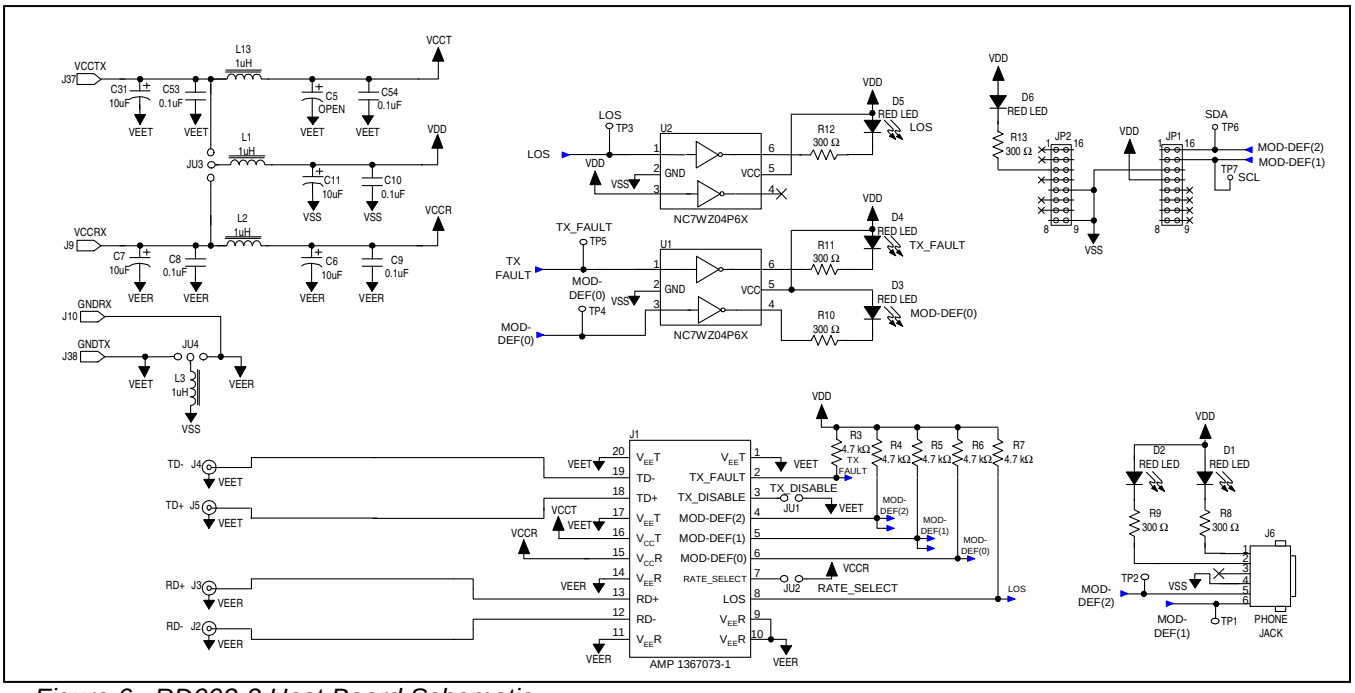


Figure 6. RD003-2 Host Board Schematic

15 Board Dimensions (RD004-1)

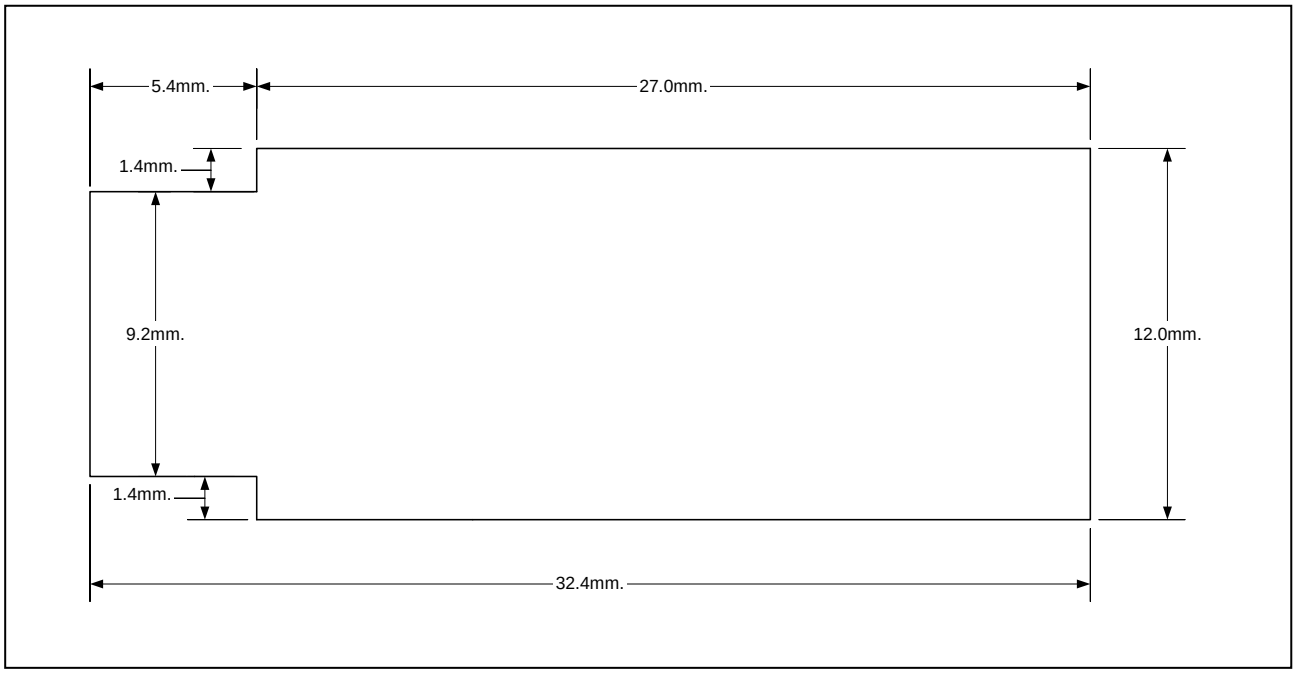


Figure 7. Board Dimensions See SFP MSA for additional dimensions.

16 Board Layout (RD004-1)

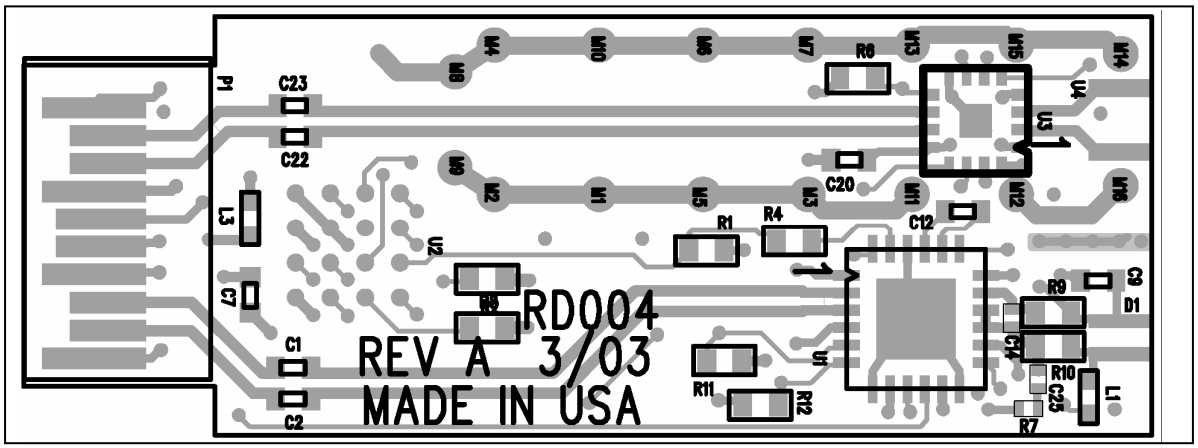


Figure 8. RD004-1 Component Placement Guide – Component Side

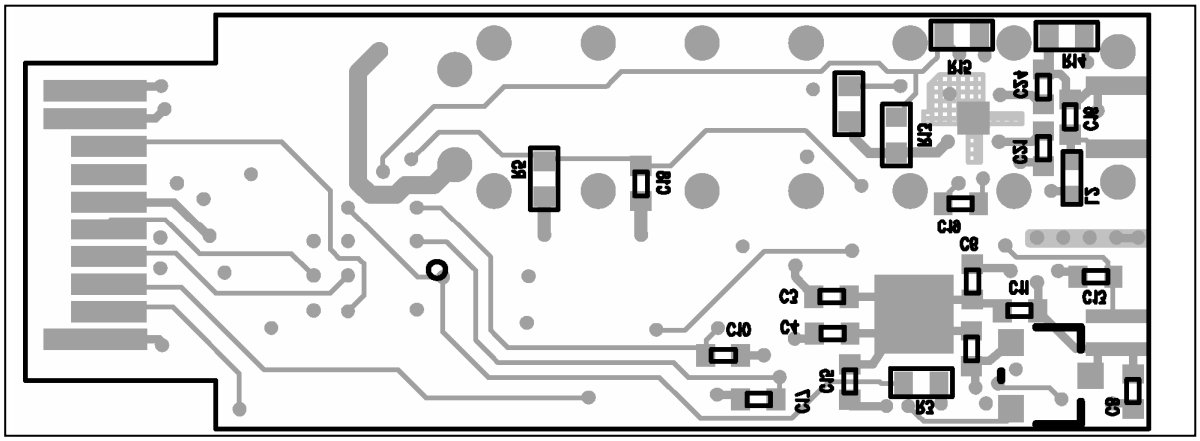


Figure 9. RD004-1 Component Placement Guide – Solder Side

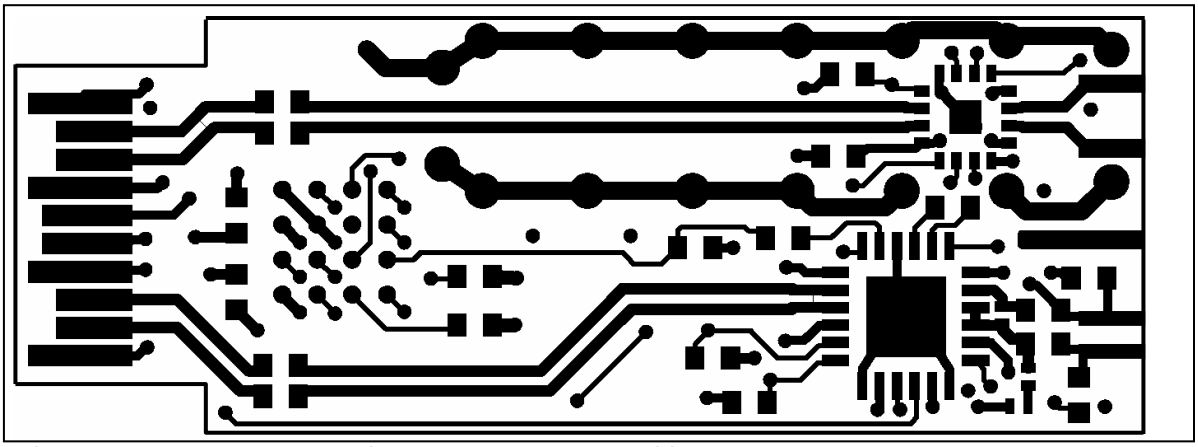


Figure 10. RD004-1 PC Board Layout – Component Side

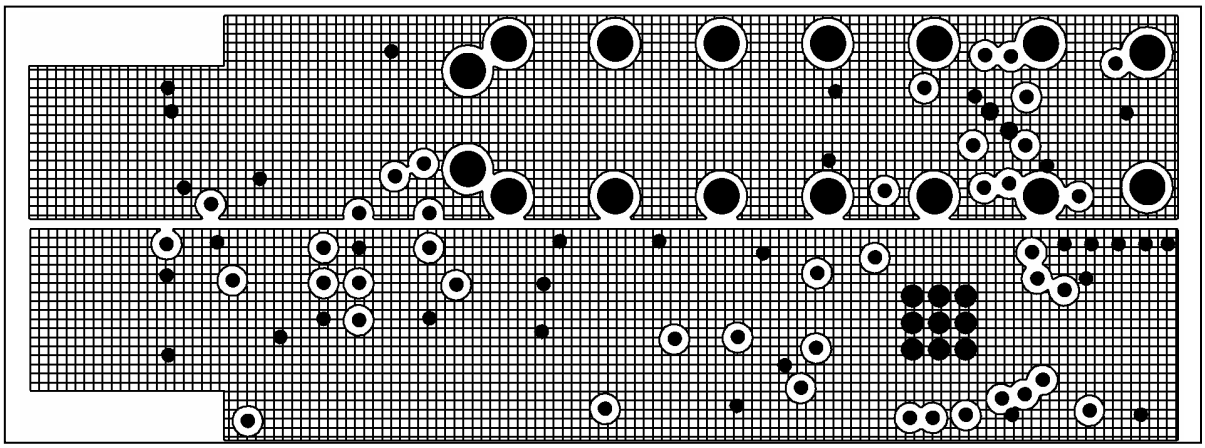


Figure 11. RD004-1 PC Board Layout – Ground Plane

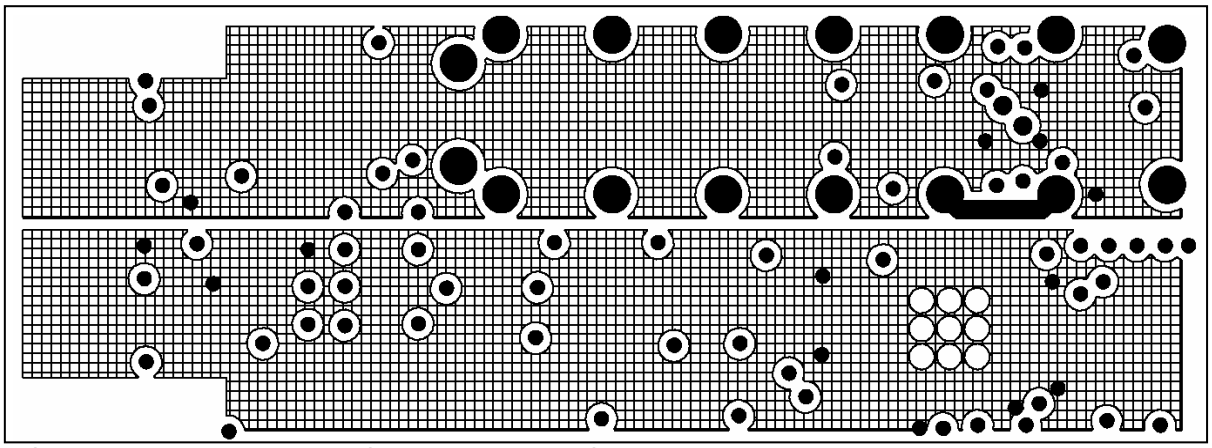


Figure 12. RD004-1 PC Board Layout – Power Plane

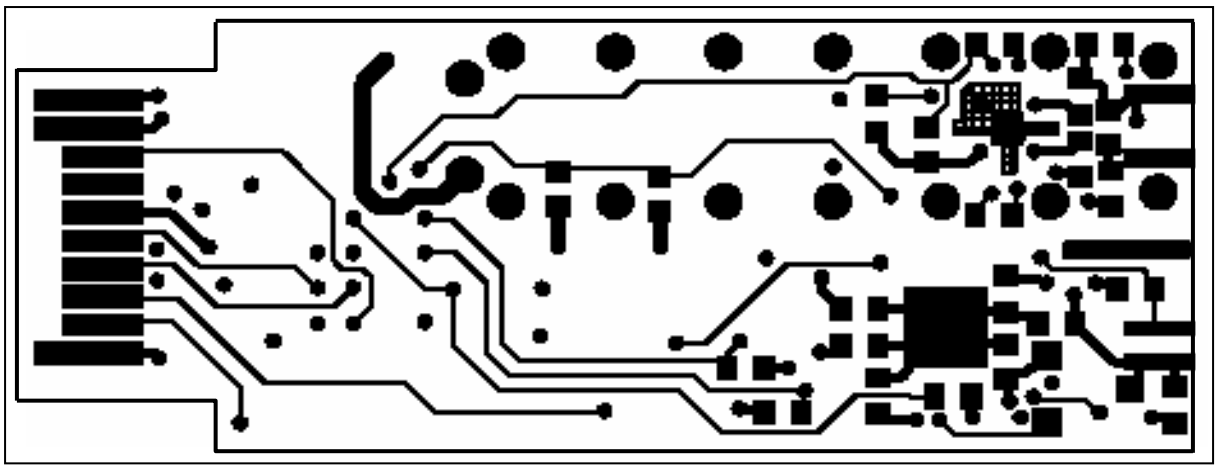


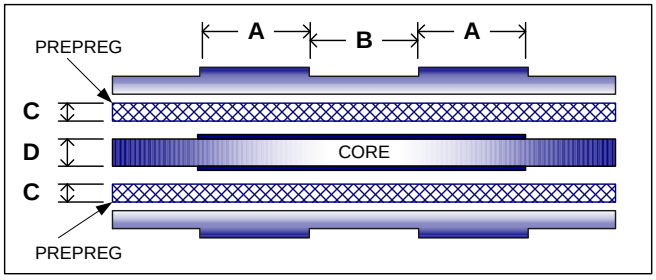
Figure 13. RD004-1 PC Board Layout – Solder Side

17 Layer Profile

The RD004-1 SFP transmitter board includes controlled-impedance transmission lines. The layer profile is based on the following assumptions:

1. Dielectric material is FR4 with a dielectric constant of ~ 4.7
2. 1oz copper foil

	SINGLE ENDED	COUPLED
A	N.A.	12.5mil
B	>50mil	10mil
C	16mil	16mil
D	As Needed	As Needed



18 Additional Evaluation Materials

The following materials may be needed to program the DS1859.

1. DS1859 Evaluation Software: Software that can be run on a standard PC. The software facilitates the interface to the DS1859 controller IC. Software sends and receives data by communication with the serial port, and the DS3900 serial port adapter.
2. DS3900 Serial Port Adapter: Converts RS232 protocol to 2-wire protocol with appropriate levels. Functions with the software to communicate with the DS1859 controller IC. The DS3900 plugs directly onto the RD003-2 host board.
3. RS232 Cable: Cable with standard DB9 connector that is used to connect the DS3900 serial port adapter to the computer.
4. RD003-2 Reference Design Host Board: Contains plug-in connectors for SFP modules, high-speed data connector (SMA), and 2-wire digital communication connections for the DS3900.

For further information email to: https://support.maxim-ic.com/ .