

SN65MLVD204B Multipoint-LVDS Line Drivers and Receivers (Transceivers) With IEC ESD Protection

1 Features

- Compatible with the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange
- Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates⁽¹⁾ Up to 100 Mbps, Clock Frequencies up to 50 MHz
 - Type-2 Receiver Provides an Offset Threshold to Detect Open-Circuit and Idle-Bus Conditions
- Bus I/O Protection
 - >±8-kV HBM
 - >±8-kV IEC 61000-4-2 Contact Discharge
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- 1-V to 3.4-V Common-Mode Voltage Range Allows Data Transfer With 2 V of Ground Noise
- Bus Pins High Impedance When Disabled or $V_{CC} \leq 1.5$ V
- 200-Mbps Devices Available (SN65MLVD201, 203, 206, 207)
- Improved Alternatives to SN65MLVD200A, 202A, 204A and 205A

⁽¹⁾ The signaling rate of a line is the number of voltage transitions that are made per second expressed in the bps of the unit (bits per second).

2 Applications

- Low-Power, High-Speed, and Short-Reach Alternative to TIA/EIA-485
- Backplane or Cabled Multipoint Data and Clock Transmission
- Cellular Base Stations
- Central Office Switches
- Network Switches and Routers

3 Description

The SN65MLVD204B device is a multipoint-low-voltage differential (M-LVDS) line drivers and receivers which are optimized to operate at signaling rates up to 100 Mbps. This device family has robust 3.3-V drivers and receivers in the standard SOIC footprint for demanding industrial applications. The bus pins are robust to ESD events, with high levels of protection to human-body model and IEC contact discharge specifications.

The SN65MLVD204B combine a differential driver and a differential receiver (transceiver), which operate from a single 3.3-V supply. The transceivers are optimized to operate at signaling rates up to 100 Mbps.

The SN65MLVD204B has enhancements over similar devices. Improved features include a controlled slew rate on the driver output to help minimize reflections from unterminated stubs, resulting in better signal integrity. The same footprint definition was maintained, allowing for an easy drop-in replacement for a system performance upgrade. The devices are characterized for operation from -40°C to 85°C.

The SN65MLVD204B M-LVDS transceivers are part of TI's extensive [M-LVDS portfolio](#).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65MLVD204B	SOIC (8)	4.90 mm x 3.91 mm

⁽¹⁾ For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic, SN65MLVD204B

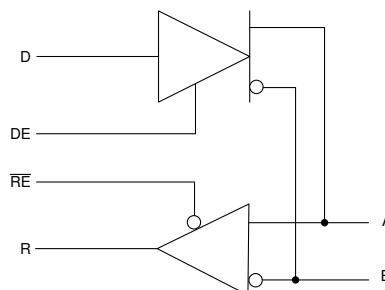


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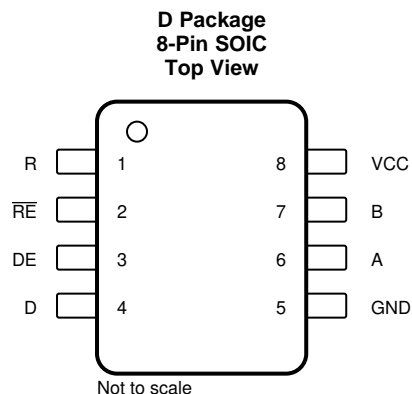
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4 Revision History

Changes from Revision A (December 2016) to Revision B	Page
Deleted all references in the text, tables, and figures for devices SN65MLVD200B, SN65MLVD202B, and SN65MLVD205B	1
Deleted the D 14-Pin Package from the <i>Pin Configuration and Functions</i>	3
In Bus Input and Output electrical characteristics, changed C_A and C_B from 5 pF to 12pF	6
In Bus Input and Output electrical characteristics, changed C_{AB} from 4pF to 7pF	6
Removed Type1 receiver input threshold test voltage table	12
Removed pin numbers from Functional Block Diagrams.	16
Removed Type-1 receiver table in Device Function Table section.	17

Changes from Original (November 2015) to Revision A	Page
Changed the device status From: Preview To: Production	1

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	I/O	Differential I/O
B	7	I/O	Differential I/O
D	4	Input	Driver input
DE	3	Input	Driver enable pin; High = Enable, Low = Disable
GND	5	Power	Supply ground
NC	—	NC	No internal connection
R	1	Output	Receiver output
RE	2	Input	Receiver enable pin; High = Disable, Low = Enable
V _{CC}	8	Power	Power supply, 3.3 V
Y	—	I/O	Differential I/O
Z	—	I/O	Differential I/O

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range, V_{CC} ⁽²⁾		−0.5	4	V
Input voltage range	D, DE, \overline{RE}	−0.5	4	V
	A, B	−1.8	4	V
Output voltage range	R	−0.3	4	V
	A, B	−1.8	4	V
Continuous power dissipation		See the Thermal Information table		
Storage temperature, T_{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2	A, B	±8000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	A, B	±8000	
			All pins except A and B	±4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	All pins	±1500	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
	Voltage at any bus terminal V_A or V_B	−1.4		3.8	V
$ V_{ID} $	Magnitude of differential input voltage			V_{CC}	V
R_L	Differential load resistance	30	50		Ω
$1/t_{UI}$	Signaling rate			100	Mbps
T_A	Operating free-air temperature for D package	−40		85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN65MLVD204B	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	52.8	
Ψ_{JT}	Junction-to-top characterization parameter	10.3	
Ψ_{JB}	Junction-to-board characterization parameter	52.3	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)⁽¹⁾

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{CC}	Supply current	Driver only	\overline{RE} and DE at V _{CC} , R _L = 50 Ω, All others open		13	22	mA
		Both disabled	\overline{RE} at V _{CC} , DE at 0 V, R _L = No Load, All others open		1	4	
		Both enabled	\overline{RE} at 0 V, DE at V _{CC} , R _L = 50 Ω, All others open		16	24	
		Receiver only	\overline{RE} at 0 V, DE at 0 V, All others open		4	13	
P _D	Device power dissipation		R _L = 50 Ω, Input to D is a 50-MHz 50% duty cycle square wave, DE = high, RE = low, T _A = 85°C			100	mW

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

6.6 Electrical Characteristics – Driver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
V _{AB}	Differential output voltage magnitude ⁽³⁾	See Figure 3	480		650	mV
Δ V _{AB}	Change in differential output voltage magnitude between logic states		–50		50	mV
V _{OS(SS)}	Steady-state common-mode output voltage	See Figure 4	0.8		1.2	V
ΔV _{OS(SS)}	Change in steady-state common-mode output voltage between logic states		–50		50	mV
V _{OS(PP)}	Peak-to-peak common-mode output voltage				150	mV
V _{A(OC)}	Maximum steady-state open-circuit output voltage	See Figure 8	0		2.4	V
V _{B(OC)}	Maximum steady-state open-circuit output voltage		0		2.4	V
V _{P(H)}	Voltage overshoot, low-to-high level output	See Figure 6			1.2 V _{SS}	V
V _{P(L)}	Voltage overshoot, high-to-low level output		–0.2 V _{SS}			V
I _{IH}	High-level input current (D, DE)	V _{IH} = 2 V to V _{CC}	0		10	μA
I _{IL}	Low-level input current (D, DE)	V _{IL} = GND to 0.8 V	0		10	μA
I _{OS}	Differential short-circuit output current magnitude	See Figure 5			24	mA

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) All typical values are at 25°C and with a 3.3-V supply voltage.

(3) Measurement equipment accuracy is 10 mV at –40°C

6.7 Electrical Characteristics – Receiver

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold ⁽²⁾	Type 2	See Figure 10 and Table 1			150	mV
V_{IT-}	Negative-going differential input voltage threshold ⁽²⁾	Type 2			50		
V_{HYS}	Differential input voltage hysteresis, ($V_{IT+} - V_{IT-}$)	Type 2			0		
V_{OH}	High-level output voltage (R)		$I_{OH} = -8$ mA	2.4			V
V_{OL}	Low-level output voltage (R)		$I_{OL} = 8$ mA			0.4	V
I_{IH}	High-level input current (\overline{RE})		$V_{IH} = 2$ V to V_{CC}	-10		0	μ A
I_{IL}	Low-level input current (\overline{RE})		$V_{IL} = GND$ to 0.8 V	-10		0	μ A
I_{OZ}	High-impedance output current (R)		$V_O = 0$ V or 3.6 V	-10		15	μ A

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) Measurement equipment accuracy is 10 mV at -40°C

6.8 Electrical Characteristics – BUS Input and Output

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
I_A	Receiver or transceiver with driver disabled input current	$V_A = 3.8$ V,	$V_B = 1.2$ V,		0		32	μ A
		$V_A = 0$ V or 2.4 V,	$V_B = 1.2$ V		-20		20	
		$V_A = -1.4$ V,	$V_B = 1.2$ V		-32		0	
I_B	Receiver or transceiver with driver disabled input current	$V_B = 3.8$ V,	$V_A = 1.2$ V		0		32	μ A
		$V_B = 0$ V or 2.4 V,	$V_A = 1.2$ V		-20		20	
		$V_B = -1.4$ V,	$V_A = 1.2$ V		-32		0	
I_{AB}	Receiver or transceiver with driver disabled differential input current ($I_A - I_B$)	$V_A = V_B$,	$1.4 \leq V_A \leq 3.8$ V		-4		4	μ A
$I_{A(OFF)}$	Receiver or transceiver power-off input current	$V_A = 3.8$ V,	$V_B = 1.2$ V,	$0 \text{ V} \leq V_{CC} \leq 1.5 \text{ V}$	0		32	μ A
		$V_A = 0$ V or 2.4 V,	$V_B = 1.2$ V,	$0 \text{ V} \leq V_{CC} \leq 1.5 \text{ V}$	-20		20	
		$V_A = -1.4$ V,	$V_B = 1.2$ V,	$0 \text{ V} \leq V_{CC} \leq 1.5 \text{ V}$	-32		0	
$I_{B(OFF)}$	Receiver or transceiver power-off input current	$V_B = 3.8$ V,	$V_A = 1.2$ V,	$0 \text{ V} \leq V_{CC} \leq 1.5 \text{ V}$	0		32	μ A
		$V_B = 0$ V or 2.4 V,	$V_A = 1.2$ V,	$0 \text{ V} \leq V_{CC} \leq 1.5 \text{ V}$	-20		20	
		$V_B = -1.4$ V,	$V_A = 1.2$ V,	$0 \text{ V} \leq V_{CC} \leq 1.5 \text{ V}$	-32		0	
$I_{AB(OFF)}$	Receiver input or transceiver power-off differential input current ($I_A - I_B$)	$V_A = V_B$, $0 \text{ V} \leq V_{CC} \leq 1.5 \text{ V}$, $-1.4 \leq V_A \leq 3.8 \text{ V}$			-4		4	μ A
C_A	Transceiver with driver disabled input capacitance.	$V_A = 0.4 \sin(30E6\pi t) + 0.5 \text{ V}^{(2)}$, $V_B = 1.2 \text{ V}$				12		pF
C_B	Transceiver with driver disabled input capacitance	$V_B = 0.4 \sin(30E6\pi t) + 0.5 \text{ V}^{(2)}$, $V_A = 1.2 \text{ V}$				12		pF
C_{AB}	Transceiver with driver disabled differential input capacitance	$V_{AB} = 0.4 \sin(30E6\pi t) \text{ V}^{(2)}$				7		pF
$C_{A/B}$	Transceiver with driver disabled input capacitance balance, (C_A/C_B)				0.99		1.01	pF

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

6.9 Switching Characteristics – Driver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	See Figure 6	2	2.5	3.5	ns
t_{pHL}	Propagation delay time, high-to-low-level output		2	2.5	3.5	ns
t_r	Differential output signal rise time			2		ns
t_f	Differential output signal fall time			2		ns
$t_{sk(p)}$	Pulse skew ($ t_{pHL} - t_{pLH} $)			30	150	ps
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾				0.9	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽³⁾	50-MHz clock input ⁽⁴⁾		2	3	ps
$t_{jit(pp)}$	Peak-to-peak jitter ⁽³⁾⁽⁵⁾	100 Mbps 2 ¹⁵ –1 PRBS input ⁽⁶⁾		55	150	ps
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 7		4	7	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output			4	7	ns
t_{PZH}	Enable time, high-impedance-to-high-level output			4	7	ns
t_{PZL}	Enable time, high-impedance-to-low-level output			4	7	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) Part-to-part skew is defined as the difference in propagation delays between two devices that operate at the same V/T conditions.

(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(4) $t_r = t_f = 0.5$ ns (10% to 90%), measured over 30K samples.

(5) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

(6) $t_r = t_f = 0.5$ ns (10% to 90%), measured over 100K samples.

6.10 Switching Characteristics – Receiver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	$C_L = 15$ pF, See Figure 11	2	6	10	ns
t_{pHL}	Propagation delay time, high-to-low-level output		2	6	10	ns
t_r	Output signal rise time				2.3	ns
t_f	Output signal fall time				2.3	ns
$t_{sk(p)}$	Pulse skew ($ t_{pHL} - t_{pLH} $)	Type 2 $C_L = 15$ pF, See Figure 11		400	750	ps
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	$C_L = 15$ pF, See Figure 11			1	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽³⁾	50-MHz clock input ⁽⁴⁾		2		ps
$t_{jit(pp)}$	Peak-to-peak jitter ⁽³⁾⁽⁵⁾	Type 2 100 Mbps 2 ¹⁵ –1 PRBS input ⁽⁶⁾		225	800	ps
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 12		6	10	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output			6	10	ns
t_{PZH}	Enable time, high-impedance-to-high-level output			10	15	ns
t_{PZL}	Enable time, high-impedance-to-low-level output			10	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) Part-to-part skew is defined as the difference in propagation delays between two devices that operate at the same V/T conditions.

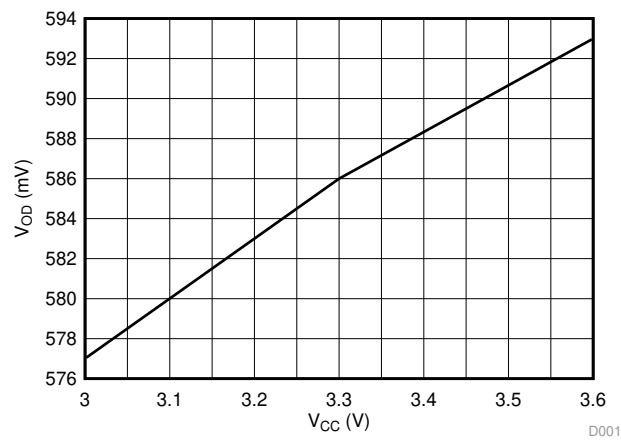
(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(4) , $V_{ID} = 400$ mV_{pp}, $V_{cm} = 1$ V, $t_r = t_f = 0.5$ ns (10% to 90%), measured over 30K samples.

(5) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$)

(6) , $V_{ID} = 400$ mV_{pp}, $V_{cm} = 1$ V, $t_r = t_f = 0.5$ ns (10% to 90%), measured over 100K samples.

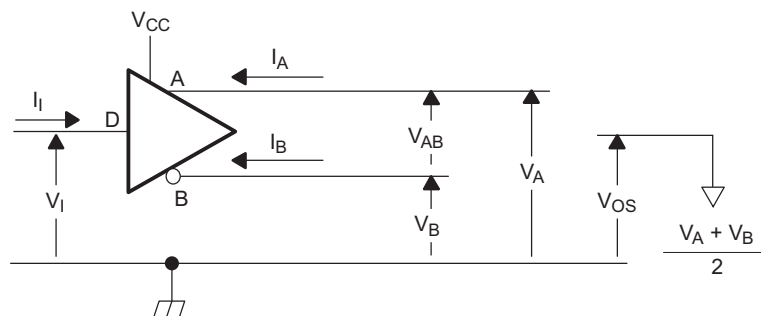
6.11 Typical Characteristics



$T_A = 25^\circ\text{C}$

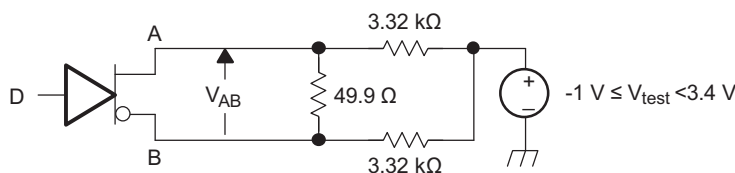
Figure 1. Differential Output Voltage vs Supply Voltage

7 Parameter Measurement Information



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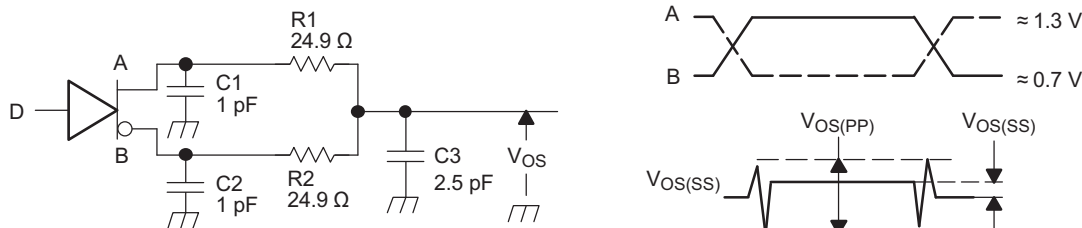
Figure 2. Driver Voltage and Current Definitions



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- A. All resistors are 1% tolerance.

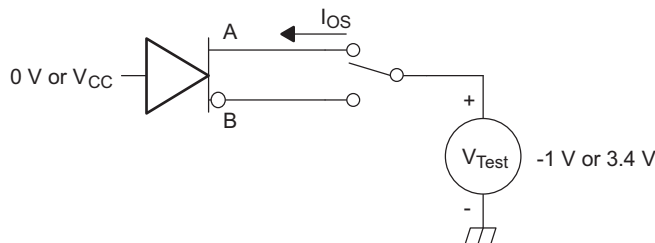
Figure 3. Differential Output Voltage Test Circuit



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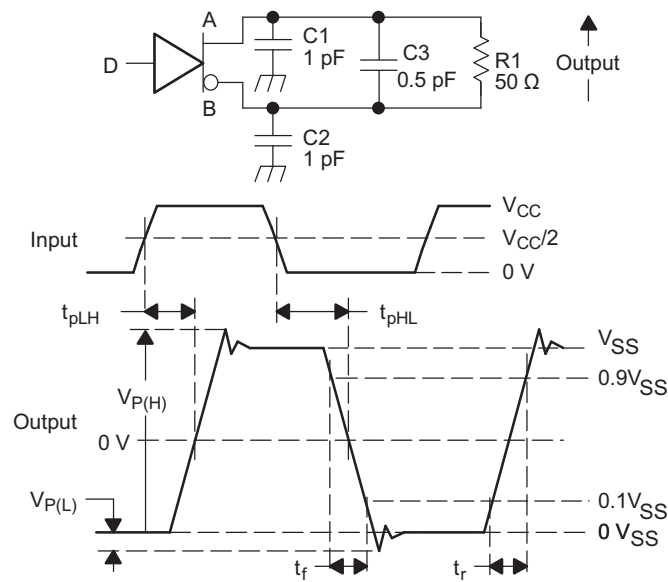
- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.
- C. R1 and R2 are metal film, surface mount, $\pm 1\%$, and located within 2 cm of the D.U.T.
- D. The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



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Figure 5. Driver Short-Circuit Test Circuit

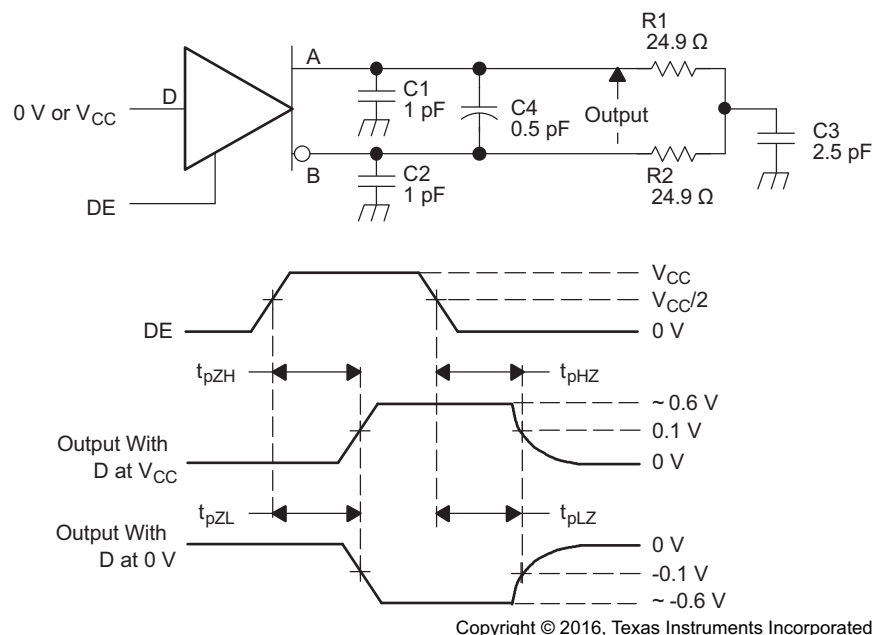
Parameter Measurement Information (continued)


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- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.
- C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 6. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

Parameter Measurement Information (continued)



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.
- C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 7. Driver Enable and Disable Time Circuit and Definitions

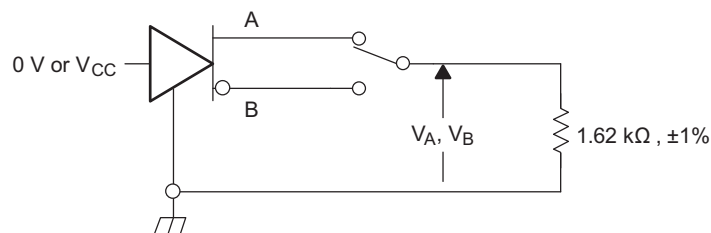
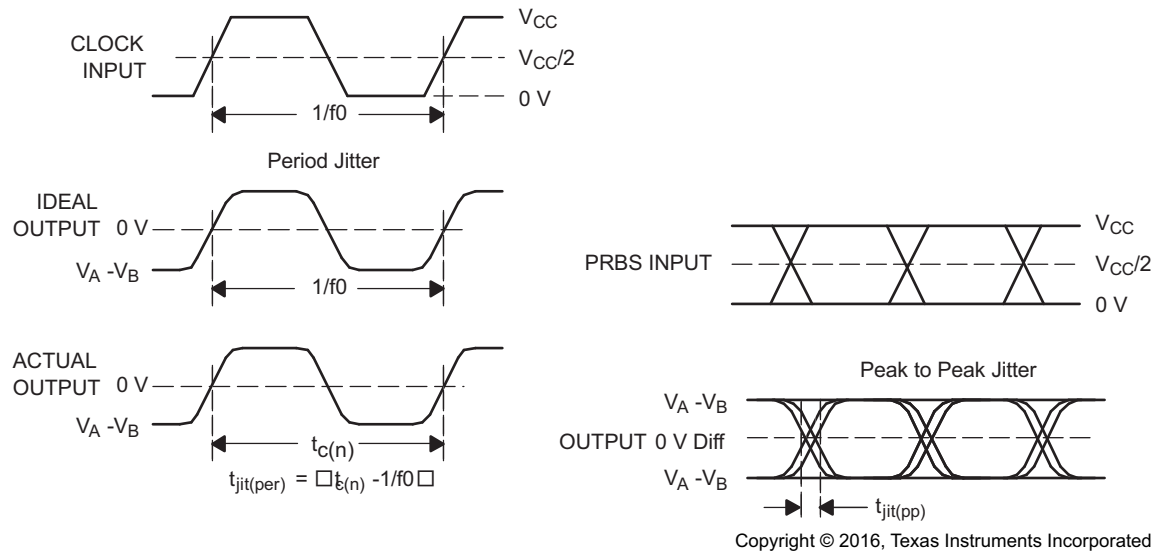


Figure 8. Maximum Steady State Output Voltage

Parameter Measurement Information (continued)



- All input pulses are supplied by an Agilent 81250 Stimulus System.
- The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
- Peak-to-peak jitter is measured using a 100 Mbps 2¹⁵-1 PRBS input.

Figure 9. Driver Jitter Measurement Waveforms

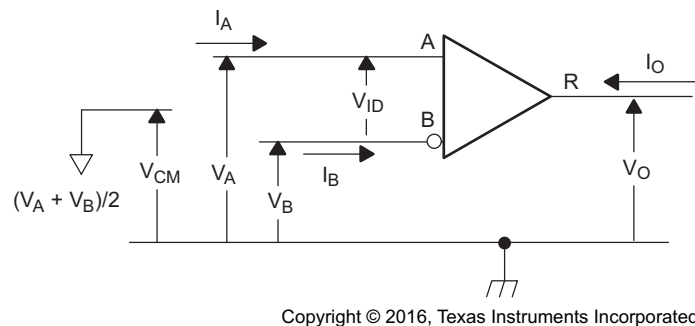
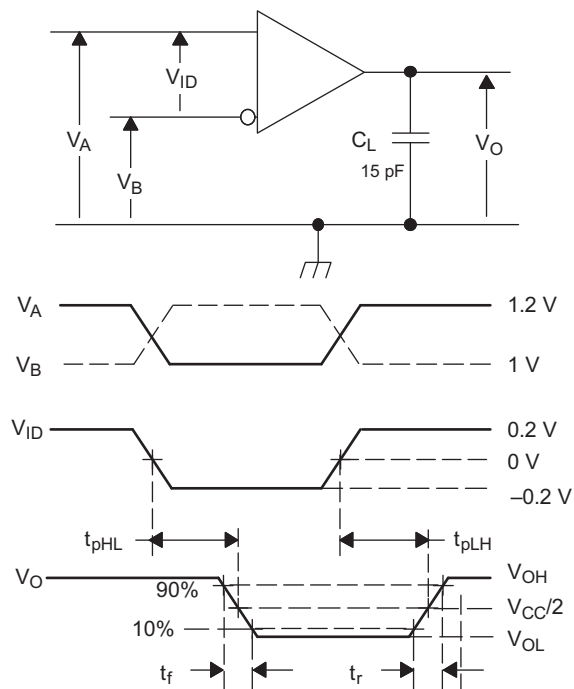


Figure 10. Receiver Voltage and Current Definitions

Table 1. Type-2 Receiver Input Threshold Test Voltages

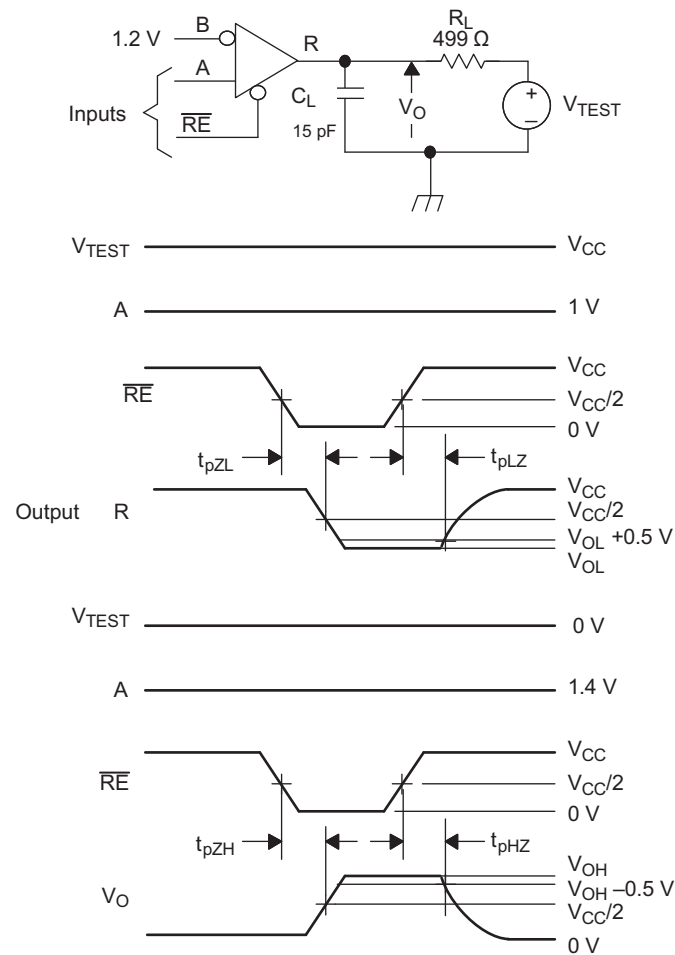
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	RECEIVER OUTPUT ⁽¹⁾
V _{IA}	V _{IB}	V _{ID}	V _{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.475	3.325	0.150	3.4	H
3.425	3.375	0.050	3.4	L
-0.925	-1.075	0.150	-1	H
-0.975	-1.025	0.050	-1	L

(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE} = L$)



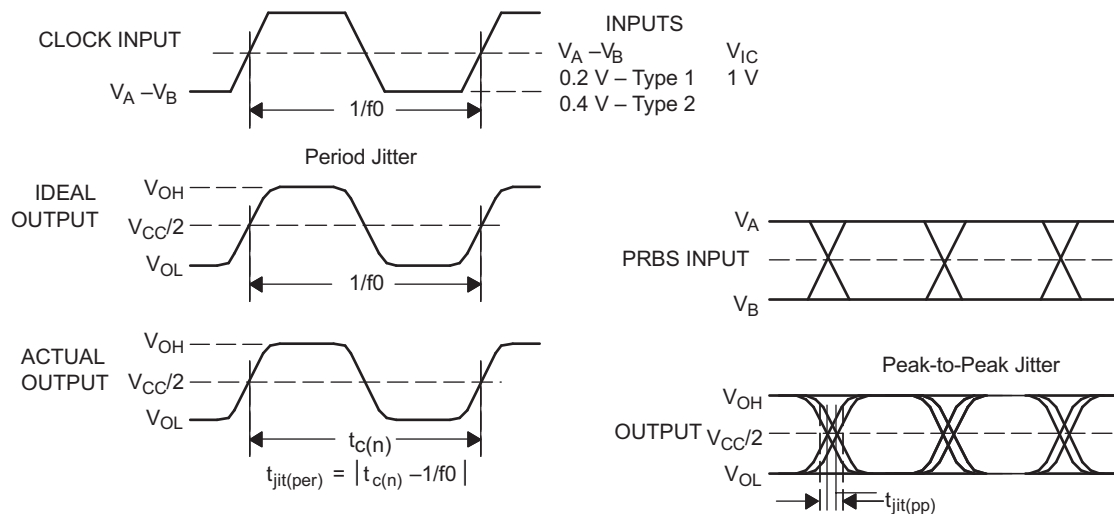
- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.
- B. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 11. Receiver Timing Test Circuit and Waveforms



- All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
- C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and $\pm 20\%$.

Figure 12. Receiver Enable and Disable Time Test Circuit and Waveforms



- A. All input pulses are supplied by an Agilent 8304A Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter is measured using a 50 MHz 50 \pm 1% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 100 Mbps 2^{15} -1 PRBS input.

Figure 13. Receiver Jitter Measurement Waveforms

Feature Description (continued)

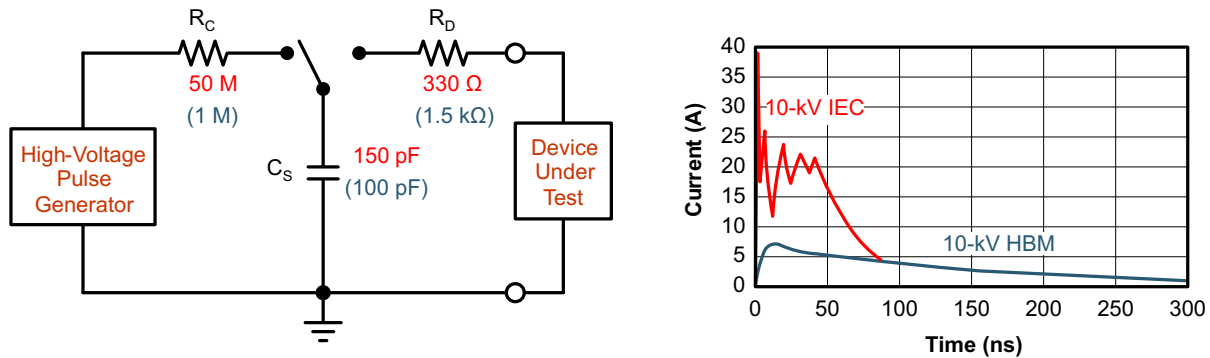


Figure 15. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

8.4 Device Functional Modes

8.4.1 Operation with $V_{CC} < 1.5\text{ V}$

Bus pins will be high impedance under this condition.

8.4.2 Operations with $1.5\text{ V} \leq V_{CC} < 3\text{ V}$

Operation with supply voltages in the range of $1.5\text{ V} \leq V_{CC} < 3\text{ V}$ is undefined and no specific device performance is guaranteed in this range.

8.4.3 Operation with $3\text{ V} \leq V_{CC} < 3.6\text{ V}$

Operation with the supply voltages greater than or equal to 3 V and less than or equal to 3.6 V is normal operation.

8.4.4 Device Function Tables

Table 2. Type-2 Receiver⁽¹⁾

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	\overline{RE}	R
$V_{ID} \geq 150\text{ mV}$	L	H
$50\text{ mV} < V_{ID} < 150\text{ mV}$	L	?
$V_{ID} \leq 50\text{ mV}$	L	L
X	H	Z
X	Open	Z

(1) H = high level, L = low level, Z = high impedance, X = Don't care, ? - indeterminate

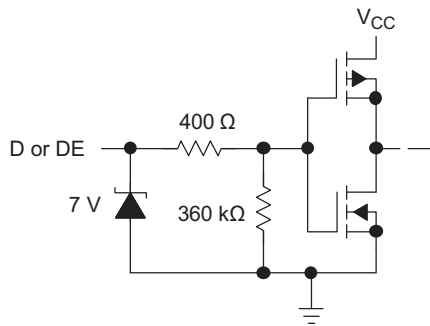
Table 3. Driver⁽¹⁾

INPUTS	ENABLE	OUTPUTS	
D	DE	A	B
L	H	L	H
H	H	H	L
Open	H	L	H
X	Open	Z	Z
X	L	Z	Z

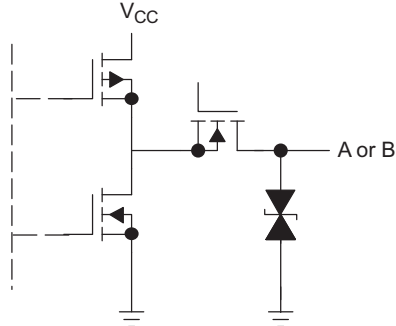
(1) H = high level, L = low level, Z = high impedance, X = Don't care, ? - indeterminate

8.4.5 Equivalent Input and Output Schematic Diagrams

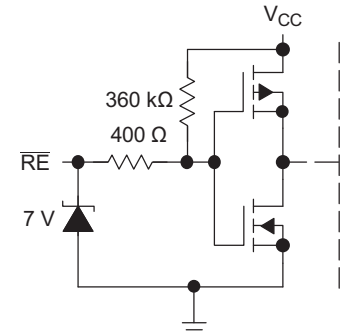
DRIVER INPUT AND DRIVER ENABLE



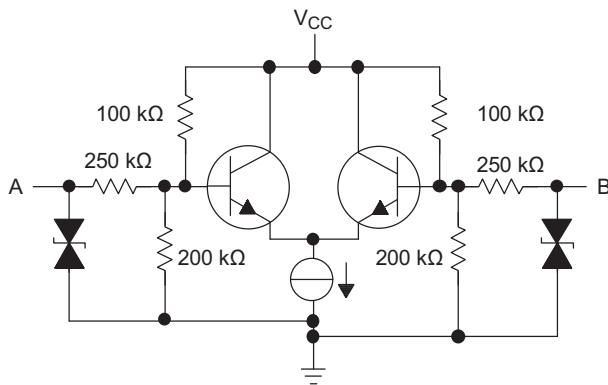
DRIVER OUTPUT



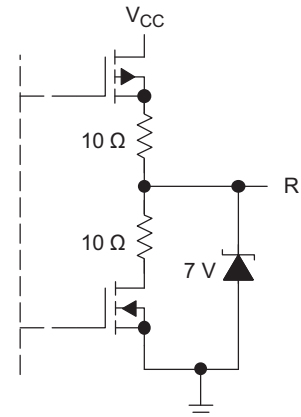
RECEIVER ENABLE



RECEIVER INPUT



RECEIVER OUTPUT



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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65MLVD204B is a multipoint line drivers and receivers. The functionality of these devices is simple, yet extremely flexible, leading to their use in designs ranging from wireless base stations to desktop computers.

9.2 Typical Application

9.2.1 Multipoint Communications

In a multipoint configuration many transmitters and many receivers can be interconnected on a single transmission line. The key difference compared to multi-drop is the presence of two or more drivers. Such a situation creates contention issues that need not be addressed with point-to-point or multidrop systems. Multipoint operation allows for bidirectional, half-duplex communication over a single balanced media pair. To support the location of the various drivers throughout the transmission line, double termination of the transmission line is now necessary.

The major challenge that system designers encounter are the impedance discontinuities that device loading and device connections (stubs) introduce on the common bus. Matching the impedance of the loaded bus and using signal drivers with controlled signal edges are the keys to error-free signal transmissions in multipoint topologies.

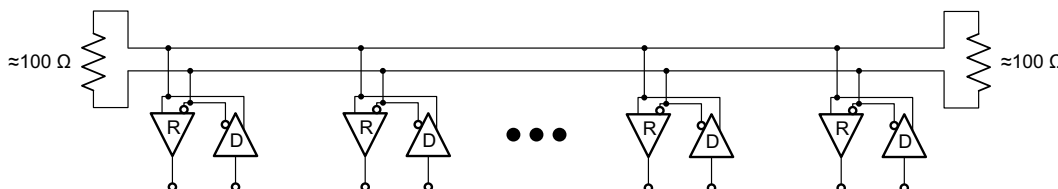


Figure 16. Multipoint Configuration

9.2.2 Design Requirements

For this design example, use the parameters listed in [Table 4](#).

Table 4. Design Parameters

PARAMETERS	VALUES
Driver supply voltage	3 to 3.6 V
Driver input voltage	0.8 to 3.3 V
Driver signaling rate	DC to 100 Mbps
Interconnect characteristic impedance	100 Ω
Termination resistance (differential)	100 Ω
Number of receiver nodes	2 to 32
Receiver supply voltage	3 to 3.6 V
Receiver input voltage	0 to ($V_{CC} - 0.8$) V
Receiver signaling rate	DC to 100 Mbps
Ground shift between driver and receiver	± 1 V

9.2.3 Detailed Design Procedure

9.2.3.1 Supply Voltage

The SN65MLVD204B operates from a single supply. The devices can support operation with a supply as low as 3 V and as high as 3.6 V.

9.2.3.2 Supply Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. At low frequencies, power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μF to 1000 μF) at the board level do a good job up into the kHz range. Due to their size and length of their leads, large capacitors tend to have large inductance values at the switching frequencies. To solve this problem, smaller capacitors (in the nF to μF range) must be installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with M-LVDS chips can be determined by [Equation 1](#) and [Equation 2](#), according to *High Speed Digital Design – A Handbook of Black Magic* by Howard Johnson and Martin Graham (1993). A conservative rise time of 4 ns and a worst-case change in supply current of 100 mA covers the whole range of M-LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 100 mV; however, this figure varies depending on the noise budget available for the design.

$$C_{\text{chip}} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{\text{MLVDS}} = \left(\frac{100 \text{ mA}}{100 \text{ mV}} \right) \times 4 \text{ ns} = 0.004 \mu\text{F} \quad (2)$$

[Figure 17](#) shows a configuration that lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 μF) and the value of capacitance found above (0.004 μF). Place the smallest value of capacitance as close as possible to the chip.



Figure 17. Recommended M-LVDS Bypass Capacitor Layout

9.2.3.3 Driver Input Voltage

The input stage accepts LVTTTL signals. The driver will operate with a decision threshold of approximately 1.4 V.

9.2.3.4 Driver Output Voltage

The driver outputs a steady state common mode voltage of 1 V with a differential signal of 540 V under nominal conditions.

9.2.3.5 Termination Resistors

As shown earlier, an M-LVDS communication channel employs a current source driving a transmission line which is terminated with two resistive loads. These loads serve to convert the transmitted current into a voltage at the receiver input. To ensure good signal integrity, the termination resistors should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistors are within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistors should be between 90 Ω and 110 Ω. The line termination resistors are typically placed at the ends of the transmission line.

9.2.3.6 Receiver Input Signal

The M-LVDS receivers herein comply with the M-LVDS standard and correctly determine the bus state. These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV of differential voltage over the common mode range of –1 V to 3.4 V.

9.2.3.7 Receiver Input Threshold (Failsafe)

The MLVDS standard defines a Type-1 and Type-2 receiver. Type-1 receivers have their differential input voltage thresholds near zero volts. Type-2 receivers have their differential input voltage thresholds offset from 0 V to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in Table 5 and Figure 18.

Table 5. Receiver Input Voltage Threshold Requirements

RECEIVER TYPE	OUTPUT LOW	OUTPUT HIGH
Type 1	$-2.4\text{ V} \leq V_{ID} \leq -0.05\text{ V}$	$0.05\text{ V} \leq V_{ID} \leq 2.4\text{ V}$
Type 2	$-2.4\text{ V} \leq V_{ID} \leq 0.05\text{ V}$	$0.15\text{ V} \leq V_{ID} \leq 2.4\text{ V}$

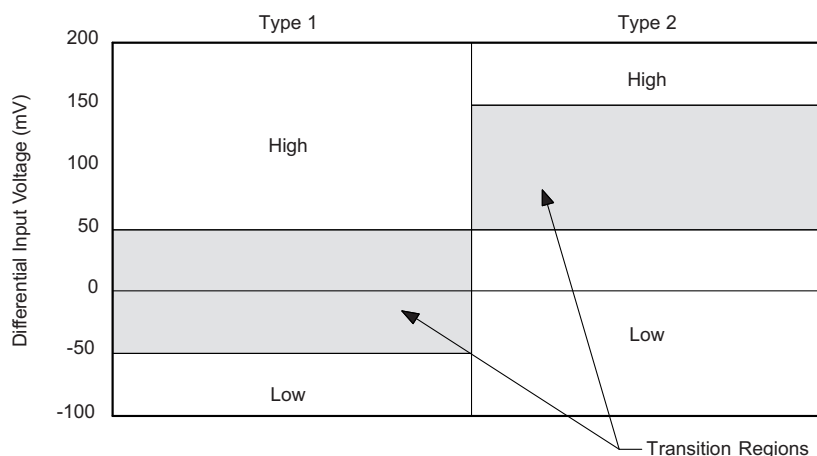


Figure 18. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region

9.2.3.8 Receiver Output Signal

Receiver outputs comply with LVTTTL output voltage standards when the supply voltage is within the range of 3 V to 3.6 V.

9.2.3.9 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the M-LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

9.2.3.10 PCB Transmission Lines

As per [SNLA187](#), [Figure 19](#) depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. [Figure 19](#) shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, if S is less than $2 \times W$, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

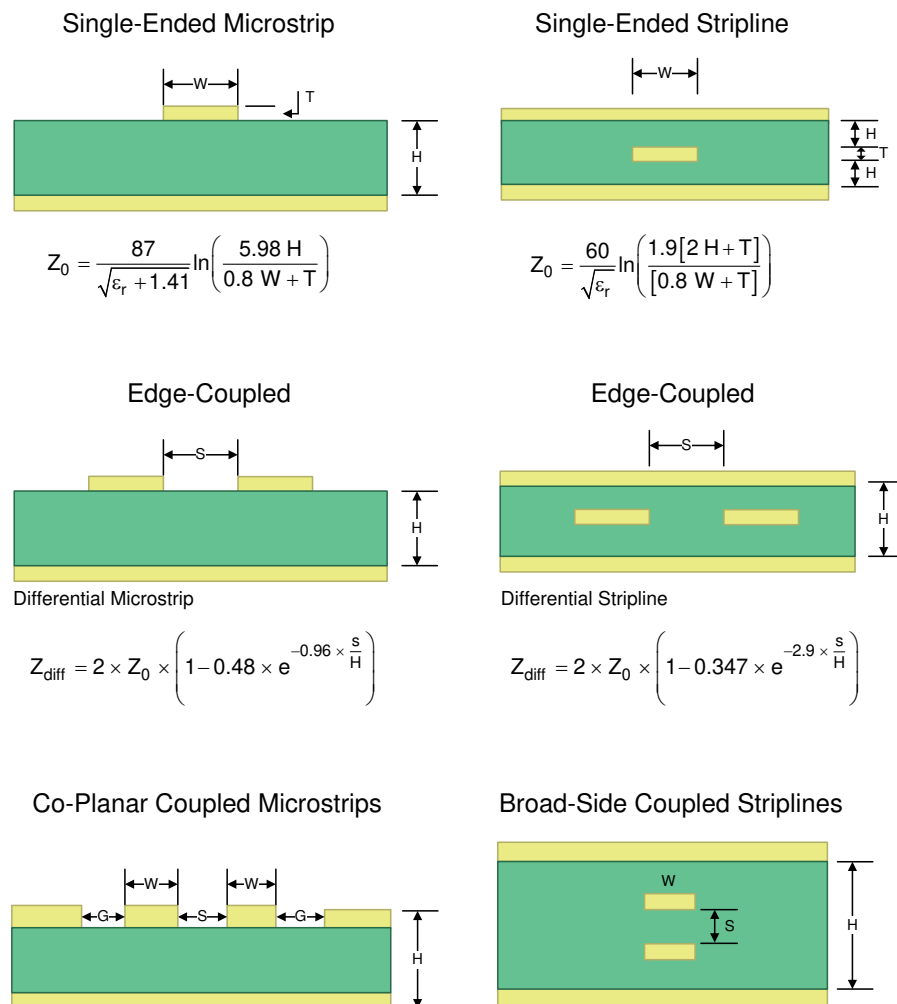
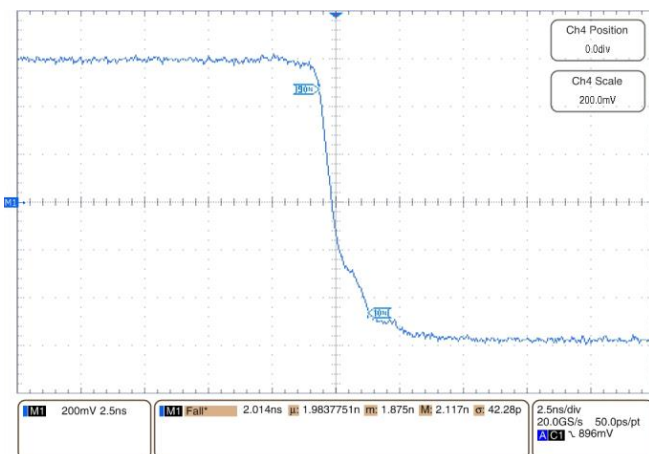


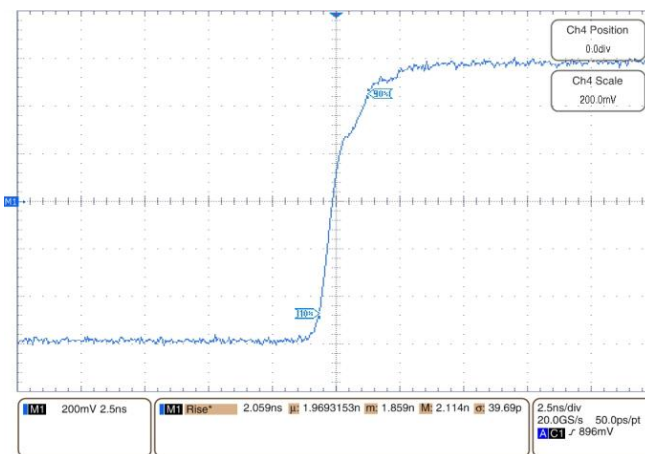
Figure 19. Controlled-Impedance Transmission Lines

9.2.4 Application Curves



$V_{CC} = 3.3\text{ V}$ $T_A = 25^\circ\text{C}$

Figure 20. Driver Fall Time



$V_{CC} = 3.3\text{ V}$ $T_A = 25^\circ\text{C}$

Figure 21. Driver Rise Time

10 Power Supply Recommendations

The M-LVDS driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 3 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than ± 1 V. Board level and local device level bypass capacitance should be used and are covered Supply Bypass Capacitance.

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per [SLLD009](#), printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in [Figure 22](#).

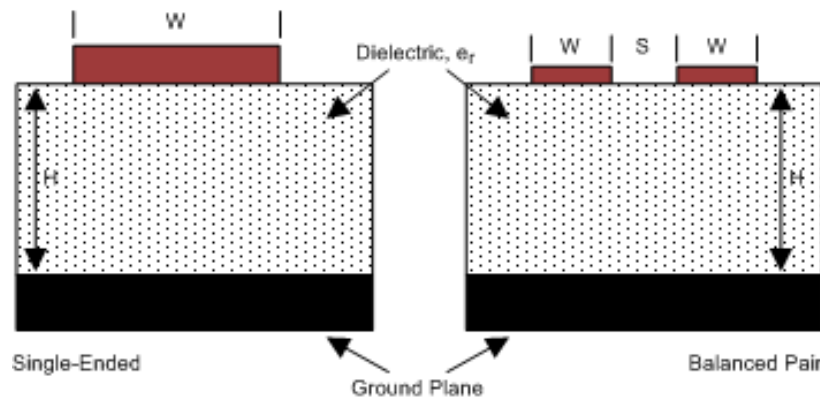


Figure 22. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing M-LVDS signals on microstrip transmission lines if possible. The PCB traces allow designers to specify the necessary tolerances for Z_0 based on the overall noise budget and reflection allowances. Footnotes 1⁽¹⁾, 2⁽²⁾, and 3⁽³⁾ provide formulas for Z_0 and t_{PD} for differential and single-ended traces. ⁽¹⁾ ⁽²⁾ ⁽³⁾

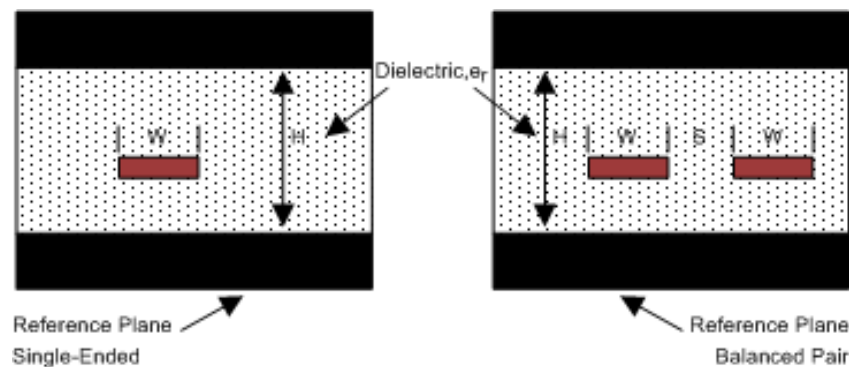


Figure 23. Stripline Topology

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.

(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Layout Guidelines (continued)

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with M-LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving M-LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 μm or 0.0003 in (minimum).
- Copper plating should be 25.4 μm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to M-LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in [Figure 24](#).

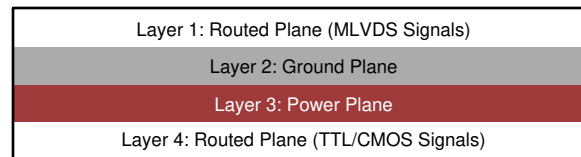


Figure 24. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 μm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in [Figure 25](#).

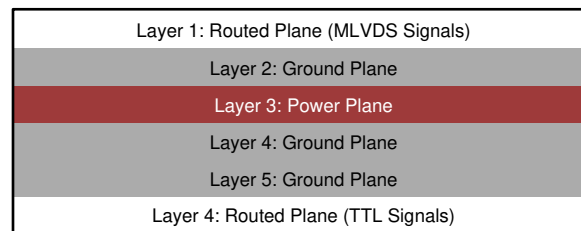


Figure 25. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

Layout Guidelines (continued)

11.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an M-LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent M-LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

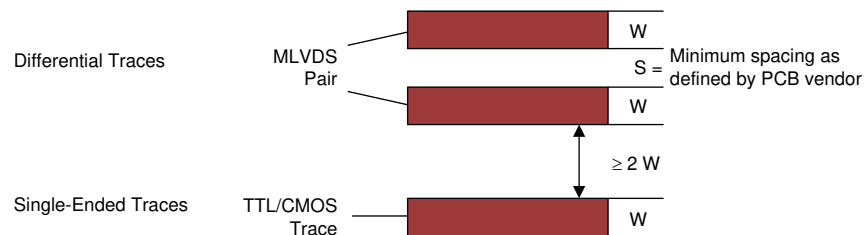


Figure 26. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

Layout Guidelines (continued)

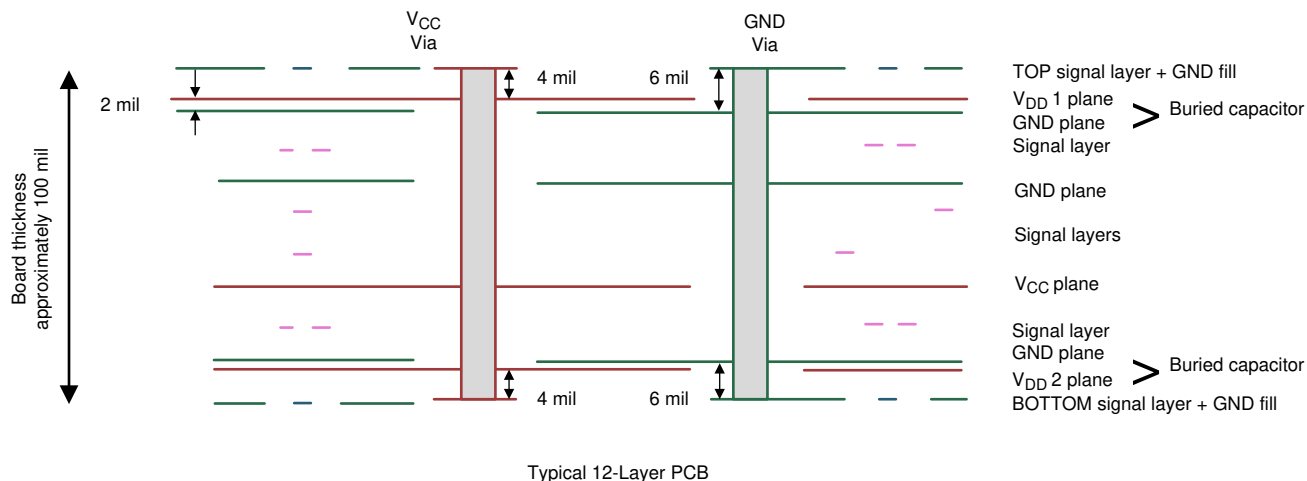


Figure 27. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402, 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 28(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 μ F, and 0.1 μ F are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center pad must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the pad connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 19) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND pad makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-pad spacing as shown in Figure 28(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.



Figure 28. Typical Decoupling Capacitor Layouts

11.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in [Figure 29](#).

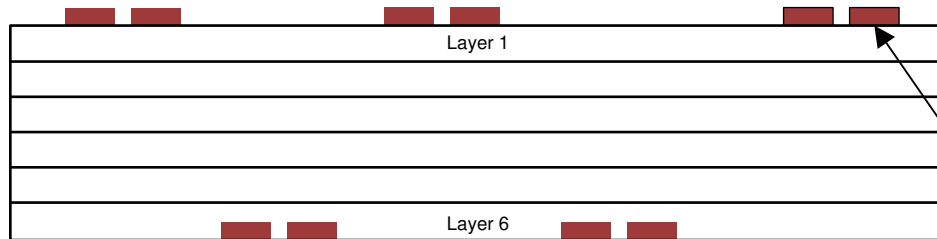


Figure 29. Staggered Trace Layout

Layout Example (continued)

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in [Figure 30](#). Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

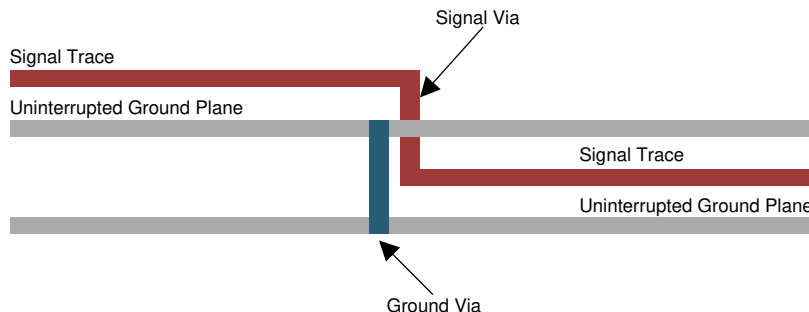


Figure 30. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 Trademarks

E2E is a trademark of Texas Instruments.

Rogers is a trademark of Rogers Corporation.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65MLVD204BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF204B	Samples
SN65MLVD204BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF204B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD204BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD204BDR	SOIC	D	8	2500	533.4	186.0	36.0

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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