Si8935/36/37 Data Sheet

Delta-Sigma Modulator for Voltage Measurement

The Si8935/36/37 is a galvanically isolated delta-sigma modulator optimized for voltage sensing. Its 2.5 V input range is ideal for isolated voltage sensing applications. The Si8935/36/37 provides excellent linearity with low offset and gain drift to ensure that accuracy is maintained over the entire operating temperature range. Exceptionally high common-mode transient immunity means that the Si8935/36/37 delivers accurate measurements even in the presence of high-power switching as is found in motor drive systems and inverters.

The output of the Si8935/36/37 comes from a second-order, delta-sigma modulator. The modulator can be clocked either from an onboard oscillator (Si8936/37) or from an external clock (Si8935). The output is typically digitally filtered by a MCU or FPGA in the system.

The Si8935/36/37 isolated delta-sigma modulator utilizes Silicon Labs' proprietary isolation technology. It supports up to 5.0 kVrms withstand voltage per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes compared to other isolation technologies.

Applications:

- Industrial, HEV and renewable energy inverters
- AC, Brushless, and DC motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies
- Automotive BMS and charging
- General industrial data acquisition and sensor interface

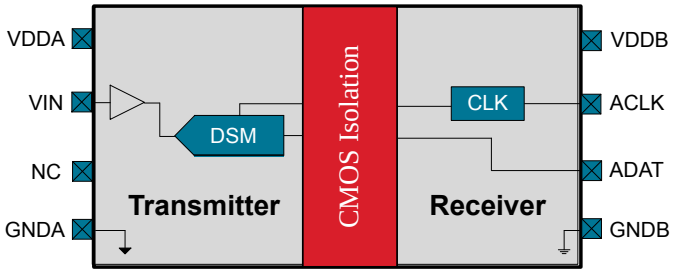
Safety Approvals (Pending):

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
  -
- CSA component notice 5A approval
  - IEC 60950-1 (reinforced insulation)
- VDE certification conformity
  - VDE0884 Part 10 (basic/reinforced insulation)
- CQC certification approval
  - GB4943.1

KEY FEATURES

- 0 to 2.5 V nominal input voltage
- Modulator clock options
  - External clock up to 25 MHz (Si8935)
  - 10 MHz internal clock (Si8936)
  - 20 MHz internal clock (Si8937)
- Typical input offset: ±0.6 mV
- Typical gain error: ±0.1%
- Excellent drift specifications
  - 1 µV/°C typical offset drift
  - 30 ppm/°C typical gain drift
- Typical nonlinearity: 0.02%
- Typical SNR: 81 dB
- High common-mode transient immunity: 75 kV/µs
- Compact packages
  - 8-pin wide body stretched SOIC
  - 8-pin narrow body SOIC
- –40 to 125 °C

Si8935, Si8936, Si8937



1. Ordering Guide

New Ordering Part Number (OPN)	Ordering Options			
	Input Range	Isolation Rating	Output	Package Type
Si8935D-IS4	0 to 2.5 V nominal	5.0 kVrms	DSM	WB Stretched SOIC-8
Si8935B-IS	0 to 2.5 V nominal	2.5 kVrms	DSM	NB SOIC-8
Si8936D-IS4	0 to 2.5 V nominal	5.0 kVrms	DSM	WB Stretched SOIC-8
Si8936B-IS	0 to 2.5 V nominal	2.5 kVrms	DSM	NB SOIC-8
Si8937D-IS4	0 to 2.5 V nominal	5.0 kVrms	DSM	WB Stretched SOIC-8
Si8937B-IS	0 to 2.5 V nominal	2.5 kVrms	DSM	NB SOIC-8

Note:

1. All packages are RoHS-compliant.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 pending qualification.

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2. System Overview

The input to the Si8935/36/37 is designed for 0 to 2.5 V nominal input.

The analog input stage of the Si8935/36/37 is a single-ended amplifier feeding the input of a second-order, delta-sigma (ΔΣ) modulator that digitizes the input signal into a 1-bit output stream. The isolated data output ADAT pin of the converter provides a stream of digital ones and zeros that is synchronous to the ACLK pin. The Si8936/37 clock is generated internally while the Si8935 clock is provided externally. The time average of this serial bit-stream output is proportional to the analog input voltage.

The Si8935/36/37 implements a fail-safe output when the high-side supply voltage VDDA goes away. The fail-safe output is steady state logic 0 on ADAT for the externally clocked Si8935. The fail-safe output is a steady state logic 1 on ADAT for the internally clocked Si8936/37. The clock output ACLK of the Si8946/47 will stop after 256 cycles with a steady state logic 1. When the supply comes back, the clock will be turned back on and normal DSM data stream will be output in approximately 200 µs. To differentiate from the fail-safe output, a full-scale input signal will generate a single one or zero every 128 bits at ADAT, depending on the actual polarity of the signal being sensed.

When a loss of VDDA supply occurs the part will automatically move into a lower power mode that reduces IDDB current to approximately 1 mA. Similarly, a loss of VDDB supply will reduce IDDA current to approximately 1 mA. When the supply voltage is returned, normal operation begins in approximately 250 µs.

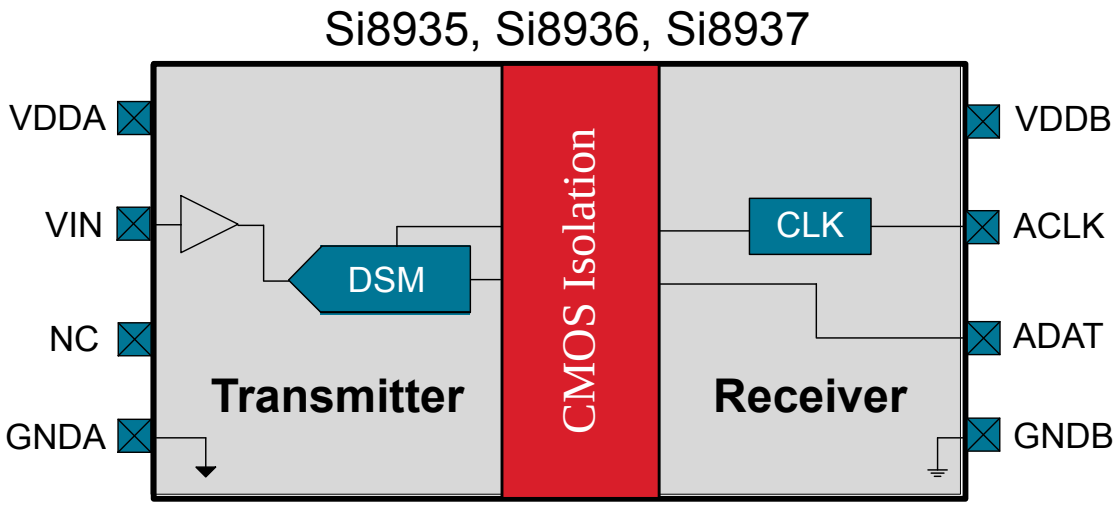


Figure 2.1. Si8935/36/37 Functional Block Diagram

2.1 Modulator

The output of the Si8935/36/37 comes from a second-order, delta-sigma modulator like that shown in the figure below. The modulator provides 1-bit datastream whose average represents the input analog voltage. 0 V across the inputs is represented at the output by a pulse train that has 50% ones density. Specified full-scale at the input (e.g., +2.25 V) produces an output datastream that has 92.87% ones density.

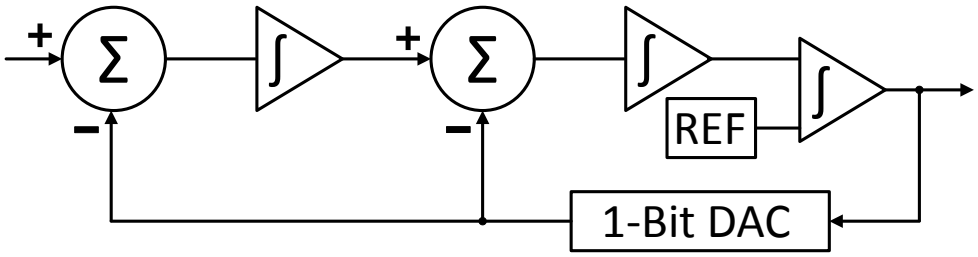


Figure 2.2. Typical 2nd Order Delta-Sigma Modulator Block Diagram

Table 2.1. Modulator Output

Single-Ended Input	Bitstream % Ones
2.25 V	92.87%
1.125 V	71.44%
0 V	50%

3. Voltage Sense Application

A typical isolated voltage sensing application circuit is shown below. In this example, a high voltage is divided down to produce a voltage (VIN) within the optimum input signal range of the Si8935/36/37. Numerous alternative inputs configurations are possible with the flexibility of a high impedance input isolator. The Si8935/36/37 senses the single-ended input voltage where it is oversampled and converted into a 1-bit bitstream, then transmitted across the isolation barrier to be processed by the system controller/FPGA. If the voltage sensed is > 2.5 V, a simple voltage divider consisting of R1 and R2 can be used to scale down any voltage to fit the input range of the Si8935/36/37. R2 < 10 kΩ is recommended for best performance.

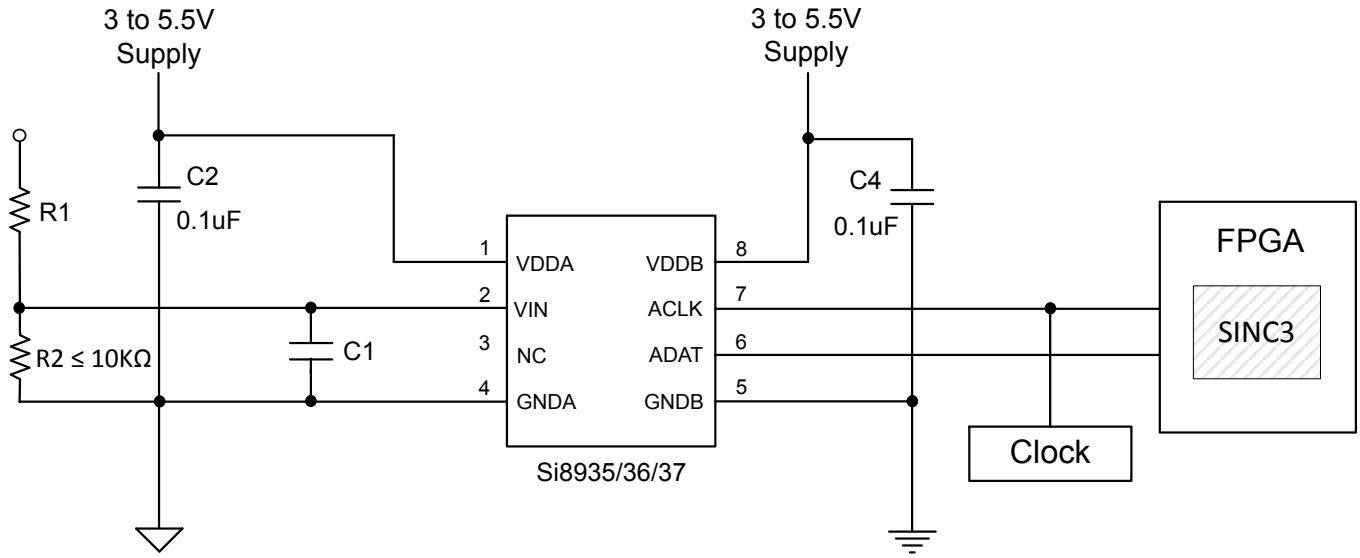


Figure 3.1. Voltage Sense Application

The Si8935/36/37 has intrinsic low-pass filtering at approximately 800 kHz. For applications where input filtering is required, a passive, differential RC low-pass filter can be placed at the input pin. Consider the source resistance of the signal measured (or the parallel combination of R1 and R2 if using a voltage divider) as it should be included in the filter calculation. Capacitor C1 should be sized to make a band limiting filter at the desired frequency.

C4, the local bypass capacitor for the B-side of Si8935/36/37, should be placed closed to VDDB supply pin with its return close to GNDB. The output signal typically goes directly to a digital filter for additional processing. The digital filter may be implemented by a dedicated FPGA in the system or may be a peripheral in the main system controller. The Si8935 expects an external clock to provide the clock signal for the modulator. That external clock can be provided by the same device that implements the digital filtering or another device that syncs both the modulator and the digital filter. The Si8936/37 generates an internal clock to the digital filter.

4. Electrical Specifications

Table 4.1. Electrical Specifications

V_{DDA}, V_{DDB} = 5 V, T_A = –40 to +125 °C; typical specs at 25 °C, SINC3 filter with 256 oversampling ratio and 20 MHz clock

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Side Supply Voltage	VDDA		3.0		5.5	V
Input Supply Current	IDDA	VDDA = 3.3 V	6.3	6.9	8.9	mA
Output Side Supply Voltage	VDDB		3.0		5.5	V
Output Supply Current (Si8935)	IDDB	VDDB = 3.3 V		4		mA
Output Supply Current (Si8936/37)	IDDB	VDDB = 3.3 V		8		mA
Amplifier Input						
Specified Linear Input Range	VIN		0.25		2.25	V
Maximum Input Voltage Before Clipping	VIN			2.5		V
Input Referred Offset	VOS	T_A = 25 °C, AIP = AIN = 0	–3	±0.6	3	mV
Input Offset Drift	VOS_T			1		µV/°C
Input Impedance	RIN			500		MΩ
Dynamic Characteristics						
Gain				1		
Gain Error		T_A = 25 °C	–0.3	±0.1	0.3	%
Gain Error Drift				±30		ppm/°C
Nonlinearity		T_A = 25 °C		0.02	0.05	%
Nonlinearity Drift				1		ppm/°C
Signal-to-Noise Ratio	SNR	F_{IN} = 5 kHz BW = 40 kHz (Si8935/37) BW = 20 kHz (Si8936)		81		dB
Total Harmonic Distortion	THD	F_{IN} = 5 kHz BW = 40 kHz (Si8935/37) BW = 20 kHz (Si8936)		–80		dB
Common-Mode Transient Immunity[1]	CMTI	VIN = GNDA, VCM = 1500 V	50	75		kV/µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power-Supply Rejection Ratio	PSRR	PSRR vs. VDDA at DC		–100		dB
		PSRR vs. VDDA at 100 mV and 10 kHz ripple		–100		dB
		PSRR vs. VDDB at DC		–100		dB
		PSRR vs. VDDB at 100 mV and 10 kHz ripple		–100		dB
Digital						
Logic high input threshold	V_{IH}		70% of VDDB			V
Logic low input threshold	V_{IL}				20% of VDDB	V
Input hysteresis	VIHYST			120		mV
Output load capacitance	C_{LOAD}			15		pF
External Clock (Si8935)						
Clock Frequency	FCLKIN		5		25	MHz
Duty Cycle	FDUTY		45	50	55	%
Delay to Data Valid	TDELAY				23	ns
Data Hold Time	THOLD		6			ns
Internal Clock (Si8936)						
Clock Frequency	FCLKOUT	T_A = 25 °C	9.9	10	10.1	MHz
		T_A = –40 °C to 125 °C	9.8	10	10.2	MHz
Duty Cycle	FDUTY		45	50	55	%
Delay to Data Valid	TDELAY				60	ns
Data Hold Time	THOLD		40			ns
Internal Clock (Si8937)						
Clock Frequency	FCLKOUT	T_A = 25 °C	19.8	20	20.2	MHz
		T_A = –40 °C to 125 °C	19.6	20	20.4	MHz
Duty Cycle	FDUTY		45	50	55	%
Delay to Data Valid	TDELAY				30	ns
Data Hold Time	THOLD		20			ns

Note:

1. An analog CMTI failure is defined as an output error of more than 100 mV persisting for at least 1 µs.

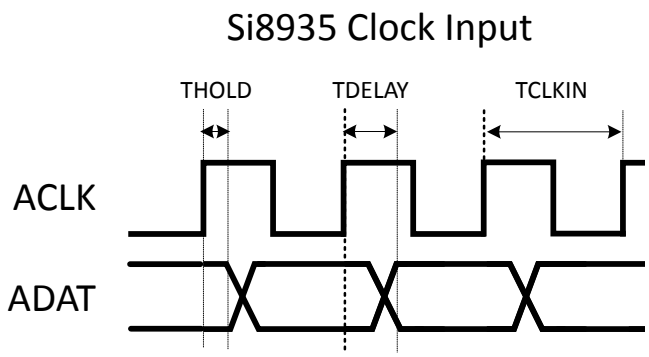


Figure 4.1. Si8935 Clock Input

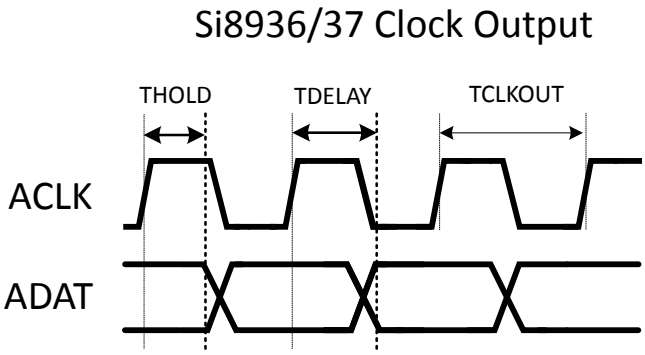


Figure 4.2. Si8936/37 Clock Output

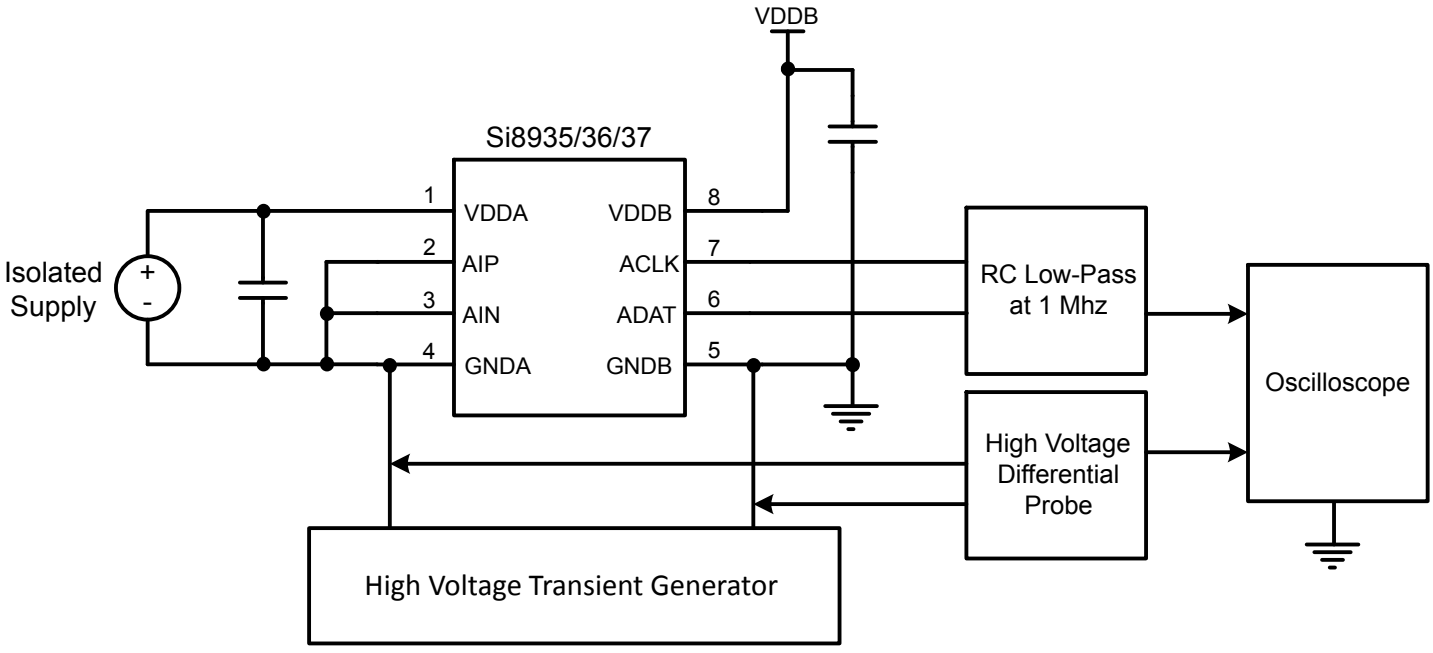


Figure 4.3. Common-Mode Transient Immunity Characterization Circuit

Table 4.2. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
Safety Temperature	T_S		150	°C
Safety Input Current (WB Stretched SOIC-8)	I_S	θ_{JA} = 90 °C/W VDD = 5.5 V T_J = 150 °C T_A = 25 °C	253	mA
		θ_{JA} = 90 °C/W VDD = 3.6 V T_J = 150 °C T_A = 25 °C	386	mA
Safety Input Current (NB SOIC-8)	I_S	θ_{JA} = 112 °C/W VDD = 5.5 V T_J = 150 °C T_A = 25 °C	310	mA
		θ_{JA} = 112 °C/W VDD = 3.6 V T_J = 150 °C T_A = 25 °C	203	mA
Safety Input Power (WB Stretched SOIC-8)	P_S	θ_{JA} = 90 °C/W T_J = 150 °C T_A = 25 °C	1389	mW
Safety Input Power (NB SOIC-8)	P_S	θ_{JA} = 112 °C/W T_J = 150 °C T_A = 25 °C	1116	mW
Device Power Dissipation (WB Stretched SOIC-8)	P_D		1.39	W
Device Power Dissipation (NB SOIC-8)	P_D		1.12	W

Note:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curves below.

Table 4.3. Thermal Characteristics

Parameter	Symbol	WB Stretched SOIC-8	NB SOIC-8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	90	112	°C/W

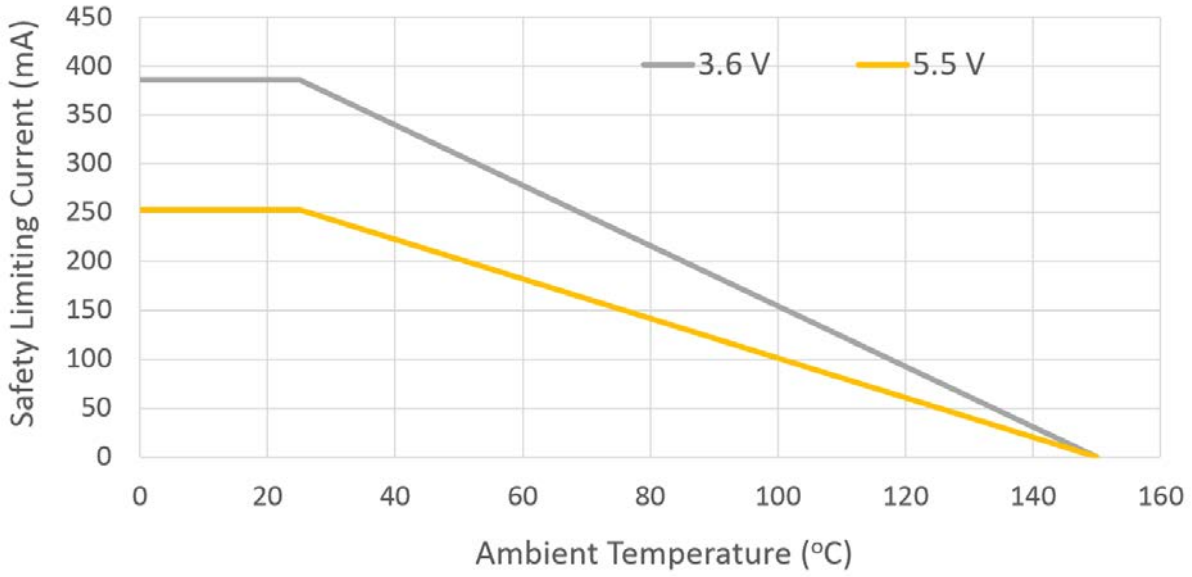


Figure 4.4. WB Stretched SOIC-8 Thermal Derating Curve for Safety Limiting Current

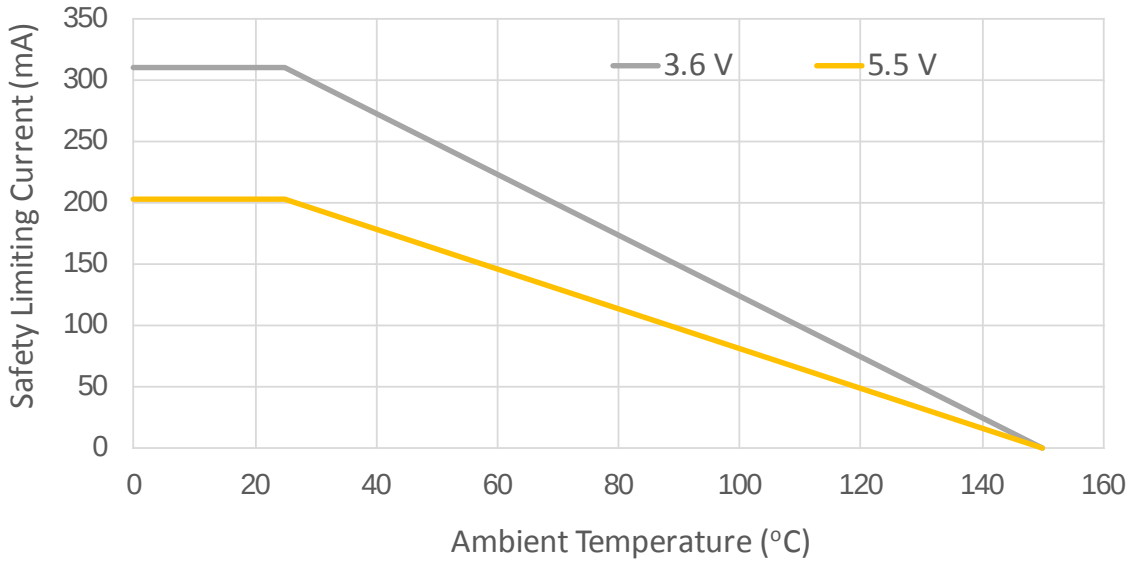


Figure 4.5. NB SOIC-8 Thermal Derating Curve for Safety Limiting Current

Table 4.4. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	150	°C
Ambient Temperature Under Bias	T_A	–40	125	°C
Junction Temperature	T_J	—	150	°C
Supply Voltage	VDDA, VDDB	–0.5	6.0	V
Input Voltage respect to GNDA	VIN	–0.5	VDDx + 0.5	V
Output Sink or Source Current	$\|I_O\|$	—	5	mA
Total Power Dissipation	P_T	—	212	mW
Lead Solder Termperature (10 s)		—	260	°C
Human Body Model ESD Rating		6000	—	V
Capacitive Discharge Model ESD Rating		2000	—	V
Maximum Isolation (WB Stretched SOIC-8 Input to Output) (1 s)		—	6500	V_{RMS}
Maximum Isolation (NB SOIC-8 package Input to Output) (1 s)		—	3250	V_{RMS}

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of the data sheet.

4.1 Regulatory Information

Table 4.5. Regulatory Information (Pending)[1, 2]

CSA
The Si8935/36/37 is certified under CSA Component Acceptance Notice 5A. For more details, see Master Contract File 232873.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si8935/36/37 is certified according to VDE 0884-10. For more details, see File 5006301-4880-0001.
VDE 0884-10: Up to 1414 V_{peak} for reinforced insulation working voltage.
UL
The Si8935/36/37 is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si8935/36/37 is certified under GB4943.1-2011.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Note: 1. Regulatory Certifications apply to 5 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. 2. Regulatory Certifications apply to 2.5 kVRMS rated devices which are production tested to 3.0 kVRMS for 1 sec.

Table 4.6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Nominal External Air Gap (Clearance)	CLR		9.0[1]	4.9	mm
Nominal External Tracking (Creepage)	CPG		9.0[1]	4.01	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.762	0.254	mm
Tracking Resistance (Proof Tracking Index)	PTI or CTI	IEC60112	600	600	V
Erosion Depth	ED		0.04	0.04	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1	1	pF

Note:

1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as x.x mm minimum for the WB Stretched SOIC-8 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as x.x mm minimum for the WB Stretched SOIC-8 package.
2. To determine resistance and capacitance, the Si8935/36/37 is converted into a two-terminal device. Pins 1–4 are shorted together to form the first terminal, and pins 5–8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 4.7. IEC 60664-1 (VDE 0884) Ratings

Parameter	Test Conditions	Specification
		WB Stretched SOIC-8
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 450 V_{RMS}	I-III
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III

Table 4.8. VDE 0884-10 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
			WB Stretched SOIC-8	
Maximum Working Insulation Voltage	V_{IORM}		1414	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2650	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	8000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

Note:

1. This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si8935/36/37 provides a climate classification of 40/125/21.

5. Pin Descriptions

5.1 Si8935/36/37 Pin Descriptions

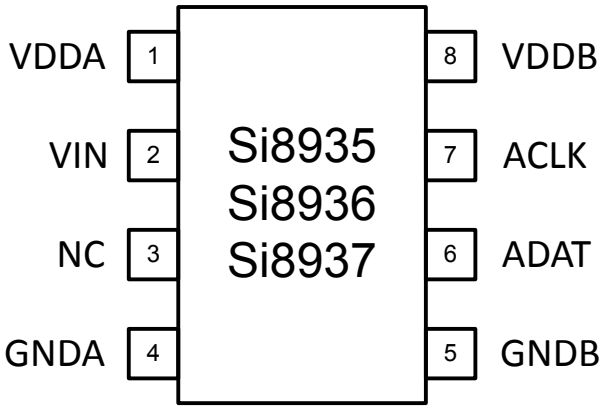


Table 5.1. Si8935/36/37 Pin Descriptions

Name	Pin #	Description
VDDA	1	Input side power supply
VIN	2	Voltage input
NC[1]	3	No Connect
GNDA	4	Input side ground
GNDB	5	Output side ground
ADAT	6	Delta-Sigma Modulator data output
ACLK	7	Delta-Sigma Modulator clock (input on Si8935, output on Si8936/37)
VDDB	8	Output power supply

Note:

1. No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

6. Packaging

6.1 Package Outline: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the package details for the Si8935/36/37 in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

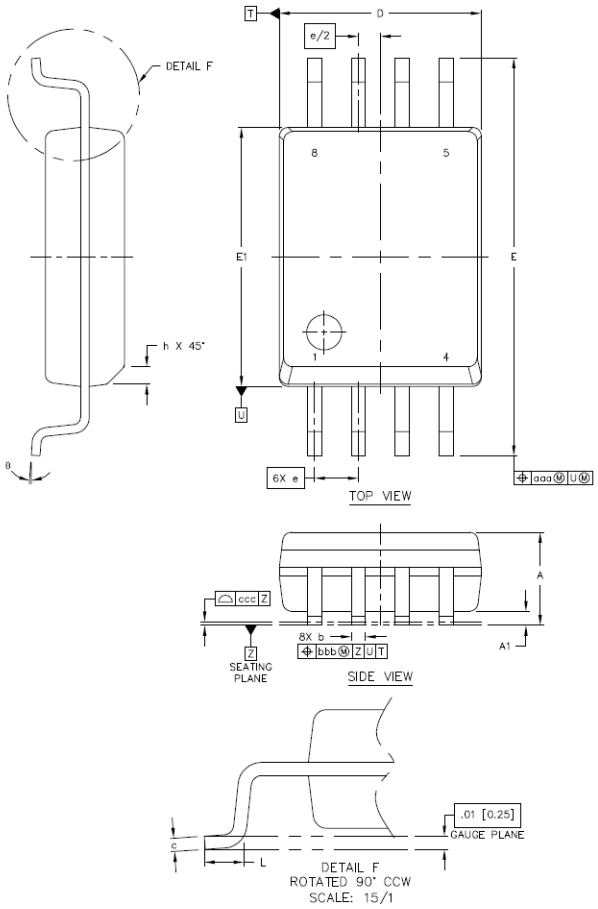


Figure 6.1. 8-Pin Wide Body Stretched SOIC Package

Table 6.1. 8-Pin Wide Body Stretched SOIC Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.20	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
h	0.25	0.76

Symbol	Millimeters	
	Min	Max
θ	0°	8°
aaa	—	0.25
bbb	—	0.25
ccc	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

6.2 Package Outline: 8-Pin Narrow Body SOIC

The figure below illustrates the package details for the Si8935/36/37 in an 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

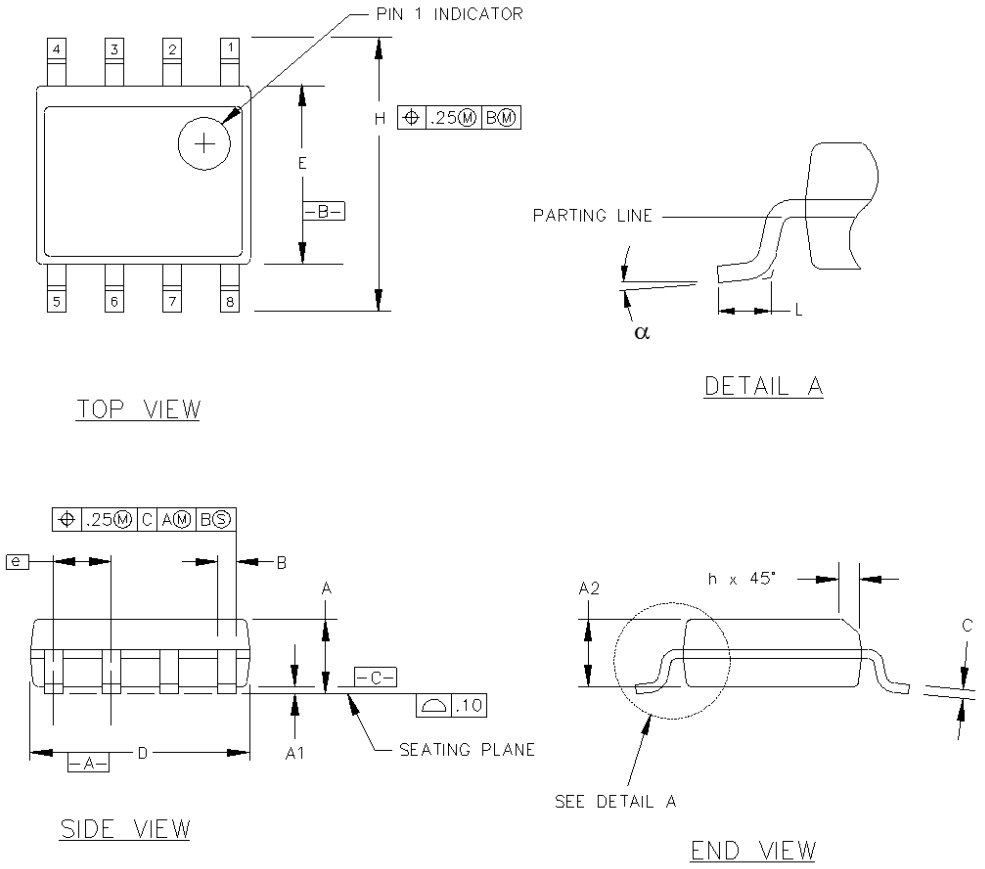


Figure 6.2. 8-Pin Narrow Body SOIC Package

Table 6.2. 8-Pin Narrow Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for Small Body Components.

6.3 Land Pattern: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the recommended land pattern details for the Si8935/36/37 in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

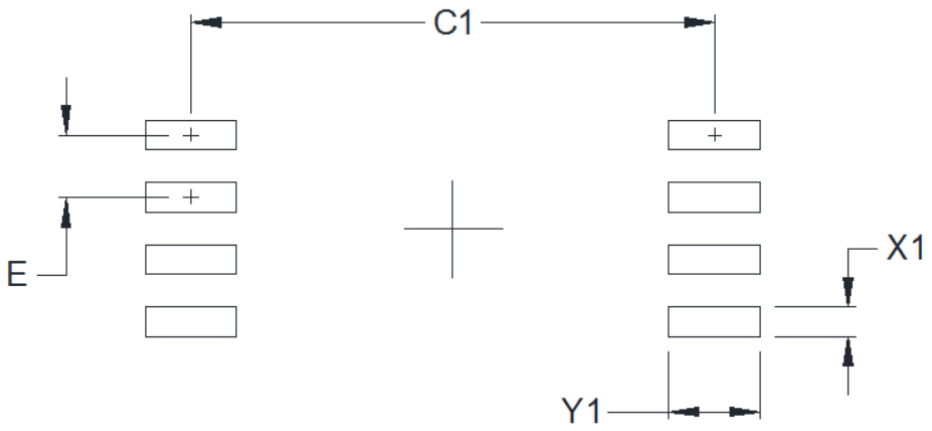


Figure 6.3. 8-Pin Wide Body Stretched SOIC Land Pattern

Table 6.3. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions[1]

Dimension	(mm)
C1	10.60
E	1.27
X1	0.60
Y1	1.85

Note:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.4 Land Pattern: 8-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the Si8935/36/37 in an 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

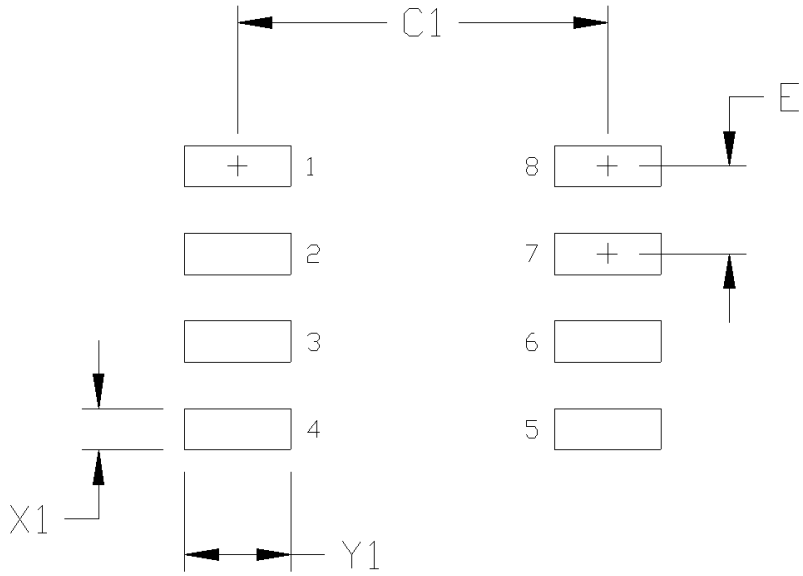


Figure 6.4. 8-Pin Narrow Body SOIC Land Pattern

Table 6.4. 8-Pin Narrow Body SOIC Land Pattern Dimensions

Symbol	mm
C1	5.40
E	1.27
X1	0.60
Y1	1.55

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

6.5 Top Marking: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the top markings for the Si8935/36/37 in an 8-Pin Wide Body Stretched SOIC package. The table explains the top marks shown in the illustration.

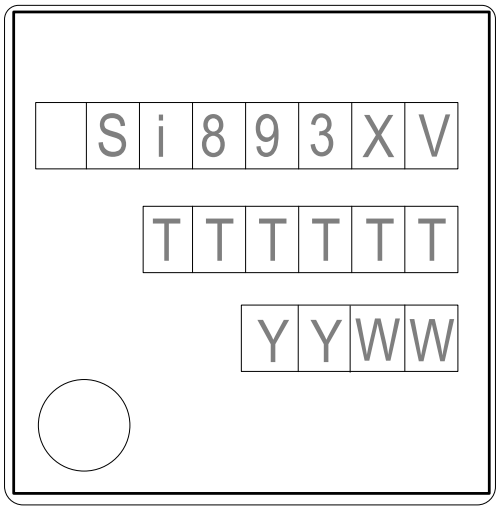


Figure 6.5. Si893x Wide Body Stretched 8-Pin SOIC Top Marking

Table 6.5. Si893x Wide Body Stretched 8-Pin SOIC Top Mark Explanation

Line 1 Marking:	Customer Part Number	Si893X X = Base part number • 5 = External clock • 6 = Internal 10 MHz clock • 7 = Internal 20 MHz clock V = Insulation rating: • D = 5.0 kV
Line 2 Marking:	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	YY = Year WW = Work Week Circle = 43 mils Diameter Left-Justified	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

6.6 Top Marking: 8-Pin Narrow Body SOIC

The figure below illustrates the top markings for the Si8935/36/37 in an 8-Pin Narrow Body SOIC package. The table explains the top marks shown in the illustration.

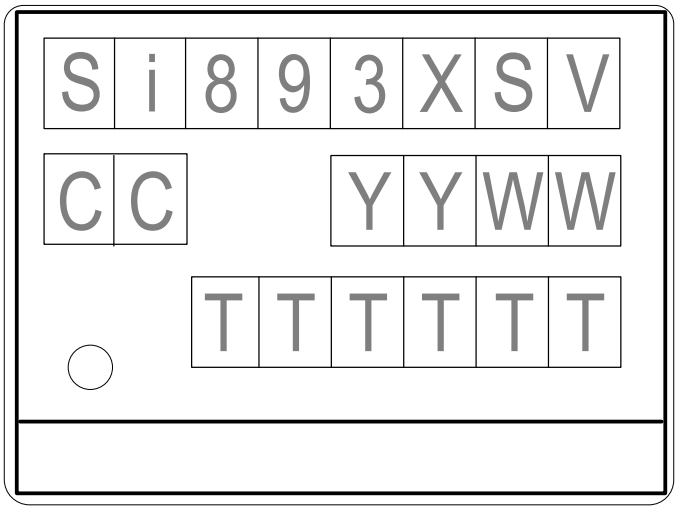


Figure 6.6. 8-Pin Narrow Body SOIC Top Marking

Table 6.6. 8-Pin Narrow Body SOIC Top Marking Explanation

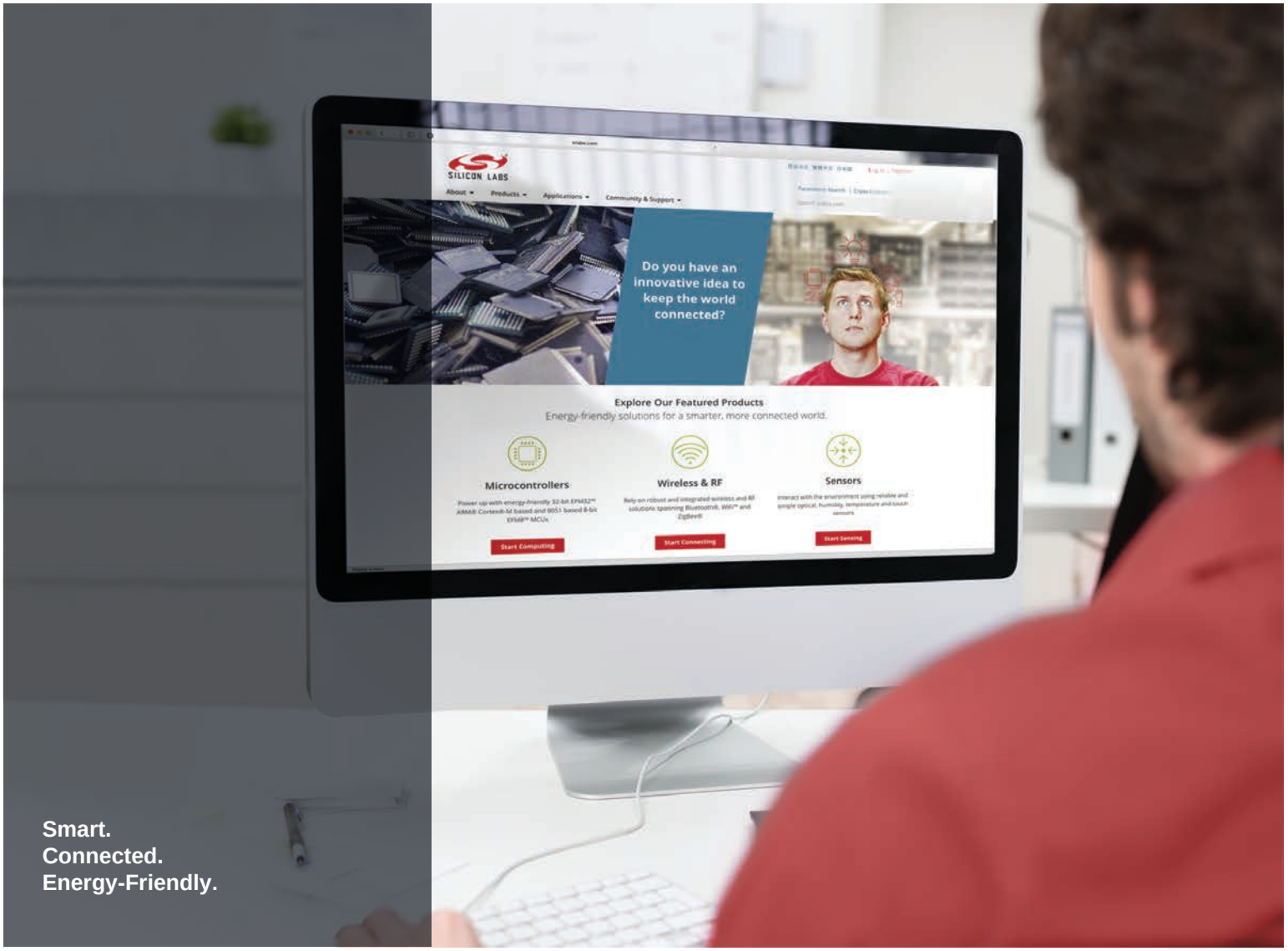
Line 1 Marking:	Customer Part Number	Si893X X = Base part number • 5 = External clock • 6 = Internal 10 MHz clock • 7 = Internal 20 MHz clock V = Insulation rating: • B = 2.5 kV
Line 2 Marking:	CC = Country of Origin ISO Code Abbreviation YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Line 3 Marking:	TTTTTT = Mfg Code Circle = 19.7 mils Diameter Left-Justified	Manufacturing Code from the Assembly Purchase Order form.

7. Document Revision History

Revision 0.1

March, 2019

- Initial release.



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