UCC2753x 2.5-A and 5-A, 35-V_{MAX} VDD FET and IGBT Single-Gate Driver

1 Features

- Low-cost gate driver (offering optimal solution for driving FET and IGBTs)
- Superior replacement to discrete transistor pair drive (providing easy interface with controller)
- TTL and CMOS compatible input logic threshold (independent of supply voltage)
- Split output options allow for tuning of turnon and turnoff currents
- Inverting and noninverting input configurations
- Enable with fixed TTL compatible threshold
- High 2.5-A source and 2.5-A or 5-A sink peak drive currents at 18-V VDD
- Wide VDD range from 10 V to 35 V
- Input and enable pins capable of with standing up to –5-V DC below ground
- Output held low when inputs are floating or during VDD UVLO
- Fast propagation delays (17-ns Typical)
- Fast rise and fall times
  (15-ns and 7-ns typical with 1800-pF Load)
- Undervoltage lockout (UVLO)
- Used as a high-side or low-side driver (if designed with proper bias and signal isolation)
- Low-cost, space-saving 5-pin or 6-pin DBV (SOT-23) package options
- UCC27536 and UCC27537 pin-to-pin compatible to TPS2828 and TPS2829
- Operating temperature range of –40°C to 140°C

2 Applications

- Switched-mode power supplies
- DC-to-DC converters
- Solar inverters, motor control, UPS
- HEV and EV chargers
- Home appliances
- Renewable energy power conversion
- SiC FET converters

3 Description

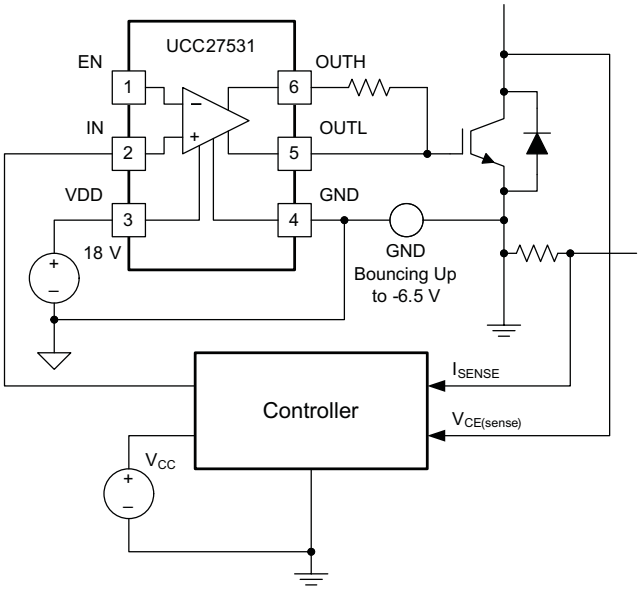
The UCC2753x single-channel, high-speed gate drivers can effectively drive MOSFET and IGBT power switches. Using a design that allows for a source of up to 2.5 A and 5-A sink through asymmetrical drive (split outputs), coupled with the ability to support a negative turn-off bias, rail-to-rail drive capability, extremely small propagation delay (17 ns typical), the UCC2753x devices are ideal solutions for MOSFET and IGBT power switches. The UCC2753x family of devices can also support enable, dual input, and inverting and non-inverting input functionality. The split outputs and strong asymmetrical drive boost the devices immunity against parasitic Miller turn-on effect and can help reduce ground debouncing.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27531	SOIC (8)	4.90 mm × 3.91 mm
UCC27531	SOT-23 (6)	2.90 mm × 1.60 mm
UCC27533	SOT-23 (5)	2.90 mm × 1.60 mm
UCC27536	SOT-23 (5)	2.90 mm × 1.60 mm
UCC27537	SOT-23 (5)	2.90 mm × 1.60 mm
UCC27538	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Driving IGBT Without Negative Bias



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2015) to Revision G — **Page**

- Changed to "H" from "L" ... 21
- Changed to "L" from "H" ... 21

Changes from Revision E (July 2014) to Revision F — **Page**

- Changed EN for UCC27531 From: Yes To: Yes / No in *Device Comparison Table* ... 4
- Changed OUTPUT for UCC27531 From: Split To: Split / Single*Device Comparison Table* ... 4
- Added the 8-Pin SOIC package to the *Pin Configuration and Functions* section ... 5
- Added UCC27531D to the *Pin Functions* table ... 6
- Changed PMOS Symbol in Figure 32 ... 16
- Changed PMOS and Logic Symbol in Figure 33 ... 16
- Changed PMOS and Logic Symbols in Figure 34 ... 16
- Changed PMOS and Logic Symbol in Figure 35 ... 17
- Changed PMOS Symbol in Figure 36 ... 17
- Added Figure 37 ... 18
- Changed PMOS Symbol in Figure 39 ... 20
- Changed Enable Pin Column to Table 3 ... 21
- Added Table 6 ... 22

Changes from Revision D (April 2013) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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Changes from Revision C (April 2013) to Revision D **Page**

- Added Startup Current UCC27537 Bias Current Parameters to the ELECTRICAL CHARACTERISTICS..... 7
- Added UCC27531 Start-Up Current vs. Temperature TYPICAL CHARACTERISTICS diagram. 11
- Added UCC27537 Start-Up Current vs. Temperature TYPICAL CHARACTERISTICS diagram. 11

Changes from Revision B (April 2013) to Revision C **Page**

- Added additional DESCRIPTION information. 15

Changes from Revision A (December 2012) to Revision B **Page**

- Added UCC27533, UCC27536, UCC27537 and UCC27538 parts to the datasheet..... 1

Changes from Original (December 2012) to Revision A **Page**

- Changed Block Diagram..... 4

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5 Description (continued)

Leaving the input pin open holds the driver output low. The logic behavior of the driver is shown in the application diagram, timing diagram, and input and output logic truth table.

Internal circuitry on VDD pin provides an undervoltage lockout function that holds output low until VDD supply voltage is within operating range.

6 Device Comparison Table

	UCC27531	UCC27533	UCC27536	UCC27537	UCC27538
I_{ON} PEAK	2.5 A	2.5 A	2.5 A	2.5 A	2.5 A
I_{OFF} PEAK	5 A	5 A	2.5 A	5 A	5 A
PACKAGE	SOT-23-6 / SOIC-8	SOT-23-5	SOT-23-5	SOT-23-5	SOT-23-6
IN	Single	Dual	Single	Single	Dual
IN LOGIC	TTL/CMOS	TTL/CMOS	TTL/CMOS	TTL/CMOS	TTL/CMOS
EN	Yes / No	No	Yes	Yes	No
OUTPUT	Split / Single	Single	Single	Single	Split
INVERTING	No	Inverting/Non-Inverting	Yes	No	No
MAX VDD	35 V	35 V	35 V	35 V	35 V

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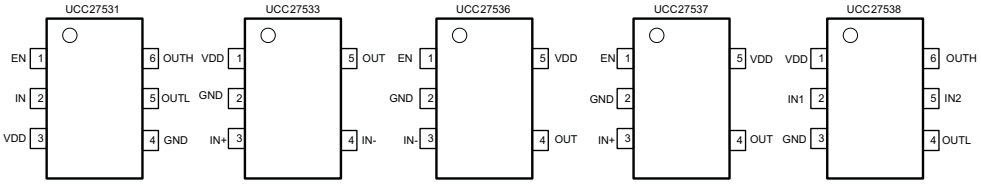
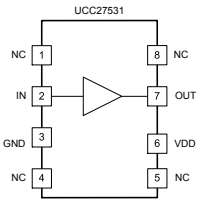
7 Pin Configuration and Functions

5-Pin or 6-Pin SOT-23
DBV Package
Top View



8-Pin SOIC
D Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
UCC27531DBV			
1	EN	I	Enable (Pull EN to GND to disable output, pull it high or leave open to enable output)
2	IN	I	Driver non-inverting input
3	VDD	I	Bias supply input
4	GND	-	Ground (all signals are referenced to this node)
5	OUTL	O	5-A sink current output of driver
6	OUTH	O	2.5-A Source Current Output of driver
UCC27533DBV			
1	VDD	I	Bias supply input
2	GND	-	Ground (All signals are referenced to this node)
3	IN+	I	Driver non-inverting input
4	IN-	I	Driver inverting input
5	OUT	O	2.5-A source and 5-A sink current output of driver
UCC27536DBV			
1	EN	I	Enable (pull EN to GND to disable output, pull it high or leave open to enable output)
2	GND	-	Ground (all signals are referenced to this node)
3	IN-	I	Driver inverting input
4	OUT	O	2.5-A source and 2.5-A sink current output of driver
5	VDD	I	Bias supply input
UCC27537DBV			
1	EN	I	Enable (Pull EN to GND to disable Output, Pull it high or leave open to enable Output)
2	GND	-	Ground (All signals are referenced to this node)
3	IN+	I	Driver non-inverting input
4	OUT	O	2.5-A source and 5-A sink current output of driver
5	VDD	I	Bias supply input

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
UCC27538DBV			
1	VDD	I	Bias supply input
2	IN1	I	Driver non-inverting input
3	GND	-	Ground (all signals are referenced to this node)
4	OUTL	O	5-A sink current output of driver
5	IN2	I	Driver non-inverting input
6	OUTH	O	2.5-A source current output of driver
UCC27531D			
1	NC	-	No connection
2	IN	I	Driver non-inverting input
3	GND	-	Ground (all signals are referenced to this node)
4	NC	-	No connection
5	NC	-	No connection
6	VDD	I	Bias supply input
7	OUT	O	5-A Sink Current Output of driver and 2.5-A Source Current Output of driver
8	NC	-	No connection

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	35	V
Continuous	OUTH, OUTL, OUT	–0.3	VDD +0.3	V
Pulse	OUTH, OUTL, OUT (200 ns)	–2	VDD +0.3	V
Continuous IN, EN, IN+, IN-, IN1, IN2		–5	27	V
Pulse IN, EN, IN+, IN–, IN1, IN2 (1.5 µs)		–6.5	27	V
Operating virtual junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See *Thermal Information* of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	10	18	32	V
Operating junction temperature	–40		140	°C
Input voltage, IN, IN+, IN-, IN1, IN2	–5		25	V
Enable, EN	–5		25	V

8.4 Thermal Information

THERMAL METRIC(1)		UCC27533, UCC27536, UCC27537	UCC27531, UCC27538	UCC27531	UNIT
		DBV	DBV	SOIC	
		5 PINS	6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	178.3	178.3	129.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	109.7	109.7	79.9	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	28.3	28.3	68.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	14.7	14.7	22.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	27.8	27.8	69.8	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

8.5 Electrical Characteristics

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = –40°C to 140°C, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together for UCC27531/8. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
I_{DDoff}	Start-up current (UCC25731)	VDD = 7.0, IN, EN=VDD	100	200	300	µA
		IN, EN = GND	100	217	300	
I_{DDoff}	Start-up current (UCC27533)	VDD = 7.0, IN+ = GND, IN- = VDD	100	200	300	µA
		IN+ = VDD, IN- = GND	100	217	300	
I_{DDoff}	Start-up current (UCC27536)	VDD = 7.0, IN- = GND, EN = VDD	100	217	300	µA
		IN- = VDD, EN = GND	100	217	300	
I_{DDoff}	Start-up current (UCC27537)	VDD =7.0, IN+, EN = VDD	100	200	300	µA
		IN+, EN = GND	100	217	300	
I_{DDoff}	Start-up Current (UCC27538)	VDD = 7.0, IN1, IN2=VDD	100	200	300	µA
		IN1, IN2=GND	100	200	300	
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{ON}	Supply start threshold		8	8.9	9.8	V
V_{OFF}	Minimum operating voltage after supply start		7.3	8.2	9.1	V
V_{DD_H}	Supply voltage hysteresis			0.7		V

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Electrical Characteristics (continued)

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = –40°C to 140°C, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together for UCC27531/8. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (IN, IN+, IN1, IN2)						
V_{IN_H}	Input signal high threshold, output high	Output High, IN- = LOW, EN=HIGH, IN2 or IN1 = HIGH (other is INPUT)	1.8	2	2.2	V
V_{IN_L}	Input signal low threshold, output low	Output Low, IN- = LOW, EN=HIGH, IN2 or IN1 = HIGH (other is INPUT)	0.8	1	1.2	V
V_{IN_HYS}	Input signal hysteresis			1		V
INPUT (IN-)						
V_{IN_H}	Input signal high threshold, output low	Output low, IN+ = HIGH, EN = High	1.7	1.9	2.1	V
V_{IN_L}	Input signal low threshold, output high	Output high,, IN+ = HIGH, EN = High	0.8	1	1.2	V
V_{IN_HYS}	Input signal hysteresis			0.9		V
ENABLE (EN)						
V_{EN_H}	Enable signal high threshold	Output High	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	Output Low	0.8	1	1.2	V
V_{EN_HYS}	Enable signal hysteresis			0.9		V
OUTPUTS (OUTH/OUTL)						
$I_{SRC/SNK}$	Source peak current (OUTH)/ sink peak current (OUTL)	C_{LOAD} = 0.22 µF, f = 1 kHz		–2.5/+5		A
V_{OH}	OUTH, high voltage	I_{OUTH} = -10 mA	VDD –0.2	VDD –0.12	VDD –0.07	V
V_{OL}	OUTL, low voltage	I_{OUTL} = 100 mA		0.065	0.125	V
V_{OL}	OUTL, Low Voltage UCC27536	I_{OUTL} = 100 mA		0.13	0.23	V
R_{OH}	OUTH, pull-up resistance	T_A = 25°C, I_{OUT} = –10 mA	11	12	12.5	Ω
		T_A = –40°C to 140°C, I_{OUT} = –10 mA	7	12	20	
R_{OL}	OUTL, pull-down resistance	T_A = 25°C, I_{OUT} = 100 mA	0.45	0.65	0.85	Ω
		T_A = –40°C to 140°C, I_{OUT} = 100 mA	0.3	0.65	1.25	
R_{OL}	OUTL, pull-down resistance UCC27536	T_A = 25°C, I_{OUT} = 100 mA	0.9	1.3	1.7	Ω
		T_A = –40°C to 140°C, I_{OUT} = 100 mA	0.6	1.3	2.3	

8.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	C_{LOAD} = 1.8 nF, See Figure 1, Figure 2, Figure 3		15		ns
t_F	Fall time	C_{LOAD} = 1.8 nF, See Figure 1, Figure 2, Figure 3		7		ns
		C_{LOAD} (UCC27536DBV) = 1.8 nF, See Figure 1, Figure 2, Figure 3		10		
t_{D1}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, IN, IN+ = 0 V to 5 V, See Figure 1, Figure 2, Figure 3		17	26	ns
t_{D2}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, IN, IN+ = 5 V to 0 V, See Figure 1, Figure 2, Figure 3		17	26	ns
t_{D3}	Inverting turn-off propagation delay	C_{LOAD} = 1.8 nF, IN- = 0 V to 5 V		17	28	ns
t_{D4}	Inverting turn-on propagation delay	C_{LOAD} = 1.8 nF, IN- = 5 V to 0 V		20	28	ns

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8.7 Timing Diagrams

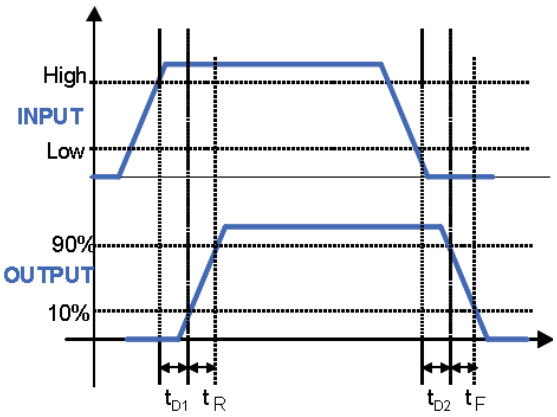

Figure 1. UCC27531: (Output = OUTH Tied to OUTL) Input = IN, (EN = VDD), or Input = EN, (IN = VDD)
UCC27537: (Output = OUT) Input = IN+, (EN = VDD), or Input = EN, (IN+ = VDD)
UCC27538: (Output = OUTH Tied to OUTL) Input = IN1, (IN2 = VDD), or Input = IN2, (IN1 = VDD)

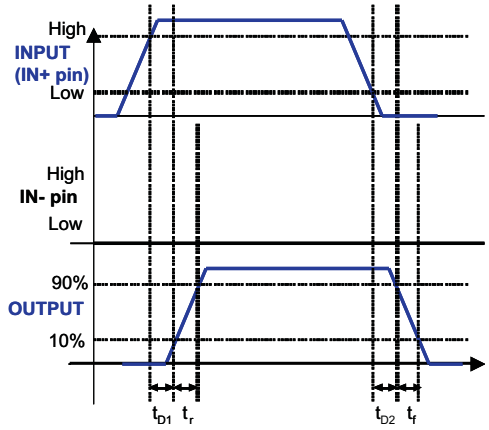

Figure 2. UCC27533: (Output = OUT) Input = IN+
UCC27536: (Output = OUT) Input = EN

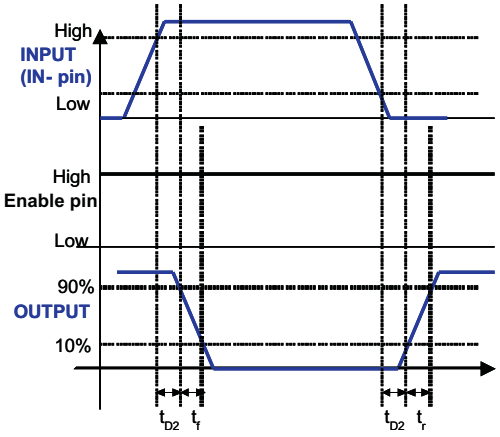

Figure 3. UCC27533: (Output = OUT) Enable = IN+
UCC27536: (Output = OUT) Enable = EN

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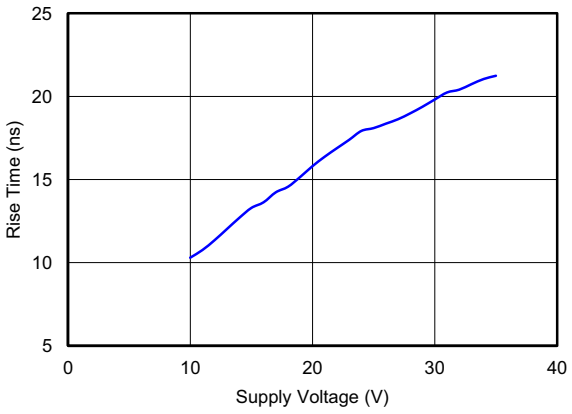
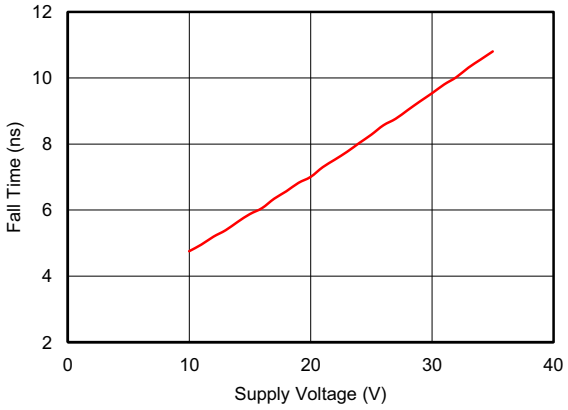
8.8 Typical Characteristics

If not specified, INPUT refers to non-inverting input



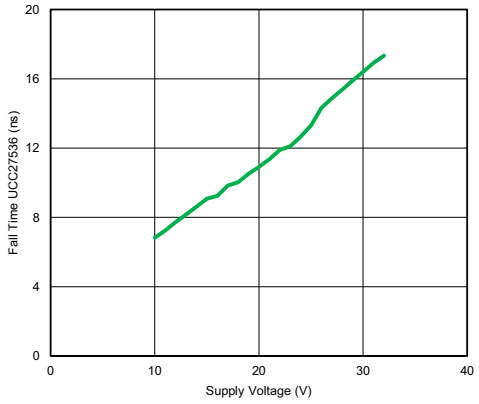
C_{LOAD} = 1.8 nF

Figure 4. Rise Time vs. Supply Voltage



C_{LOAD} = 1.8 nF

Figure 5. Fall Time vs. Supply Voltage



C_{LOAD} = 1.8 nF

Figure 6. UCC27536 Fall Time vs. Supply Voltage

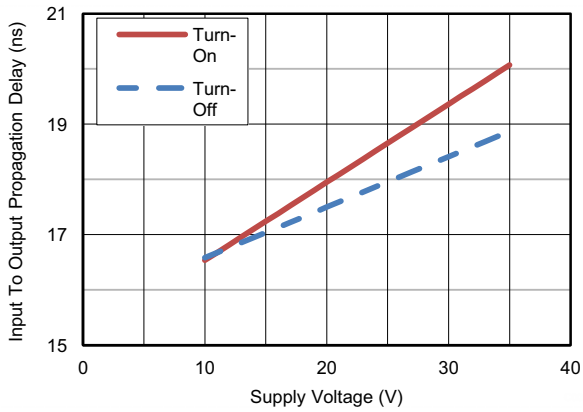


Figure 7. Propagation Delay vs. Supply Voltage

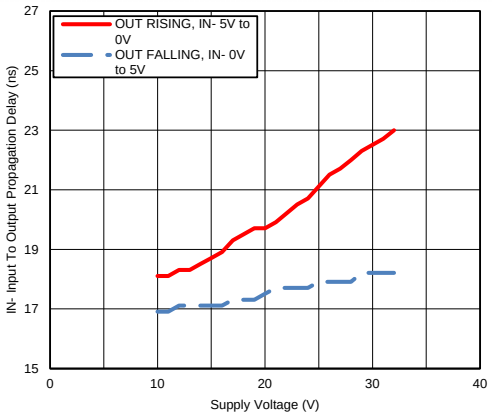
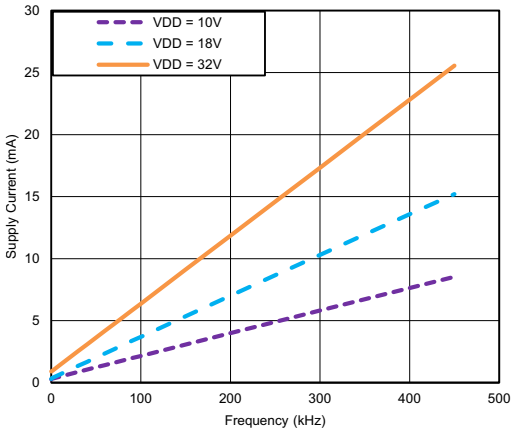


Figure 8. IN- Propagation Delay vs. Supply



C_{LOAD} = 1.8 nF

Figure 9. Operating Supply Current vs. Frequency

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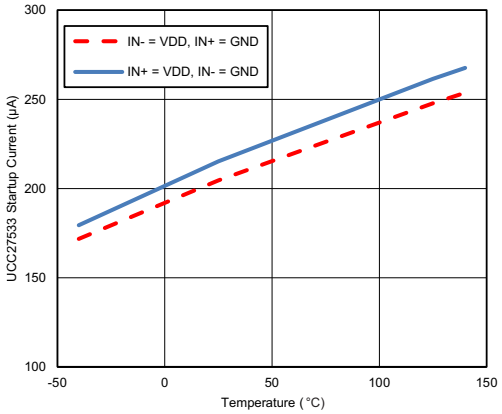
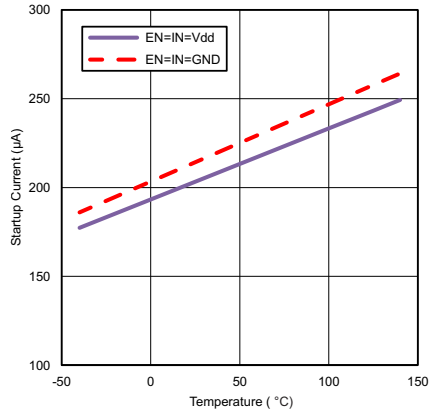
Typical Characteristics (continued)

If not specified, INPUT refers to non-inverting input



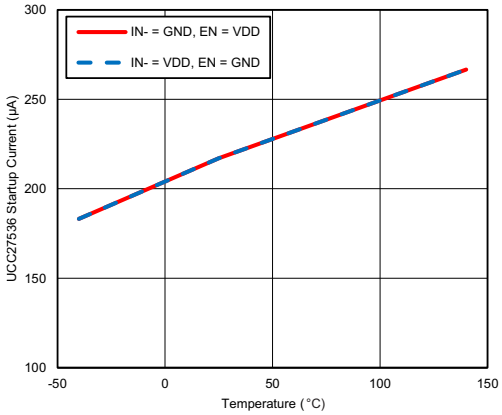
V_{DD} = 7 V

Figure 10. UCC27533 Start-Up Current vs. Temperature



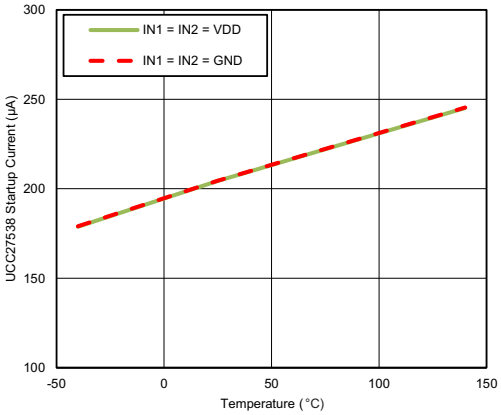
V_{DD} = 7 V

Figure 11. UCC27531 Start-Up Current vs. Temperature



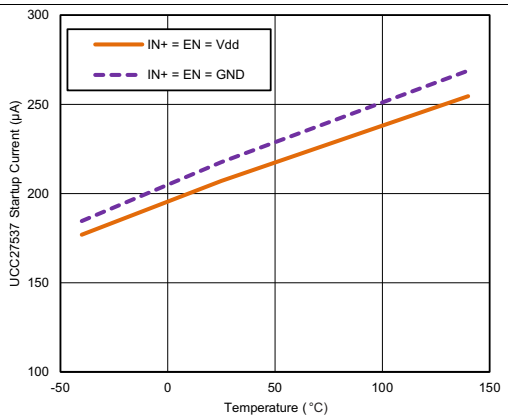
V_{DD} = 7 V

Figure 12. UCC27536 Start-Up Current vs. Temperature



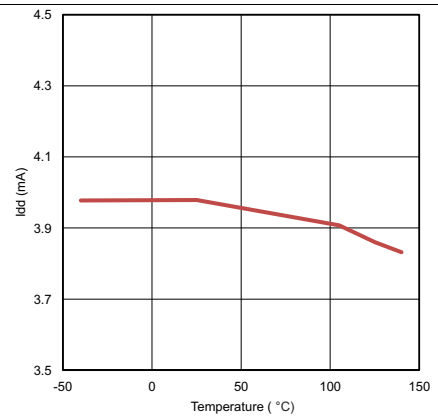
V_{DD} = 7 V

Figure 13. UCC27538 Start-Up Current vs. Temperature



V_{DD} = 7 V

Figure 14. UCC27537 Start-Up Current vs. Temperature



C_{LOAD} = 1.8 nF V_{DD} = 7 V f_{SW} = 100 kHz

Figure 15. Operating Supply Current vs. Temperature (Output Switching)

Typical Characteristics (continued)

If not specified, INPUT refers to non-inverting input

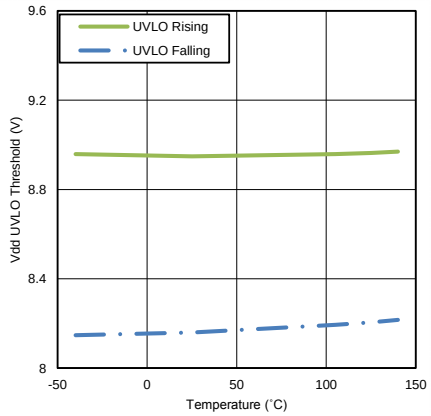


Figure 16. UVLO Threshold Voltage vs. Temperature

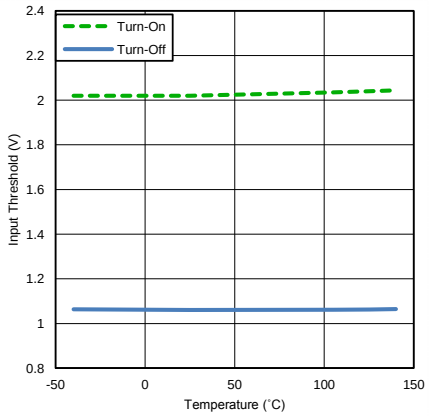


Figure 17. Input Threshold vs. Temperature

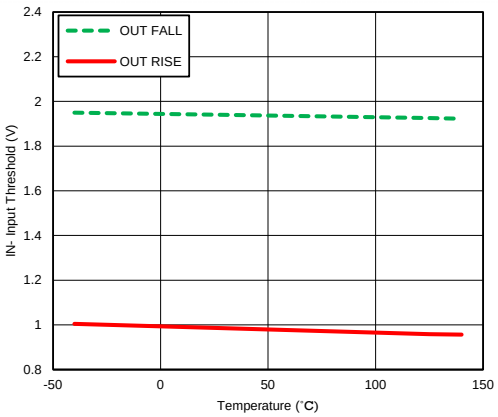


Figure 18. In- Input Threshold vs. Temperature

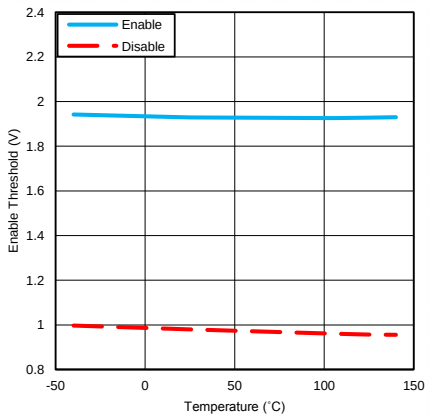
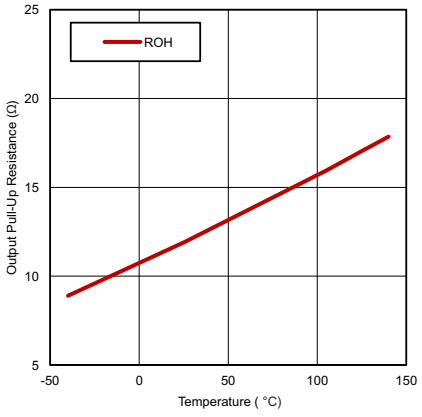
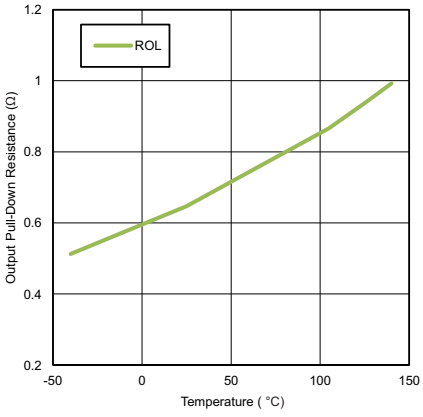


Figure 19. Enable Threshold vs. Temperature



V_{DD} = 18 V

Figure 20. Output Pullup Resistance vs. Temperature



V_{DD} = 18 V

Figure 21. Output Pulldown Resistance vs. Temperature

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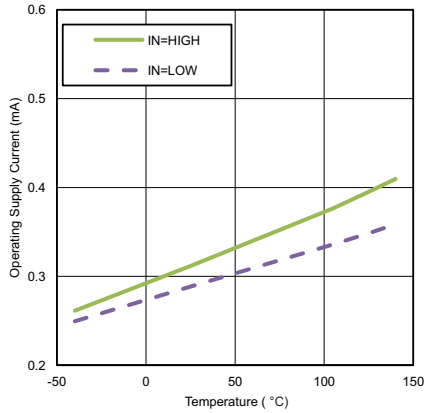
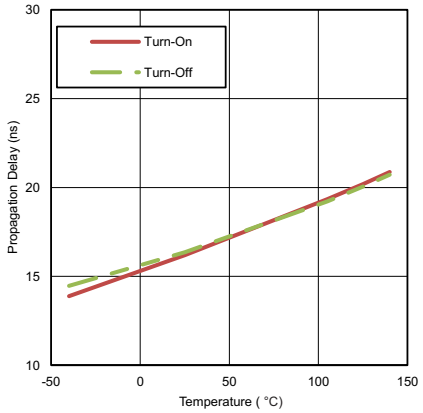
Typical Characteristics (continued)

If not specified, INPUT refers to non-inverting input



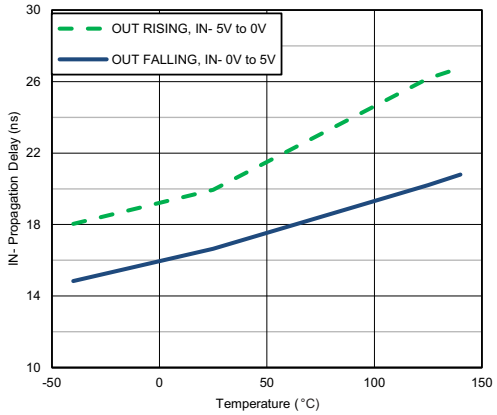
V_{DD} = 18 V

Figure 22. Operating Supply Current vs. Temperature (Output In DC On/Off Condition)



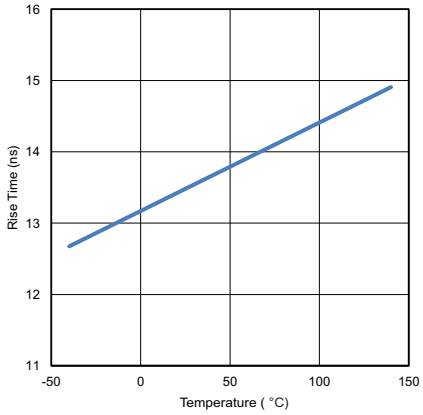
V_{DD} = 18 V

Figure 23. Input-To-Output Propagation Delay vs. Temperature



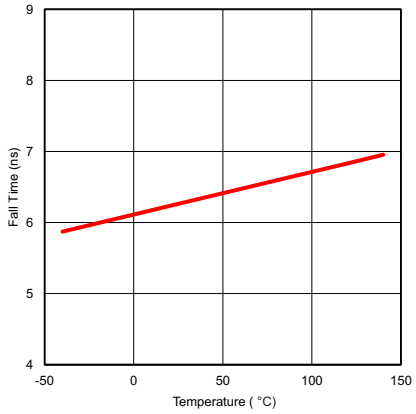
V_{DD} = 18 V

Figure 24. IN– Input-To-Output Propagation Delay vs. Temperature



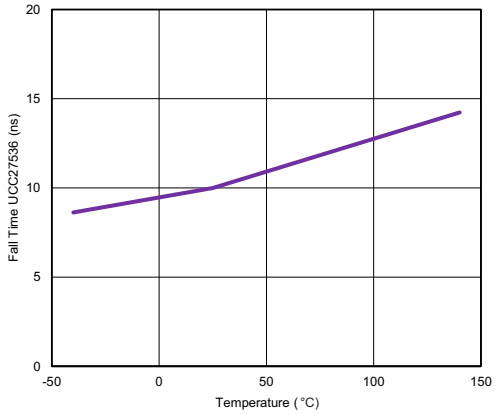
C_{LOAD} = 1.8 nF V_{DD} = 18 V

Figure 25. Rise Time vs. Temperature



C_{LOAD} = 1.8 nF V_{DD} = 18 V

Figure 26. Fall Time vs. Temperature



C_{LOAD} = 1.8 nF V_{DD} = 18 V

Figure 27. UCC27536 Fall Time vs. Temperature

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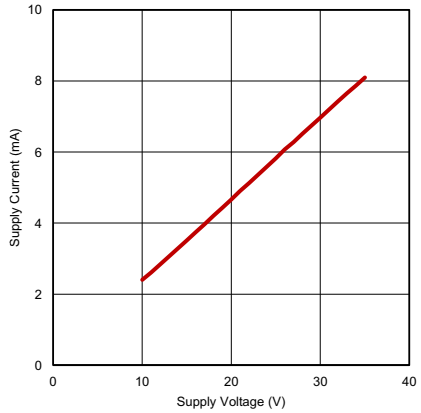
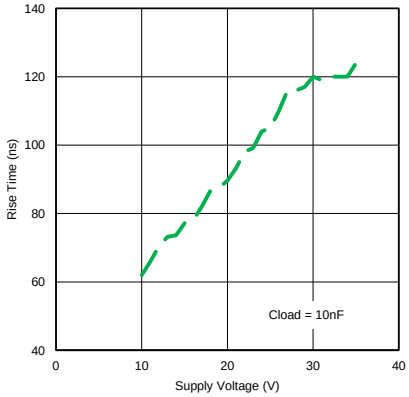
Typical Characteristics (continued)

If not specified, INPUT refers to non-inverting input



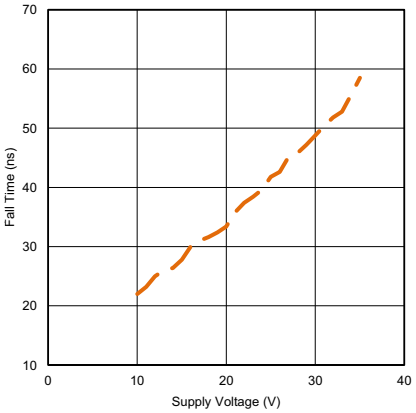
C_{LOAD} = 1.8 nF V_{DD} = 18 V

Figure 28. Operating Supply Current vs. Supply Voltage (Output Switching)



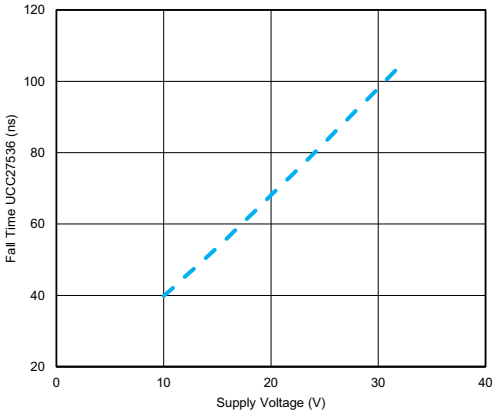
C_{LOAD} = 1.8 nF

Figure 29. Rise Time vs. Supply Voltage



C_{LOAD} = 1.8 nF

Figure 30. Fall Time vs. Supply Voltage



C_{LOAD} = 1.8 nF

Figure 31. UCC27536 Fall Time vs. Supply Voltage

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9 Detailed Description

9.1 Overview

The UCC2753x family of devices are single-channel, high-speed, gate drivers capable of effectively driving MOSFET and IGBT power switches by up to 2.5-A source and 5-A sink (asymmetrical drive) peak current. Strong sink capability in asymmetrical drive boosts immunity against parasitic Miller turn-on effect. The UCC2753x device can also feature a split-output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This pin arrangement allows the user to apply independent turn-on and turn-off resistors to the OUTH and OUTL pins, respectively, and easily control the switching slew rates.

The driver has rail-to-rail drive capability and extremely small propagation delay, typically 17 ns.

The input threshold of UCC2753x is based on TTL and CMOS compatible low-voltage logic, which is fixed and independent of VDD supply voltage. The 1-V typical hysteresis offers excellent noise immunity.

The driver has an EN pin with fixed TTL compatible threshold. EN is internally pulled up; pulling EN low disables the driver, while leaving EN open provides normal operation. The EN pin can be used as an additional input with the same performance as the IN, IN+, IN1, and IN2 pins.

Table 1. UCC2753x Features and Benefits

FEATURE	BENEFIT
High source and sink current capability, 2.5 A and 5 A (asymmetrical).	High current capability offers flexibility in employing UCC2753x device to drive a variety of power switching devices at varying speeds.
Low 17 ns (typ) propagation delay.	Extremely low pulse transmission distortion.
Wide VDD operating range of 10 V to 32 V.	Flexibility in system design.
	Can be used in split-rail systems such as driving IGBTs with both positive and negative(relative to Emitter) supplies.
	Optimal for many SiC FETs.
VDD UVLO protection.	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power up and power down.
	High UVLO of 8.9 V typical ensures that power switch is not on in high-impedance state which could result in high power dissipation or even failures.
Outputs held low when input pin (INx) in floating condition.	Safety feature, especially useful in passing abnormal condition tests during safety certification
Split output structure option (OUTH, OUTL).	Allows independent optimization of turn-on and turn-off speeds using series gate resistors.
Strong sink current (5 A) and low pull-down impedance (0.65 Ω).	High immunity to high dV/dt Miller turn-on events.
CMOS and TTL compatible input threshold logic with wide hysteresis.	Enhanced noise immunity, while retaining compatibility with microcontroller logic level input signals (3.3 V, 5 V) optimized for digital power.
Input capable of withstanding –6.5 V.	Enhanced signal reliability in noisy environments that experience ground bounce on the gate driver.

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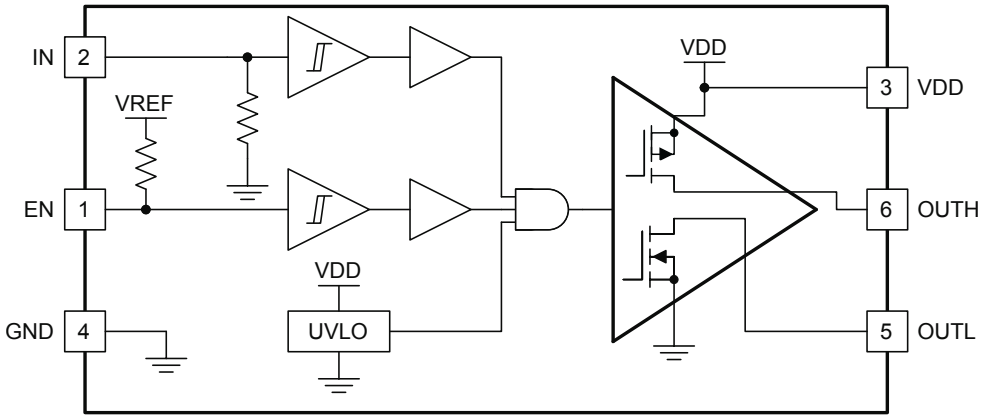
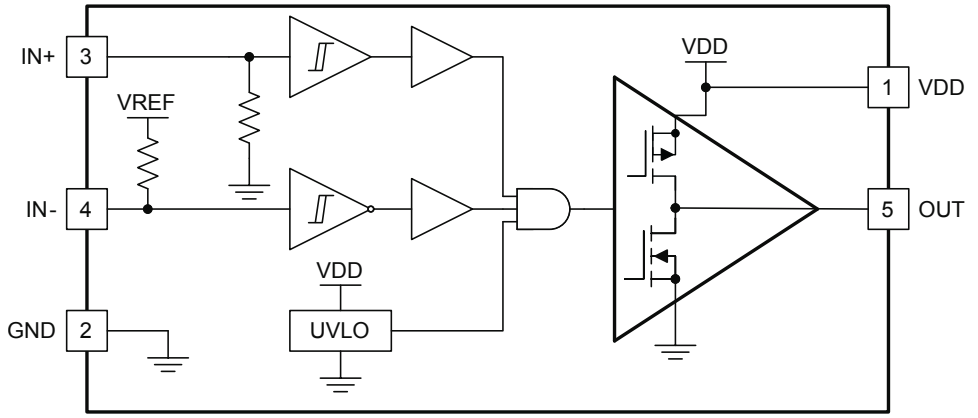
9.2 Functional Block Diagrams



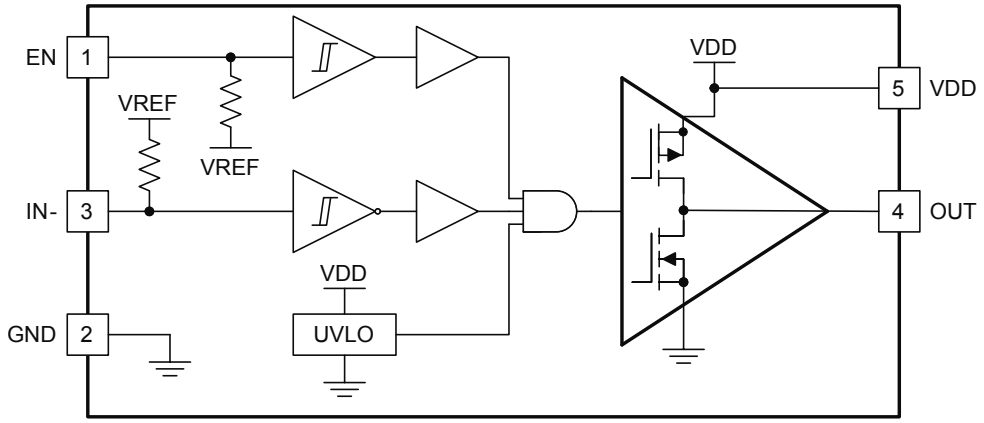
EN Pull-Up Resistance to VREF = 500 kΩ, VREF = 5.8 V, IN Pull-Down Resistance to GND = 230 kΩ

Figure 32. UCC27531



IN– Pull-Up Resistance to VREF = 500 kΩ, VREF = 5.8 V, IN+ Pull-Down Resistance to GND = 230 kΩ

Figure 33. UCC27533



EN Pull-Up Resistance to VREF = 500 kΩ, VREF = 5.8 V, IN- Pull-Up Resistance to VREF = 500 kΩ

Figure 34. UCC27536

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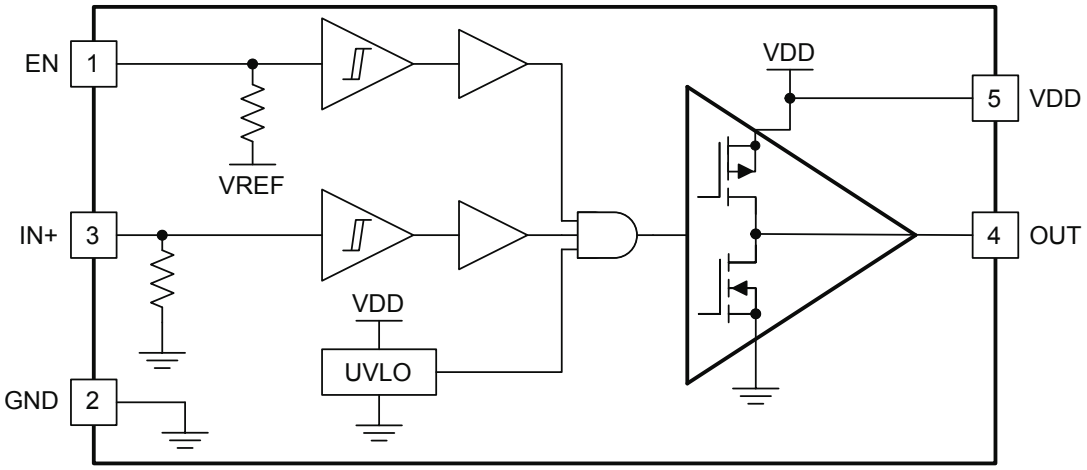
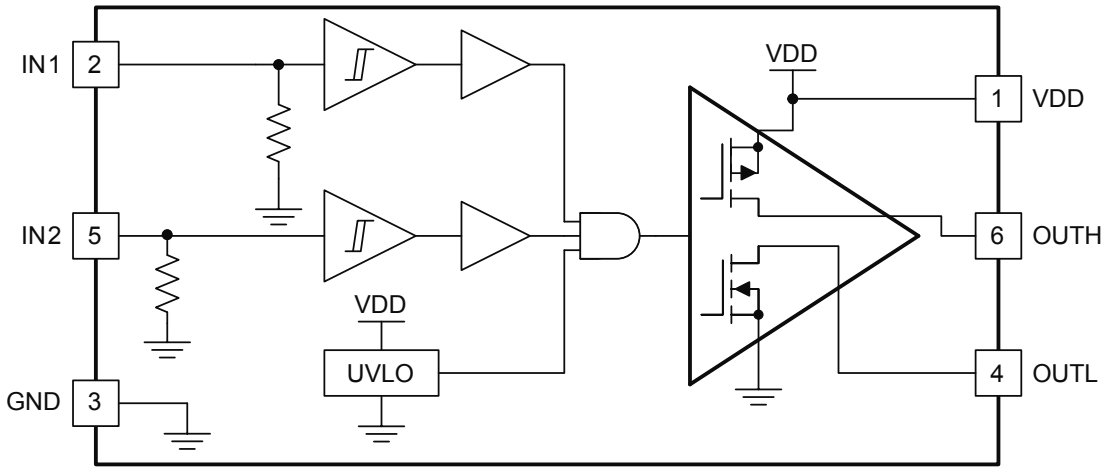
Functional Block Diagrams (continued)



EN Pull-Up Resistance to VREF = 500 kΩ, VREF = 5.8 V, IN+ Pull-Down Resistance to GND = 230 kΩ

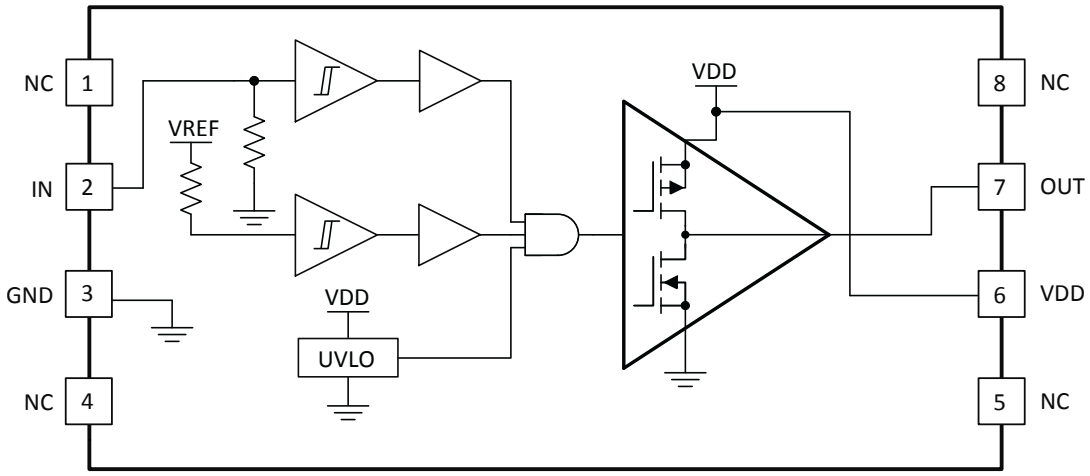
Figure 35. UCC27537



IN1 Pull-Down Resistance to GND = 230 kΩ, IN2 Pull-Down Resistance to GND = 230 kΩ

Figure 36. UCC27538

Functional Block Diagrams (continued)



IN Pull-Down Resistance to GND = 230 kΩ, VREF = 5.8 V, Pull-Up Resistance to VREF = 500 kΩ

Figure 37. UCC27531D

9.3 Feature Description

9.3.1 VDD Undervoltage Lockout

The UCC2753x device has internal UVLO protection feature on the VDD pin supply circuit blocks. To ensure acceptable power dissipation in the power switch, this UVLO prevents the operation of the gate driver at low supply voltages. Whenever the driver is in UVLO condition (when VDD voltage less than V_{ON} during power up and when VDD voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 8.9 V with 700-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at voltage levels such as 10 V to 32 V provides flexibility to drive Si MOSFETs, IGBTs, and emerging SiC FETs.

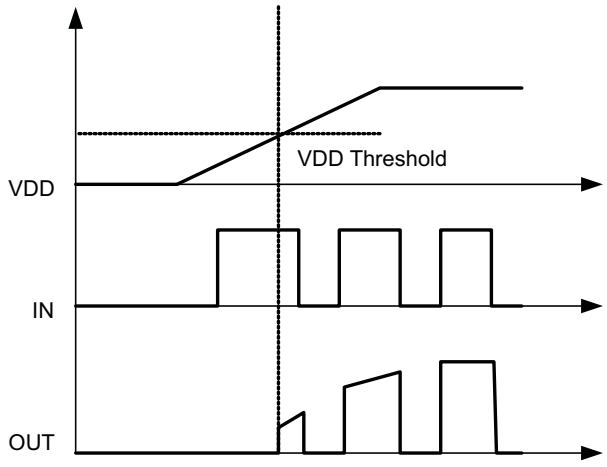


Figure 38. Power Up

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Feature Description (continued)

9.3.2 Input Stage

The input pins of UCC2753x device are based on a TTL and CMOS compatible input threshold logic that is independent of the VDD supply voltage. With typical high threshold = 2 V and typical low threshold = 1 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V logic. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance, typically 20 pF, on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using pull-up or pull-down resistors on the input pins as shown in the block diagrams.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Because the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and GND and trigger an unintended change of output state. Because of fast 17 ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage
- 1-V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

If limiting the rise or fall times to the power device to reduce EMI is necessary, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Finally, because of the unique input structure that allows negative voltage capability on the Input and Enable pins, caution must be used in the following applications:

- Input or Enable pins are switching to amplitude > 15 V
- Input or Enable pins are switched at dV/dt > 2 V/ns

If both of these conditions occur, it is advised to add a series 150-Ω resistor for the pin(s) being switched to limit the current through the input structure.

9.3.3 Enable Function

The Enable (EN) pin of the UCC2753x has an internal pull-up resistor to an internal reference voltage so leaving Enable floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver.

9.3.4 Output Stage

The output stage of the UCC2753x device is illustrated in Figure 39. The UCC2753x device features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pull-up structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turnon.

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Feature Description (continued)

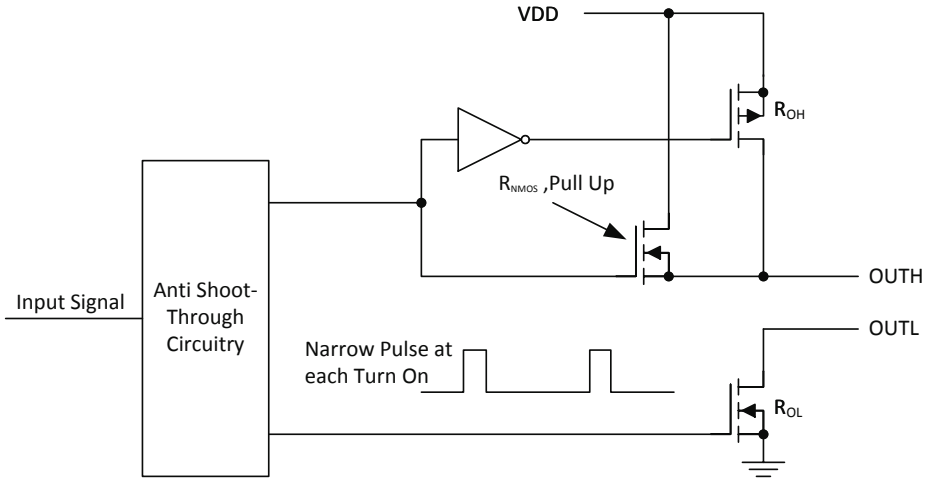

Figure 39. UCC27531 Gate Driver Output Stage

Split output depicted in Figure 39. For devices with single OUT pin, OUTH and OUTL are connected internally and then connected to OUT.

The R_{OH} parameter (see Electrical Table) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, because the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pull-up stage is much lower than what is represented by R_{OH} parameter. The pull-down structure is composed of a N-channel MOSFET only. The R_{OL} parameter (see *Electrical Characteristics*), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device. In UCC2753x, the effective resistance of the hybrid pull-up structure is approximately 3 x R_{OL}.

The UCC2753x can deliver 2.5-A source, and up to 5-A sink at VDD = 18 V. Strong sink capability results in a very low pull-down impedance in the driver output stage which boosts immunity against the parasitic Miller turn-on (high slew rate dV/dt turnon) effect that is seen in both IGBT and FET power switches .

An example of a situation where Miller turnon is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in OFF state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pull-down stage of the driver. If the pull-down impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turnon. This phenomenon is illustrated in Figure 40.

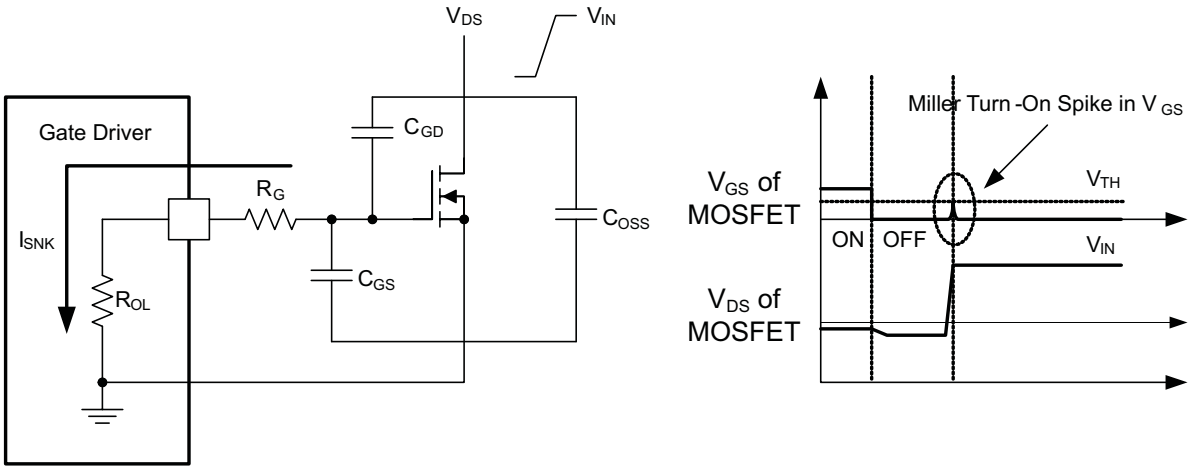

Figure 40. Low Pull-Down Impedance in UCC2753x (Output Stage Mitigates Miller Turn-On Effect)

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Feature Description (continued)

The driver output voltage swings between VDD and GND providing rail-to-rail operation because of the low dropout of the output stage. In many cases, the external Schottky diode clamps may be eliminated because the presence of the MOSFET body diodes offers low impedance to switching overshoots and undershoots.

9.4 Device Functional Modes

The UCC2753x devices operate in normal mode and UVLO mode (see *VDD Undervoltage Lockout* section for information on UVLO operation). In normal mode, the output state is dependent on the states of the device, and the input pins.

The UCC27531 features a single, non-inverting input, but also contains enable and disable functionality through the EN pin. Setting the EN pin to logic HIGH will enable the non-inverting input to output on the IN pin. The device uses a split output (OUTH, and OUTL) to allow for separate sourcing and sinking pins, which can help reduce ground de-bouncing.

The UCC27533 features a dual input. One inverting (IN+), and one non-inverting (IN–). This device does not contain an enable feature, and has a single output.

The UCC27536 is similar to the UCC27531, but uses an inverting input, and a single output.

The UCC27537 is also similar to the UCC27531, but uses a single output.

The UCC27538 is again similar to the UCC27531, but features dual inputs IN1 and IN2, rather than an enable and disable feature.

The UCC27531D features a single input and a single output. The device is always enabled.

See Table 2, Table 4, and Table 5 for lists of the output states of the different devices and their inputs:

Table 2. Input/Output Logic Truth Table (For Single Output Driver)

IN PIN	EN PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
UCC27531DBV				
L	L	High-Impedance	L	L
L	H	High-Impedance	L	L
H	L	High-Impedance	L	L
H	H	H	High-Impedance	H
H	FLOAT	H	High-Impedance	H
FLOAT	H	High-Impedance	L	L

Table 3. Input/Output Logic Truth Table (For Single Output Driver with Enable Pin)

EN PIN	IN- / IN+ PIN	OUT PIN
UCC27536DBV		
L	L	L
L	H	L
H	L	H
H	H	L
H	X	L
UCC27537DBV		
L	L	L
L	H	L
H	L	L
H	H	H
H	X	L

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Table 4. Input/Output Logic Truth Table

IN+ PIN	IN- PIN	OUT PIN
UCC27533DBV		
L	L	L
L	H	L
H	L	H
H	H	L
FLOAT	X	L
X	FLOAT	L

Table 5. Input/Output Logic Truth Table (For Single Output Driver)

IN1 PIN	IN2 PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
UCC27538DBV				
L	L	High-Impedance	L	L
L	H	High-Impedance	L	L
H	L	High-Impedance	L	L
H	H	H	High-Impedance	H
X	FLOAT	High-Impedance	L	L
FLOAT	X	High-Impedance	L	L

Table 6. Input/Output Logic Truth Table (For Single Input/Output Driver)

IN PIN	OUT PIN
UCC27531D	
L	L
H	H
FLOAT	L

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10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P- N-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC2753x is very flexible in this role with a strong current drive capability and wide supply voltage range up to 32 V. This allows the driver to be used in 12-V Si MOSFET applications, 20-V and -5-V (relative to Source) SiC FET applications, 15-V and -15-V (relative to Emitter) IGBT applications and many others. As a single-channel driver, the UCC2753x can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node however, signal isolation is needed from the controller as well as an isolated bias to the UCC2753x. Alternatively, in a high-side drive configuration the UCC2753x can be tied directly to the controller signal and biased with a nonisolated supply. However, in this configuration the outputs of the UCC2753x must drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch. Further, having the ability to control turn-on and turn-off speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for low propagation delays and availability in compact, low-inductance packages with good thermal capability makes gate driver devices such as the UCC2753x extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

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10.2 Typical Application

10.2.1 Driving IGBT Without Negative Bias

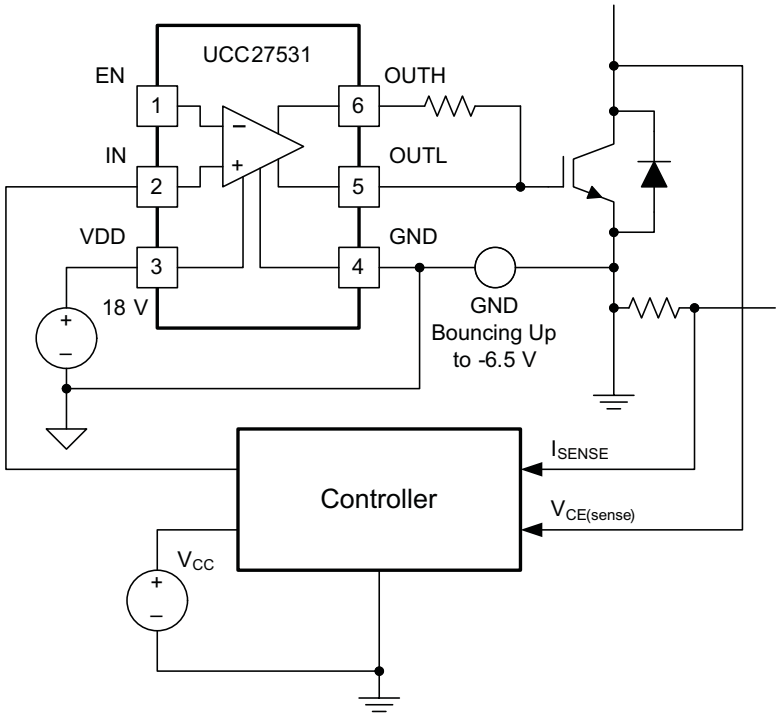

Figure 41. Driving IGBT Without Negative Bias

10.2.1.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first in order to make the most appropriate selection. The following design parameters should be used when selecting the proper gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in Table 7.

Table 7. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
IN-OUT configuration	Noninverting
Input threshold type	CMOS
Bias supply voltage levels	+18 V
Negative output low voltage	N/A
dVDS/dt(1)	20 V/ns
Enable function	Yes
Disable function	N/A
Propagation delay	<30 ns
Power dissipation	<0.25 W
Package type	DBV

(1) dVDS/dt is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in *Peak Source and Sink Currents*.

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10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Input-to-Output Configuration

The design should specify which type of input-to-output configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the non-inverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the inverting configuration must be chosen.

If ground-debouncing is a potential issue, a split output device should be chosen (UCC27531, or UCC27538). On these devices, OUTH sources current to charge the MOSFET or IGBT gate when transitioning from an output LOW to HIGH, and OUTL sinks current to discharge the MOSFET or IGBT gate when transitioning from an output HIGH to LOW.

If dual inputs are required, the chosen device should be either the UCC27533, or the UCC27538.

Based on these requirements, the proper device out of the UCC27531, UCC27533, UCC27536, UCC27537, or UCC27538 should be selected. See the *Device Functional Modes* section for information on individual device functionality and the *Device Comparison Table* table.

10.2.1.2.2 Input Threshold Type

The type of Input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC2753x devices feature a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the *Electrical Characteristics* table for the actual input threshold voltage levels and hysteresis specifications for the UCC2753x devices.

10.2.1.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the *Recommended Operating Conditions* table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With an operating range from 10 V to 32 V, the UCC2753x devices can be used to drive a power switches such as power MOSFETS and IGBTs (VGE = 15 V, 18 V).

10.2.1.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dVDS/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned on with a dVDS/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turn-on event (from 400 V in the OFF state to VDS(on) in on state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, VGS(TH).

To achieve the targeted dVDS/dt, the gate driver must be capable of providing the QGD charge in 20 ns or less. In other words a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC2753x series of gate drivers can provide 2.5-A peak sourcing current, and 5A peak sinking current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 1.5x sourcing, and 3x sinking overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace

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inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ ×IPEAK × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the IPEAK value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

10.2.1.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. A pin which offers an enable and disable function achieves this requirement. For these applications, the UCC27531, UCC27536, or UCC27537 are suitable as they feature an input pin (IN– for UCC27536) and an Enable pin.

Other applications require multiple inputs. Under those requirements, the UCC27533 or UCC27538 are suitable. The UCC27533 features an IN+ and IN– pin, both of which control the state of the output as listed in Table 3. Based on whether an inverting or non-inverting input signal is provided to the driver, the appropriate input pin can be selected as the primary input for controlling the gate driver. The other unused input pin can be conveniently used for the enable and disable functionality if needed. If the design does not require an enable function, the unused input pin can be tied to either the VDD pin (in case IN+ is the unused pin), or GND (in case IN– is unused pin) in order to ensure it does not affect the output status. The UCC27538 features two independent inputs IN1 and IN2. These contain the same functionality as the UCC27533, but instead both of these IN1 and IN2 pins are non-inverting.

10.2.1.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27516 and UCC27517 devices feature 17-ns (typical) (20-ns for inverting turn-on) propagation delays which ensures very little pulse distortion and allows operation at very higher frequencies. See *Switching Characteristics* for the propagation and switching characteristics of the UCC2753x devices.

10.2.1.2.7 Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC2753x features very low quiescent currents (less than 1 mA) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

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$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver. (2)

There is an equal amount of energy dissipated when the capacitor is discharged. During turnoff the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw}$$

where

- f_{SW} is the switching frequency (3)

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD} V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pull-up structure) = 3 x R_{OL} (5)

10.2.1.3 Application Curve

The following application curves were observed using the UCC27531 on the UCC27531EVM-184.

NOTE

Legend: Green: EVM PWM Input, Blue: UCC27531 IN, Red: EVM GATE Output

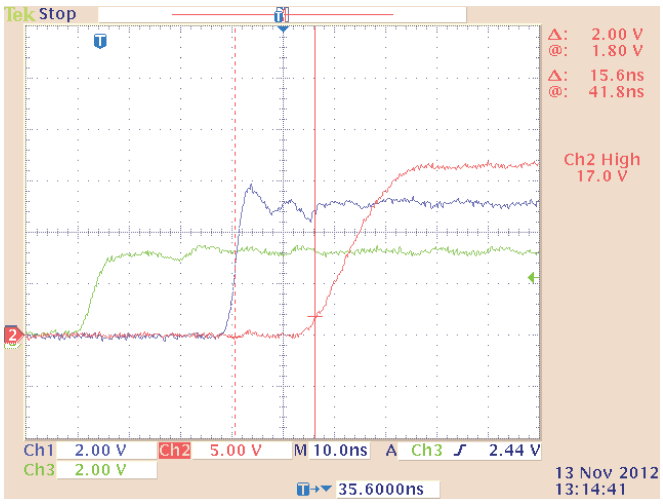

Figure 42. UCC27531DBV Input vs. Output PWM Propagation Delay (High)

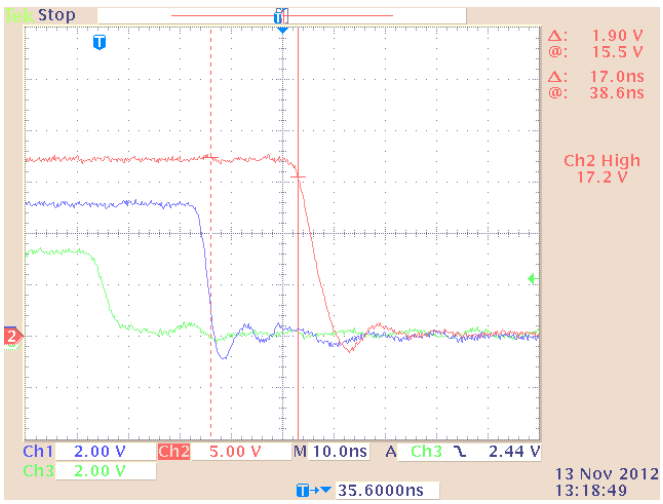

Figure 43. UCC27531DBV Input vs. Output PWM Propagation Delay (Low)

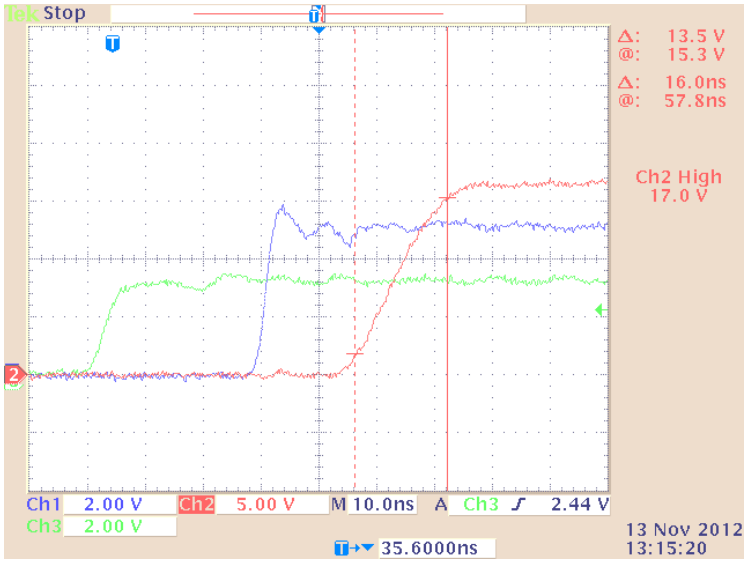

Figure 44. UCC27531DBV Input vs. Output PWM Rise Time

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10.2.2 Driving IGBT With 13-V Negative Turn-Off BIAS

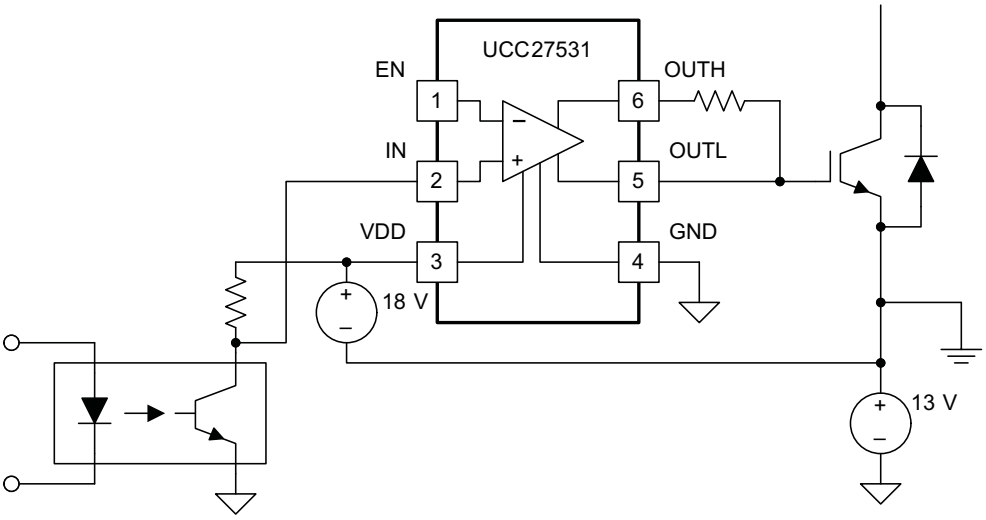

Figure 45. Driving IGBT With 13-V Negative Turn-Off BIAS

10.2.2.1 Design Requirements

Refer to the previous *Design Requirements* section.

10.2.2.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

10.2.2.3 Application Curve

Refer to the previous *Application Curve* section.

10.2.3 Single-Output Driver

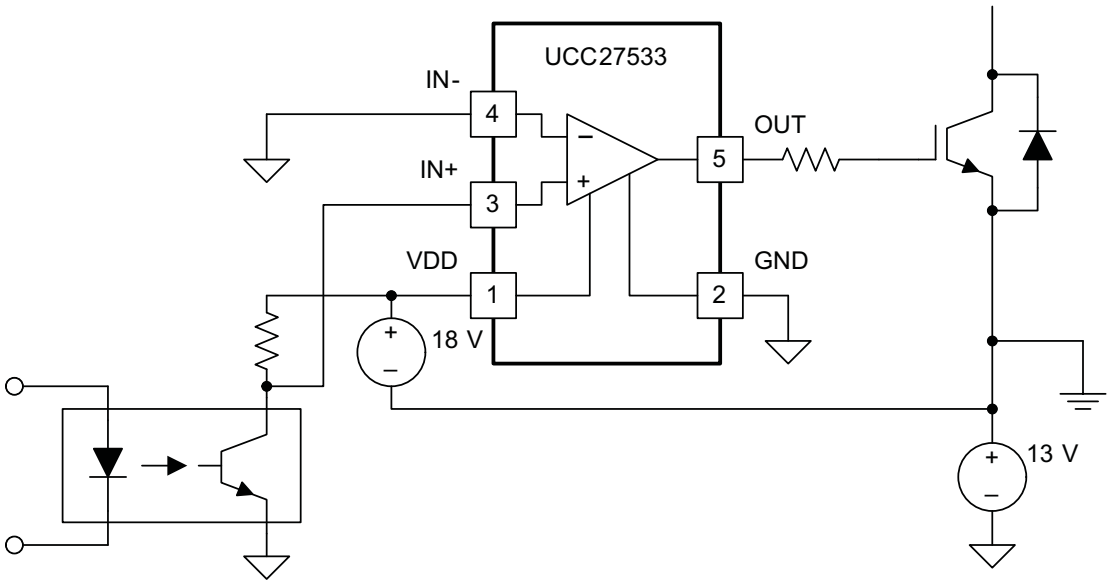

Figure 46. Single-Output Driver

10.2.3.1 Design Requirements

Refer to the previous *Design Requirements* section.

10.2.3.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

10.2.3.3 Application Curve

Refer to the previous *Application Curve* section.

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10.2.4 Using UCC2753x Drivers in an Inverter

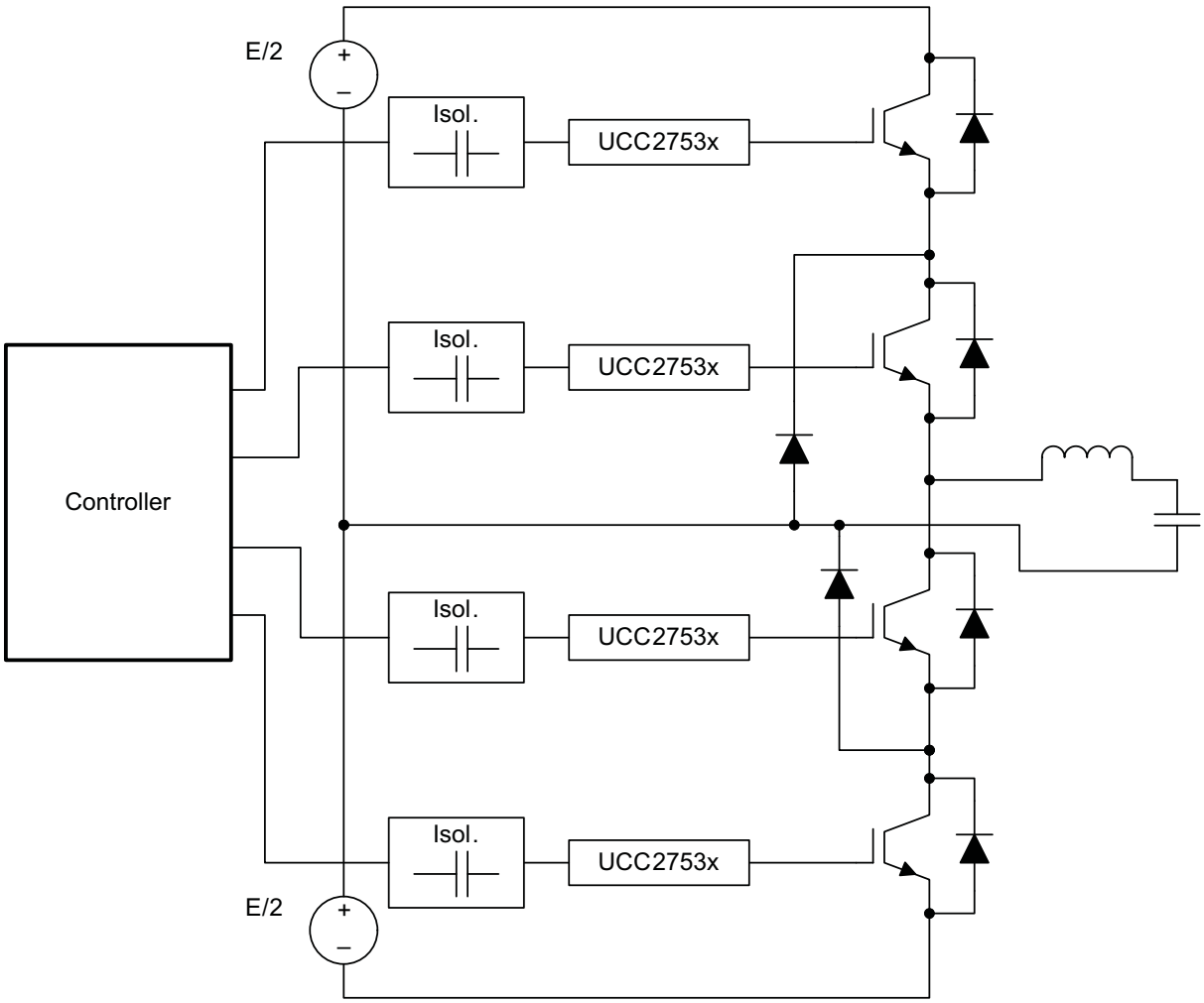

Figure 47. Using UCC2753x Drivers in an Inverter

10.2.4.1 Design Requirements

Refer to the previous *Design Requirements* section.

10.2.4.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

10.2.4.3 Application Curve

Refer to the previous *Application Curve* section.

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11 Power Supply Recommendations

The bias supply voltage range for which the UCC2753x devices are rated to operate is from 10 V to 32 V. The lower end of this range is governed by the internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 35-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 32 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD(hys). Therefore, ensuring that, while operating at or near the 9.8 V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the V(OFF) threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up, the device does not begin operation until the VDD pin voltage has exceeded above the V(ON) threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUT pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is mandatory.

12 Layout

12.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC2753x gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (2.5-A and 5-A peak current is at VDD = 18 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device to minimize the length of high-current traces between the driver output pins and the gate of the power switch device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turn-on of power switch. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turn-on and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller, and so forth, at a single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

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12.2 Layout Example

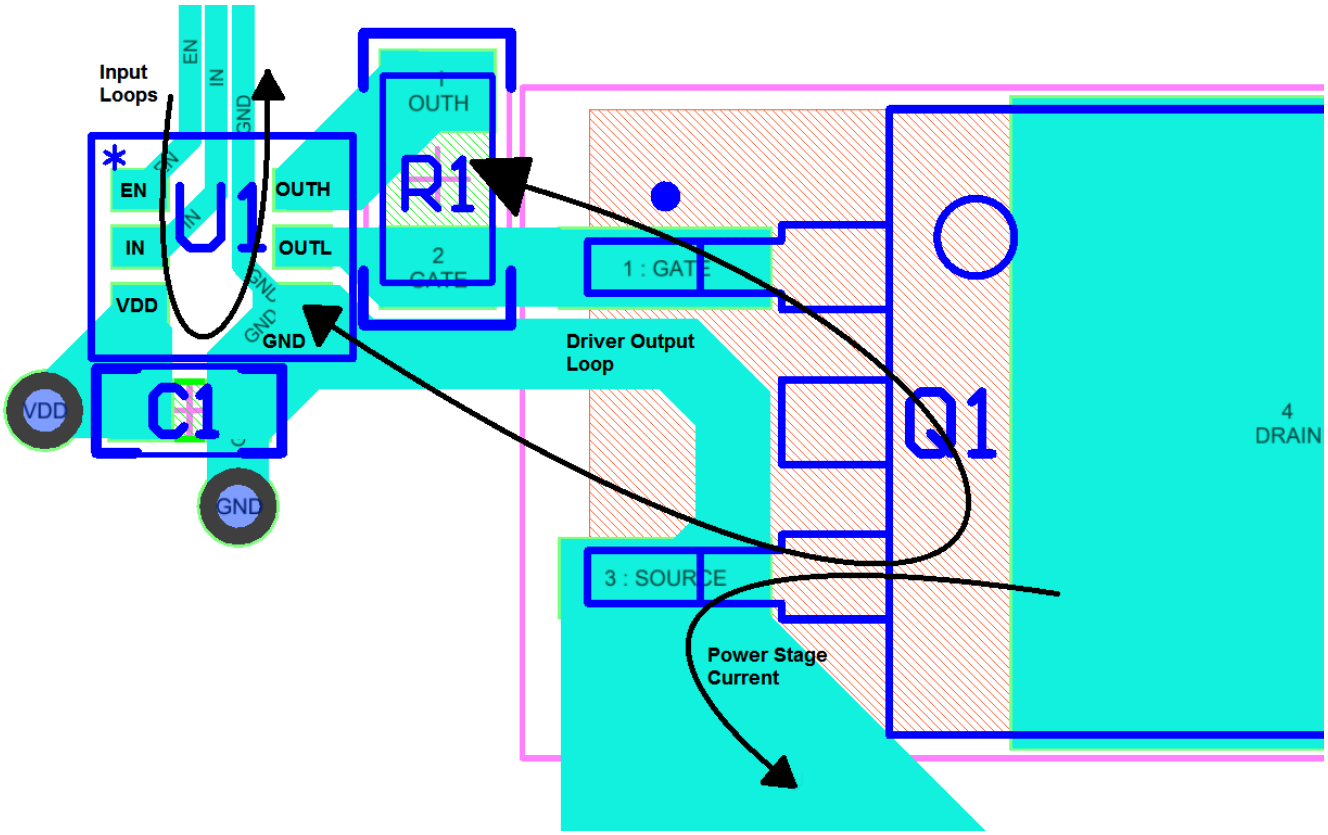

Figure 48. Layout Example: UCC27531DBV

12.3 Thermal Consideration

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the *Thermal Information* section of the datasheet. For detailed information regarding the thermal information table, refer to Application Note from Texas Instruments entitled *IC Package Thermal Metrics* (SPRA953).

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13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27531	Click here	Click here	Click here	Click here	Click here
UCC27533	Click here	Click here	Click here	Click here	Click here
UCC27536	Click here	Click here	Click here	Click here	Click here
UCC27537	Click here	Click here	Click here	Click here	Click here
UCC27538	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27531D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27531D	Samples
UCC27531DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7531	Samples
UCC27531DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7531	Samples
UCC27531DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27531D	Samples
UCC27533DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7533	Samples
UCC27533DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7533	Samples
UCC27536DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7536	Samples
UCC27536DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7536	Samples
UCC27537DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7537	Samples
UCC27537DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7537	Samples
UCC27538DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7538	Samples
UCC27538DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7538	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UCC27531 :

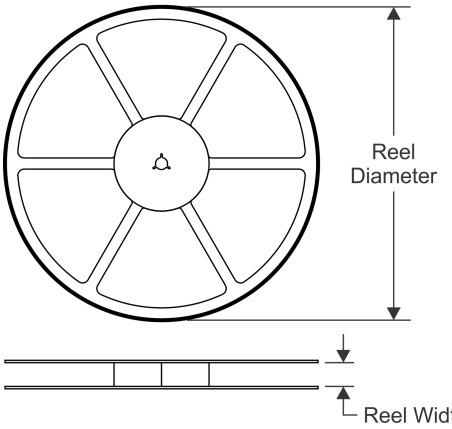
- Automotive: UCC27531-Q1

NOTE: Qualified Version Definitions:

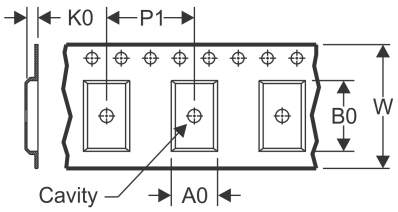
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

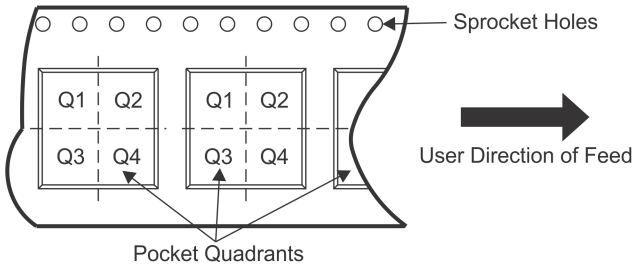


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

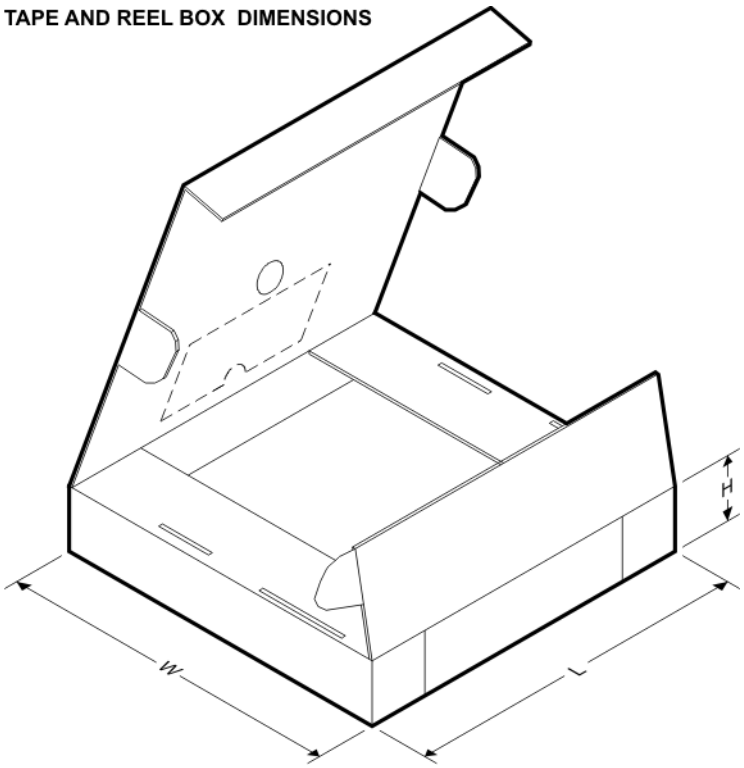
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27531DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27531DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC27531DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27531DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC27531DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27533DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27533DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27536DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27536DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27537DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27537DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27538DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27538DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

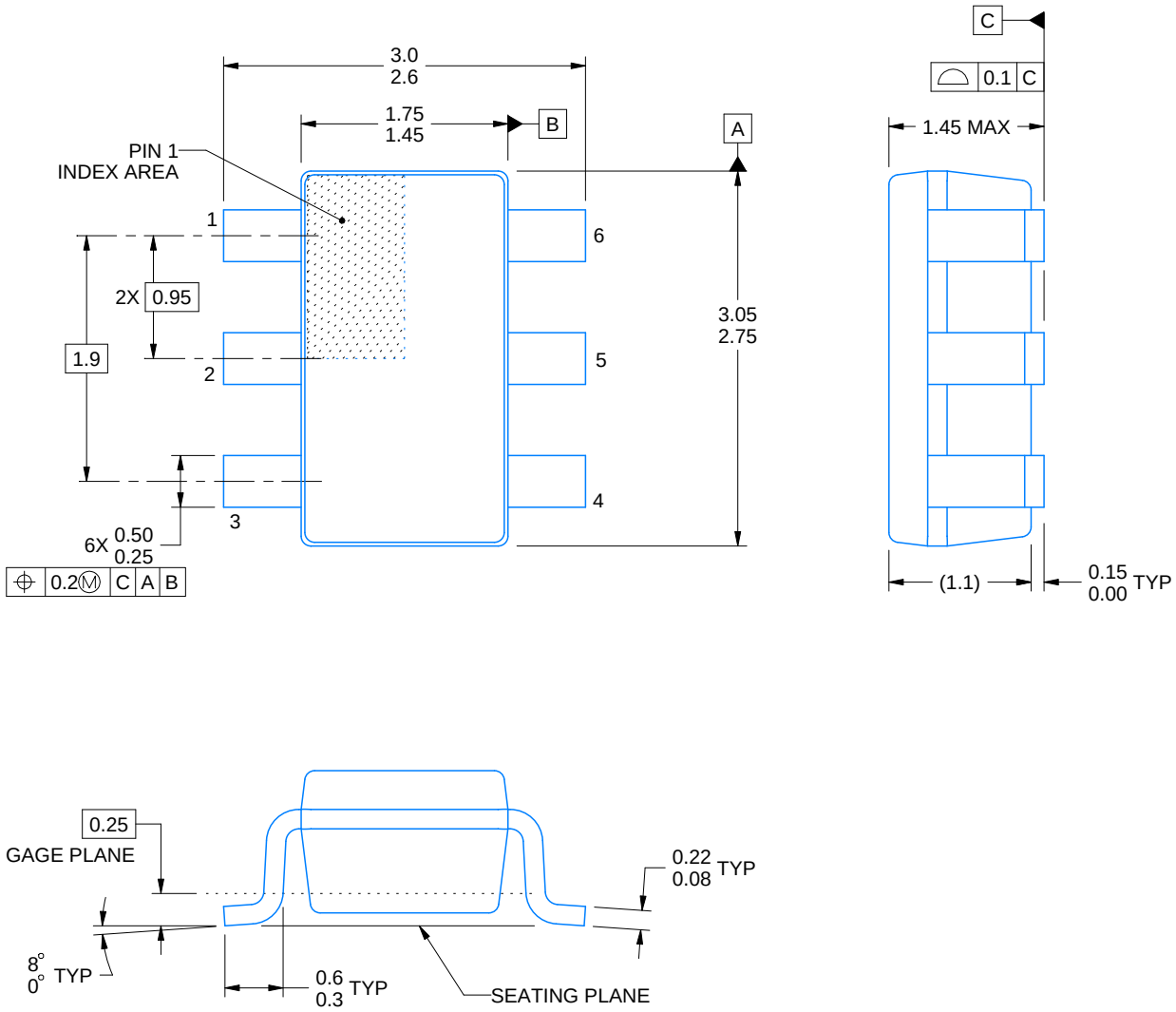
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27531DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
UCC27531DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC27531DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
UCC27531DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
UCC27531DR	SOIC	D	8	2500	367.0	367.0	35.0
UCC27533DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
UCC27533DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
UCC27536DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
UCC27536DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
UCC27537DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
UCC27537DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
UCC27538DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
UCC27538DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

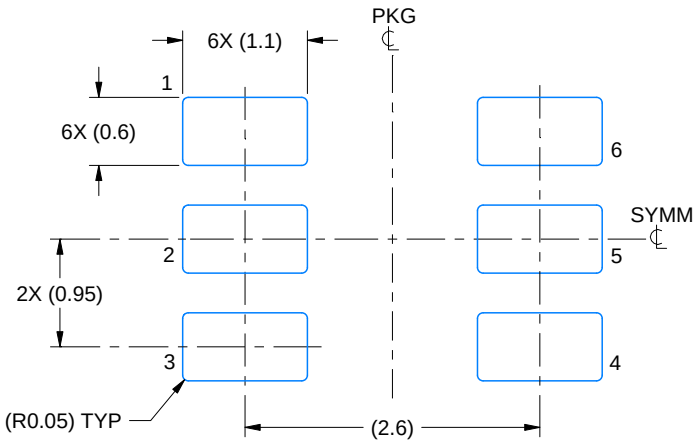
SMALL OUTLINE TRANSISTOR



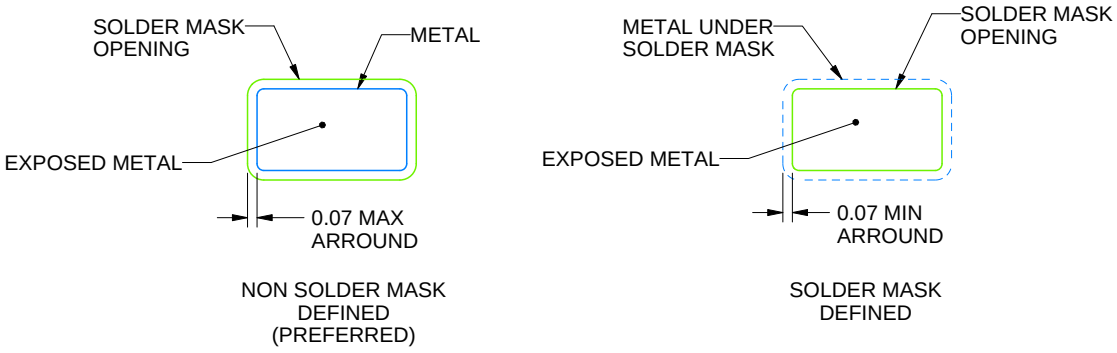
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

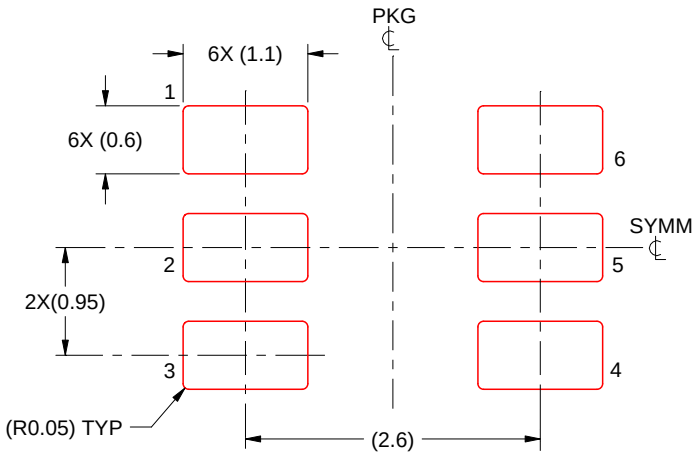


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

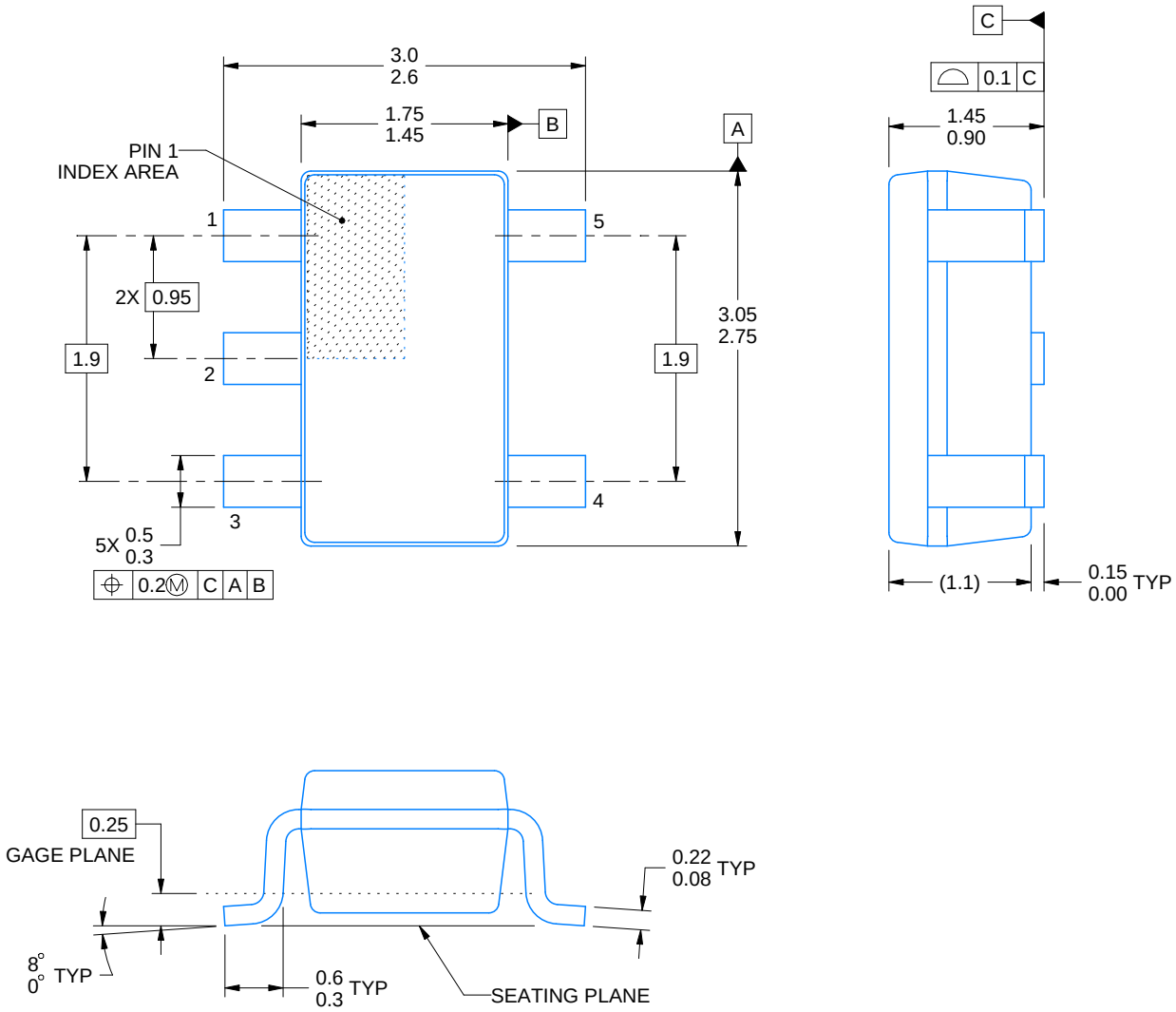
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

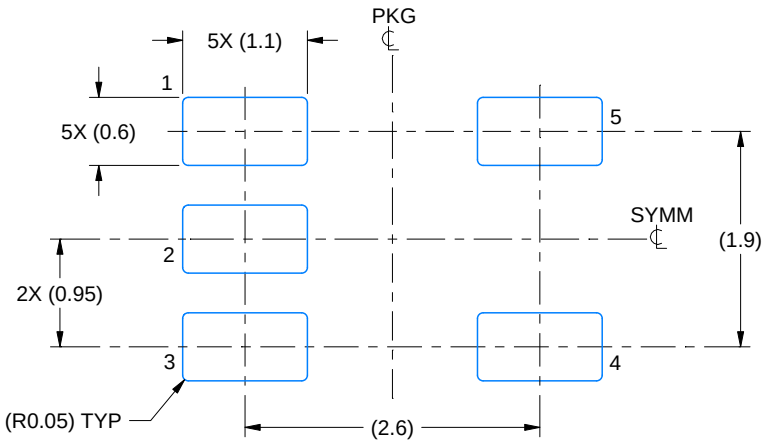
SMALL OUTLINE TRANSISTOR



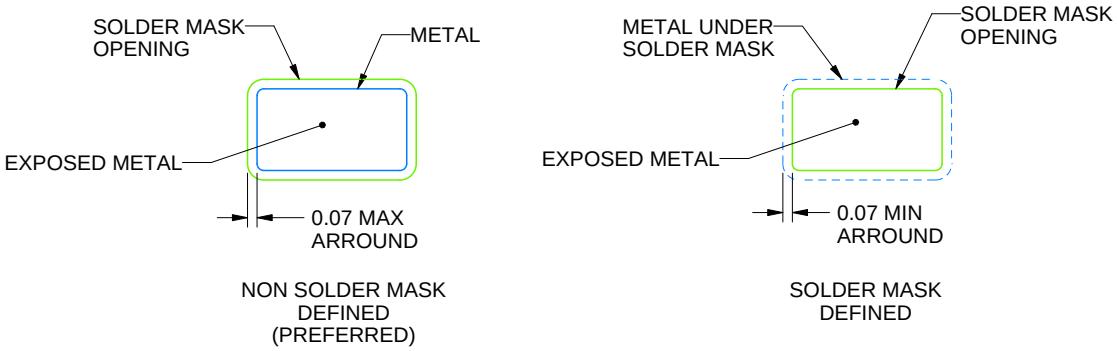
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

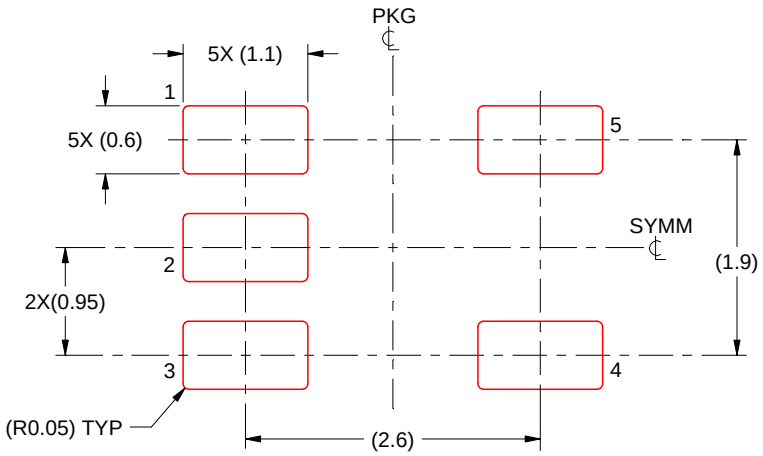


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

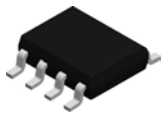


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

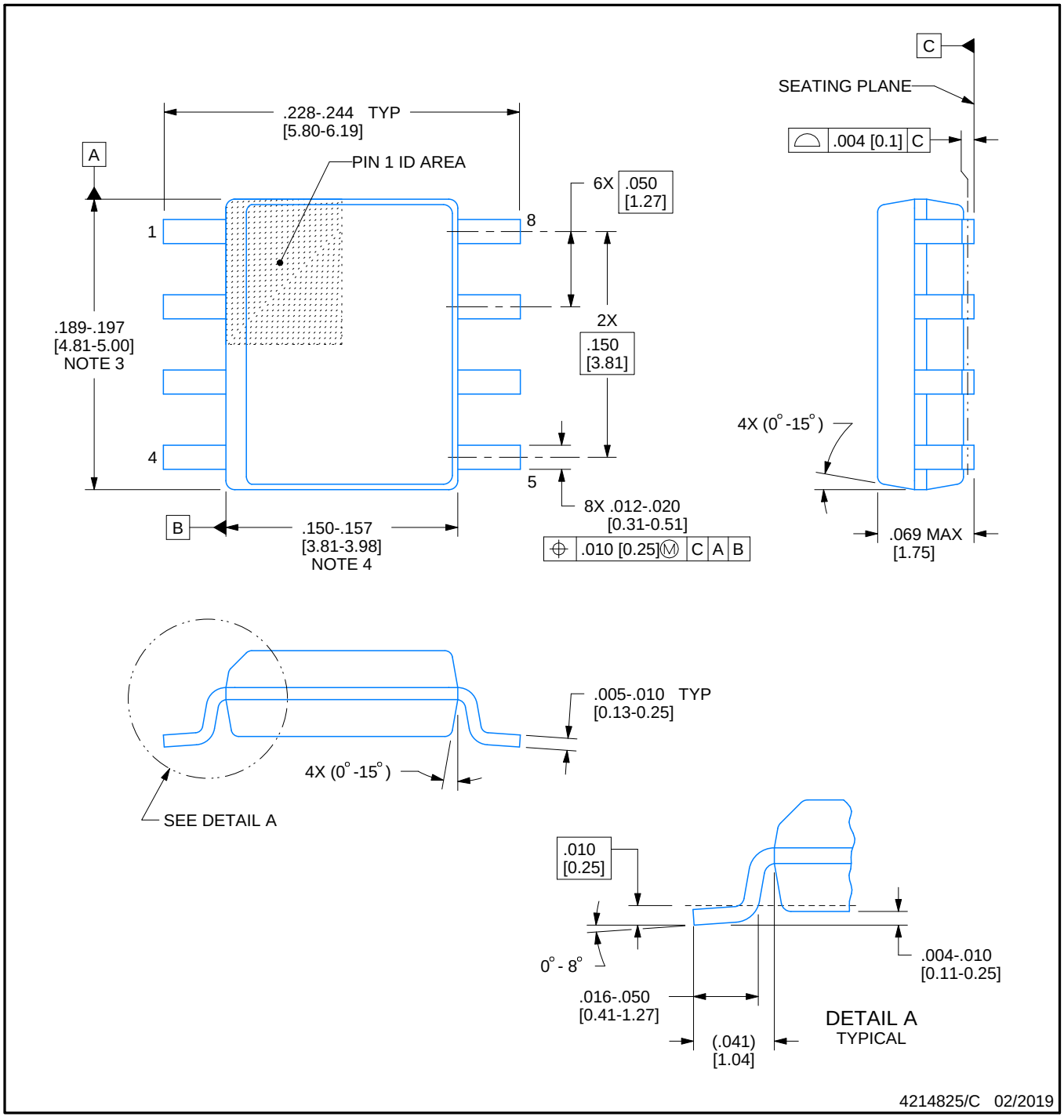


PACKAGE OUTLINE

D0008A

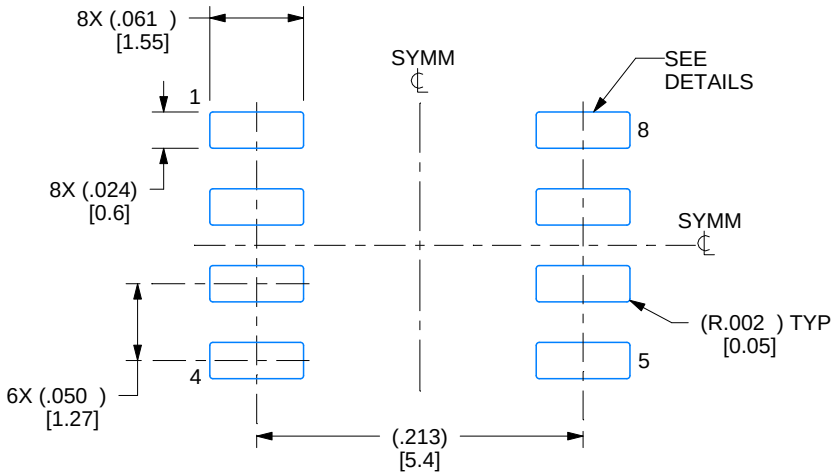
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

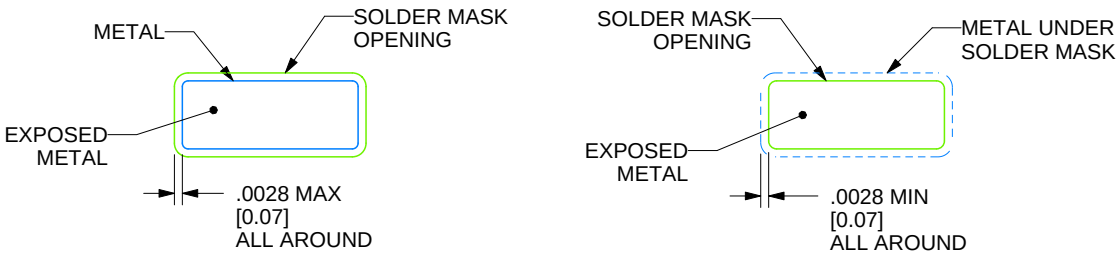


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

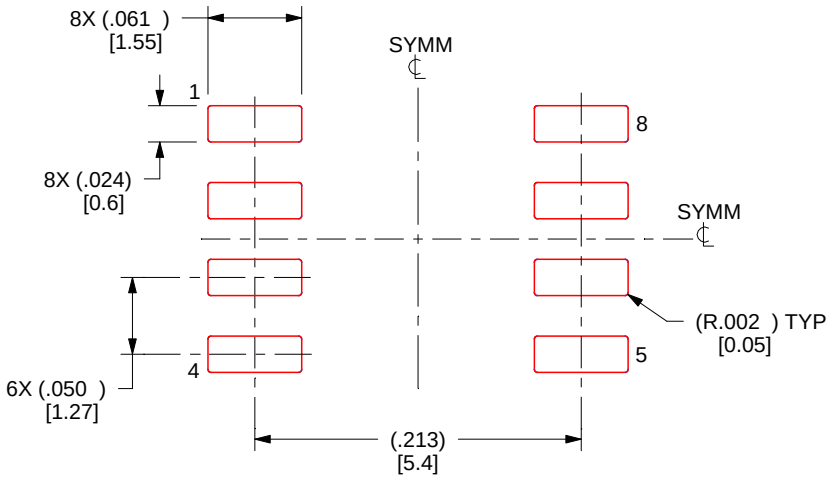
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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