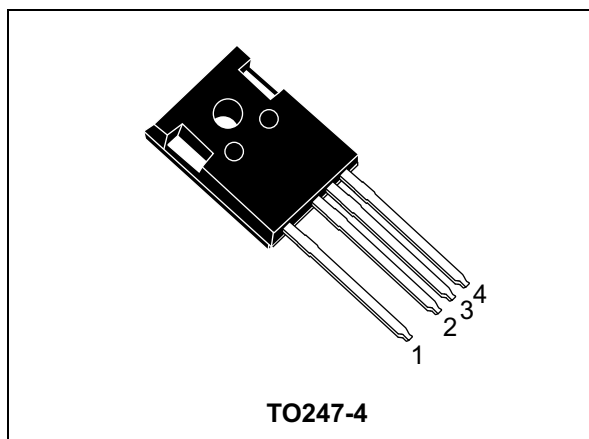


N-channel 650 V, 0.049 Ω typ., 49 A MDmesh™ M2 Power MOSFET in a TO247-4 package

Datasheet - production data



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STW56N65M2-4	650 V	0.062 Ω	49 A

- Excellent switching performance thanks to the extra driving source pin
- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

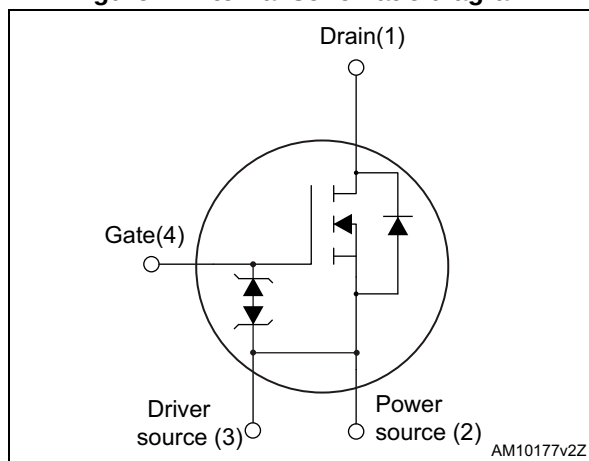


Table 1. Device summary

Order code	Marking	Package	Packaging
STW56N65M2-4	56N65M2	TO247-4	Tube

Contents

1 **Electrical ratings** **3**

2 **Electrical characteristics** **4**

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** **8**

4 **Package mechanical data** **9**

 4.1 TO247-4, STW56N65M2-4 9

5 **Revision history** **11**



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	49	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	31	A
$I_{DM}^{(1)}$	Drain current (pulsed)	196	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	358	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
T_j	Max. operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 49\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, $V_{DS(\text{peak})} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$

3. $V_{DS} \leq 520\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^{\circ}\text{C}/\text{W}$
$R_{thj-case}$	Thermal resistance junction-case max	0.35	$^{\circ}\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	1300	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 10	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 24.5\text{ A}$		0.049	0.062	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	3900	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{rss}	Reverse transfer capacitance		-	2.8	-	pF
$C_{o(er)}^{(1)}$	Equivalent Output Capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }520\text{ V}$	-	838	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	4.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 49\text{ A}$, $V_{GS} = 10\text{ V}$, (see Figure 15)	-	93	-	nC
Q_{gs}	Gate-source charge		-	16	-	nC
Q_{gd}	Gate-drain charge		-	40	-	nC

1. C_{oss} eq. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325 \text{ V}$, $I_D = 24.5 \text{ A}$, $R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 16 and Figure 19)	-	19	-	ns
t_r	Rise time		-	27.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	146	-	ns
t_f	Fall time		-	13	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		49	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		196	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 49 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 49 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 16)	-	554		ns
Q_{rr}	Reverse recovery charge		-	13.5		μC
I_{RRM}	Reverse recovery current		-	49.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 49 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 19)	-	688		ns
Q_{rr}	Reverse recovery charge		-	18		μC
I_{RRM}	Reverse recovery current		-	52		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

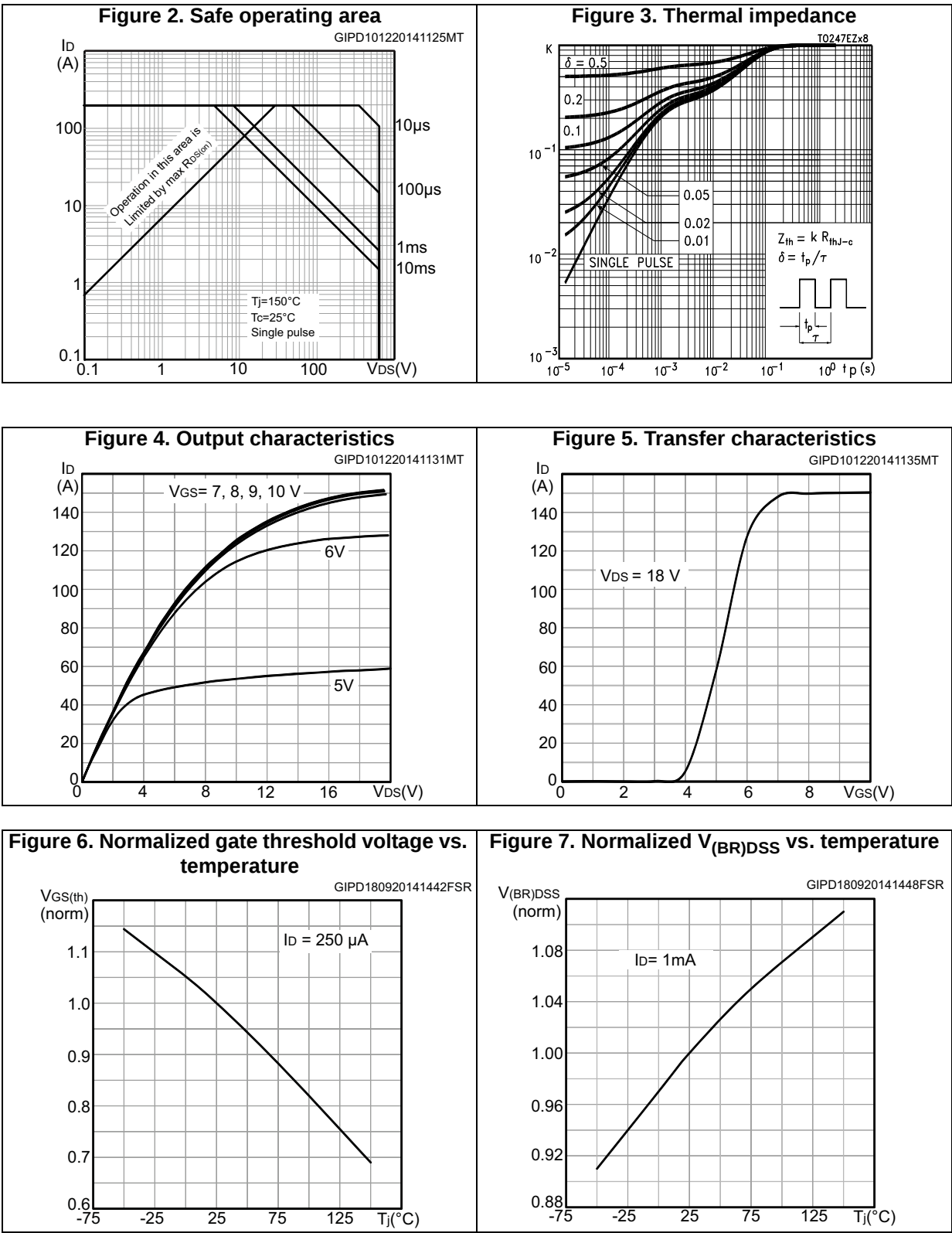


Figure 8. Static drain-source on-resistance

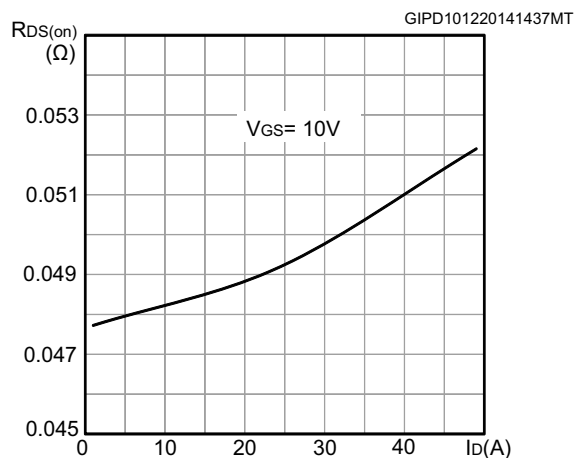


Figure 9. Normalized on-resistance vs. temperature

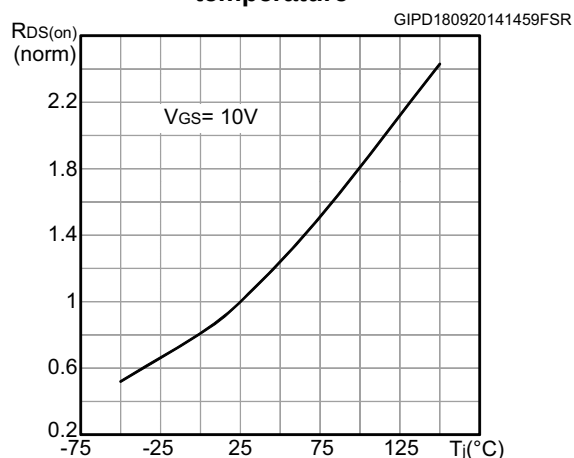


Figure 10. Gate charge vs. gate-source voltage

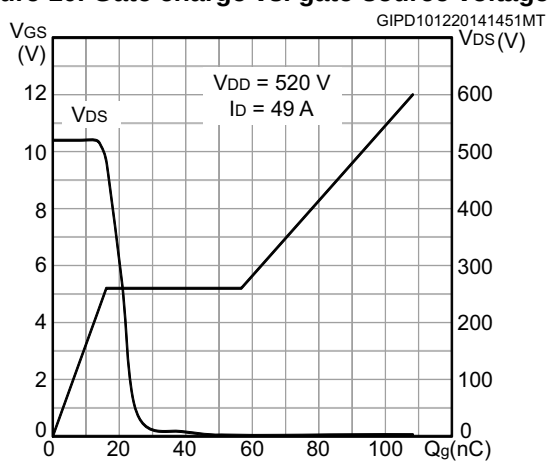


Figure 11. Capacitance variations

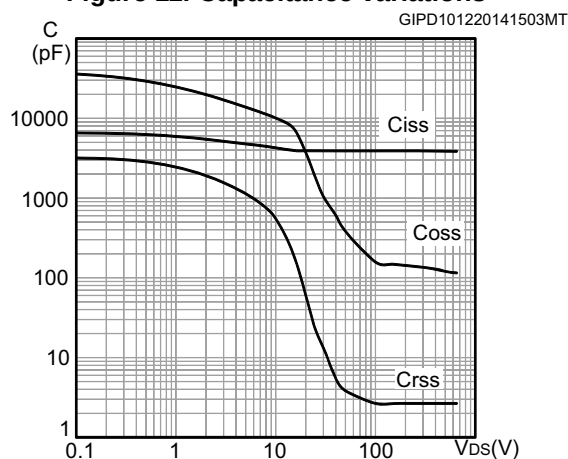


Figure 12. Output capacitance stored energy

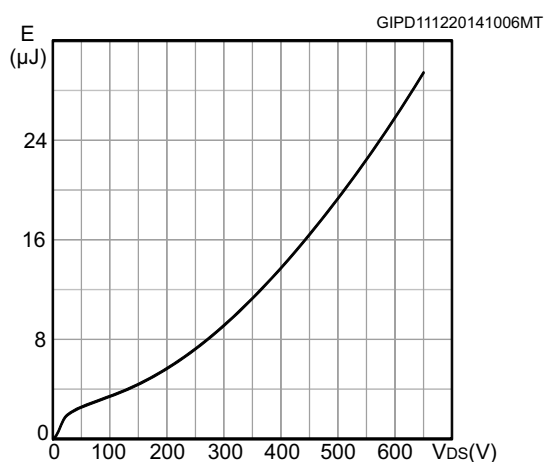
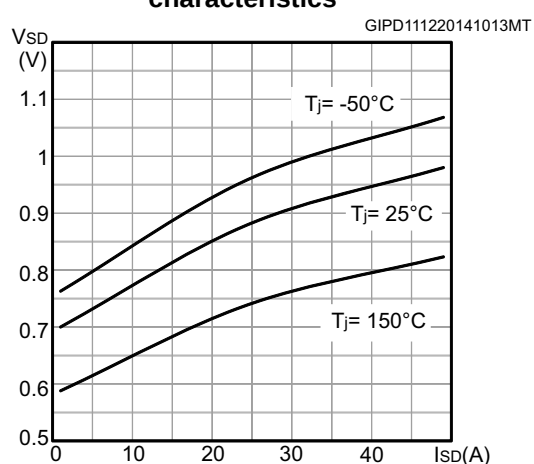
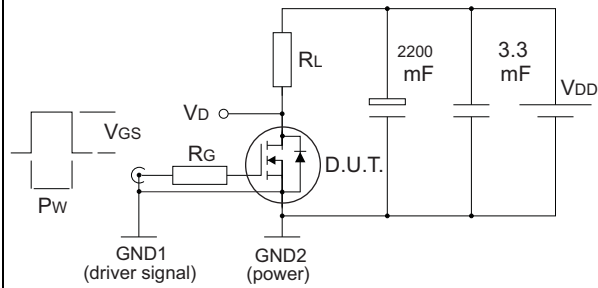


Figure 13. Source-drain diode forward characteristics



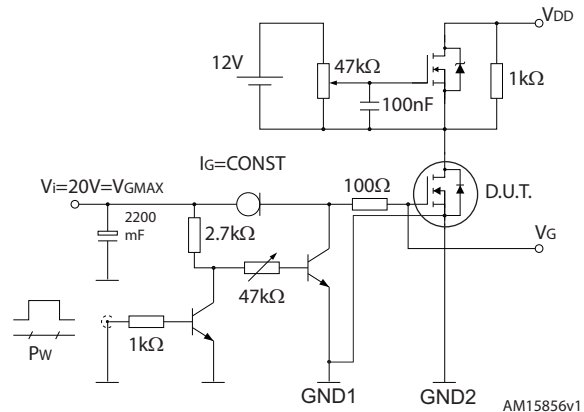
3 Test circuits

Figure 14. Switching times test circuit for resistive load



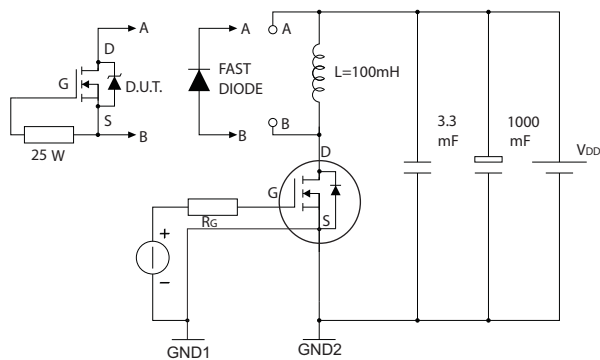
AM15855v1

Figure 15. Gate charge test circuit



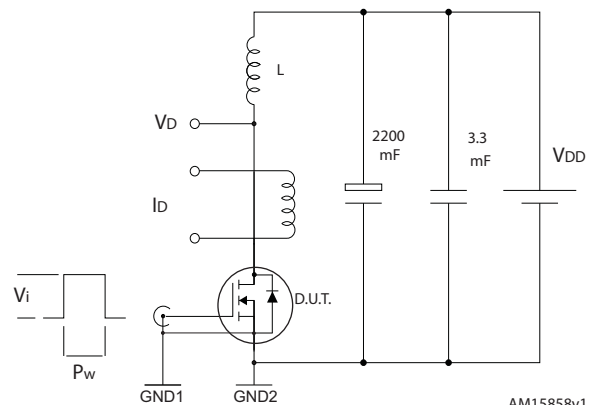
AM15856v1

Figure 16. Test circuit for inductive load switching and diode recovery times



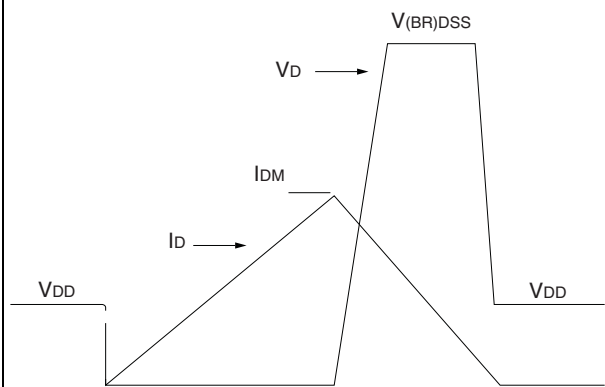
AM15857v1

Figure 17. Unclamped inductive load test circuit



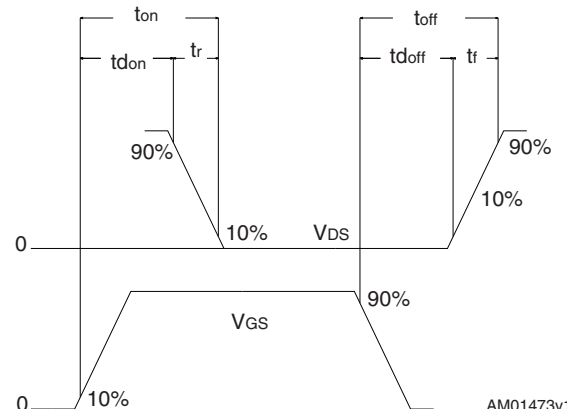
AM15858v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



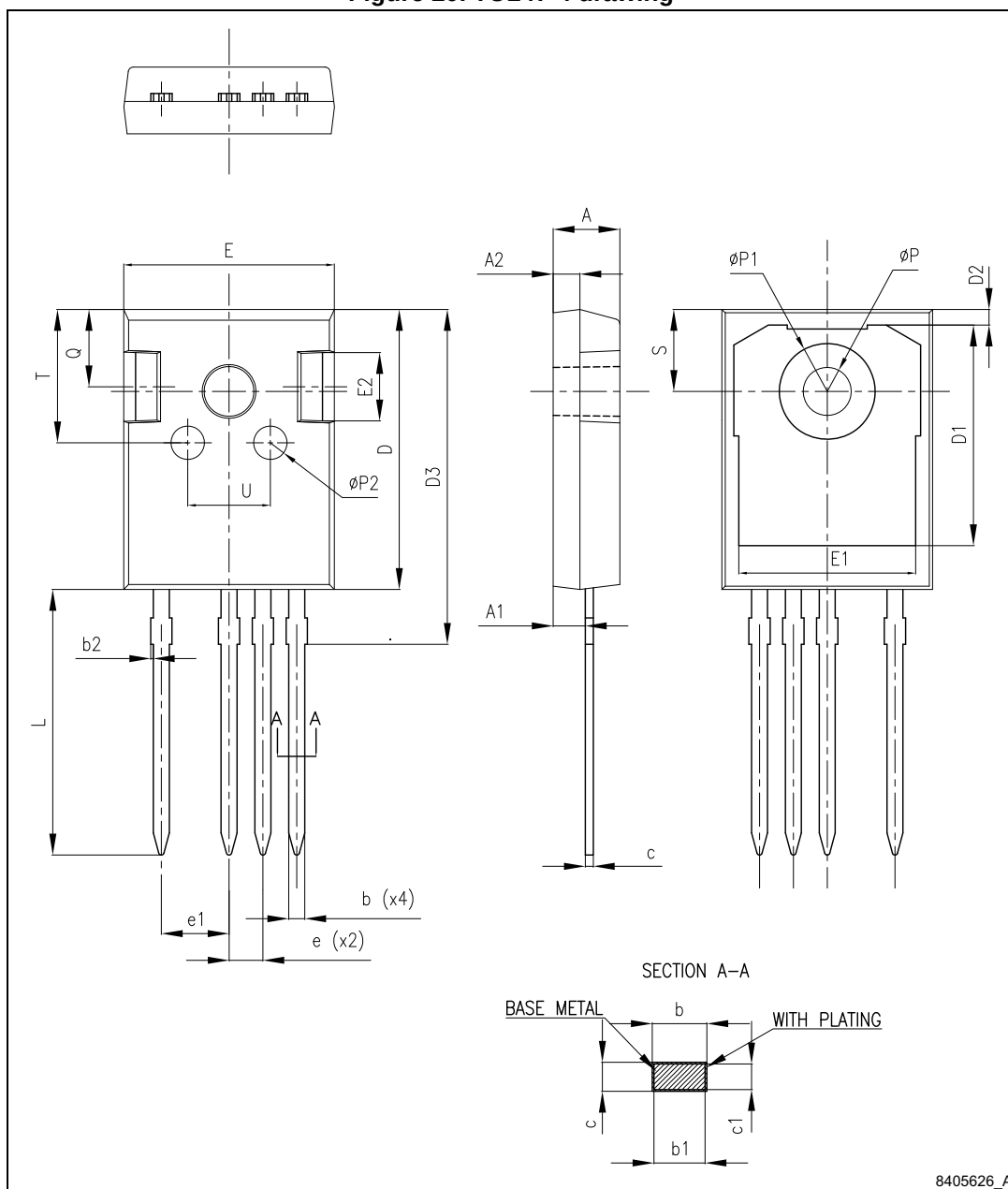
AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO247-4, STW56N65M2-4

Figure 20. TO247-4 drawing



8405626_A

Table 9. TO247-4 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-Dec-2014	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved