L6728

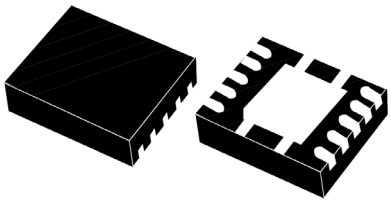
Single phase PWM controller with Power Good

Features

- Flexible power supply from 5 V to 12 V
- Power conversion input as low as 1.5 V
- 0.8 V internal reference
- 0.8 % output voltage accuracy
- High-current integrated drivers
- Power Good output
- Sensorless and programmable OCP across low-side $R_{DS(on)}$
- OV / UV protections
- VSEN disconnection protection
- Oscillator internally fixed at 300 kHz
- LSless to manage pre-bias start-up
- Adjustable output voltage
- Disable function
- Internal soft-start
- DFN10 package

Applications

- Memory and termination supply
- Subsystem power supply (MCH, IOCH, PCI...)
- CPU and DSP power supply
- Distributed power supply
- General DC-DC converters



DFN10

Description

L6728 is a single-phase step-down controller with integrated high-current drivers that provides complete control logic and protection to realize in a simple way general DC-DC converters by using a compact DFN10 package.

Device flexibility allows managing conversions with power input V_{IN} as low as 1.5 V and device supply voltage ranging from 5 V to 12 V.

L6728 provides simple control loop with voltage mode EA. The integrated 0.8 V reference allows regulating output voltages with ±0.8 % accuracy over line and temperature variations. Oscillator is internally fixed to 300 kHz.

L6728 provides programmable dual level over current protection as well as over and under voltage protection. Current information is monitored across the low-side MOSFET $R_{DS(on)}$ saving the use of expensive and space-consuming sense resistors.

PGOOD output easily provides real-time information on output voltage status, through VSEN dedicated output monitor.

Obsolete Product(s) - Obsolete Product(s)

Table 1. Device summary

Order codes	Package	Packaging
L6728	DFN10	Tube
L6728TR		Tape and reel

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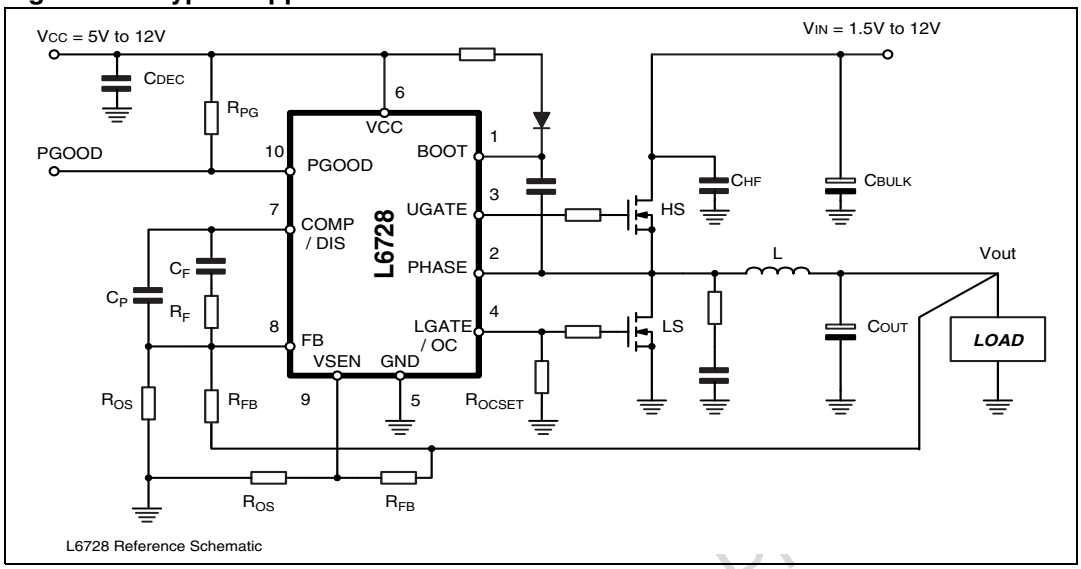
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1 Typical application circuit and block diagram

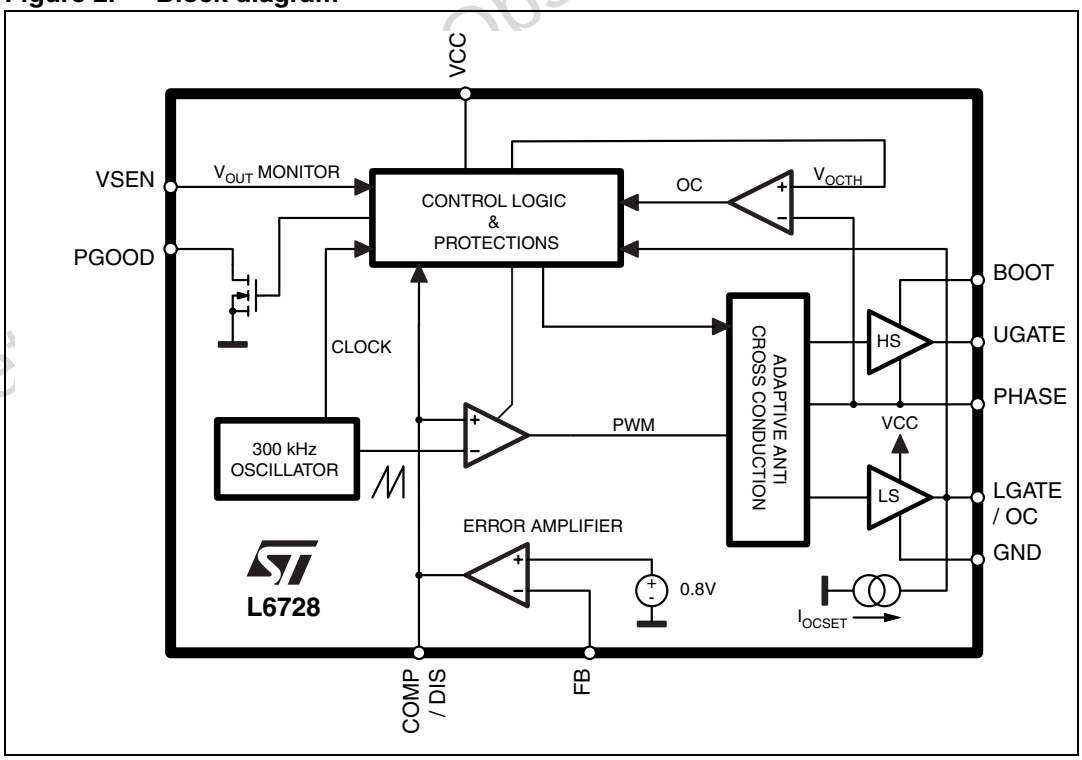
1.1 Application circuit

Figure 1. Typical application circuit



1.2 Block diagram

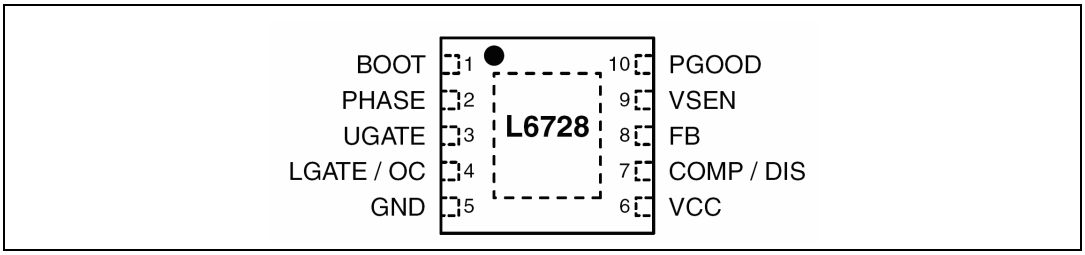
Figure 2. Block diagram



Obsolete

2 Pin description and connection diagrams

Figure 3. Pin connection (top view)



2.1 Pin descriptions

Table 2. Pins description

Pin #	Name	Function
1	BOOT	HS driver supply. Connect through a capacitor (100 nF) to the floating node (LS-Drain) pin and provide necessary bootstrap diode from VCC.
2	PHASE	HS driver return path, current-reading and adaptive-dead-time monitor. Connect to the LS drain to sense $R_{DS(on)}$ drop to measure the output current. This pin is also used by the adaptive-dead-time control circuitry to monitor when HS MOSFET is OFF.
3	UGATE	HS driver output. Connect directly to HS MOSFET gate.
4	LGATE / OC	*LGATE*. LS driver output. Connect directly to LS MOSFET gate. *OC*. Over Current threshold set. During a short period of time following VCC rising over UVLO threshold, a 10 µA current is sourced from this pin. Connect to GND with an R_{OCSET} resistor greater than 5 kΩ to program OC Threshold. The resulting voltage at this pin is sampled and held internally as the OC set point. Maximum programmable OC threshold is 0.55 V. A voltage greater than 0.6 V activates an internal clamp and causes OC threshold to be set at the maximum value.
5	GND	All internal references, logic and drivers are connected to this pin. Connect to the PCB ground plane.
6	VCC	Device and drivers power supply. Operative range from 5 V to 12 V. Filter with at least 1 nF MLCC to GND.
7	COMP / DIS	*COMP*. Error amplifier output. Connect with an R_F - C_F // C_P to FB to compensate the device control loop. *DIS*. The device can be disabled by pushing this pin lower than 0.75 V (typ). Setting free the pin, the device enables again.
8	FB	Error amplifier inverting input. Connect with a resistor R_{FB} to the output regulated voltage. Output resistor divider may be used to regulate voltages higher than the reference.

Obsolete Product(s) - Obsolete Product(s)

Table 2. Pins description (continued)

Pin #	Name	Function
9	VSEN	Regulated voltage sense pin for OVP and UVP protections and PGOOD. Connect to the output regulated voltage, or to the output resistor divider if the regulated voltage is higher than the reference.
10	PGOOD	Open drain output set free after SS has finished and pulled low when VSEN is outside the relative window. Pull up to a voltage equal or lower than VCC. If not used it can be left floating.

3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient (Device soldered on 2s2p, 67 mm x 69 mm board)	45	°C/W
$R_{th(JC)}$	Thermal resistance junction to case	5	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-40 to 125	°C
P_{TOT}	Maximum power dissipation at T_A = 25 °C	2.25	W

Obsolete Product(s) - Obsolete Product(s)

4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	to GND	-0.3 to 15	V
V_{BOOT}, V_{UGATE}	to PHASE to GND to GND; t < 200 ns	15 33 45	V
V_{PHASE}	to GND to GND; t < 200 ns	-5 to 18 -8 to 30	V
V_{LGATE}	to GND	-0.3 to VCC+0.3	V
	FB, COMP, VSEN to GND	-0.3 to 3.6	V
	PGOOD to GND	-0.3 to VCC+0.3	V

4.2 Electrical characteristics

Table 5. Electrical characteristics
(V_{CC} = 5 V to 12 V; T_J = 0 to 70 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Supply current and power-ON						
I_{CC}	VCC supply current	UGATE and LGATE = OPEN		6		mA
I_{BOOT}	BOOT supply current	UGATE = OPEN; PHASE to GND		0.7		mA
UVLO	VCC Turn-ON	VCC rising			4.1	V
	Hysteresis			0.2		V
Oscillator						
F_{SW}	Main oscillator accuracy		270	300	330	kHz
ΔV_{OSC}	PWM ramp amplitude			1.4		V
d_{MAX}	Maximum duty cycle		80			%
Reference and error amplifier						
	Output voltage accuracy		-0.8	-	0.8	%
A_0	DC gain (1)			120		dB
GBWP	Gain-bandwidth product (1)			15		MHz
SR	Slew-rate (1)			8		V/µs
DIS	Disable threshold	COMP falling	0.70		0.85	V

Obsolete Product(s) - Obsolete Product(s)

Table 5. Electrical characteristics (continued)
(V_{CC} = 5 V to 12 V; T_J = 0 to 70 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Gate drivers						
I_{UGATE}	HS source current	BOOT - PHASE = 5 V		1.5		A
R_{UGATE}	HS sink resistance	BOOT - PHASE = 5 V		1.1		Ω
I_{LGATE}	LS source current	VCC = 5 V		1.5		A
R_{LGATE}	LS sink resistance	VCC = 5 V		0.65		Ω
Over-current protection						
I_{OCSET}	OCSET current source	Sourced from LGATE pin, during OC setting phase.	9	10	11	µA
V_{OC_SW}	OC switch-over threshold	$V_{LGATE/OC}$ rising		600		mV
Over and under-voltage protections						
OVP	OVP threshold	VSEN rising	0.970	1.000	1.030	V
		un-latch, VSEN falling	0.35	0.40	0.45	V
UVP	UVP threshold	VSEN falling	0.570	0.600	0.630	V
VSEN	VSEN bias current	Sourced from VSEN		100		nA
PGOOD						
PGOOD	Upper threshold	VSEN rising	0.860	0.890	0.920	V
	Lower threshold	VSEN falling	0.680	0.710	0.740	V
V_{PGOODL}	PGOOD voltage low	I_{PGOOD} = -4 mA			0.4	V

1. Guaranteed by design, not subject to test.

Obsolete Product(s) - Obsolete Product(s)

5 Device description

L6728 is a single-phase PWM controller with embedded high-current drivers that provides complete control logic and protections to realize in an easy and simple way a general DC-DC step-down converter. Designed to drive N-channel MOSFETs in a synchronous buck topology, with its high level of integration this 10-pin device allows reducing cost and size of the power supply solution also providing real-time PGOOD in a compact DFN10 3x3 mm.

L6728 is designed to operate from a 5 V or 12 V supply. The output voltage can be precisely regulated to as low as 0.8 V with ±0.8 % accuracy over line and temperature variations. The switching frequency is internally set to 300 kHz.

This device provides a simple control loop with a voltage-mode error-amplifier. The error-amplifier features a 15 MHz gain-bandwidth product and 8 V/µs slew rate, allowing high regulator bandwidth for fast transient response.

To avoid load damages, L6728 provides over current protection as well as over voltage, under voltage and feedback disconnection protection. The over current trip threshold is programmable by a simple resistor connected from Lgate to GND. Output current is monitored across low-side MOSFET $R_{DS(on)}$, saving the use of expensive and space-consuming sense resistor. Output voltage is monitored through dedicated VSEN pin.

L6728 implements soft-start increasing the internal reference in closed loop regulation. Low-side-less feature allows the device to perform soft-start over pre-biased output avoiding high current return through the output inductor and dangerous negative spike at the load side.

L6728 is available in a compact DFN10 3x3 mm package with exposed pad.

Obsolete Product(s) - Obsolete Product(s)

6 Driver section

The integrated high-current drivers allow using different types of power MOSFET (also multiple MOSFETs to reduce the equivalent $R_{DS(on)}$), maintaining fast switching transition.

The driver for the high-side MOSFET uses BOOT pin for supply and PHASE pin for return. The driver for low-side MOSFET uses the VCC pin for supply and GND pin for return.

The controller embodies an anti-shoot-through and adaptive dead-time control to minimize low side body diode conduction time, maintaining good efficiency while saving the use of Schottky diode:

- to check high-side MOSFET turn off, PHASE pin is sensed. When the voltage at PHASE pin drops down, the low-side MOSFET gate drive is suddenly applied;
- to check low-side MOSFET turn off, LGATE pin is sensed. When the voltage at LGATE has fallen, the high-side MOSFET gate drive is suddenly applied.

If the current flowing in the inductor is negative, voltage on PHASE pin will never drop. To allow the low-side MOSFET to turn-on even in this case, a watchdog controller is enabled: if the source of the high-side MOSFET doesn't drop, the low side MOSFET is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Power conversion input is flexible: 5 V, 12 V bus or any bus that allows the conversion (See maximum duty cycle limitations) can be chosen freely.

6.1 Power dissipation

L6728 embeds high current MOSFET drivers for both high side and low side MOSFETs: it is then important to consider the power that the device is going to dissipate in driving them in order to avoid overcoming the maximum junction operative temperature.

Two main terms contribute in the device power dissipation: bias power and drivers' power.

- Device bias power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow (assuming to supply HS and LS drivers with the same VCC of the device):

$$P_{DC} = V_{CC} \cdot (I_{CC} + I_{BOOT})$$

- Drivers power is the power needed by the driver to continuously switch on and off the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs (easy calculable) is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation. The total power dissipated to switch the MOSFETs results:

$$P_{SW} = F_{SW} \cdot (Q_{gHS} \cdot V_{BOOT} + Q_{gLS} \cdot V_{CC})$$

External gate resistors helps the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.

Obsolete Product(s) - Obsolete Product(s)

7 Soft-start

L6728 implements a soft-start to smoothly charge the output filter avoiding high in-rush currents to be required from the input power supply. The device gradually increases the internal reference from 0 V to 0.8 V in 4.5 ms (typ.), in closed loop regulation, linearly charging the output capacitors to the final regulation voltage.

In the event of an over current triggering during soft start, the over current logic will override the soft start sequence and will shut down the PWM logic and both the high side and low side gates. This condition is latched, cycle VCC to recover.

The device begins soft start phase only when VCC power supply is above UVLO threshold and over current threshold setting phase has been completed.

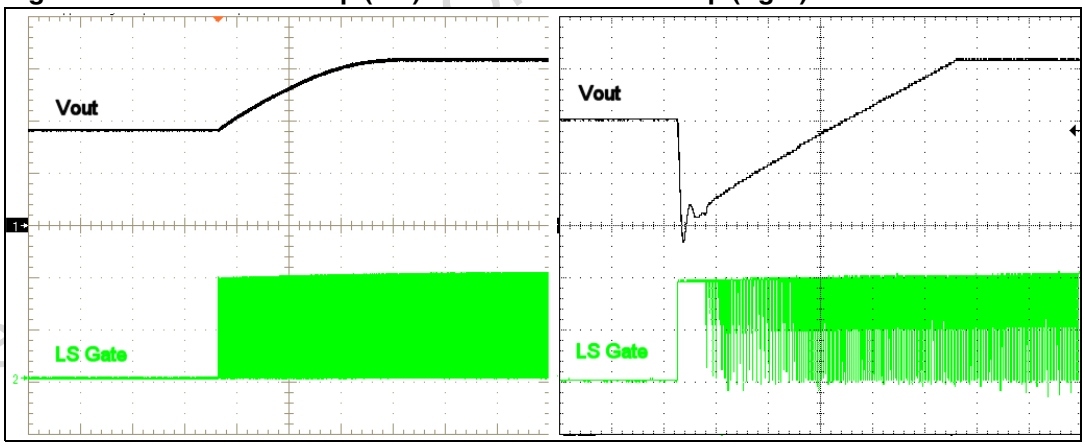
7.1 Low-side-less start up (LSLess)

In order to avoid any kind of negative undershoot and dangerous return from the load during start-up, L6728 performs a special sequence in enabling LS driver to switch: during the soft-start phase, the LS driver results disabled (LS = OFF) until the HS starts to switch. This avoid the dangerous negative spike on the output voltage that can happen if starting over a pre-biased output.

If the output voltage is pre-biased to a voltage higher than the final one, the HS would never start to switch. In this case, at the end of soft start time, LS is enabled and discharge the output to the final regulation value.

This particular feature of the device masks the LS turn-on only from the control loop point of view: protections by-pass this turning ON the LS MOSFET in case of need.

Figure 4. LSLess start up (left) vs non-LSLess start up (right)



Obsolete Product(s)

8 Over current protection

The over current function protects the converter from a shorted output or overload, by sensing the output current information across the low side MOSFET drain-source on-resistance, $R_{DS(on)}$. This method reduces cost and enhances converter efficiency by avoiding the use of expensive and space-consuming sense resistors.

The low side $R_{DS(on)}$ current sense is implemented by comparing the voltage at the PHASE node when LS MOSFET is turned on with the programmed OCP thresholds voltages, internally held. If the monitored voltage is bigger than these thresholds, an over current event is detected.

For maximum safety and load protection, L6728 implements a dual level over current protection system:

- **1st level threshold**: it is the user externally set threshold. If the monitored voltage on PHASE exceeds this threshold, a 1st level over current is detected. If four 1st level OC events are detected in four consecutive switching cycles, over current protection will be triggered.
- **2nd level threshold**: it is an internal threshold whose value is equal to 1st level threshold multiplied by a factor 1.5. If the monitored voltage on PHASE exceeds this threshold, over current protection will be triggered immediately.

When over current protection is triggered, the device turns off both LS and HS MOSFETs in a latched condition.

To recover from over current protection triggered condition, VCC power supply must be cycled.

Obsolete Product(s) - Obsolete Product(s)

8.1 Over current threshold setting

L6728 allows to easily program a 1st level over current threshold ranging from 50 mV to 550 mV, simply by adding a resistor (R_{OCSET}) between LGATE and GND. 2nd level threshold will be automatically set accordingly.

During a short period of time (about 5 ms) following VCC rising over UVLO threshold, an internal 10 µA current (I_{OCSET}) is sourced from LGATE pin, determining a voltage drop across R_{OCSET}. This voltage drop will be sampled and internally held by the device as 1st level over current threshold. The OC setting procedure overall time length is about 5 ms.

Connecting a R_{OCSET} resistor between LGATE and GND, the programmed 1st level threshold will be:

$$I_{OCth1} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{dsON}}$$

the programmed 2nd level threshold will be:

$$I_{OCth2} = 1.5 \cdot \frac{I_{OCSET} \cdot R_{OCSET}}{R_{dsON}}$$

R_{OCSET} values range from 5 kΩ to 55 kΩ.

In case R_{OCSET} is not connected, the device sets the OCP thresholds to the maximum values: an internal safety clamp on LGATE is triggered as soon as LGATE voltage reaches 600 mV, setting the maximum threshold and suddenly ending OC setting phase.

Obsolete Product(s) - Obsolete Product(s)

9 Output voltage setting and protections

L6728 is capable to precisely regulate an output voltage as low as 0.8 V. In fact, the device comes with a fixed 0.8 V internal reference that guarantee the output regulated voltage to be within ±0.8 % tolerance over line and temperature variations (excluding output resistor divider tolerance, when present).

Output voltage higher than 0.8 V can be easily achieved by adding a resistor R_{OS} between FB pin and ground. Referring to *Figure 1*, the steady state DC output voltage will be:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB}}{R_{OS}}\right)$$

where V_{REF} is 0.8 V.

L6728 monitors the voltage at VSEN pin and compares it to internal reference voltage in order to provide under voltage and over voltage protections as well as PGOOD signal. According to the level of VSEN, different actions are performed from the controller:

- PGOOD

  If the voltage monitored through VSEN exits from the PGOOD window limits, the device de-asserts the PGOOD signal still continuing switching and regulating. PGOOD is asserted at the end of the soft-start phase.

- Under voltage protection

  If the voltage at VSEN pin drops below UV threshold, the device turns off both HS and LS MOSFETs, latching the condition. Cycle VCC to recover.

- Over voltage protection

  If the voltage at VSEN pin rises over OV threshold (1 V typ), over voltage protection turns off HS MOSFET and turns on LS MOSFET. The LS MOSFET will be turned off as soon as VSEN goes below Vref/2 (0.4 V). The condition is latched, cycle VCC to recover. Notice that, even if the device is latched, the device still controls the LS MOSFET and can switch it on whenever VSEN rises above OV threshold.

- Feedback disconnection protection

  In order to provide load protection even if VSEN pin is not connected, a 100 nA bias current is always sourced from this pin. If VSEN pin is not connected, this current will permanently pull it up causing the device to detect an OV: thus LS will be latched on preventing output voltage from rising out of control.

Obsolete Product(s) - Obsolete Product(s)

10 Application details

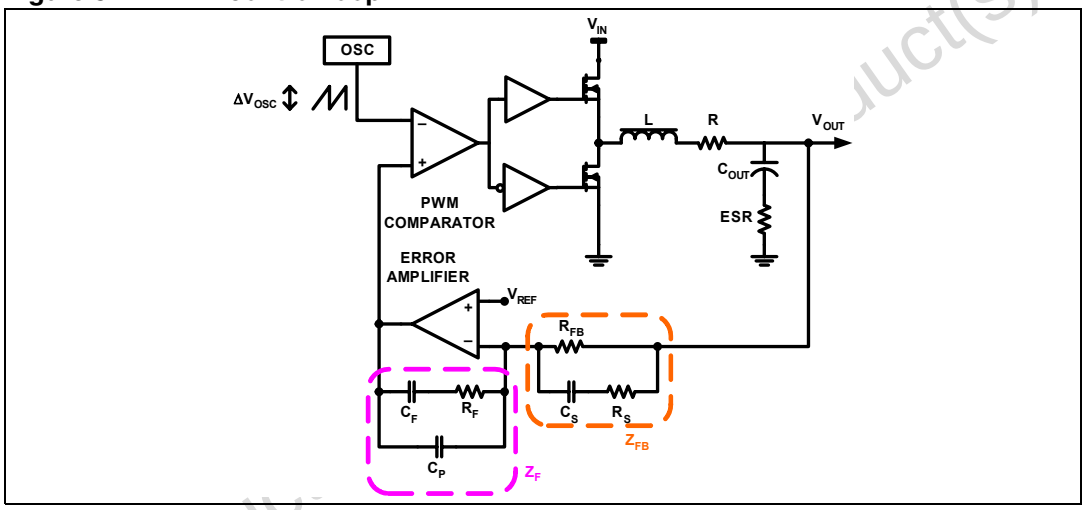
10.1 Compensation network

The control loop showed in *Figure 5* is a voltage mode control loop. The output voltage is regulated to the internal reference (when present, offset resistor between FB node and GND can be neglected in control loop calculation).

Error Amplifier output is compared to oscillator saw-tooth waveform to provide PWM signal to the driver section. PWM signal is then transferred to the switching node with V_{IN} amplitude. This waveform is filtered by the output filter.

The converter transfer function is the small signal transfer function between the output of the EA and V_{OUT}. This function has a double pole at frequency F_{LC} depending on the L-C_{OUT} resonance and a zero at F_{ESR} depending on the output capacitor ESR. The DC Gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Figure 5. PWM control loop



The compensation network closes the loop joining V_{OUT} and EA output with transfer function ideally equal to $-Z_F / Z_{FB}$.

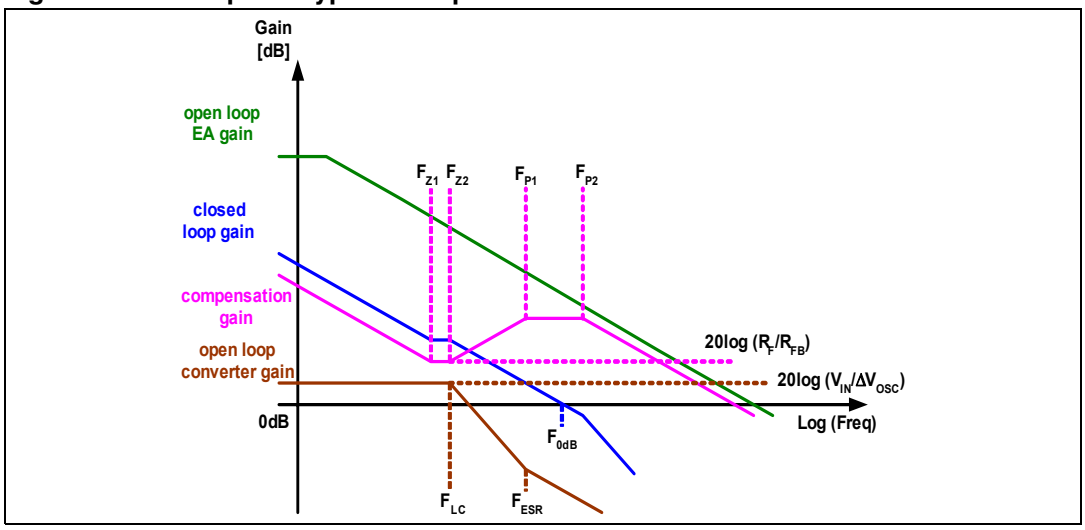
Compensation goal is to close the control loop assuring high DC regulation accuracy, good dynamic performances and stability. To achieve this, the overall loop needs high DC gain, high bandwidth and good phase margin.

High DC gain is achieved giving an integrator shape to compensation network transfer function. Loop bandwidth (F_{0dB}) can be fixed choosing the right R_F/R_{FB} ratio, however, for stability, it should not exceed $F_{SW}/2\pi$. To achieve a good phase margin, the control loop gain has to cross 0 dB axis with -20 dB/decade slope.

As an example, *Figure 6* shows an asymptotic bode plot of a type III compensation.

Obsolete Product(s)

Figure 6. Example of type III compensation



- Open loop converter singularities:

  a) $F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}}$

  b) $F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$

- Compensation network singularities frequencies:

  a) $F_{Z1} = \frac{1}{2\pi \cdot R_F \cdot C_F}$

  b) $F_{Z2} = \frac{1}{2\pi \cdot (R_{FB} + R_S) \cdot C_S}$

  c) $F_{P1} = \frac{1}{2\pi \cdot R_F \cdot \left(\frac{C_F \cdot C_P}{C_F + C_P}\right)}$

  d) $F_{P2} = \frac{1}{2\pi \cdot R_S \cdot C_S}$

To place the poles and zeroes of the compensation network, the following suggestions may be followed:

a) Set the gain R_F/R_{FB} in order to obtain the desired closed loop regulator bandwidth according to the approximated formula (suggested values for R_{FB} are in the range of some kΩ):

$$\frac{R_F}{R_{FB}} = \frac{F_{0dB}}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN}}$$

Obsolete Product(s) - Obsolete Product(s)

b) Place F_{Z1} below F_{LC} (typically 0.5*F_{LC}):

$$C_F = \frac{1}{\pi \cdot R_F \cdot F_{LC}}$$

c) Place F_{P1} at F_{ESR}:

$$C_P = \frac{C_F}{2\pi \cdot R_F \cdot C_F \cdot F_{ESR} - 1}$$

d) Place F_{Z2} at F_{LC} and F_{P2} at half of the switching frequency:

$$R_S = \frac{R_{FB}}{\frac{F_{SW}}{2 \cdot F_{LC}} - 1}$$

$$C_S = \frac{1}{\pi \cdot R_S \cdot F_{SW}}$$

e) Check that compensation network gain is lower than open loop EA gain before F_{0dB};

f) Check phase margin obtained (it should be greater than 45°) and repeat if necessary.

10.2 Layout guidelines

L6728 provides control functions and high current integrated drivers to implement high-current step-down DC-DC converters. In this kind of application, a good layout is very important.

The first priority when placing components for these applications has to be reserved to the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (EMI and losses) power connections (highlighted in *Figure 7*) must be a part of a power plane and anyway realized by wide and thick copper traces: loop must be anyway minimized. The critical components, i.e. the power MOSFETs, must be close one to the other. The use of multi-layer printed circuit board is recommended.

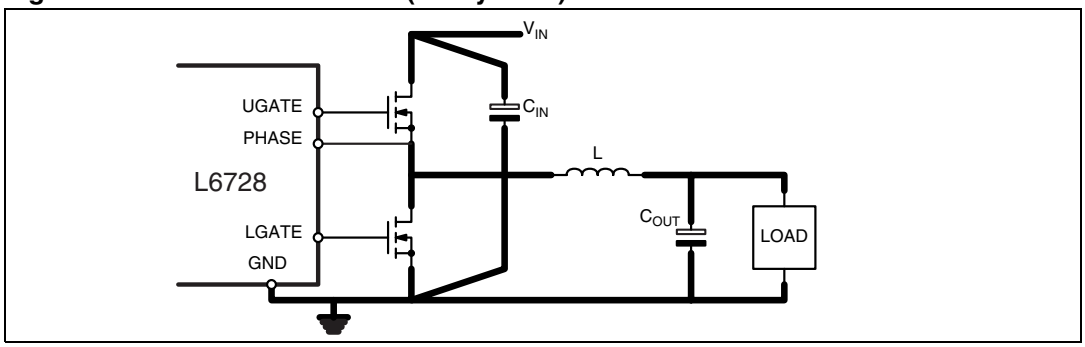
The input capacitance (C_{IN}), or at least a portion of the total capacitance needed, has to be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are preferred, MLCC are suggested to be connected near the HS drain.

Use proper VIAs number when power traces have to move between different planes on the PCB in order to reduce both parasitic resistance and inductance. Moreover, reproducing the same high-current trace on more than one PCB layer will reduce the parasitic resistance associated to that connection.

Connect output bulk capacitors (C_{OUT}) as near as possible to the load, minimizing parasitic inductance and resistance associated to the copper trace, also adding extra decoupling capacitors along the way to the load when this results in being far from the bulk capacitors bank.

Obsolete Product(s) - Obsolete Product(s)

Figure 7. Power connections (heavy lines)

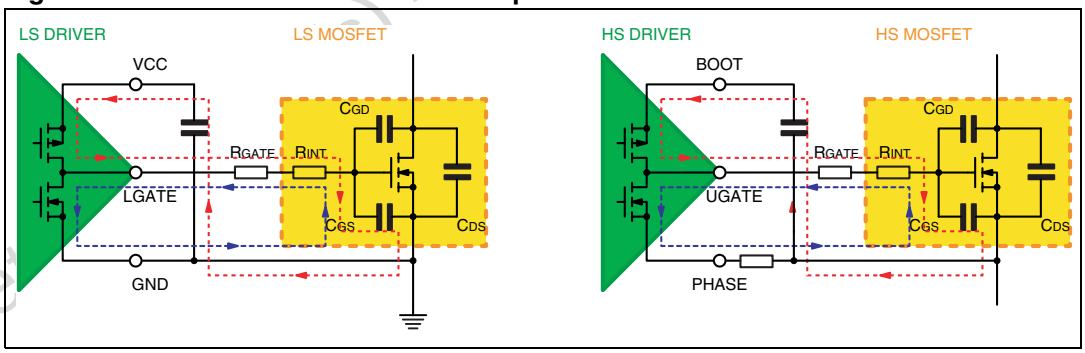


Gate traces and phase trace must be sized according to the driver RMS current delivered to the power MOSFET. The device robustness allows managing applications with the power section far from the controller without losing performances. Anyway, when possible, it is recommended to minimize the distance between controller and power section.

Small signal components and connections to critical nodes of the application, as well as bypass capacitors for the device supply, are also important. Locate bypass capacitor (VCC and Bootstrap capacitor) and feedback compensation components as close to the device as practical. For over current programmability, place R_{OCSET} close to the device and avoid leakage current paths on LGATE / OC pin, since the internal current source is only 10 µA.

Systems that do not use Schottky diode in parallel to the low-side MOSFET might show big negative spikes on the phase pin. This spike must be limited within the absolute maximum ratings (for example, adding a gate resistor in series to HS MOSFET gate), as well as the positive spike, but has an additional consequence: it causes the bootstrap capacitor to be over-charged. This extra-charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the absolute maximum ratings also causing device failures. It is then suggested in this cases to limit this extra-charge by adding a small resistor in series to the bootstrap diode.

Figure 8. Drivers turn-on and turn-off paths



Obsolete Product(s) - Obsolete Product(s)

11 Application information

11.1 Inductor design

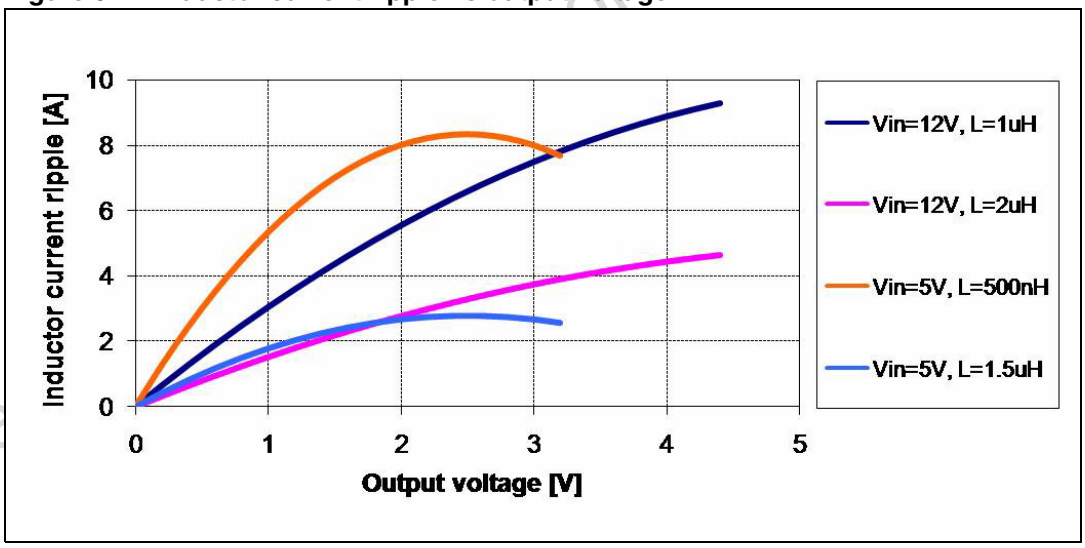
The inductance value is defined by a compromise between the dynamic response time, the efficiency, the cost and the size. The inductor has to be calculated to maintain the ripple current (ΔI_L) between 20 % and 30 % of the maximum output current (typ). The inductance value can be calculated with the following relationship:

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage. *Figure 9* shows the ripple current vs. the output voltage for different values of the inductor, with V_{IN} = 5 V and V_{IN} = 12 V.

Increasing the value of the inductance reduces the current ripple but, at the same time, increases the converter response time to a dynamic load change. The response time is the time required by the inductor to change its current from initial to final value. Until the inductor has not finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required. If the compensation network is well designed, during a load variation the device is able to set a duty cycle value very different (0 % or 80 %) from steady state one. When this condition is reached, the response time is limited by the time required to change the inductor current.

Figure 9. Inductor current ripple vs output voltage



Obsolete Product(s)

11.2 Output capacitor(s)

The output capacitors are basic components to define the ripple voltage across the output and for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient.

During steady-state conditions, the output voltage ripple is influenced by both the ESR and capacitive value of the output capacitors as follow:

$$\Delta V_{OUT_ESR} = \Delta I_L \cdot ESR$$

$$\Delta V_{OUT_C} = \Delta I_L \cdot \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}$$

Where ΔI_L is the inductor current ripple. In particular, the expression that defines ΔV_{OUT_C} takes in consideration the output capacitor charge and discharge as a consequence of the inductor current ripple.

During a load variation, the output capacitors supplies the current to the load or absorb the current stored into the inductor until the converter reacts. In fact, even if the controller recognizes immediately the load transient and sets the duty cycle at 80 % or 0 %, the current slope is limited by the inductor value. The output voltage has a drop that also in this case depends on the ESR and capacitive charge/discharge as follow:

$$\Delta V_{OUT_ESR} = \Delta I_{OUT} \cdot ESR$$

$$\Delta V_{OUT_C} = \Delta I_{OUT} \cdot \frac{L \cdot \Delta I_{OUT}}{2 \cdot C_{OUT} \cdot \Delta V_L}$$

Where ΔV_L is the voltage applied to the inductor during the transient response ($D_{MAX} \cdot V_{IN} - V_{OUT}$ for the load appliance or V_{OUT} for the load removal).

MLCC capacitors have typically low ESR to minimize the ripple but also have low capacitance that do not minimize the voltage deviation during dynamic load variations. On the contrary, electrolytic capacitors have big capacitance to minimize voltage deviation during load transients while they does not show the same ESR values of the MLCC resulting then in higher ripple voltages. For these reasons, a mix between electrolytic and MLCC capacitor is suggested to minimize ripple as well as reducing voltage deviation in dynamic mode.

11.3 Input capacitors

The input capacitor bank is designed considering mainly the input rms current that depends on the output deliverable current (I_{OUT}) and the duty-cycle (D) for the regulation as follow:

$$I_{rms} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The equation reaches its maximum value, $I_{OUT}/2$, with D = 0.5. The losses depends on the input capacitor ESR and, in worst case, are:

$$P = ESR \cdot (I_{OUT}/2)^2$$

Obsolete Product(s) - Obsolete Product(s)

12 20 A demonstration board

L6728 demonstration board realizes in a four-layer PCB a step-down DC/DC converter and shows the operation of the device in a general purpose application. The input voltage can range from 5 V to 12 V buses and the output voltage is fixed at 1.25 V. The application can deliver an output current up to 30 A. The switching frequency is 300 kHz.

Figure 10. 20 A demonstration board (left) and components placement (right)

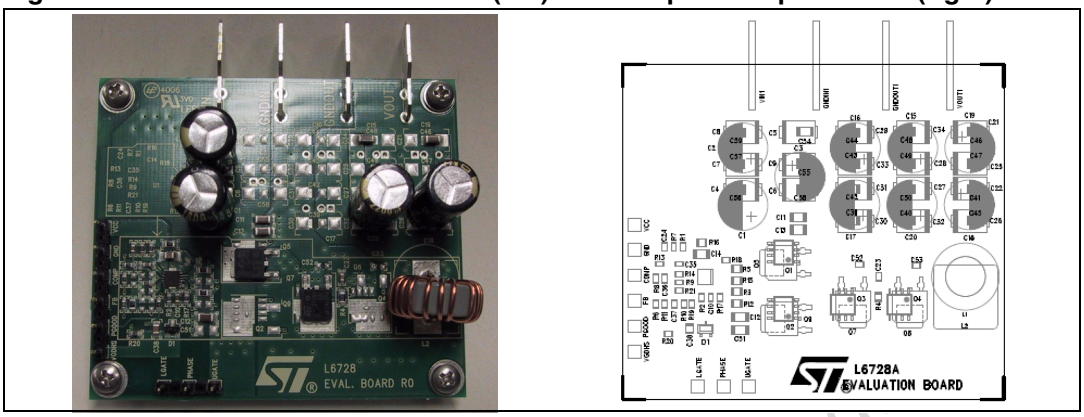


Figure 11. L6728 - 20 A demonstration board top (left) and bottom (right) layers

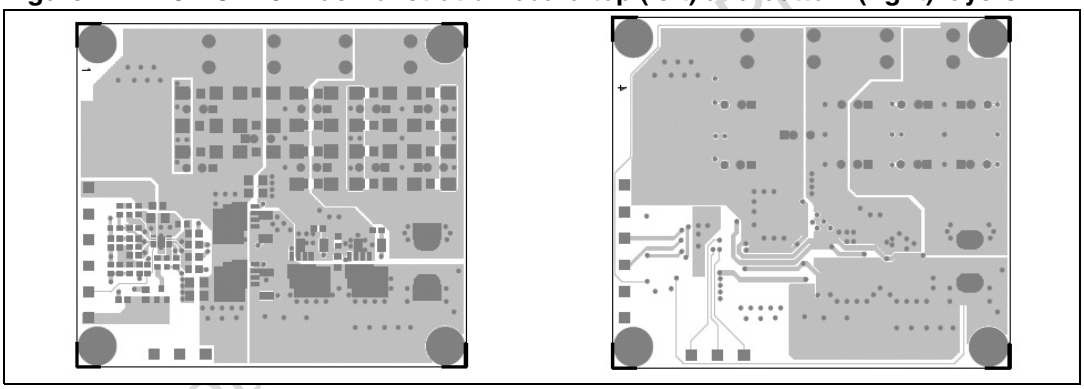
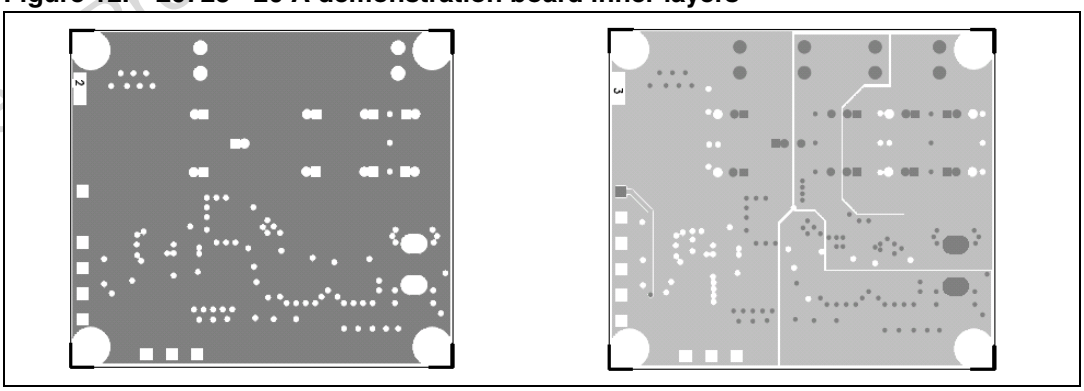
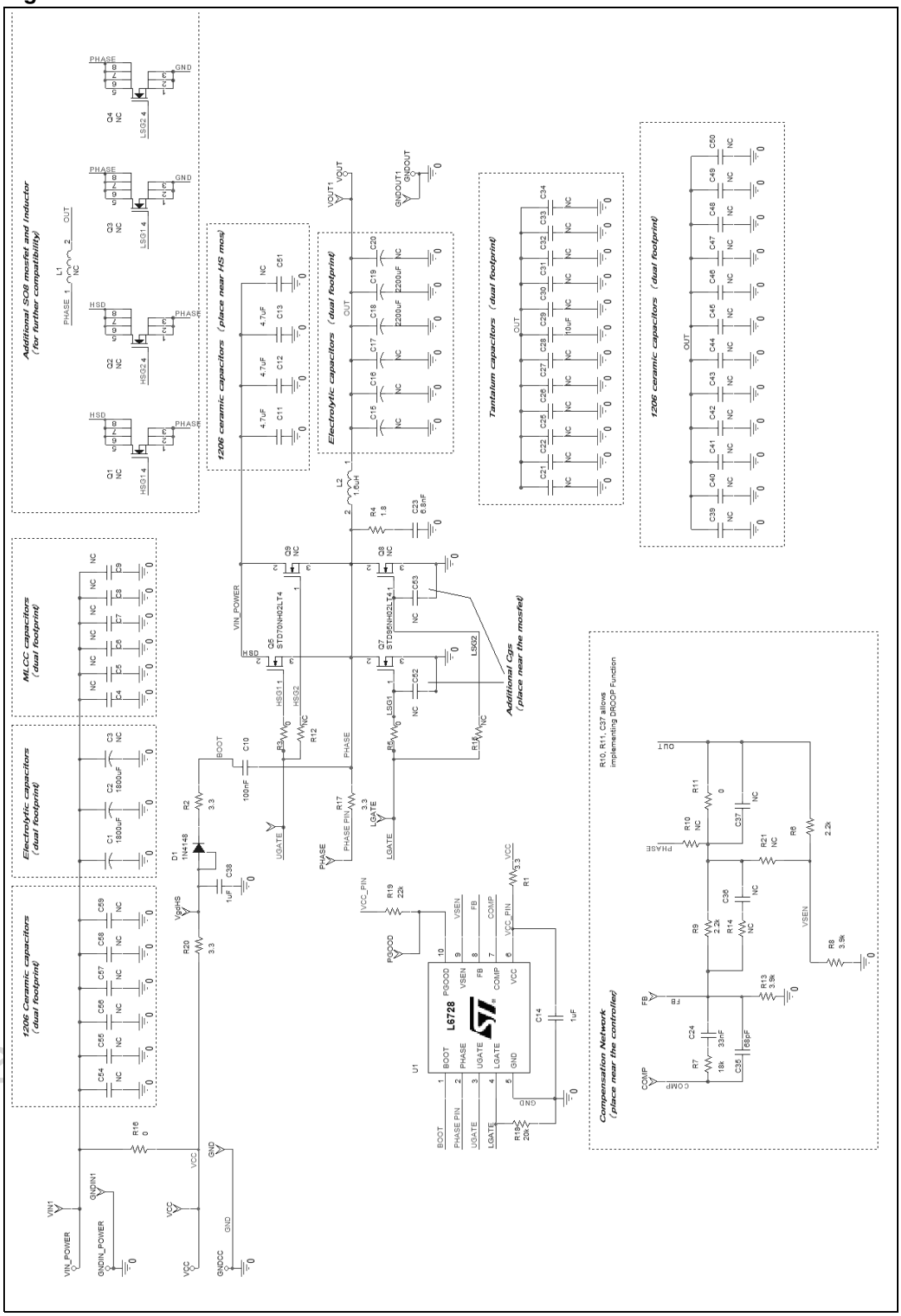


Figure 12. L6728 - 20 A demonstration board inner layers



Obsole

Figure 13. 20 A demonstration board schematic



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Table 6. 20 A demonstration board - bill of material

Qty	Reference	Description	Package
Capacitors			
2	C1, C2	Electrolytic capacitor 1800 µF 16 V Nippon chemi-con KZJ or KZG	Radial 10 x 25 mm
1	C10	MLCC, 100 nF, 16V, X7R	SMD0603
3	C11 to C13	MLCC, 4.7 µF, 16V, X5R Murata GRM31CR61C475MA01	SMD1206
2	C14, C38	MLCC, 1 µF, 16V, X7R	SMD0805
2	C15, C19	MLCC, 10 µF, 6.3 V, X7R Murata GRM31CR70J106KA01L	SMD1206
2	C18, C20	Electrolytic capacitor 2200 µF 6.3 V Nippon chemi-con KZJ or KZG	Radial 10 x 20 mm
1	C23	MLCC, 6.8 nF, X7R	SMD0603
1	C24	MLCC, 33 nF, X7R	
1	C35	MLCC, 68 pF, X7R	
Resistors			
4	R1, R2, R20, R17	Resistor, 3R3, 1/16W, 1 %	SMD0603
4	R3, R5, R11, R16	Resistor, 0R, 1/8W, 1 %	SMD0805
1	R4	Resistor, 1R8, 1/8W, 1 %	
2	R6, R9	Resistor, 2K2, 1/16W, 1 %	SMD0603
2	R8, R13	Resistor, 3K9, 1/16W, 1 %	
1	R7	Resistor, 18K, 1/16W, 1 %	
1	R19	Resistor, 22K, 1/16W, 1 %	
1	R18	Resistor, 20K, 1/16W, 1 %	
Inductor			
1	L1	Inductor, 1.25 µH, T60-18, 6 turns Easymagnet AP106019006P-1R1M	na
Active components			
1	D1	Diode, 1N4148 or BAT54	SOT23
1	Q5	STD70N02L	DPACK
1	Q7	STD95NH02LT4	
1	U1	Controller, L6728	DFN10, 3x3 mm

Obsolete Product(s) - Obsolete Product(s)

12.1 Board description

12.1.1 Power input (Vin)

This is the input voltage for the power conversion. The High-Side drain is connected to this input. This voltage can range from 1.5 V to 12 V bus.

If the voltage is between 4.5 V and 12 V it can supply also the device (through the Vcc pin) and in this case the R16 (0 Ω) resistor must be present.

12.1.2 Output (Vout)

The output voltage is fixed at 1.25 V but it can be changed by replacing the resistors R8 (sense partition lower resistor) and R13 (feedback partition lower resistor). R18 allows to adjust OCP threshold.

12.1.3 Signal input (Vcc)

Using the input voltage Vin to supply the controller no power is required at this input. However the controller can be supplied separately from the power stage through the Vcc input (4.5-12 V) and, in this case, the R16 (0 Ω) resistor must be unsoldered.

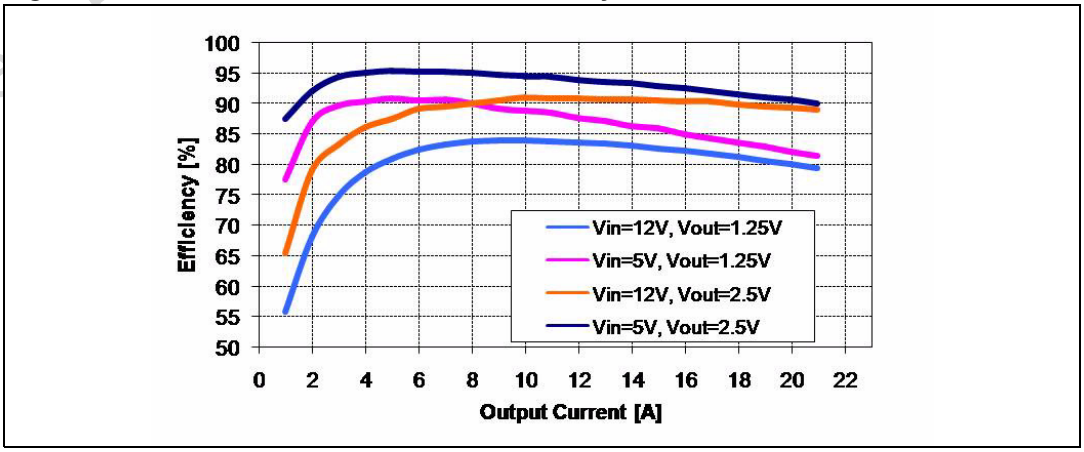
12.1.4 Test points

Several test points are provided to have easy access at all important signal characterizing the device:

- COMP: the output of the error amplifier;
- FB: the inverting input of the error amplifier;
- PGOOD: signaling the regular functioning (active high);
- VGDHS: the bootstrap diode anode;
- PHASE: Phase node;
- LGATE: Low-side gate pin of the device;
- HGATE: High-side gate pin of the device.

12.1.5 Board characterization

Figure 14. 20 A demonstration board efficiency



Obsolete Product(s) - Obsolete Product(s)

13 5 A demonstration board

L6728 demonstration board realizes in a two-layer PCB a step-down DC/DC converter and shows the operation of the device in a general-purpose low-current application. The input voltage can range from 5 V to 12 V buses and the output voltage is fixed at 1.25 V. The application can deliver an output current in excess of 5 A. The switching frequency is 300 kHz.

Figure 15. L6728 - 5 A demonstration board (left) and components placement (right)

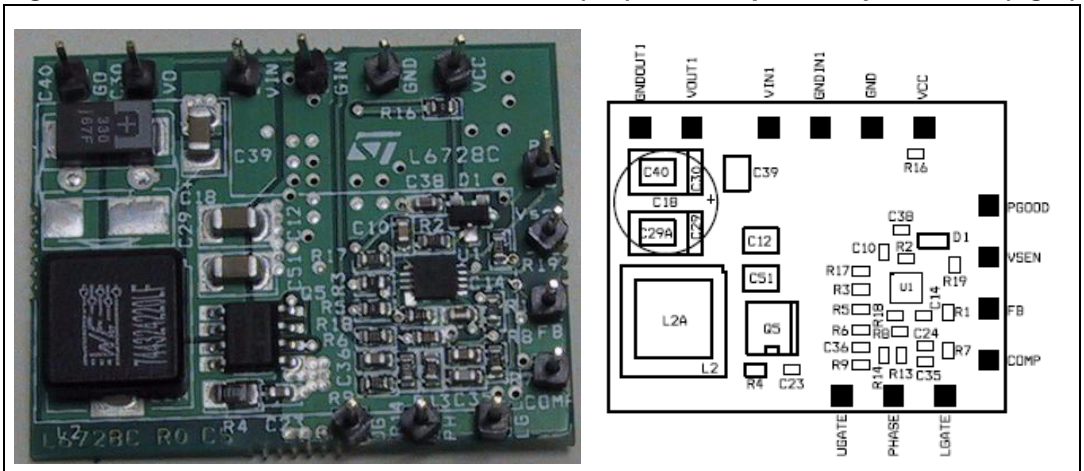
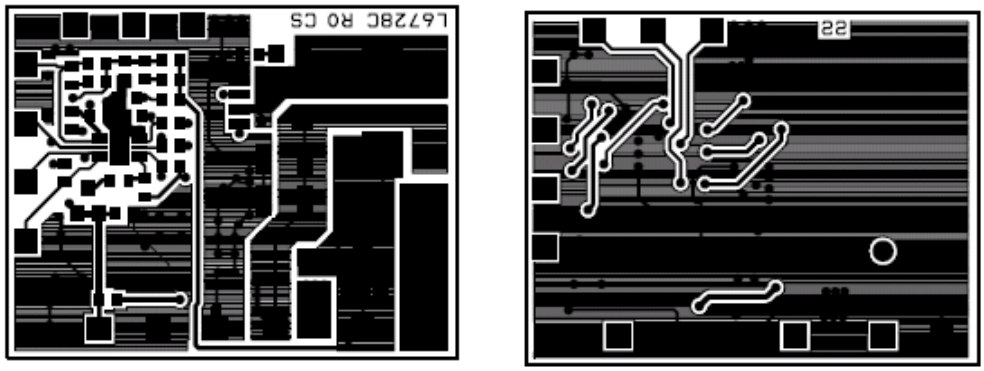
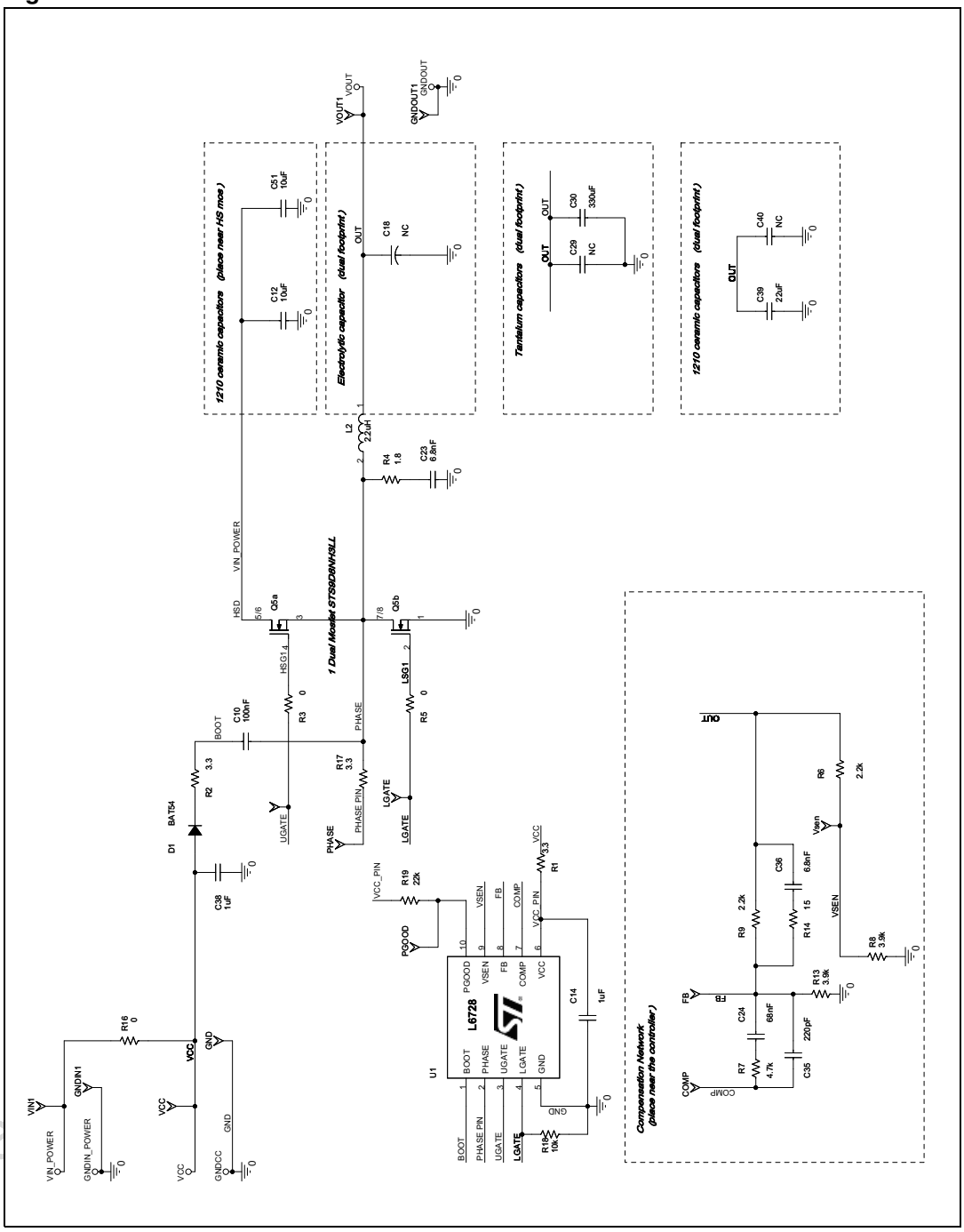


Figure 16. L6728 - 5 A demonstration board top (left) and bottom (right) layers



Obsolete Product(s)

Figure 17. 5 A demonstration board schematic



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Table 7. 5 A demonstration board - bill of material

Qty	Reference	Description	Package
Capacitors			
2	C12, C51	MLCC, 10 µF, 25 V, X5R Murata GRM31CR61E106KA12	SMD1206
1	C10	MLCC, 100 nF, 16 V, X7R	SMD0603
2	C14, C38	MLCC, 1 µF, 16 V, X7R	SMD0805
1	C39	MLCC, 22 µF, 6.3 V, X5R Murata GRM31CR60J226ME19L	SMD1206
1	C30	330 µF, 6.3 V, 9 mΩ Sanyo 6TPF330M9L	SMD7343
2	C23, C36	MLCC, 6.8 nF, X7R	SMD0603
1	C24	MLCC, 68 nF, X7R	
1	C35	MLCC, 220 pF, X7R	
Resistors			
3	R1, R2, R17	Resistor, 3R3, 1/16 W, 1 %	SMD0603
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1	R7	Resistor, 4K7, 1/16 W, 1 %	
1	R19	Resistor, 22K, 1/16 W, 1 %	
1	R18	Resistor, 10K, 1/16 W, 1 %	
Inductor			
1	L1	Inductor, 2.2 µH, WURTH 744324220LF	na
Active Components			
1	D1	Diode, BAT54	SOT23
1	Q5	STS9D8NH3LL	SO8
1	U1	Controller, L6728	DFN10, 3x3 mm

Obsolete Product(s) - Obsolete Product(s)

13.1 Board description

13.1.1 Power input (Vin)

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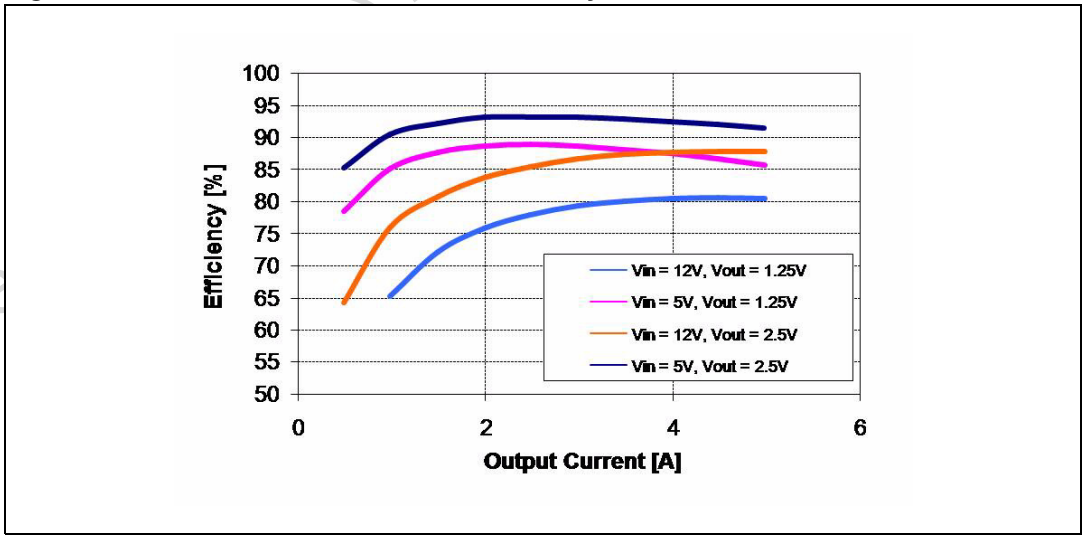
13.1.4 Test points

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- COMP: the output of the error amplifier;
- FB: the inverting input of the error amplifier;
- PGOOD: signaling the regular functioning (active high);
- VGDHS: the bootstrap diode anode;
- PHASE: Phase node;
- LGATE: Low-side gate pin of the device;
- HGATE: High-side gate pin of the device.

13.1.5 Board characterization

Figure 18. 5 A demonstration board efficiency



Obsolete Product(s)

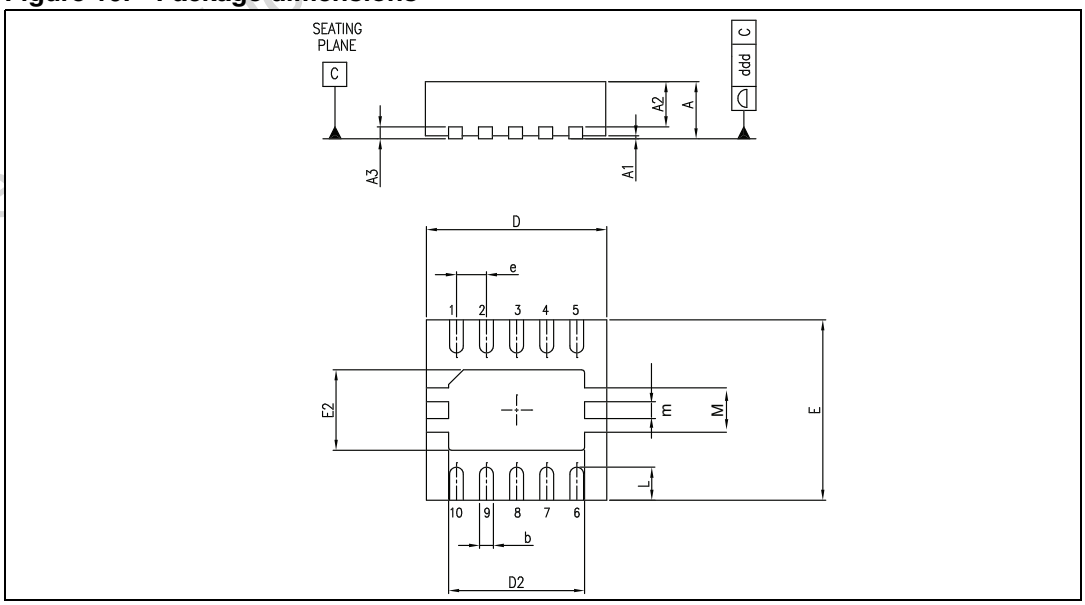
14 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 8. DFN10 mechanical data

Dim.	mm			mils		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		3.00			118.1	
D2	2.21	2.26	2.31	87.0	89.0	90.9
E		3.00			118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.3	0.4	0.5	11.8	15.7	19.7
M		0.75			29.5	
m		0.25			9.8	

Figure 19. Package dimensions



Obsolete Product(s) - Obsolete Product(s)

15 Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Jun-2007	1	Initial release
17-Sep-2007	2	Updated T_J value in *Table 3: Thermal data on page 6*
05-Jun-2008	3	Added *Figure 11 on page 21* Updated *Section 14 on page 29*, coverpage, *Table 6 on page 23*, *Figure 17 on page 26*, *Table 7 on page 27*
18-Nov-2008	4	Updated *Table 5 on page 7*

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