NCP5331

Two-Phase PWM Controller with Integrated Gate Drivers

The NCP5331 is a second−generation, two−phase, buck controller that incorporates advanced control functions to power 64−bit AMD Athlon™ processors and low voltage, high current power supplies. Proprietary multiphase architecture guarantees balanced load−current sharing, reduces output voltage and input current ripple, decreases filter requirements and inductor values, and increases output current slew rate. Traditional Enhanced V^{2}™ has been combined with an internal PWM ramp and voltage feedback directly from V_{CORE} to the internal PWM comparator. These features and enhancements deliver the fastest transient response, reduce output voltage jitter, provide greater design flexibility and portability, and minimize overall solution cost.

Advanced features include adjustable power−good delay, programmable overcurrent shutdown timer, superior overvoltage protection (OVP), and differential remote sensing. An innovative overvoltage protection (OVP) scheme safeguards the CPU during extreme situations including power up with a shorted upper MOSFET, shorting of an upper MOSFET during normal operation, and loss of the voltage feedback signal, COREFB+.

Features

- Reduced SMT Package Size (7 mm × 7 mm)
- Enhanced V^{2} Control Method
- Four On−Board Gate Drivers
- Internal PWM Ramps
- Differential Remote Voltage Sense
- Fast Feedback Pin (V_{FFB})
- 5−Bit DAC with 0.8% System Tolerance
- Timed Hiccup Mode Current Limit
- Power Good Output with Programmable Delay
- Advanced Overvoltage Protection (OVP)
- Adjustable Output Voltage Positioning
- 150 kHz to 600 kHz Operation Set by Resistor
- “Lossless” Current Sensing through Output Inductors
- Independent Current Sense Amplifiers
- 5.0 V, 2 mA Reference Output
- Pb−Free Package is Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

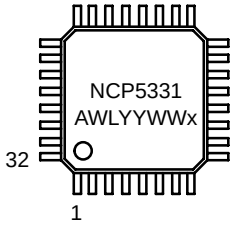
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LQFP−32
FT SUFFIX
CASE 873A

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
x = G or ▪

*Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

ORDERING INFORMATION

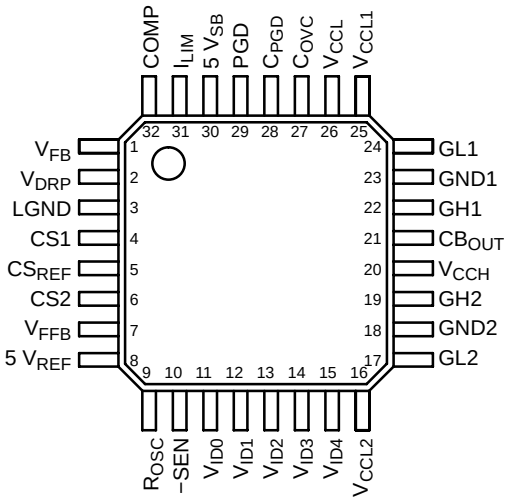
Device	Package	Shipping†
NCP5331FTR2	LQFP−32	2000 Tape & Reel
NCP5331FTR2G	LQFP−32 (Pb−Free)	2000 Tape & Reel

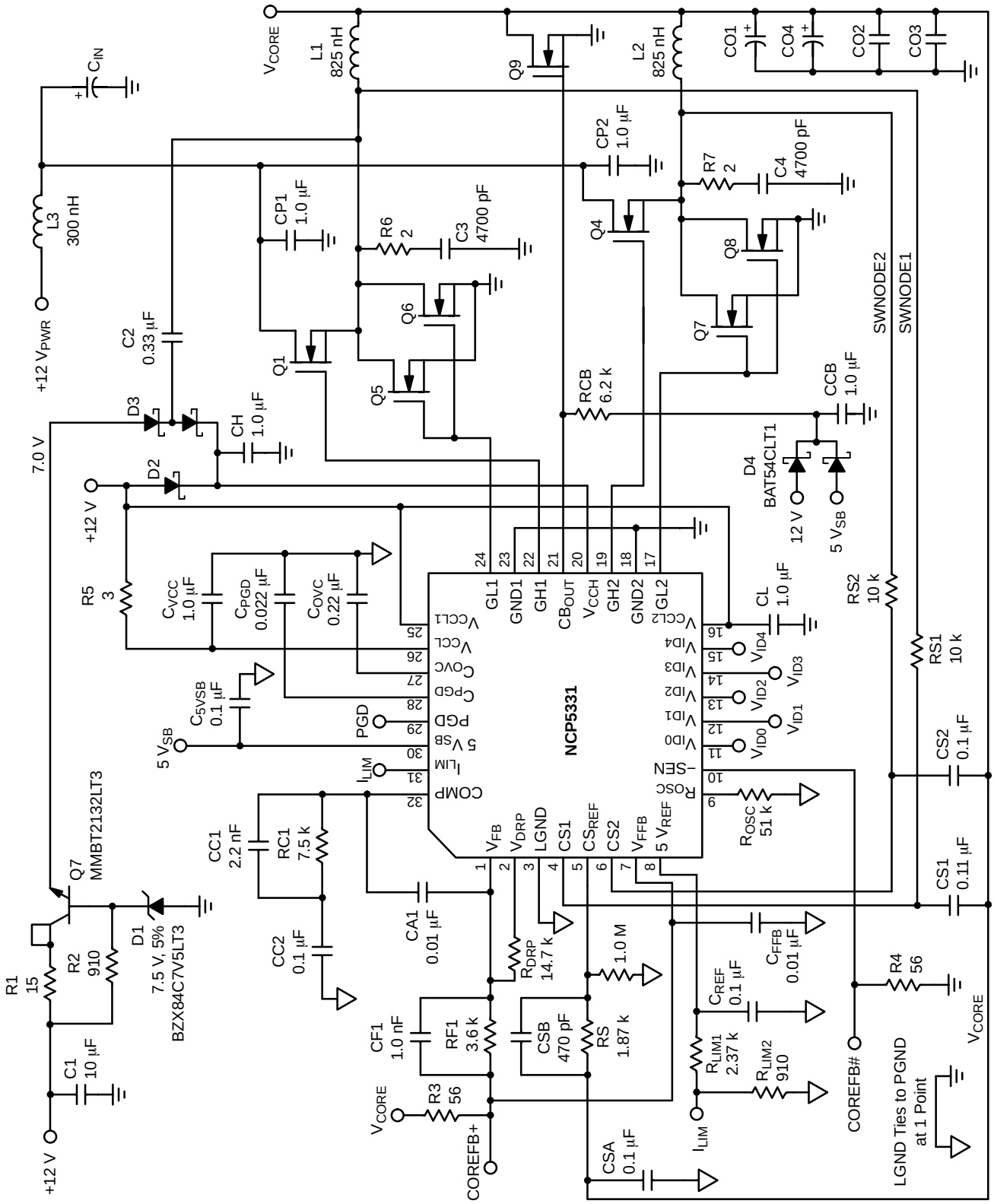
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PIN CONNECTIONS

LQFP−32





Recommended Components:

Q1, Q4: ON Semiconductor NTD60N03 (60 A, 28 V, 6.1 mΩ)
Q5–Q9: ON Semiconductor NTD80N02 (80 A, 24 V, 5.0 mΩ)
L1, L2: Coiltronics CTX22−15274 or T50−8B/90 w/ 6 T of #16 AWG Bifilar (1 mΩ)
L3: Coiltronics CTX15−14771 or T30−26 w/ 3 T of #16 AWG
C_{IN}: 5 × Rubycon 16MBZ1500M10X20 (1500 µF, 16 V, 2.55 A_{RMS})
CO1: 10 × Rubycon 16MBZ1000M10X16 (1000 µF, 16 V, 19 mΩ)
CO2: 24 × TDK C2012X5R0J106M (10 µF, 6.3 V, 0805)
CO3: 16 × TDK C1608X5R1A224KT (0.22 F, 10 V, 0603)
CO4: 2 × Sanyo PosCAP 6TPD330M (330 µF, 6.3 V, 10 mΩ, 4.4 A_{RMS})

Figure 1. Application Diagram, 12 V to 1.2 V at 52 A, 200 kHz for 64−Bit AMD Athlon Processor

MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature	150	°C
Lead Temperature Soldering SMD Reflow Profile (60 seconds maximum)	230 183	°C peak °C
Storage Temperature Range	−65 to 150	°C
Package Thermal Resistance: Junction−to−Ambient, $R_{\theta JA}$	52	°C/W
ESD Susceptibility (Human Body Model)	2.0	kV
JEDEC Moisture Sensitivity	TBD	−

*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP	6.0 V	−0.3 V	1.0 mA	1.0 mA
V_{FB}	6.0 V	−0.3 V	1.0 mA	1.0 mA
V_{DRP}	6.0 V	−0.3 V	1.0 mA	1.0 mA
CS1, CS2	6.0 V	−0.3 V	1.0 mA	1.0 mA
CS_{REF}	6.0 V	−0.3 V	1.0 mA	1.0 mA
R_{OSC}	6.0 V	−0.3 V	1.0 mA	1.0 mA
PGD	6.0 V	−0.3 V	1.0 mA	8.0 mA
VID Pins	6.0 V	−0.3 V	1.0 mA	1.0 mA
I_{LIM}	6.0 V	−0.3 V	1.0 mA	1.0 mA
5 V_{REF}	6.0 V	−0.3 V	1.0 mA	20 mA
CB_{OUT}	13.2 V	−0.3 V	1.0 mA	4.0 mA
C_{PGD}	6.0 V	−0.3 V	1.0 mA	1.0 mA
C_{OVC}	6.0 V	−0.3 V	1.0 mA	1.0 mA
V_{CCL}	16 V	−0.3 V	N/A	50 mA
V_{CCH}	20 V	−0.3 V	N/A	1.5 A for 1.0 μs, 200 mA dc
V_{CCLx}	16 V	−0.3 V	N/A	1.5 A for 1.0 μs, 200 mA dc
5 V_{SB}	6.0 V	−0.3 V	N/A	1.0 mA
GHx	20 V	−2.0 V for 100 ns, −0.3 V dc	1.5 A for 1.0 μs, 200 mA dc	1.5 A for 1.0 μs, 200 mA dc
GLx	16 V	−2.0 V for 100 ns, −0.3 V dc	1.5 A for 1.0 μs, 200 mA dc	1.5 A for 1.0 μs, 200 mA dc
GND1, GND2	0.3 V	−0.3 V	2.0 A for 1.0 μs, 200 mA dc	N/A
LGND	0 V	0 V	50 mA	N/A
−SEN	0.3 V	−0.3 V	1.0 mA	1.0 mA

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $9.0\ V < V_{CCL} < 16\ V$; $9.0\ V < V_{CCH} < 20\ V$; $9.0\ V < V_{CCL1} = V_{CCL2} < 14\ V$; $C_{GATE} = 3.3\ nF$, $R_{ROSC} = 32.4\ k\Omega$, $C_{COMP} = 1.0\ nF$, $C_{5V(REF)} = 0.1\ \mu F$, DAC Code 01110 (1.2 V), $C_{VCC} = 1.0\ \mu F$, $0.25\ V \le I_{LIM} \le 1.0\ V$; unless otherwise noted)

Characteristic					Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC									
Voltage Identification (VID) Codes					Measure V_{FB} = COMP, −SEN = LGND				
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}					
0	0	0	0	0	−	−	1.550	−	V
0	0	0	0	1	−	−	1.525	−	V
0	0	0	1	0	−	−	1.500	−	V
0	0	0	1	1	−	−	1.475	−	V
0	0	1	0	0	−	−	1.450	−	V
0	0	1	0	1	−	−	1.425	−	V
0	0	1	1	0	−	−	1.400	−	V
0	0	1	1	1	−	−	1.375	−	V
0	1	0	0	0	−	−	1.350	−	V
0	1	0	0	1	−	−	1.325	−	V
0	1	0	1	0	−	−	1.300	−	V
0	1	0	1	1	−	−	1.275	−	V
0	1	1	0	0	−	−	1.250	−	V
0	1	1	0	1	−	−	1.225	−	V
0	1	1	1	0	−	−	1.200	−	V
0	1	1	1	1	−	−	1.175	−	V
1	0	0	0	0	−	−	1.150	−	V
1	0	0	0	1	−	−	1.125	−	V
1	0	0	1	0	−	−	1.100	−	V
1	0	0	1	1	−	−	1.075	−	V
1	0	1	0	0	−	−	1.050	−	V
1	0	1	0	1	−	−	1.025	−	V
1	0	1	1	0	−	−	1.000	−	V
1	0	1	1	1	−	−	0.975	−	V
1	1	0	0	0	−	−	0.950	−	V
1	1	0	0	1	−	−	0.925	−	V
1	1	0	1	0	−	−	0.900	−	V
1	1	0	1	1	−	−	0.875	−	V
1	1	1	0	0	−	−	0.850	−	V
1	1	1	0	1	−	−	0.825	−	V
1	1	1	1	0	−	−	0.800	−	V
1	1	1	1	1	−	Shutdown			V
System Accuracy					Percent deviation from programmed VID codes	−0.8	−	0.8	%
Shutdown Time Delay					VID = 11111	5.0	10	15	μs
Input Threshold					V_{ID0}–V_{ID4}	1.00	1.25	1.50	V
VID Pin Bias Current					V_{ID0}–V_{ID4}	12	25	40	μA
VID Pin Clamp Voltage					−	−	2.3	2.6	V

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $9.0\ V < V_{CCL} < 16\ V$; $9.0\ V < V_{CCH} < 20\ V$; $9.0\ V < V_{CCL1} = V_{CCL2} < 14\ V$; $C_{GATE} = 3.3\ nF$, $R_{ROSC} = 32.4\ k\Omega$, $C_{COMP} = 1.0\ nF$, $C_{5V(REF)} = 0.1\ \mu F$, DAC Code 01110 (1.2 V), $C_{VCC} = 1.0\ \mu F$, $0.25\ V \le I_{LIM} \le 1.0\ V$; unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC (continued)					
−SEN Bias Current	LGND < 55 mV, All DAC Codes	40	80	120	μA
−SEN Offset from GND	−	−150	−	200	mV
Power Good Output					
Internal Delay Time	−	175	290	425	μs
PWRGD Low Output Voltage	$I_{PGD} = 4.0\ mA$	−	250	400	mV
Output Leakage Current	$V_{PGD} = 5.5\ V$	−	0.1	2.0	μA
V_{CORE}/CS_{REF} Comparator Threshold Voltage	Tolerance from DAC Setting	−15%	−12.5%	−10%	%
C_{PGD} Charge Current	$R_{OSC} = 32.4\ k\Omega$	14.5	16	17.5	μA
C_{PGD} Comparator Threshold Voltage	−	2.8	3.0	3.2	V
C_{PGD} External Delay Time	$C_{PGD} = 0.033\ \mu F$. Note 1.	4.8	6.0	7.8	ms
Voltage Feedback Error Amplifier					
V_{FB} Bias Current	$0.7\ V < V_{FB} < 1.6\ V$. Note 2.	9.4	10.3	11.1	μA
COMP Source Current	COMP = 0.5 V to 2.0 V; $V_{FB} = 0.8\ V$	15	30	60	μA
COMP Sink Current	COMP = 0.5 V to 2.0 V; $V_{FB} = 1.5\ V$	15	30	60	μA
COMP Discharge Threshold Voltage	−	0.20	0.33	0.40	V
Transconductance	$-10\ \mu A < I_{COMP} < +10\ \mu A$	−	32	−	mmho
Output Impedance	−	−	2.5	−	MΩ
Open Loop Dc Gain	Note 1.	60	90	−	dB
Unity Gain Bandwidth	$C_{COMP} = 0.01\ \mu F$	−	400	−	kHz
PSRR @ 1.0 kHz	−	−	70	−	dB
COMP Max Voltage	$V_{FB} = 0.8\ V$, COMP Open	4.1	4.4	−	V
COMP Min Voltage	$V_{FB} = 1.5\ V$, COMP Open	−	0.1	0.2	V
Hiccup Latch Discharge Current	−	4.0	7.5	13	μA
Hiccup Latch Charge/Discharge Ratio	−	−	4.0	−	−
PWM Comparators					
Minimum Pulse Width	$CS1 = CS2 = CS_{REF}$	−	235	280	ns
Channel Start−Up Offset	$CS1 = CS2 = V_{FB} = CS_{REF} = 0\ V$; Measure COMP when GHx switch High	0.45	0.60	0.80	V
Overcurrent Shutdown Timer					
Overcurrent Shutdown Voltage Threshold	−	2.8	3.0	3.2	V
C_{OVC} Low Output Voltage	−	−	250	400	mV
C_{OVC} Source Current	−	3.0	5.0	8.0	μA

1. Guaranteed by design. Not tested in production.
2. The V_{FB} Bias Current changes with the value of R_{OSC} per Figure 5.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $9.0\ V < V_{CCL} < 16\ V$; $9.0\ V < V_{CCH} < 20\ V$; $9.0\ V < V_{CCL1} = V_{CCL2} < 14\ V$; $C_{GATE} = 3.3\ nF$, $R_{ROSC} = 32.4\ k\Omega$, $C_{COMP} = 1.0\ nF$, $C_{5V(REF)} = 0.1\ \mu F$, DAC Code 01110 (1.2 V), $C_{VCC} = 1.0\ \mu F$, $0.25\ V \le I_{LIM} \le 1.0\ V$; unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Overcurrent Shutdown Timer (continued)					
Overcurrent Shutdown Time	$C_{OVC} = 0.22\ \mu F$. Note 3.	65	120	230	ms
Internal Overvoltage Protection (OVP)					
Overvoltage Threshold	LGND = 0 V, V_{FB} = 0 V, CS_{REF} = 0 V, Increase CS_{REF} until GL1 and GL2 switch High.	2.0	2.1	2.2	V
External Overvoltage Protection (CB_{OUT})					
Overvoltage Positive Threshold	5 V_{SB} = 5.0 V, LGND = 0 V, CS_{REF} = 0 V, Increase CS_{REF} until CB_{OUT} = High.	2.0	2.1	2.2	V
Overvoltage Negative Threshold	5 V_{SB} = 5.0 V, LGND = 0 V, CS_{REF} = 3.0 V, Decrease CS_{REF} until CB_{OUT} = Low.	0.8	0.9	1.0	V
CB_{OUT} Maximum Allowable Sink Current	–	–	–	2.0	mA
CB_{OUT} Low Voltage	6.6 kΩ Pull−Up to 13.2 V	–	–	0.4	V
GATE DRIVERS					
High Voltage (AC)	Measure V_{CCLx} − GLx or V_{CCHx} − GHx. Note 3.	–	0	1.0	V
Low Voltage (AC)	Measure GLx $_{or}$ GHx. Note 3.	–	0	0.5	V
Rise Time GHx	1.0 V < GHx < 8.0 V; V_{CCH} = 10 V	–	35	80	ns
Rise Time GLx	1.0 V < GLx < 8.0 V; V_{CCLx} = 10 V	–	35	80	ns
Fall Time GHx	8.0 V > GHx > 1.0 V; V_{CCH} = 10 V	–	35	80	ns
Fall Time GLx	8.0 V > GLx > 1.0 V; V_{CCLx} = 10 V	–	35	80	ns
GHx to GLx Delay	GHx < 2.0 V, GLx > 2.0 V	30	65	110	ns
GLx to GHx Delay	GLx < 2.0 V, GHx > 2.0 V	30	65	110	ns
GATE Pull−Down	Force 100 μA into GATE with no power applied to V_{CCH} and V_{CCLx} = 2.0 V.	–	1.2	1.6	V
Oscillator					
Switching Frequency	R_{OSC} = 32.4 k	255	300	345	kHz
Switching Frequency	R_{OSC} = 63.4 k; Note 3.	110	150	190	kHz
Switching Frequency	R_{OSC} = 16.2 k; Note 3.	450	600	750	kHz
R_{OSC} Voltage	–	–	1.0	–	V
Phase Delay	–	165	180	195	deg
Adaptive Voltage Positioning					
V_{DRP} Output Voltage to DAC_{OUT} Offset	CS1 = CS2 = CS_{REF}, V_{FB} = COMP, Measure V_{DRP} − COMP		6		mV
Maximum V_{DRP} Voltage	10 mV ≤ (CS1 = CS2) − CS_{REF} ≤ 50 mV, V_{FB} = COMP, Measure V_{DRP} − COMP	300	400	500	mV
Current Sense Amp to V_{DRP} Gain	10 mV ≤ (CS1 = CS2) − CS_{REF} ≤ 50 mV V_{FB} = COMP, Measure V_{DRP} − COMP	3.9	4.2	4.75	V/V

3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $9.0\ V < V_{CCL} < 16\ V$; $9.0\ V < V_{CCH} < 20\ V$; $9.0\ V < V_{CCL1} = V_{CCL2} < 14\ V$; $C_{GATE} = 3.3\ nF$, $R_{ROSC} = 32.4\ k\Omega$, $C_{COMP} = 1.0\ nF$, $C_{5V(REF)} = 0.1\ \mu F$, DAC Code 01110 (1.2 V), $C_{VCC} = 1.0\ \mu F$, $0.25\ V \le I_{LIM} \le 1.0\ V$; unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Current Sensing					
CS1−CS2 Input Bias Current	$CSx = CS_{REF} = 0\ V$	−	0.1	0.5	μA
CS_{REF} Input Bias Current	$CSx - CS_{REF} = 50\ mV$	−	0.35	1.5	μA
V_{FFB} Pull−Up Resistor	−	80	110	145	kΩ
Current Sense Amplifier Gain	$CSx - CS_{REF} = 40\ mV$	1.85	2.1	2.35	V/V
Current Sense Input to I_{LIM} Gain	$I_{LIM} = 1.00\ V$	9.5	12	14	V/V
Current Limit Filter Slew Rate	−	4.0	7.0	13	mV/μs
I_{LIM} Operating Voltage Range	Note 4.	−	−	3.0	V
I_{LIM} Bias Current	$0 < I_{LIM} < 1.0\ V$	−	0.1	1.0	μA
Current Sense Amplifier Bandwidth	Note 4.	1.0	−	−	MHz
General Electrical Specifications					
V_{CCL} Operating Current	V_{FB} = COMP (no switching)	−	22	26	mA
V_{CCL1} or V_{CCL2} Operating Current	V_{FB} = COMP (no switching)	−	5.0	10	mA
V_{CCH} Operating Current	V_{FB} = COMP (no switching)	−	6.4	9.0	mA
5 V_{SB} Quiescent Current	CB_{OUT} = Low	−	−	400	μA
V_{CCL} Start Threshold	GATEs switching, COMP charging	8.1	8.5	8.9	V
V_{CCL} Stop Threshold	GATEs stop switching, COMP discharging	5.75	6.15	6.55	V
V_{CCL} Hysteresis	GATEs not switching, COMP not charging	2.05	2.35	2.65	V
V_{CCH} Start Threshold	GATEs switching, COMP charging	8.1	8.5	8.9	V
V_{CCH} Stop Threshold	GATEs stop switching, COMP discharging	6.35	6.75	7.15	V
V_{CCH} Hysteresis	GATEs not switching, COMP not charging	1.45	1.75	2.05	V
Reference Output					
5 V_{REF} Output Voltage	$0\ mA < I(5\ V_{REF}) < 1.0\ mA$	4.85	5.0	5.15	V
Internal Ramp					
Ramp Height @ 50% PWM Duty Cycle	$CS1 = CS2 = CS_{REF}$	−	125	−	mV

4. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{FB}	Voltage Feedback Pin. To use Adaptive Voltage Positioning (AVP), set the light load offset voltage by connecting a resistor between V_{FB} and V_{CORE}. The resistor and the V_{FB} bias current determine the offset. For no adaptive positioning connect V_{FB} directly to V_{CORE}.
2	V_{DRP}	Current sense output for Adaptive Voltage Positioning (AVP). The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to V_{FB} to set the amount AVP or leave this pin open for no AVP. This pin's maximum working voltage is 4.1 Vdc.
3	LGND	Return for the internal control circuits and the IC substrate connection.
4, 6	CS1, CS2	Current sense inputs. Connect the current sense network for the corresponding phase to each input. The input voltages to these pins must be kept within 125 mV of CS_{REF}.
5	CS_{REF}	Reference for both differential current sense amplifiers. To balance input offset voltages between the inverting and non−inverting inputs of the Current Sense Amplifiers, connect this pin to the output voltage through a resistor equal to one third of the value of the current sense resistors.
7	V_{FFB}	Fast Feedback connection to the PWM comparators and input to the Power Good comparator.
8	5 V_{REF}	Reference output. Decouple to LGND with 0.1 μF.
9	R_{OSC}	A resistor from this pin to ground sets the operating frequency and V_{FB} bias current.
10	−SEN	Ground connection for the DAC. Provides remote sensing of ground at the load.
11−15	VID pins	Voltage ID DAC inputs. These pins are internally pulled up and clamped at 2.3 V if left unconnected.
16	V_{CCL2}	Power for GL2.
17	GL2	Low side driver #2.
18	GND2	Return for driver #2.
19	GH2	High side driver #2.
20	V_{CCH}	Power for GH1 and GH2.
21	CB_{OUT}	Open−collector crowbar output pin. This pin is high impedance when an overvoltage condition is detected at CS_{REF}. Connect this pin to the gate of a MOSFET or SCR to crowbar either V_{CORE} or V_{IN} to GND. To prevent failure of the crowbar device, this pin should be used in conjunction with logic on the motherboard to disable the ATX supply via PS_{ON} and/or a relatively fast fuse should be placed upstream to disconnect the input voltage.
22	GH1	High side driver #1.
23	GND1	Return for driver #1.
24	GL1	Low side driver #1.
25	V_{CCL1}	Power for GL1.
26	V_{CCL}	Power for the internal control circuits. UVLO sense for Logic connects to this pin.
27	C_{OVC}	A capacitor from this pin to ground sets the time the controller will be in hiccup mode current limit. This timer is started by the first overcurrent condition (set by the I_{LIM} voltage). Once timed out, voltage at the V_{CCL} pin must be cycled to reset this fault. Connecting this pin to LGND ±200 mV will disable this function and hiccup mode current limit will operate indefinitely.
28	C_{PGD}	A capacitor from this pin to ground sets the programmable time between when V_{CORE} crosses the PWRGD threshold and when the open−collector PWRGD pin transitions from a logic Low to a logic High. The minimum delay is internally set to 200 μs. Connecting this pin to 5 V_{REF} will disable the programmable timer and the delay will be set to the internal delay.
29	PGD	Power Good output. Open collector output that will transition Low when CS_{REF} (V_{CORE}) is out of regulation.
30	5 V_{SB}	Input power for the CB_{OUT} circuitry. To provide maximum overvoltage protection to the CPU, this pin should be connected to 5 V_{SB} from the ATX supply (ATX, pin 9). If the CB_{OUT} function is not used, this pin must be connected to the NCP5331 controller's internal voltage reference (5 V_{REF}, pin 8).
31	I_{LIM}	Sets the threshold for current limit. Connect to reference through a resistive divider. This pin's maximum working voltage is 3.0 Vdc.
32	COMP	Output of the error amplifier and input for the PWM comparators.

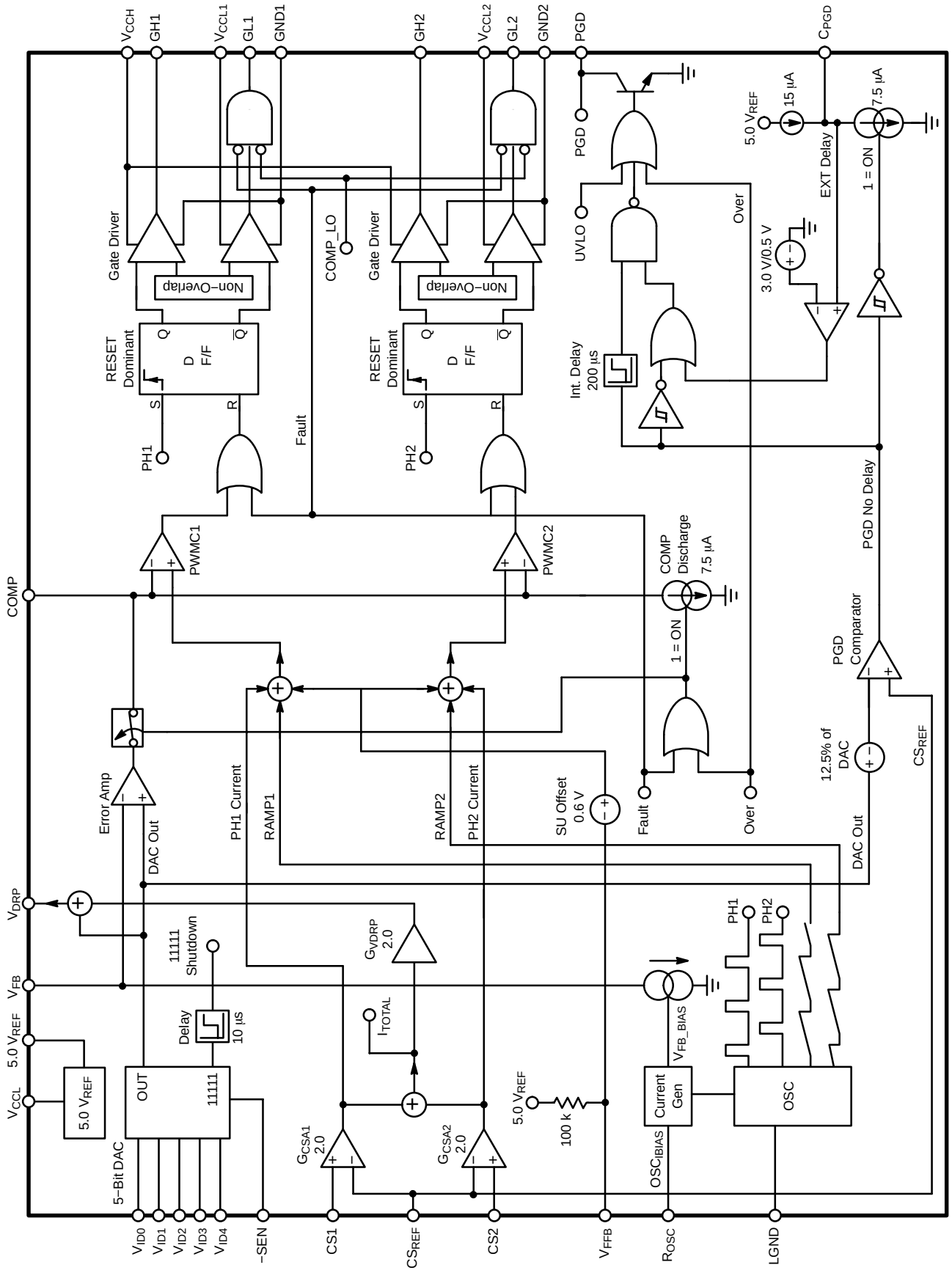


Figure 2. Block Diagram, Control Functions

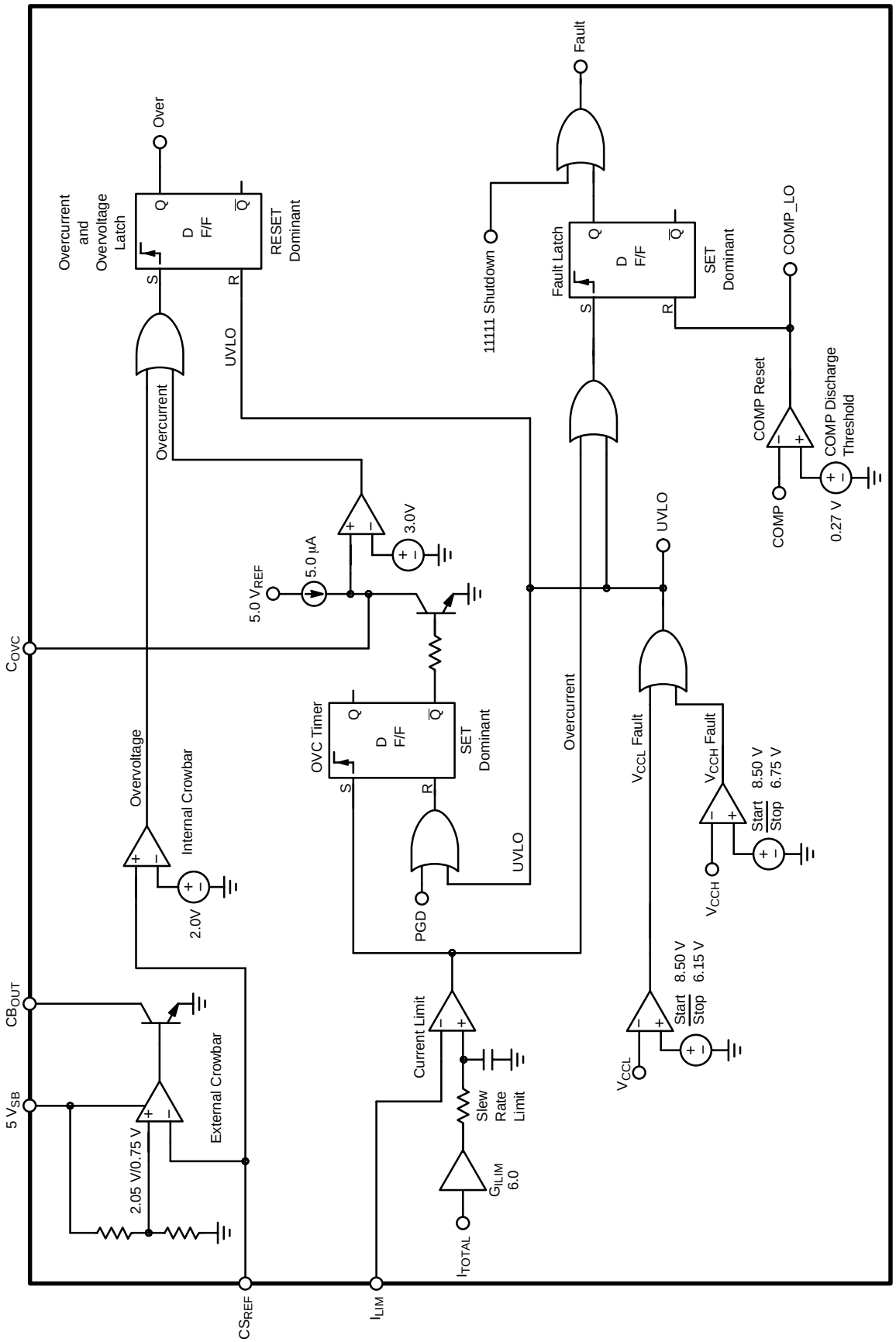


Figure 3. Block Diagram, Protection

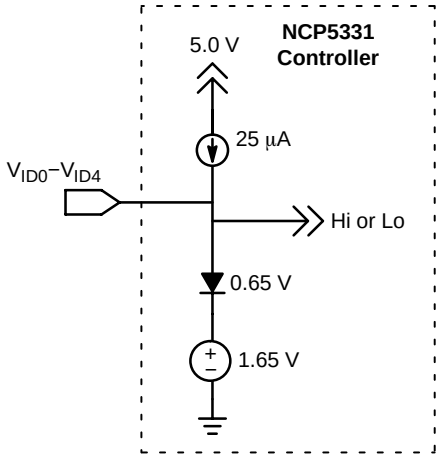


Figure 4. Simplified VID Pin Input Circuitry

TYPICAL PERFORMANCE CHARACTERISTICS

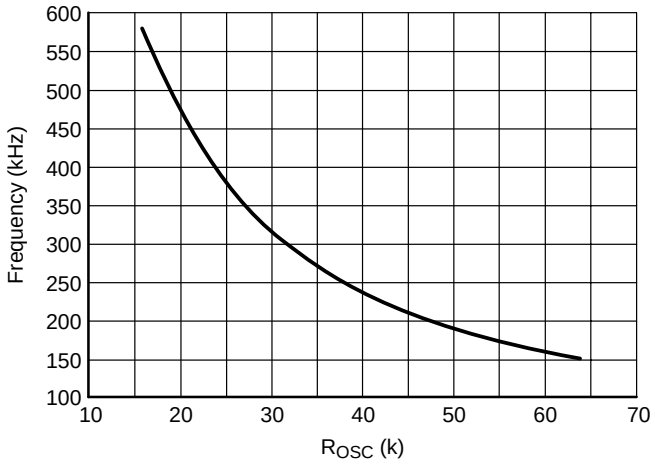


Figure 5. Oscillator Frequency vs. R_{OSC} Value

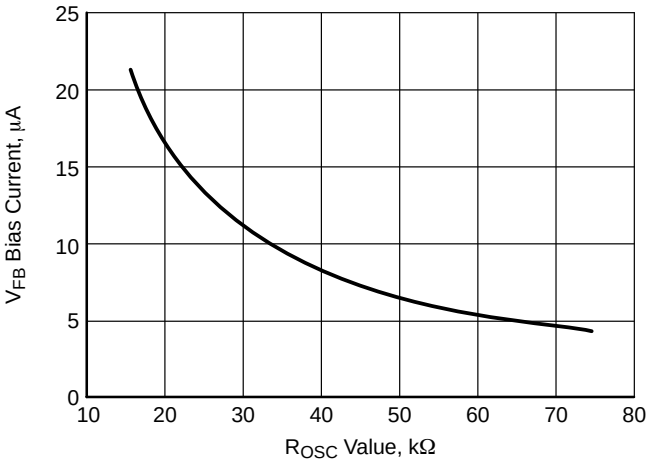


Figure 6. V_{FB} Current vs. R_{OSC} Value

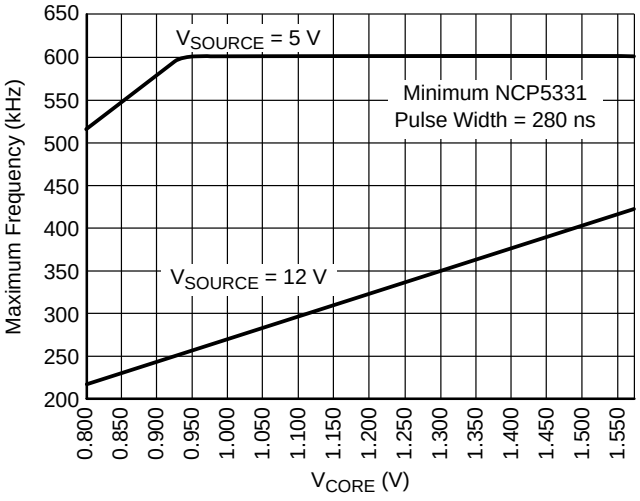


Figure 7. Maximum Frequency vs. V_{CORE}

TYPICAL PERFORMANCE CHARACTERISTICS

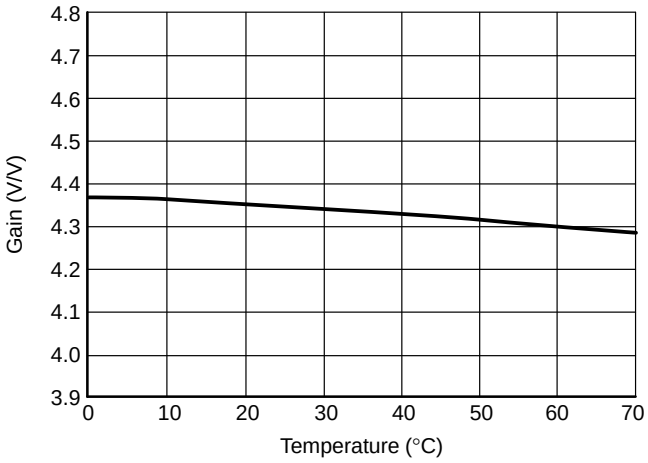


Figure 8. CSA to V_{DRP} Gain vs. Temperature

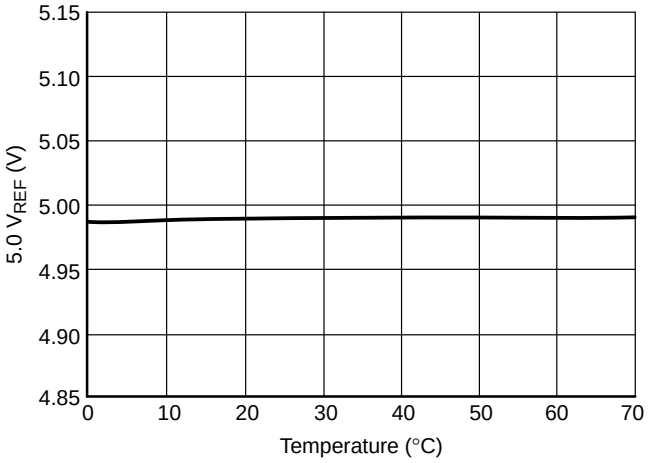


Figure 9. 5.0 V_{REF} Output Voltage vs. Temperature

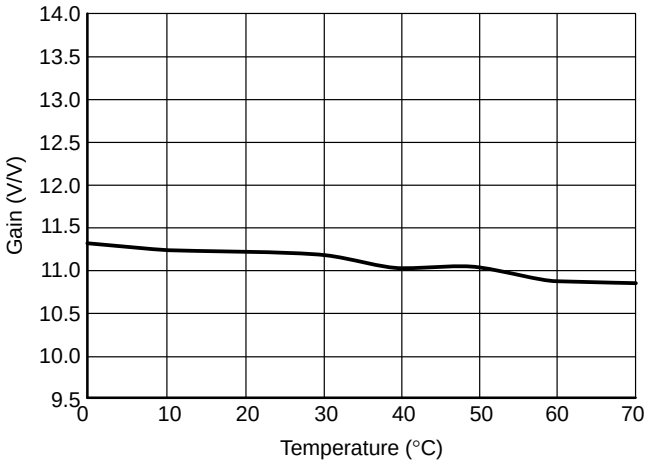


Figure 10. CSA to I_{LIM} Gain vs. Temperature

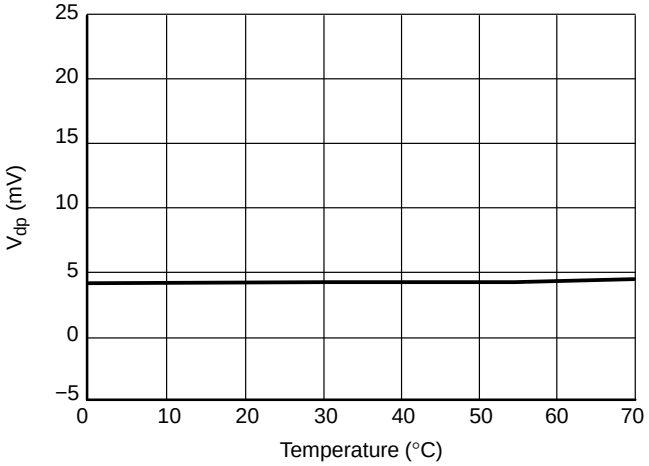


Figure 11. V_{DRP} Output to DAC_{OUT} Offset vs. Temperature

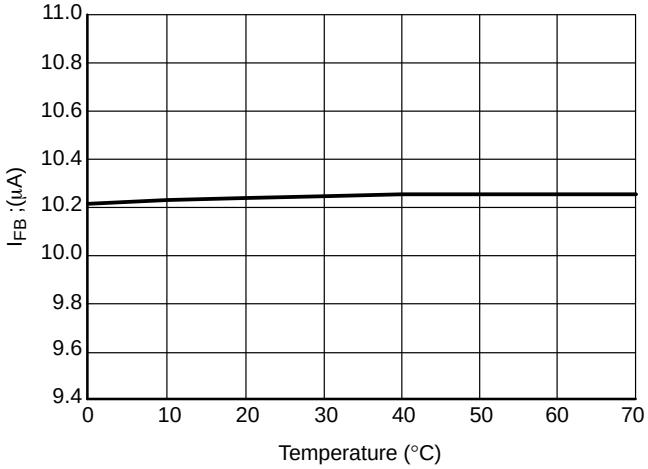


Figure 12. V_{FB} Bias Current vs. Temperature

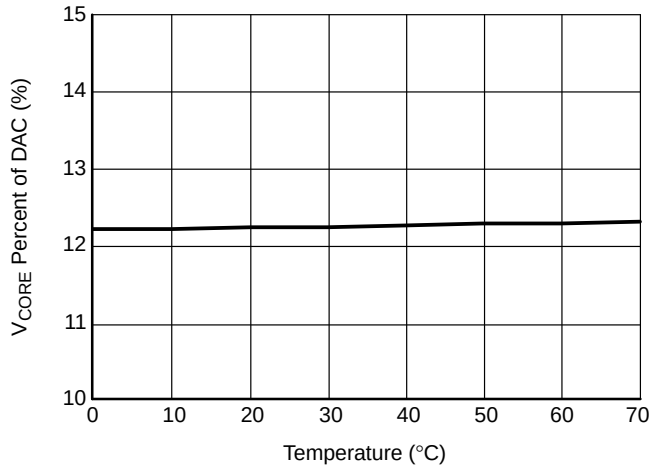


Figure 13. PGD Threshold vs. Temperature

APPLICATIONS INFORMATION

Overview

The NCP5331 dc/dc controller utilizes an Enhanced V^2 topology to meet requirements of low voltage, high current loads with fast transient requirements. Transient response has been improved and voltage jitter virtually eliminated by including an internal PWM ramp, connecting fast−feedback from V_{CORE} directly to the internal PWM comparator, and precise routing and grounding inside the controller. Advanced features such as adjustable power−good delay, programmable overcurrent shutdown time, superior overvoltage protection (OVP), and differential remote voltage sensing make it easy to obtain AMD certification. An innovative overvoltage protection (OVP) scheme safeguards the CPU during extreme situations including power up with a shorted upper MOSFET, shorting of an upper MOSFET during normal operation, and loss of the voltage feedback signal, COREFB+. The NCP5331 provides a “fully integrated solution” to simplify design, minimize circuit board area, and reduce overall system cost.

Two advantages of a multiphase converter over a single−phase converter are current sharing and increased apparent output frequency. Current sharing allows the designer to use less inductance in each phase than would be required in a single−phase converter. The smaller inductor produces larger ripple currents but the total per phase power dissipation is reduced because the rms current is lower. Transient response is improved because the control loop will measure and adjust the current faster in a smaller output inductor. Increased apparent output frequency is desirable because the off−time and the ripple voltage of the two−phase converter will be less than that of a single−phase converter.

Fixed Frequency Multiphase Control

In a multiphase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The NCP5331 controller uses a two−phase, fixed frequency, Enhanced V^2 architecture to measure and control currents in individual phases. Each phase is delayed 180° from the previous phase. Normally, GHx (x = 1 or 2) transitions to a high voltage at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal, the internal ramp and the output voltage ripple trip the PWM comparator and bring GHx low. Once GHx goes low, it will remain low until the beginning of the next oscillator cycle. While GHx is high, the Enhanced V^2 loop will respond to line and load variations (i.e. the upper gate on−time will be increased or reduced as required). On the other hand, once GHx is low, the loop can not respond until the beginning of the next PWM cycle. Therefore, constant frequency Enhanced V^2 will typically respond to disturbances within the off−time of the converter.

The Enhanced V^2 architecture measures and adjusts the output current in each phase. An additional input, CSx (x = 1 or 2), for inductor current information has been added to the V^2 loop for each phase as shown in Figure 14. The triangular inductor current is measured differentially across RS, amplified by CSA and summed with the Channel Startup Offset, the Internal Ramp, and the Output Voltage at the noninverting input of the PWM comparator. The purpose of the Internal Ramp is to compensate for propagation delays in the NCP5331. This provides greater design flexibility by allowing smaller external ramps, lower minimum pulse widths, higher frequency operation, and PWM duty cycles above 50% without external slope compensation. As the sum of the inductor current and the internal ramp increase, the voltage on the positive pin of the PWM comparator rises and terminates the PWM cycle. If the inductor starts a cycle

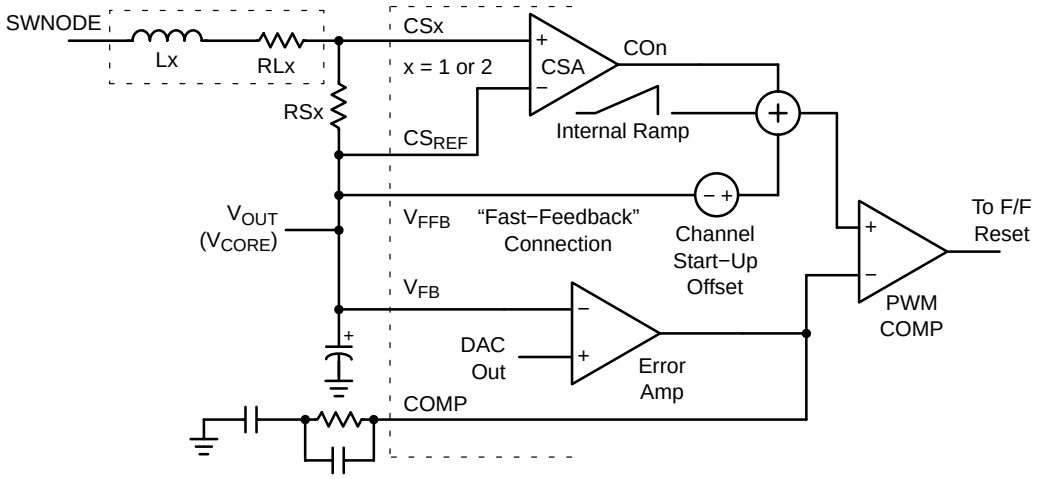


Figure 14. Enhanced V^2 Control Employing Resistive Current Sensing and Additional Internal Ramp

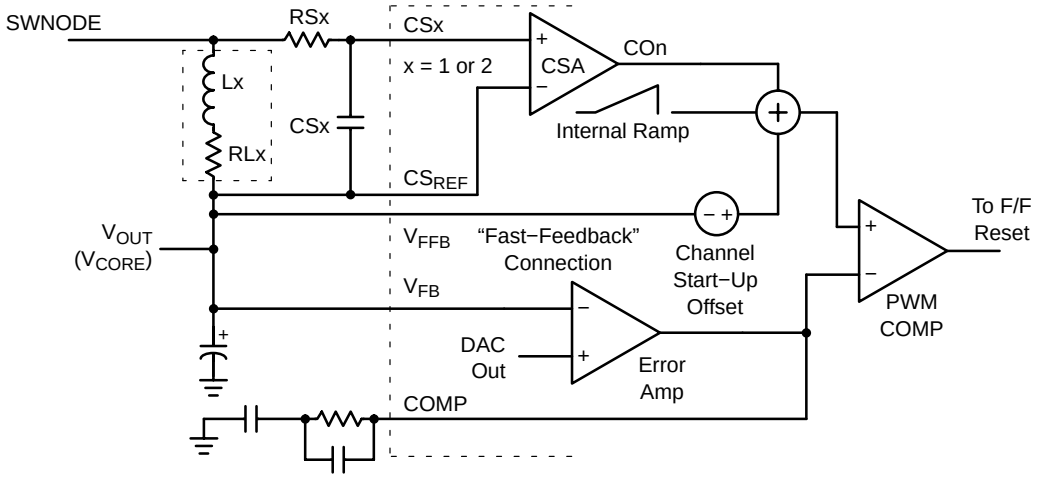


Figure 15. Enhanced V^2 Control Employing Lossless Inductive Current Sensing and Internal Ramp

with higher current, the PWM cycle will terminate earlier providing negative feedback. The NCP5331 provides a CSx input for each phase, but the CS_{REF} and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same CS_{REF} and COMP pins, so that a phase with a larger current signal will turn off earlier than a phase with a smaller current signal.

Enhanced V^2 responds to disturbances in V_{CORE} by employing both "slow" and "fast" voltage regulation. The internal error amplifier performs the slow regulation. Depending on the gain and frequency compensation set by the amplifier's external components, the error amplifier will typically begin to ramp its output to react to changes in the output voltage in 1−2 PWM cycles. Fast voltage feedback is implemented by a direct connection from V_{CORE} to the noninverting pin of the PWM comparator via the summation with the inductor current, internal ramp, and the Startup OFFSET. A rapid increase in load current will produce a negative offset at V_{CORE} and at the output of the summer. This will cause the PWM duty cycle to increase almost instantly. Fast feedback will typically adjust the PWM duty cycle within 1 PWM cycle.

As shown in Figure 14, an internal ramp (nominally 125 mV at a 50% duty cycle) is added to the inductor current ramp at the positive terminal of the PWM comparator. This additional ramp compensates for propagation time delays from the current sense amplifier (CSA), the PWM comparator, and the MOSFET gate drivers. As a result, the minimum ON time of the controller is reduced and lower duty cycles may be achieved at higher frequencies. Also, the additional ramp reduces the reliance on the inductor current ramp and allows greater flexibility when choosing the output inductor and the RSxCSx (x = 1 or 2) time constant (see Figure 15) of the feedback components from V_{CORE} to the CSx pin.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. When the average output current is zero, the COMP pin will be

$$V_{COMP} = V_{CORE} @ 0\ A + Channel_Startup_Offset + Int_Ramp + G_{CSA} \cdot Ext_Ramp/2$$

Int_Ramp is the internal ramp value at the corresponding duty cycle, Ext_Ramp is the peak−to−peak external steady−state ramp at 0 A, G_{CSA} is the Current Sense Amplifier Gain (nominally 2.0 V/V), and the Startup Offset is typically 0.60 V. The magnitude of the Ext_Ramp can be calculated from

$$Ext_Ramp = D \cdot (V_{IN} - V_{CORE})/(RSx \cdot CSx \cdot f_{SW})$$

For example, if V_{CORE} at 0 A is set to 1.225 V with AVP and the input voltage is 12.0 V, the duty cycle (D) will be 1.225/12.0 or 10.2%. Int_Ramp will be 125 mV · 10.2/50 = 25.5 mV. Realistic values for RSx, CSx and f_{SW} are 5.6 kΩ, 0.1 μF, and 200 kHz − using these and the previously mentioned formula, Ext_Ramp will be 9.8 mV.

$$V_{COMP} = 1.225\ V + 0.60\ V + 25.5\ mV + 2.0\ V/V \cdot 9.8\ mV/2 = 1.855\ Vdc.$$

If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as

$$\Delta V = RSx \cdot G_{CSA} \cdot \Delta I_{OUT}.$$

The single−phase power stage output impedance is

$$Single\ Stage\ Impedance = \Delta V_{OUT}/\Delta I_{OUT} = R_S \cdot G_{CSA}$$

The multiphase power stage output impedance is the single−phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few

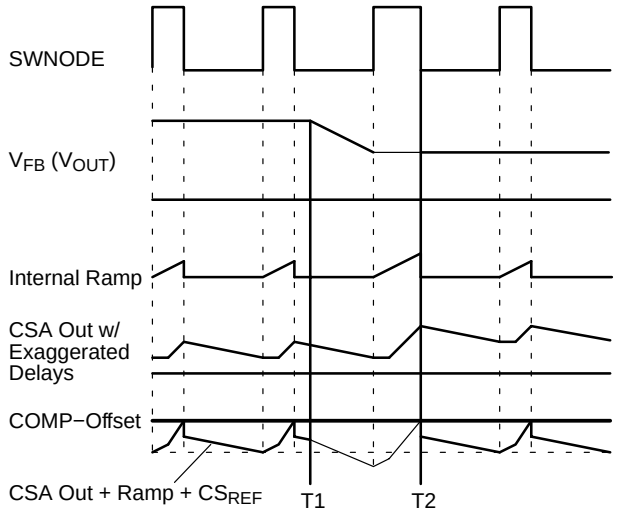


Figure 16. Open Loop Operation

microseconds of a transient before the feedback loop has repositioned the COMP pin.

The peak output current can be calculated from

$$I_{OUT,PEAK} = \frac{(V_{COMP} - V_{CORE} - Offset)}{(RSx \cdot G_{CSA})}$$

Figure 16 shows the step response of the COMP pin at a fixed level. Before time T1 the converter is in normal steady state operation. The inductor current provides a portion of the PWM ramp through the Current Sense Amplifier. The PWM cycle ends when the sum of the current ramp, the internal ramp voltage and Startup OFFSET exceed the voltage level of the COMP pin. At T1 the output current increases and the output voltage sags. The next PWM cycle begins and this PWM cycle continues longer than previously. As a result, the current signal increases enough to make up for the lower voltage at the V_{FB} pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the average current signal level (CSx output) is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.

Inductive Current Sensing

For lossless sensing, current can be sensed across the output inductor as shown in Figure 15. In the diagram, Lx is the output inductance and RLx is the inherent inductor resistance. To compensate the current sense signal, the values of RSx and CSx are chosen so that Lx/RLx = RSx · CSx. If this criteria is met, the current sense signal will be the same shape as the inductor current and the voltage signal at CSx will represent the instantaneous value of inductor current. Also, the circuit can be analyzed as if a sense resistor of value RLx was used as a sense resistor (RSx).

When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of 0.39% per °C. The increase in winding resistance at higher temperatures should be considered when setting the overcurrent (I_{LIM})threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 14.

Current Sharing Accuracy

Printed circuit board (PCB) traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is connected. For accurate current sharing, the current sense inputs should sense the current at relatively the same point for each phase and the connection to the CS_{REF} pin should be made so that no phase is favored. In some cases, especially with inductive sensing, resistance of the PCB can be useful for increasing the current sense resistance. The total current sense resistance used for calculations must include any PCB trace resistance between the CSx input and the CS_{REF} input that carries inductor current.

Current Sense Amplifier (CSA) input mismatch and the value of the current sense component will determine the accuracy of the current sharing between phases. The worst case Current Sense Amplifier input mismatch is ±5.0 mV and will typically be within ±3.0 mV. The difference in peak currents between phases will be the CSA input mismatch divided by the current sense resistance. If all current sense components are of equal resistance a 3.0 mV mismatch with a 2.0 mΩ total sense resistance will produce a 1.5 A difference in current between phases.

External Ramp Size and Current Sensing

The internal ramp allows flexibility of current sense time constant. Typically, the current sense RSxCSx time constant should be equal to or slower than the inductor's time constant. If the RC time constant is chosen to be smaller (faster) than L/R_L, the ac or transient portion of the current sensing signal will be scaled larger than the dc portion. This will provide a larger steady state ramp, but circuit performance (i.e. transient response) will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by RSx · CSx. It will eventually settle to the correct dc level, but the error will decay with the time constant of RSx · CSx. If this error is excessive it will effect transient response, adaptive positioning and current limit. During a positive current transient, the COMP pin will be required to undershoot in response to the current signal in order to maintain the output voltage. Similarly, the V_{DRP} signal will overshoot and will produce too much transient droop in the output voltage. Also, the hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.

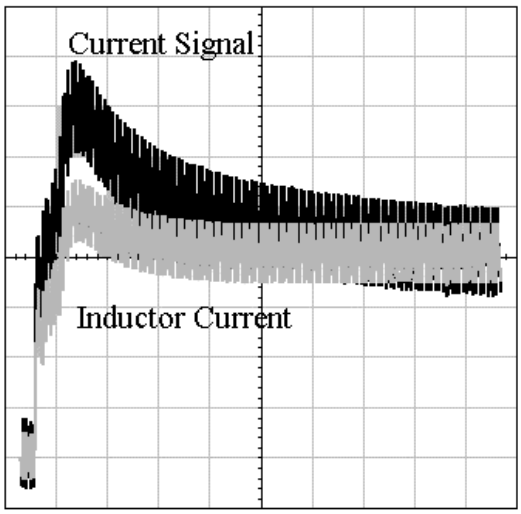


Figure 17. Inductive Sensing Waveform During a Load Step with Fast RC Time Constant (50 μs/div)

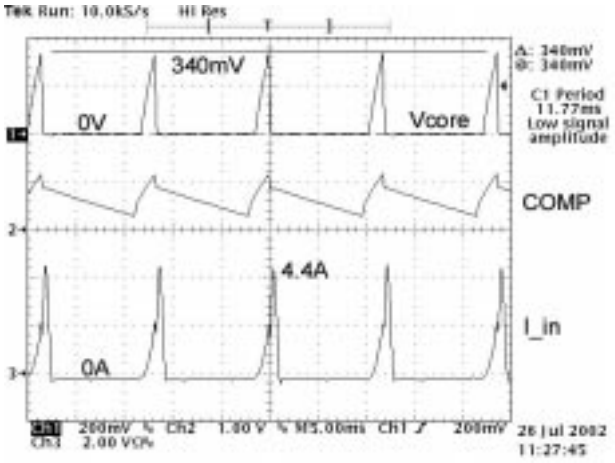


Figure 18. Hiccup Mode Operation

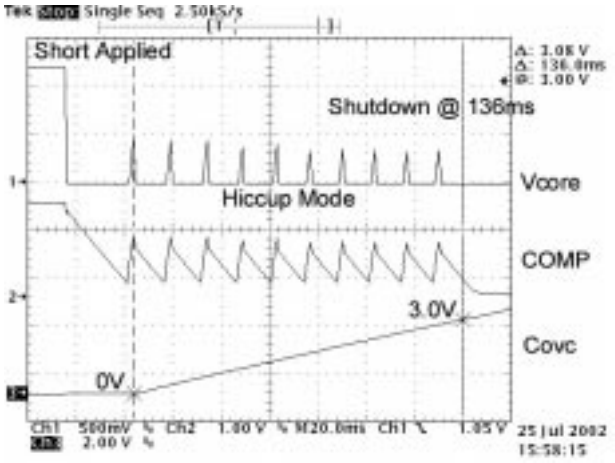


Figure 19. Overcurrent Timer Operation

The waveforms in Figure 17 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of L = 500 nH, R_L = 1.6 mΩ, RSx = 20 k and CSx = 0.01 μF. For ideal current signal compensation the value of RSx should be 31 kΩ. Due to the faster than ideal RC time constant there is an overshoot of 50% and the overshoot decays with a 200 μs time constant. With this compensation the I_{LIM} pin threshold must be set more than 50% above the full load current to avoid triggering hiccup mode during a large output load step.

Current Limit, Hiccup Mode and Overcurrent Timer

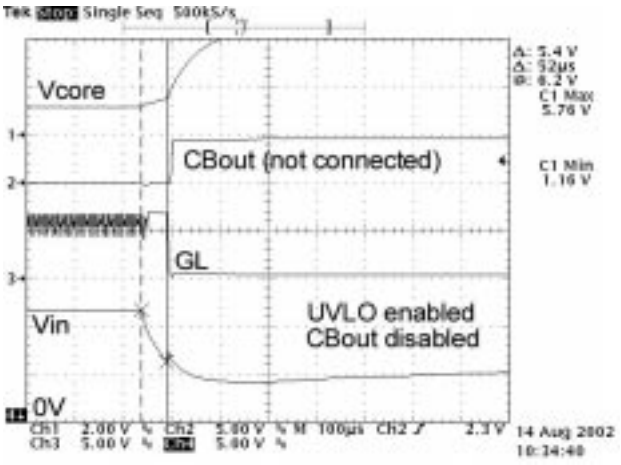
The individual phase currents are summed and low−pass filtered to create an average current signal. The average current is then compared to a user adjustable voltage at the I_{LIM} pin. If the I_{LIM} voltage is exceeded, the fault latch is set, switching stops, and the COMP pin is discharged until it decreases to 0.27 V. At this point, the fault latch is reset, the COMP voltage will begin to rise and a new startup cycle begins. During startup, the output voltage and load current will increase until either regulation is achieved or the I_{LIM} voltage is again exceeded. The converter will continue to operate in “hiccup mode” until the fault condition is corrected or the overcurrent timer expires.

When an overcurrent fault occurs the converter will enter a low duty cycle hiccup mode. During hiccup mode the converter will not switch from the time a fault is detected until the soft start capacitor (C_{C2}) has discharged below the COMP Discharge Threshold and then charged back up above the Channel Start Up Offset. Figure 18 shows the NCP5331 operating in hiccup mode with the converter output shorted to GND. Hiccup mode will continue until the overcurrent timer terminates operation.

The overcurrent timer sets a limit to how long the converter will operate in hiccup mode. Placing a capacitor from the C_{OVC} pin to GND sets the length of time − a larger capacitor sets a longer time. The first hiccup pulse starts the timer by turning on a current source that charges the capacitor at the C_{OVC} pin. If the voltage at the C_{OVC} pin rises to 3 V before the output voltage exceeds the PGD threshold, then the overcurrent latch is set, COMP is discharged, and PGD is latched Low. Once set, the overcurrent latch will hold the converter in this state until the input voltage, either V_{CCL} or V_{CCH}, is cycled. Conversely, if the timer starts and either the output short circuit is removed or the load is decreased before the overcurrent timer expires, PGD will transition High after its programmed delay time and the timer will be reset. The nominal overcurrent time can be calculated using the following equation.

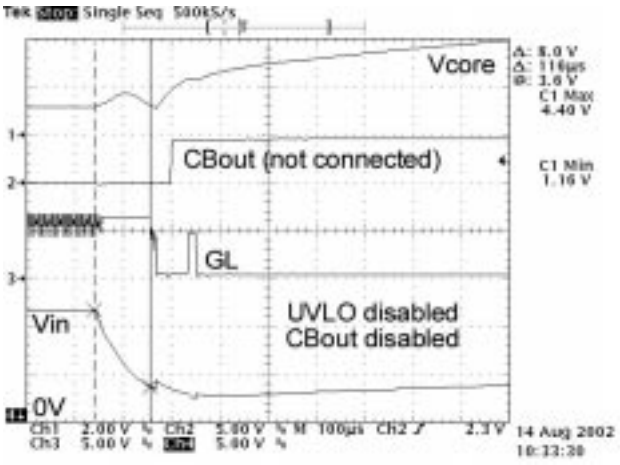
$$t_{OVC} = C_{OVC} \cdot (OVC_{THRESH} - OVC_{MIN})/I_{OVC}$$
$$= C_{OVC} \cdot (3.0\ V - 0.25\ V)/5.0\ \mu A$$
$$= C_{OVC} \cdot 5.5 \times 10^5$$

Figure 19 shows the overcurrent timer terminating hiccup mode when C_{OVC} charges up to 3.0 V.



NOTE: Using the lower MOSFETs to prevent overvoltage is not adequate if the MOSFETs are turned OFF at the UVLO threshold − V_{CORE} reaches 4.0 V within 100 μs.

Figure 20. Overvoltage Occurs with UVLO Enabled



NOTE: Even if the lower MOSFETs remain ON after UVLO, there is not enough gate drive voltage to prevent V_{CORE} from reaching 4.0 V.

Figure 21. Overvoltage Occurs with UVLO Disabled

Overvoltage Protection

The NCP5331 provides a comprehensive level of overvoltage protection. Overvoltage protection (OVP) addresses the following five cases (in decreasing level of difficulty):

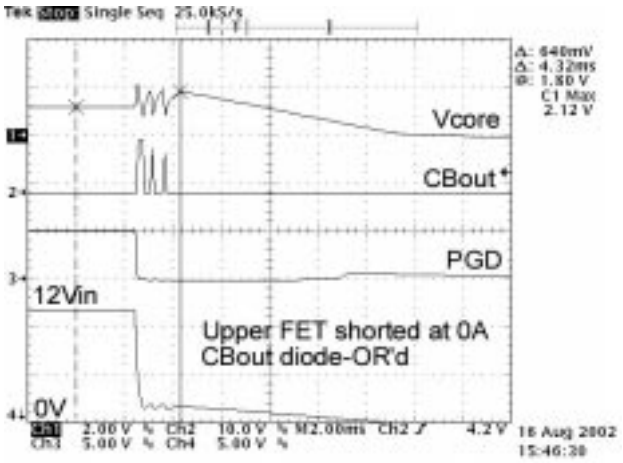
1. Normal operation, upper MOSFET shorts
2. Upper MOSFET shorted, turn on the ATX power
3. Normal operation, open the voltage feedback signal
4. Normal operation, ground the voltage feedback signal
5. Open the voltage feedback signal, apply ATX power

By far the most difficult overvoltage scenario is when the upper MOSFET shorts during normal operation. The energy stored in the output filters of both the ATX supply and the dc/dc converter must be dissipated very quickly or an overvoltage condition will occur. When the upper MOSFET shorts, V_{CORE} rises and the error amplifier, due to the closed loop control, will within approximately 400 ns, command the upper MOSFETs (those that aren't shorted) to turn OFF and all the lower MOSFETs to turn ON. This will cause two things to occur: V_{CORE} will stop increasing, and a very high current will be drawn from the ATX supply. The current limit in the ATX supply should become active and the input voltage to the converter will be removed. Now, when the input voltage drops below the NCP5331's UVLO threshold the lower MOSFETs will be turned OFF. At this point, a fair amount of the energy in the system will have been dissipated, however, the converter's output voltage will begin to rise again as shown in Figure 20. Even if the lower MOSFETs are *not* turned OFF at the UVLO threshold, as V_{IN} decays, adequate gate drive voltage will not exist to fully enhance the devices and the CPU may be damaged. This case is shown in Figure 21.

The NCP5331 avoids the problems with UVLO and the gate drive voltage. When V_{CORE} exceeds 2.05 V, the NCP5331 will activate an external crowbar MOSFET via the CB_{OUT} pin. This additional MOSFET will clamp V_{CORE} and dissipate the remainder of the energy in the system. The CB_{OUT} circuitry is powered by 5 V_{SB} and is not disabled during UVLO. Also, the CB_{OUT} pin will always have adequate gate drive to enhance the lower MOSFET. The OVP circuits in the NCP5331 are not effected when the ATX supply current limits and V_{IN} is removed. Figure 22 and Figure 23 document successful operation of the CB_{OUT} circuitry when an upper MOSFET is shorted during normal operation with 0 A and 45 A loading.

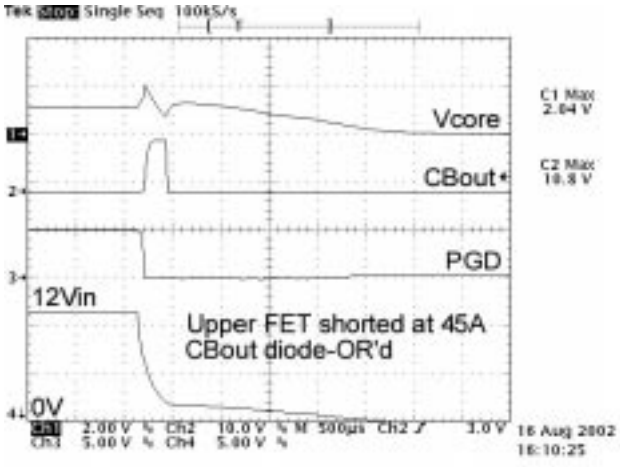
The second most difficult overvoltage scenario is when an upper MOSFET is shorted and the ATX power is applied. In this case, V_{CORE} is equal to V_{IN} due to the shorted upper MOSFET. When V_{IN} reaches the maximum rating for the CPU (2.2 V) adequate gate drive voltage is not available to enhance the lower MOSFETs or crowbar device enough to protect the CPU. A typical "Logic Level" MOSFET will conduct only 100−300 μA for a gate drive of 2.0−2.5 V ($R_{DS(on)}$ = 6 kΩ to 25 kΩ). The $R_{DS(on)}$ of the crowbar device must be lower than 15 mΩ during startup to prevent damage to the CPU. The NCP5331 avoids this problem by taking advantage of the 5 V_{SB} voltage from the ATX supply. If V_{IN} is less than 5 V_{SB}, then 5 V will be used to enhance the crowbar device. Most modern MOSFETs will be less than 10 mΩ for a V_{GS} greater than 4.5 V. Figure 24 shows the NCP5331 preventing V_{CORE} from exceeding 2.0 V with a shorted upper MOSFET during startup.

If the voltage feedback signal (COREFB+) is broken, a high value internal pull−up resistor will cause V_{FFB} (and V_{FB}) to float higher in voltage. As V_{FFB} (and V_{FB}) are pulled higher, the error amplifier will "think" V_{CORE} is too high and command a lower and lower duty cycle until V_{CORE} is driven to 0 V. Without the internal pull−up resistor the error amplifier would command 100% duty cycle and V_{CORE} would be driven very high, damaging the CPU.



NOTE: The NCP5331 maintains V_{CORE} < 2.2 V when an upper MOSFET shorts during no−load operation.

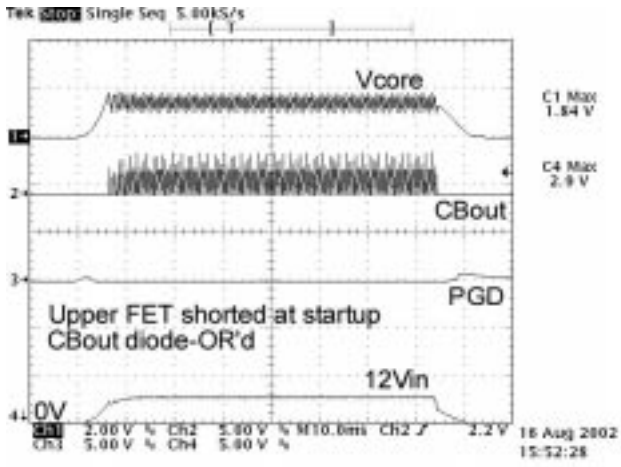
Figure 22. NCP5331 Prevents Overvoltage at 0 A



NOTE: The NCP5331 maintains V_{CORE} < 2.2 V when an upper MOSFET shorts with 45 A loading.

Figure 23. NCP5331 Prevents Overvoltage at 45 A

If the voltage feedback signal (COREFB+) is accidentally grounded (but V_{CORE} is not), the error amplifier will respond by increasing the duty cycle. Of course, this will cause V_{CORE} to rise. When V_{CORE} reaches 2.0 V, the internal crowbar circuit will be activated and the overcurrent/overvoltage latch will be set. This latch will discharge COMP, turn OFF the upper MOSFETs, and turn ON the lower MOSFETs. The overcurrent/overvoltage latch will hold the controller in this state until the input power is cycled.



NOTE: The NCP5331 maintains V_{CORE} < 2.2 V when an upper MOSFET is shorted and ATX power is applied.

Figure 24. NCP5331 Prevents Overvoltage at Startup

Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during load transients. Adaptive voltage positioning can reduce peak−to−peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is applied. Similarly, the output voltage can be set lower than nominal during heavy loads to reduce overshoot when the load current is removed. For low current applications a droop resistor can provide fast accurate adaptive positioning. However, at high currents the loss in a droop resistor becomes excessive. For example; in a 50 A converter a 1 mΩ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 W.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond to changes in load current. Figure 25 shows how adaptive positioning works. The waveform labeled “Normal” shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.

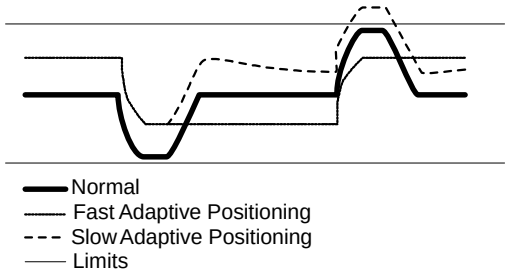
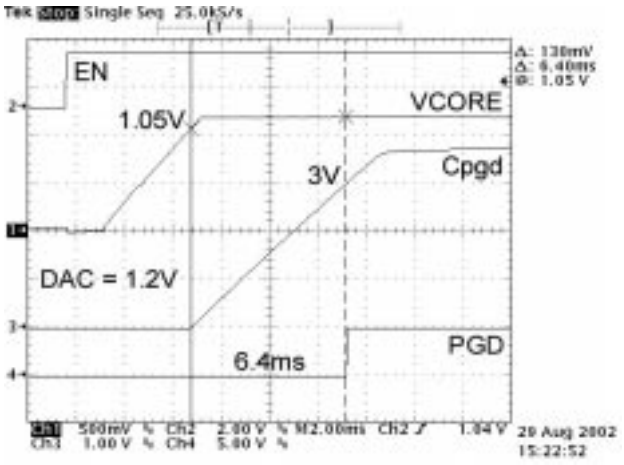


Figure 25. Adaptive Positioning

The controller can be configured to adjust the output voltage based on the output current of the converter. (Refer to the application schematic in Figure 1). To set the no−load positioning, a resistor is placed between the output voltage and V_{FB} pin. The V_{FB} bias current will develop a voltage across the resistor to adjust the no−load output voltage. The V_{FB} bias current is dependent on the value of R_{OSC} as shown in the data sheets.

During no load conditions the V_{DRP} pin is at the same voltage as the V_{FB} pin, so none of the V_{FB} bias current flows through the V_{DRP} resistor. When output current increases the V_{DRP} pin increases proportionally and the V_{DRP} pin current offsets the V_{FB} bias current and causes the output voltage to decrease.

The response during the first few microseconds of a load transient are controlled primarily by power stage output impedance and the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the total ramp size and the error amp compensation. If the current signal (external ramp) size is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.



NOTE: The PGD timer insures that PGD will transition high when V_{CORE} is in regulation.

Figure 26. Power Good Delay Operation

Error Amp Compensation, Tuning, and Soft Start

The transconductance error amplifier requires a capacitance (C_{C1} + C_{C2} in the Applications Diagram) between the COMP pin and GND for two reasons. First, this capacitance stabilizes the transconductance error amplifier. Values less than a few nF may cause oscillations of the COMP voltage and increase the output voltage jitter. Second, this capacitance sets the soft start and hiccup mode slopes. The internal error amplifier will source approximately 30 μA during soft start and hiccup mode. No switching will occur until the COMP voltage exceeds the Channel Startup Offset (nominally 0.6 V). If C_{C2} is set to 0.1 μF the 30 μA from the error amplifier will allow the output to ramp up or down at approximately 30μ A/0.1 μF or 0.3 V/ms or 1.2 V in 4 ms.

The COMP voltage will ramp up to the following value.

$$V_{COMP} = V_{CORE} @ 0\ A + Channel_Startup_Offset + Int_Ramp + G_{CSA} \cdot Ext_Ramp/2$$

The COMP pin will disable the converter when pulled below the COMP Discharge Threshold (nominally 0.27 V).

The RC network between the COMP pin and the soft start capacitor (R_{C1}, C_{C1}) allows the COMP voltage to slew quickly during transient loading of the converter. Without this network the error amplifier would have to drive the large soft start capacitor (C_{C2}) directly, which would drastically limit the slew rate of the COMP voltage. The R_{C1}/C_{C1} network allows the COMP voltage to undergo a step change of approximately $R_{C1} \cdot I_{COMP}$.

The capacitor (C_{A1}) between the COMP pin and the error amplifier's inverting input (the V_{FB} pin) and the parallel combination of the resistors R_{F1} and R_{DRP} determine the bandwidth of the error amplifier. The gain of the error amplifier crosses 0 dB at a high enough frequency to give a quick transient response, but well below the switching frequency to minimize ripple and noise on the COMP pin. A capacitor in parallel with the R_{F1} resistor (C_{F1}) adds a zero to boost phase near the crossover frequency to improve loop stability.

Setting up and tuning the error amplifier is a three step process. First, the no−load and full−load adaptive voltage positioning (AVP) are set using R_{F1} and R_{DRP}, respectively. Second, the current sense time constant and error amplifier gain are adjusted with RSx and C_{A1} while monitoring V_{CORE} during transient loading. Lastly, the peak−to−peak voltage ripple on the COMP pin is examined when the converter is fully loaded to insure low output voltage jitter. The exact details of this process are covered in the Design Procedure section.

Undervoltage Lockout (UVLO)

The controller has undervoltage lockout comparators monitoring two pins. One, intended for the logic and low−side drivers, is connected to the V_{CCL} pin with an 8.5 V turn−on and 6.15 V turn−off threshold. A second, for the high side drivers, is connected to the V_{CCH} pin with an 8.5 V turn−on and 6.75 V turn−off threshold. A UVLO fault sets the fault latch which forces switching to stop and the upper and lower gate drivers produce a logic low (i.e., all the MOSFETs are turned OFF). Power good (PGD) is pulled low when UVLO occurs. The overcurrent/overvoltage latch is reset by the UVLO signal.

Power Good (PGD) Delay Time

When V_{CORE} is less than the power good threshold, 87.5% · DAC, or greater than 2.0 V the open−collector power good pin (PGD) will be pulled low by the NCP5331. When V_{CORE} is in regulation PGD will become high impedance. An external pull−up resistor is required on PGD.

During soft start, when V_{CORE} reaches the power good threshold, 87.5% · DAC, then the "longer" of two timers will dictate when PGD becomes high impedance. One timer is internally set to 200 μs and can not be changed. Placing a capacitor from the C_{PGD} pin to GND sets the second programmable timer. When V_{CORE} crosses the PGD threshold, a current source will charge C_{PGD} starting at

0.25 V and “timing out” at 3 V. The current delivered to the C_{PGD} capacitor (I_{PGD}) is a function of the R_{OSC} resistor according to the following equation.

$$I_{PGD} = 0.52\ V/R_{OSC}$$

The programmed delay time can be calculated from

$$t_{PGD} = C_{PGD} \cdot (PGD_{THRESH} - PGD_{MIN})/I_{PGD}$$
$$= C_{PGD} \cdot (3.0\ V - 0.25\ V)/I_{PGD}$$

The programmable timer may be disabled (set to 0) by connecting the C_{PGD} pin to 5 V_{REF}. This will set the PGD delay time to the internal delay of 200 μs. Figure 26 demonstrates the use of the programmable PGD timer (set to 6.0 ms) to allow PGD to transition high when V_{CORE} is safely within the regulation limits for the processor (DAC ±50 mV).

Implementing an Enable Function

An Enable function may be implemented on the NCP5331 in one of two ways. The first method (Method A in Figure 27) is to pull low on the Ilim pin. This method is the preferred method, as both the GHx and the GLx pins will be kept low at turn−off, preventing V_{CORE} from being pulled below ground.

However, if using the “Timed Hiccup Mode Current Limit” feature with Method A, the Covc pin will time out when the Ilim pin is pulled low, and the NCP5331 will not turn back on (after time out) unless the power is recycled. This can be avoided by adding another transistor to the Covc pin, thereby keeping it low while the part is disabled.

The second method (Method B in Figure 28) is to pull low on the NCP5331’s comp pin. With this method, GHx will be low and GLx will be high while the part is disabled.

However, under Method B, if the part is disabled at turn−on, and if using the “Timed Hiccup Mode Current Limit” feature, the Covc pin will again time out and the NCP5331 will not be able to be turned on after the time out has occurred. This too can be avoided by the use of a transistor at the Covc pin keeping it low while the part is disabled.

If using Method B but not with a transistor at the Covc pin, a 1.0 K resistor must be added between the drain of the transistor and the Comp pin to prevent the current limit from being tripped when the Comp pin is quickly pulled low.

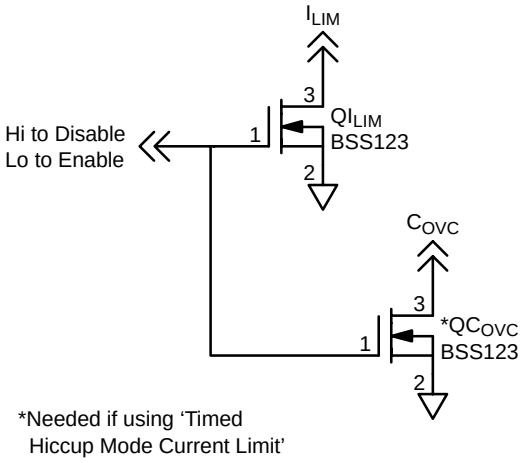


Figure 27. Enable Method A

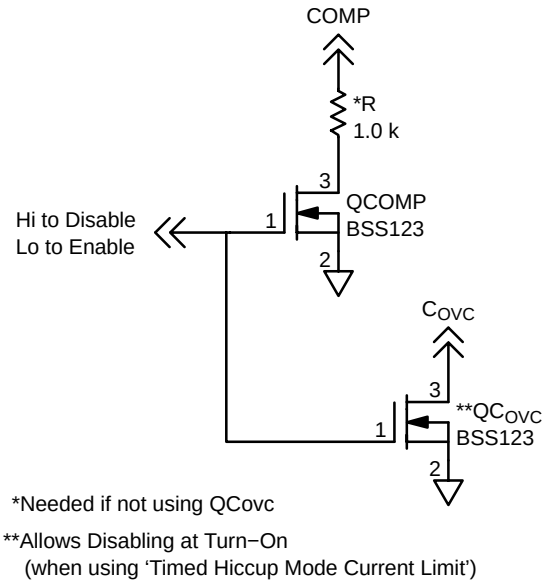


Figure 28. Enable Method B

Power Dissipation

NCP5331 power dissipation may be approximated by the following equation:

$$P_{loss} = F_{SW} \cdot (V_{CCH} \cdot Q_{THighFETs} + V_{CCLx} \cdot Q_{TLowFETs}) + P_{Quiescent}$$

where:

$$P_{Quiescent} = V_{CCL} \cdot I_{CCL} + 2 \cdot V_{CCLx} \cdot I_{CCLx} + (V_{CCH} + V_{in}) \cdot I_{CCH}$$

F_{SW} is the switching frequency

V_{CCL} is 12 V

V_{CCLx} is the low−side gate drive voltage and may be varied between 5.0 and 12 V

V_{CCH} is the high−side gate drive voltage and is between 4.5 and 7.0 V

V_{in} is the input voltage to the converter and is either 5.0 or 12 V

I_{CCL}, I_{CCLx}, I_{CCH} are typical device quiescent currents and can be found under the General Electrical Specifications.

$Q_{THighFETs}$ is the sum of the High−Side MOSFets total gate charge

$Q_{TLowFETs}$ is the sum of the Low−Side MOSFets total gate charge

Figure 29 shows device temperature rise versus switching frequency at various gate drive voltage combinations using ON Semiconductor's NTD60N03 (Qt = 31nC at 5.0 V) as the high−side MOSFet and NTD80N02 (Qt = 39nC at 7.0 V) as the low−side MOSFet. Using other MOSFets will of course result in different losses, but the general conclusion will be the same.

If trying to drive 2 lower MOSFets at frequencies higher than 200 KHz, it may be necessary to reduce the low−side gate drive voltage.

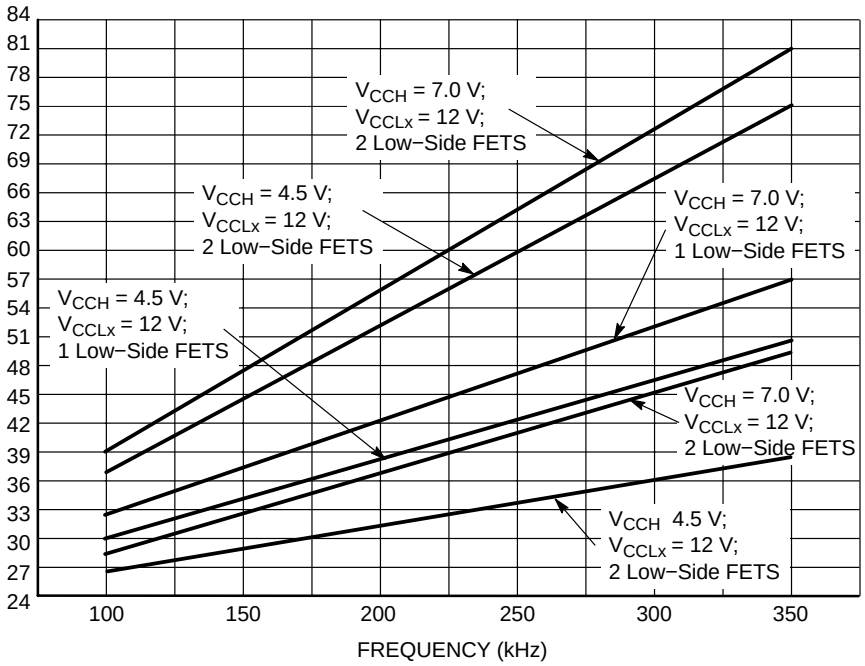


Figure 29. Calculated NCP5331 temperature rise (LQFP−32 package) versus frequency at various typical gate drive voltage combinations with typical ON Semiconductor MOSFets.

Layout Guidelines

With the fast rise, high output currents of microprocessor applications, parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically, a multilayer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to route the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.

The current sense signals are typically tens of millivolts. Noise pick−up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as the switch node and gate drive signals. If the current signals are taken from a location other than directly at the inductor any additional resistance between the pick−off point and the inductor appears as part of the inherent inductor resistances and should be considered in design calculations. The capacitors for the current feedback networks should be placed as close to the current sense pins as practical. After placing the NCP5331 control IC, follow these guidelines to optimize the layout and routing:

1. Place the 1 μF ceramic power−supply bypass capacitors close to their associated pins: V_{CCL}, V_{CCH}, V_{CCL1} and V_{CCL2}.
2. Place the MOSFETs to minimize the length of the Gate traces. Orient the MOSFETs such that the Drain connections are away from the controller and the Gate connections are closest to the controller.
3. Place the components associated with the internal error amplifier (R_{F1}, C_{F1}, C_{C1}, C_{C2}, R_{C1}, C_{A1}, R_{DRP}) to minimize the trace lengths to the pins V_{FB}, V_{DRP} and COMP.
4. Place the current sense components (R_{S1}, R_{S2}, C_{S1}, C_{S2}, R_S, C_{SA}, C_{SB}) near the CS1, CS2, and CS_{REF} pins.
5. Place the frequency setting resistor (R_{OSC}) close to the R_{OSC} pin. The R_{OSC} pin is very sensitive to noise. Route noisy traces, such as the SWNODEs and GATE traces, away from the R_{OSC} pin and resistor.
6. Place the MOSFETs and output inductors to reduce the size of the noisy SWNODEs. However, there is a trade−off between reducing the size of the SWNODEs for noise reduction and providing adequate heat−sinking for the synchronous MOSFETs.
7. Place the input inductor and input capacitor(s) near the Drain of the control (upper) MOSFETs. There is a trade−off between reducing the size of this node to save board area and providing adequate heat−sinking for the control (upper) MOSFETs.
8. Place the output capacitors (electrolytic and ceramic) close to the processor socket or output connector.
9. The trace from the SWNODEs to the current sense components (R_{S1}, R_{S2}) will be very noisy. Route this away from more sensitive, low−level traces. The Ground layer can be used to help isolate this trace.
10. The Gate traces are very noisy. Route these away from more sensitive, low−level traces. Try to keep each Gate signal on one layer and insure that there is an uninterrupted return path directly below the Gate trace. The Ground layer can be used to help isolate these traces.
11. Gate driver returns, GND1 and GND2, should not be connected to LGND, but instead directly to the ground plane.
12. Try not to “daisy chain” connections to Ground from one via. Ideally, each connection to Ground will have its own via located as close to the component as possible.
13. Use a slot in the ground plane to prevent high currents from flowing beneath the control IC. This slot should form an “island” for signal ground under the control IC. “Signal ground” and “power ground” must be separated. Examples of signal ground include the capacitors at COMP, CS_{REF}, and $5V_{REF}$, the resistors at R_{OSC} and I_{LIM}, and the LGND pin to the controller. Examples of power ground include the capacitors to V_{CCH} and V_{CCL1} and V_{CCL2}, the Source of the synchronous MOSFETs, and the GND1 and GND2 pins of the controller.

14. The CS_{REF} sense point should be equidistant between the output inductors to equalize the PCB resistance added to the current sense paths. This will insure acceptable current sharing. Also, route the CS_{REF} connection away from noisy traces such as the SWNODEs and GATE traces. If noise from the SWNODEs or GATE signals capacitively couples to the CSREF trace the external ramps will be very noisy and voltage jitter will result.
15. Ideally, the SWNODEs are exactly the same shape and the current sense points (connections to R_{S1} and R_{S2}) are made at identical locations to equalize the PCB resistance added to the current sense paths. This will help to insure acceptable current sharing.
16. Place the 1 μF ceramic capacitors, C_{P1} and C_{P2}, close to the drains of the MOSFETs Q1 and Q2, respectively.
17. If snubbers are used, they must be placed very close to their associated MOSFETs and SWNODE. The connections to the snubber components should be as short as possible.

Design Procedure

1. Output Capacitor Selection

The output capacitors filter the current from the output inductor and provide a low impedance for transient load current changes. Typically, microprocessor applications will require both bulk (electrolytic, tantalum) and low impedance, high frequency (ceramic) types of capacitors. The bulk capacitors provide “hold up” during transient loading. The low impedance capacitors reduce steady−state ripple and bypass the bulk capacitance when the output current changes very quickly. The microprocessor manufacturers usually specify a minimum number of ceramic capacitors. The designer must determine the number of bulk capacitors.

Choose the number of bulk output capacitors to meet the peak transient requirements. The following formula can be used to provide a starting point for the minimum number of bulk capacitors ($N_{OUT,MIN}$).

$$N_{OUT,MIN} = \text{ESR per capacitor} \cdot \frac{\Delta I_{O,MAX}}{\Delta V_{O,MAX}} \quad (1)$$

In reality, both the ESR and ESL of the bulk capacitors determine the voltage change during a load transient according to

$$\Delta V_{O,MAX} = (\Delta I_{O,MAX}/\Delta t) \cdot ESL + \Delta I_{O,MAX} \cdot ESR \quad (2)$$

Unfortunately, capacitor manufacturers do not specify the ESL of their components and the inductance added by the PCB traces is highly dependent on the layout and routing. Therefore, it is necessary to start a design with slightly more than the minimum number of bulk capacitors and perform transient testing or careful modeling/simulation to determine the final number of bulk capacitors.

2. Output Inductor Selection

The output inductor may be the most critical component in the converter because it will directly effect the choice of other components and dictate both the steady−state and transient performance of the converter. When selecting an inductor the designer must consider factors such as dc current, peak current, output voltage ripple, core material, magnetic saturation, temperature, physical size, and cost (usually the primary concern).

In general, the output inductance value should be as low and physically small as possible to provide the best transient response and minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, too low an inductance value will result in very large ripple currents in the power components (MOSFETs, capacitors, etc) resulting in increased dissipation and lower converter efficiency. Also, increased ripple currents will force the designer to use higher rated MOSFETs, oversize the thermal solution, and use more, higher rated input and output capacitors − the converter cost will be adversely effected.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. Equation 3 may be used to calculate the minimum inductor value to produce a given maximum ripple current (α) per phase. The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the maximum ripple current.

$$L_{O_{MIN}} = \frac{(V_{IN} - V_{CORE}) \cdot V_{CORE}}{(\alpha \cdot I_{O,MAX} \cdot V_{IN} \cdot f_{SW})} \quad (3)$$

α is the ripple current as a percentage of the maximum output current *per phase* (α = 0.15 for ±15%, α = 0.25 for ±25%, etc). If the minimum inductor value is used, the inductor current will swing ±α% about its value at the center (half the dc output current for a two−phase converter). Therefore, for a two−phase converter, the inductor must be designed or selected such that it will not saturate with a peak current of $(1 + \alpha) \cdot I_{O,MAX}/2$.

The maximum inductor value is limited by the transient response of the converter. If the converter is to have a fast transient response then the inductor should be made as small as possible. If the inductor is too large its current will change too slowly, the output voltage will droop excessively, more bulk capacitors will be required, and the converter cost will be increased. For a given inductor value, its interesting to determine the time required to increase or decrease the current.

For increasing current

$$\Delta t_{INC} = Lo \cdot \Delta I_O/(V_{IN} - V_{CORE}) \quad (3.1)$$

For decreasing current

$$\Delta t_{DEC} = Lo \cdot \Delta I_O/(V_{CORE}) \quad (3.2)$$

For typical processor applications with output voltages less than half the input voltage, the current will be increased much more quickly than it can be decreased. It may be more difficult for the converter to stay within the regulation limits when the load is removed than when it is applied − excessive overshoot may result.

The output voltage ripple can be calculated using the output inductor value derived in this Section (Lo_{MIN}), the number of output capacitors ($N_{OUT,MIN}$) and the per capacitor ESR determined in the previous Section.

$$V_{OUT,P-P} = (\text{ESR per cap} / N_{OUT,MIN}) \cdot [(V_{IN} - \#\text{Phases} \cdot V_{CORE}) \cdot D / (Lo_{MIN} \cdot f_{SW})] \quad (4)$$

This formula assumes steady−state conditions with no more than one phase on at any time. The second term in Equation 4 is the total ripple current seen by the output capacitors. The total output ripple current is the “time summation” of the two individual phase currents that are 180 degrees out−of−phase. As the inductor current in one phase ramps upward, current in the other phase ramps downward and provides a canceling of currents during part of the switching cycle. Therefore, the total output ripple current and voltage are reduced in a multiphase converter.

3. Input Capacitor Selection

The choice and number of input capacitors is primarily determined by their voltage and ripple current ratings. The designer must choose capacitors that will support the worst case input voltage with adequate margin. To calculate the number of input capacitors one must first determine the total rms input ripple current. To this end, begin by calculating the average input current to the converter.

$$I_{IN,AVG} = I_{O,MAX} \cdot D/\eta \quad (5)$$

where

D is the duty cycle of the converter, $D = V_{CORE}/V_{IN}$,

η is the specified minimum efficiency,

$I_{O,MAX}$ is the maximum converter output current.

The input capacitors will discharge when the control FET is ON and charge when the control FET is OFF as shown in Figure 30.

The following equations will determine the maximum and minimum currents delivered by the input capacitors.

$$I_{C,MAX} = I_{Lo,MAX}/\eta - I_{IN,AVG} \quad (6)$$

$$I_{C,MIN} = I_{Lo,MIN}/\eta - I_{IN,AVG} \quad (7)$$

$I_{Lo,MAX}$ is the maximum output inductor current.

$$I_{Lo,MAX} = I_{O,MAX}/2 + \Delta I_{Lo}/2 \quad (8)$$

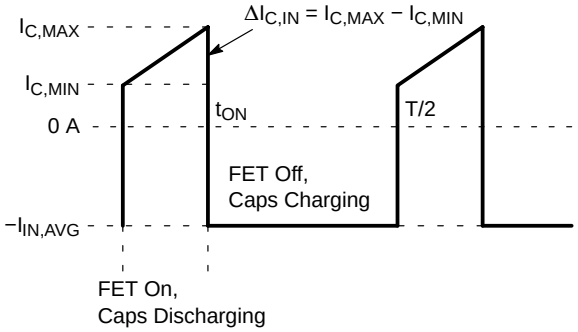


Figure 30. Input Capacitor Current for a Two−Phase Converter

$I_{Lo,MIN}$ is the minimum output inductor current.

$$I_{Lo,MIN} = I_{O,MAX}/2 - \Delta I_{Lo}/2 \quad (9)$$

ΔI_{Lo} is the peak−to−peak ripple current in the output inductor of value L_o.

$$\Delta I_{Lo} = (V_{IN} - V_{CORE}) \cdot D/(Lo \cdot f_{SW}) \quad (10)$$

For the two−phase converter, the input capacitor(s) rms current is then

$$I_{CIN,RMS} = [2D \cdot (I_{C,MIN}^2 + I_{C,MIN} \cdot \Delta I_{C,IN} + \Delta I_{C,IN}^2/3) + I_{IN,AVG}^2 \cdot (1 - 2D)]^{1/2} \quad (11)$$

Select the number of input capacitors (N_{IN}) to provide the rms input current ($I_{CIN,RMS}$) based on the rms ripple current rating per capacitor ($I_{RMS,RATED}$).

$$N_{IN} = I_{CIN,RMS}/I_{RMS,RATED} \quad (12)$$

For a two−phase converter with perfect efficiency ($\eta = 1$), the worst case input ripple current will occur when the converter is operating at a 25% duty cycle. At this operating point, the parallel combination of input capacitors must support an rms ripple current equal to 25% of the converter’s dc output current. At other duty cycles, the ripple current will be less. For example, at a duty cycle of either 10% or 40%, the two−phase input ripple current will be approximately 20% of the converter’s dc output current.

In general, capacitor manufacturers require derating to the specified ripple current based on the ambient temperature. More capacitors will be required because of the current derating. The designer should be cognizant of the ESR of the input capacitors. The input capacitor power loss can be calculated from

$$P_{CIN} = I_{CIN,RMS}^2 \cdot ESR_per_capacitor/N_{IN} \quad (13)$$

Low ESR capacitors are recommended to minimize losses and reduce capacitor heating. The life of an electrolytic capacitor is reduced 50% for every 10°C rise in the capacitor’s temperature.

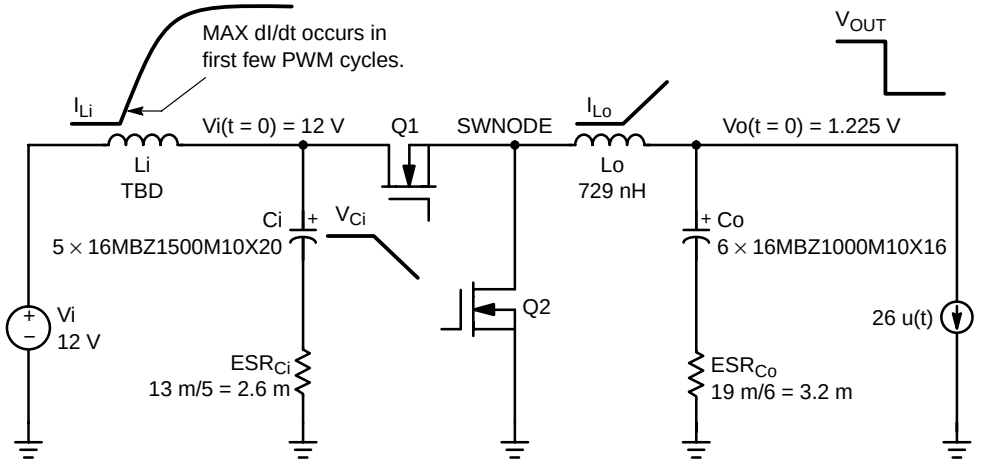


Figure 31. Calculating the Input Inductance

4. Input Inductor Selection

The use of an inductor between the input capacitors and the power source will accomplish two objectives. First, it will isolate the voltage source and the system from the noise generated in the switching supply. Second, it will limit the inrush current into the input capacitors at power up. Large inrush currents will reduce the expected life of the input capacitors. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients.

The worst case input current slew rate will occur during the first few PWM cycles immediately after a step−load change is applied as shown in Figure 31. When the load is applied, the output voltage is pulled down very quickly. Current through the output inductors will not change instantaneously so the initial transient load current must be conducted by the output capacitors. The output voltage will step downward depending on the magnitude of the output current ($I_{O,MAX}$), the per capacitor ESR of the output capacitors (ESR_{OUT}), and the number of the output capacitors (N_{OUT}) as shown in Figure 31. Assuming the load current is shared equally between the two phases, the output voltage at full, transient load will be

$$V_{CORE,FULL-LOAD} = V_{CORE,NO-LOAD} - (I_{O,MAX}/2) \cdot ESR_{OUT}/N_{OUT} \quad (14)$$

When the control MOSFET (Q1 in Figure 31) turns ON, the input voltage will be applied to the opposite terminal of the output inductor (the SWNODE). At that instant, the voltage across the output inductor can be calculated as

$$\Delta V_{Lo} = V_{IN} - V_{CORE,FULL-LOAD} = V_{IN} - V_{CORE,NO-LOAD} + (I_{O,MAX}/2) \cdot ESR_{OUT}/N_{OUT} \quad (15)$$

The differential voltage across the output inductor will cause its current to increase linearly with time. The slew rate of this current can be calculated from

$$dI_{Lo}/dt = \Delta V_{Lo}/Lo \quad (16)$$

Current changes slowly in the input inductor so the input capacitors must initially deliver the vast majority of the input current. The amount of voltage drop across the input capacitors (ΔV_{Ci}) is determined by the number of input capacitors (N_{IN}), their per capacitor ESR (ESR_{IN}), and the current in the output inductor according to

$$\Delta V_{Ci} = ESR_{IN}/N_{IN} \cdot dI_{Lo}/dt \cdot t_{ON} = ESR_{IN}/N_{IN} \cdot dI_{Lo}/dt \cdot D/f_{SW} \quad (17)$$

Before the load is applied, the voltage across the input inductor (V_{Li}) is very small − the input capacitors charge to the input voltage, V_{IN}. After the load is applied the voltage drop across the input capacitors, ΔV_{Ci}, appears across the input inductor as well. Knowing this, the minimum value of the input inductor can be calculated from

$$Li_{MIN} = V_{Li} / dI_{IN}/dt_{MAX} = \Delta V_{Ci} / dI_{IN}/dt_{MAX} \quad (18)$$

where dI_{IN}/dt_{MAX} is the maximum allowable input current slew rate.

The input inductance value calculated from Equation 18 is relatively conservative. It assumes the supply voltage is very "stiff" and does not account for any parasitic elements that will limit dI/dt such as stray inductance. Also, the ESR values of the capacitors specified by the manufacturer's data sheets are worst case high limits. In reality input voltage "sag," lower capacitor ESRs, and stray inductance will help reduce the slew rate of the input current.

As with the output inductor, the input inductor must support the maximum current without saturating the magnetic. Also, for an inexpensive iron powder core, such as the −26 or −52 from Micrometals, the inductance "swing" with dc bias must be taken into account − inductance will decrease as the dc input current increases. At the maximum input current, the inductance must not decrease below the minimum value or the dI/dt will be higher than expected.

5. MOSFET and Heatsink Selection

Power dissipation, package size, and thermal solution drive MOSFET selection. To adequately size the heat sink, the design must first predict the MOSFET power dissipation. Once the dissipation is known, the heat sink thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the nonoverlap time of the gate drivers.

For the upper or control MOSFET, the power dissipation can be approximated from

$$P_{D,CONTROL} = (I_{RMS,CNTL}^2 \cdot R_{DS(on)}) + (I_{Lo,MAX} \cdot Q_{switch}/I_g \cdot V_{IN} \cdot f_{SW}) + (Q_{oss}/2 \cdot V_{IN} \cdot f_{SW}) + (V_{IN} \cdot Q_{RR} \cdot f_{SW}) \quad (19)$$

The first term represents the conduction or IR losses when the MOSFET is ON, while the second term represents the switching losses. The third term is the losses associated with the *control and synchronous* MOSFET output charge when the control MOSFET turns ON. The output losses are caused by both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovery time of the body diode in the *synchronous* MOSFET. The first two terms are usually adequate to predict the majority of the losses.

$I_{RMS,CNTL}$ is the rms value of the trapezoidal current in the control MOSFET.

$$I_{RMS,CNTL} = [D \cdot (I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (20)$$

$I_{Lo,MAX}$ is the maximum output inductor current.

$$I_{Lo,MAX} = I_{O,MAX}/2 + \Delta I_{Lo}/2 \quad (21)$$

$I_{Lo,MIN}$ is the minimum output inductor current.

$$I_{Lo,MIN} = I_{O,MAX}/2 - \Delta I_{Lo}/2 \quad (22)$$

$I_{O,MAX}$ is the maximum converter output current.
D is the duty cycle of the converter.

$$D = V_{CORE}/V_{IN} \quad (23)$$

ΔI_{Lo} is the peak−to−peak ripple current in the output inductor of value L_o.

$$\Delta I_{Lo} = (V_{IN} - V_{CORE}) \cdot D/(Lo \cdot f_{SW}) \quad (24)$$

$R_{DS(on)}$ is the ON resistance of the MOSFET at the applied gate drive voltage.

Q_{switch} is the post gate threshold portion of the gate−to−source charge plus the gate−to−drain charge. This may be specified in the data sheet or approximated from the gate−charge curve as shown in the Figure 32.

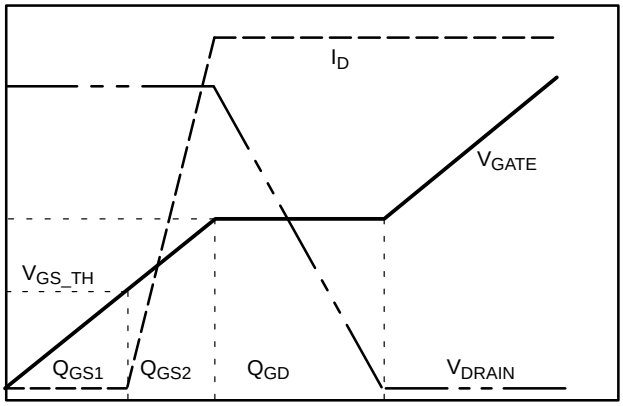


Figure 32. MOSFET Switching Characteristics

$$Q_{switch} = Q_{gs2} + Q_{gd} \quad (25)$$

I_g is the output current from the gate driver IC.
V_{IN} is the input voltage to the converter.
f_{sw} is the switching frequency of the converter.
Q_{RR} is the reverse recovery charge of the *lower* MOSFET.
Q_{oss} is the sum of all the MOSFET output charges.

For the lower or synchronous MOSFET, the power dissipation can be approximated from

$$P_{D,SYNCH} = (I_{RMS,SYNCH}^2 \cdot R_{DS(on)}) + (Vf_{diode} \cdot I_{O,MAX}/2 \cdot t_nonoverlap \cdot f_{SW}) \quad (26)$$

The first term represents the conduction or IR losses when the MOSFET is ON, and the second term represents the diode losses that occur during the gate nonoverlap time.

All terms were defined in the previous discussion for the control MOSFET with the exception of

$$I_{RMS,SYNCH} = [(1 - D) \cdot (I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (27)$$

Vf_{diode} is the forward voltage of the MOSFET's intrinsic diode at the converter output current.

t_nonoverlap is the nonoverlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the control IC.

When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature.

$$\theta_T < (T_J - T_A)/P_D \quad (28)$$

where

- θ_T is the total thermal impedance ($\theta_{JC} + \theta_{SA}$),
- θ_{JC} is the junction−to−case thermal impedance of the MOSFET,
- θ_{SA} is the sink−to−ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET (no thermal "pad" is used),
- T_J is the specified maximum allowed junction temperature,
- T_A is the worst case ambient operating temperature.

For TO−220 and TO−263 packages, standard FR−4 copper clad circuit boards will have approximate thermal resistances (θ_{SA}) as shown in the following table.

Pad Size (in^2/mm^2)	Single−Sided 1 oz. Copper
0.5/323	60−65°C/W
0.75/484	55−60°C/W
1.0/645	50−55°C/W
1.5/968	45−50°C/W
2.0/1290	38−42°C/W
2.5/1612	33−37°C/W

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e., worst case MOSFET $R_{DS(on)}$). Also, the inductors and capacitors share the MOSFET's heatsinks and will add heat and raise the temperature of the circuit board and MOSFET. For any new design, its advisable to have as much heatsink area as possible − all too often new designs are found to be too hot and require redesign to add heatsinking.

6. Adaptive Voltage Positioning

There are two resistors that determine the Adaptive Voltage Positioning, R_{F1} and R_{DRP}. R_{F1} establishes the no−load "high" voltage position and R_{DRP} determines the full−load "droop" voltage.

Resistor R_{F1} is connected between V_{CORE} and the V_{FB} pin of the controller. At no load, this resistor will conduct the internal bias current of the V_{FB} pin and develop a voltage drop from V_{CORE} to the V_{FB} pin. Because the error amplifier regulates V_{FB} to the DAC setting, the output voltage, V_{CORE}, will be higher by the amount $IBIAS_{VFB} \cdot R_{F1}$. This condition is shown in Figure 33.

To calculate R_{F1} the designer must specify the no−load voltage increase above the VID setting ($\Delta V_{NO-LOAD}$) and determine the V_{FB} bias current. Usually, the no−load voltage increase is specified in the design guide for the processor that is available from the manufacturer. The V_{FB} bias current is determined by the value of the resistor from R_{OSC} to ground (see Figure TBD for a graph of $IBIAS_{VFB}$ versus R_{OSC}). The value of R_{F1} can then be calculated.

$$R_{F1} = \Delta V_{NO-LOAD} / IBIAS_{VFB} \quad (29)$$

Resistor R_{DRP} is connected between the V_{DRP} and the V_{FB} pins. At no−load, the V_{DRP} and the V_{FB} pins will both be at the DAC voltage so this resistor will conduct zero current. However, at full−load, the voltage at the V_{DRP} pin will increase proportional to the output inductor's current while V_{FB} will still be regulated to the DAC voltage. Current will be conducted from V_{DRP} to V_{FB} by R_{DRP}. This current will be large enough to supply the V_{FB} bias current and cause a voltage drop from V_{FB} to V_{CORE} across R_{F1} − the converter's output voltage will be reduced. This condition is shown in Figure 34.

To determine the value of R_{DRP} the designer must specify the full−load voltage reduction *from the VID* (DAC) setting ($\Delta V_{CORE,FULL-LOAD}$) and predict the voltage increase at the V_{DRP} pin at full−load. Usually, the full−load voltage reduction is specified in the design guide for the processor that is available from the manufacturer. To predict the voltage increase at the V_{DRP} pin at full−load (ΔV_{DRP}), the designer must consider the output inductor's resistance (R_L), the PCB trace resistance between the current sense points (R_{PCB}), and the controller IC's gain from the current sense to the V_{DRP} pin (G_{VDRP}).

$$\Delta V_{DRP} = I_{O,MAX} \cdot (R_L + R_{PCB}) \cdot G_{VDRP} \quad (30)$$

The value of R_{DRP} can then be calculated.

$$R_{DRP} = \frac{\Delta V_{DRP}}{(IBIAS_{VFB} + \Delta V_{CORE,FULL-LOAD}/R_{F1})} \quad (31)$$

$\Delta V_{CORE,FULL-LOAD}$ is the full−load voltage reduction from the VID (DAC) setting. $\Delta V_{CORE,FULL-LOAD}$ is *not* the voltage change from the no−load AVP setting.

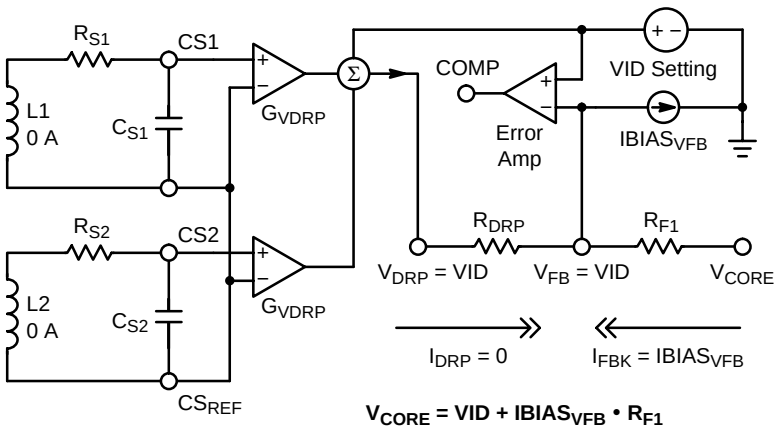
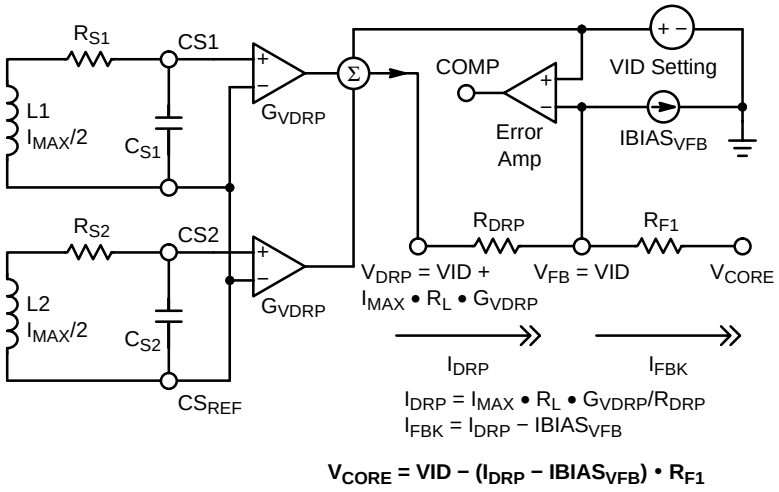
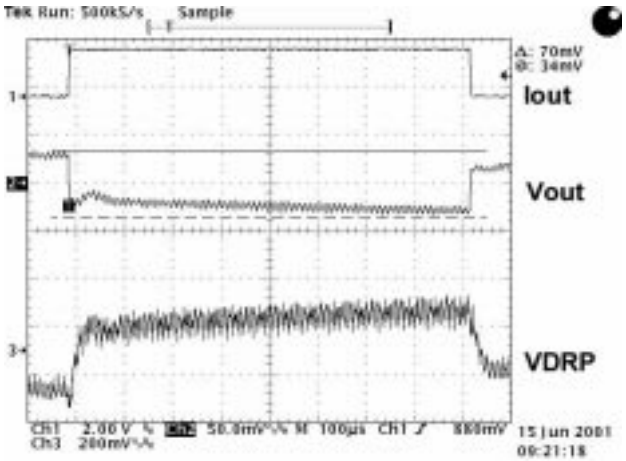


Figure 33. AVP Circuitry at No−Load



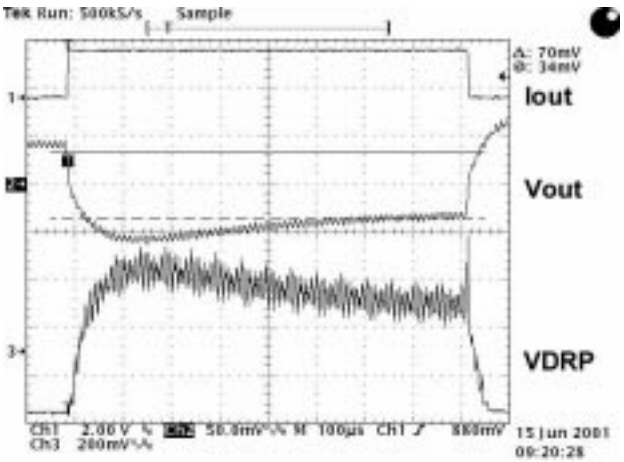
$$V_{CORE} = VID - (I_{DRP} - IBIAS_{VFB}) \cdot R_{F1}$$

Figure 34. AVP Circuitry at Full−Load



NOTE: The RC time constant of the current sense network is too long (slow); V_{DRP} and V_{CORE} respond too slowly.

Figure 35. V_{DRP} Tuning, RC Time Too Long



NOTE: The RC time constant of the current sense network is too short (fast); V_{DRP} and V_{CORE} both overshoot.

Figure 36. V_{DRP} tuning, RC Time Too Short

7. Current Sensing

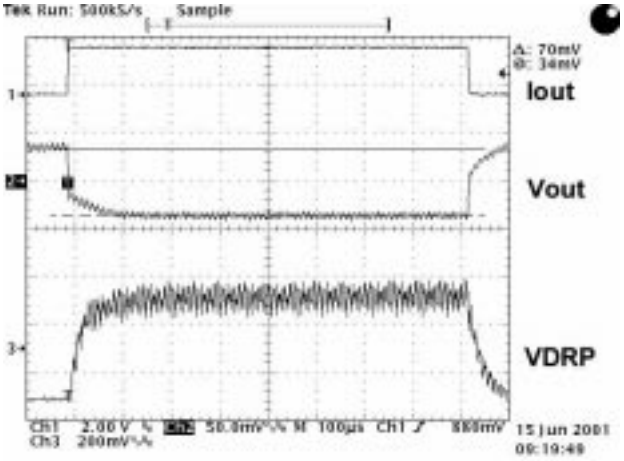
For inductive current sensing, choose the current sense network (RSx, CSx) to satisfy

$$RSx \cdot CSx = Lo/(R_L + R_{PCB}) \quad (32)$$

For resistive current sensing, choose the current sense network (RSx, CSx) to satisfy

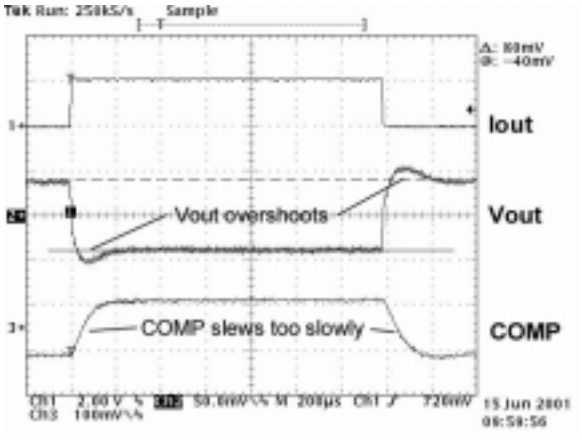
$$RSx \cdot CSx = Lo/(R_{sense}) \quad (33)$$

This will provide an adequate starting point for RSx and CSx. After the converter is constructed, the value of RSx (and/or LSx) should be fine−tuned in the lab by observing the V_{DRP} signal during a step change in load current. Tune the RSx · CSx network to provide a "square−wave" at the V_{DRP} output pin with maximum rise time and minimal overshoot as shown in Figures 34 − 36.



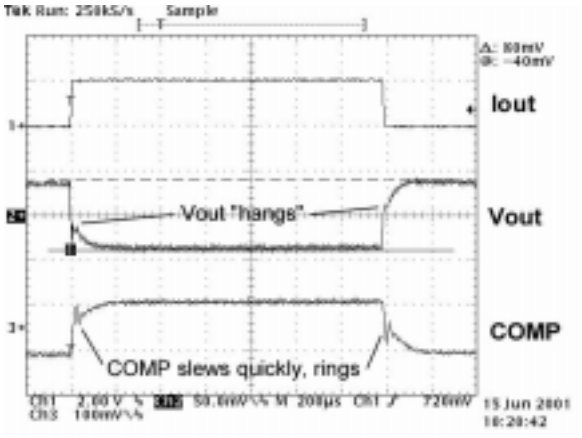
NOTE: The RC time constant of the current sense network is optimal; V_{DRP} and V_{CORE} respond to the load current quickly without overshooting.

Figure 37. V_{DRP} Tuning, RC Time Optimal



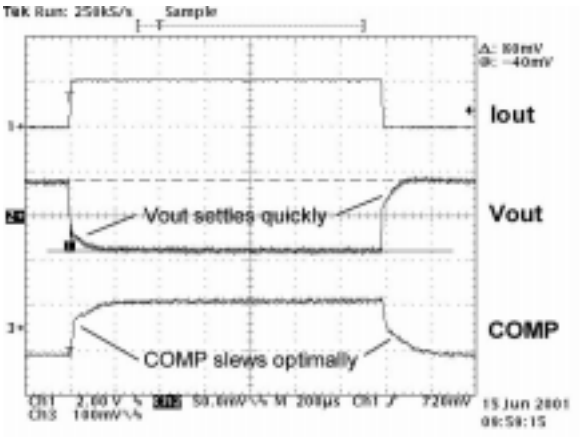
NOTE: The value of C_{A1} is too high and the loop gain/ bandwidth too low. COMP slews too slowly which results in overshoot in V_{CORE}.

Figure 38. COMP Tuning, Bandwidth Too Low



NOTE: The value of C_{A1} is too low and the loop gain/ bandwidth too high. COMP moves too quickly, which is evident from the small spike in its voltage when the load is applied or removed. The output voltage transitions more slowly because of the COMP spike.

Figure 39. COMP Tuning, Bandwidth Too High



NOTE: The value of C_{A1} is optimal. COMP slews quickly without spiking or ringing. V_{CORE} does not overshoot and monotonically settles to its final value.

Figure 40. COMP Tuning, Bandwidth Optimal

8. Error Amplifier Tuning

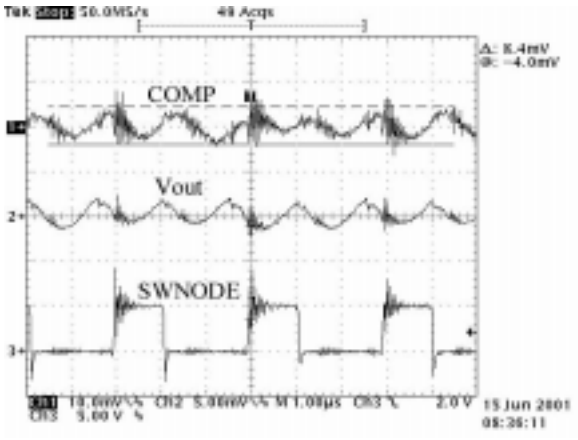
After the steady−state (static) AVP has been set and the current sense network has been optimized the Error Amplifier must be tuned. Basically, the gain of the Error Amplifier should be adjusted to provide an acceptable transient response by increasing or decreasing the Error Amplifier's feedback capacitor (C_{A1} in the Applications Diagram). The bandwidth of the control loop will vary directly with the gain of the error amplifier.

If C_{A1} is too large the loop gain/bandwidth will be low, the COMP pin will slew too slowly, and the output voltage will overshoot as shown in Figure 38. On the other hand, if C_{A1} is too small the loop gain/bandwidth will be high, the COMP pin will slew very quickly and overshoot. Integrator "wind up" is the cause of the overshoot. In this case the output voltage will transition more slowly because COMP spikes upward as shown in Figure 39. Too much loop gain/bandwidth increase the risk of instability. In general, one should use the lowest loop gain/bandwidth as possible to achieve acceptable transient response − this will insure good stability. If C_{A1} is optimal the COMP pin will slew quickly but not overshoot and the output voltage will monotonically settle as shown in Figure 40.

After the control loop is tuned to provide an acceptable transient response the steady−state voltage ripple on the COMP pin should be examined. When the converter is operating at full, steady−state load, the peak−to−peak voltage ripple on the COMP pin should be less than 20 mVpp as shown in Figure 41. Less than 10 mVpp is ideal. Excessive ripple on the COMP pin will contribute to output voltage jitter.

9. Current Limit Setting

When the output of the current sense amplifier (CO1 or CO2 in the block diagram) exceeds the voltage on the I_{LIM} pin the part will enter hiccup mode. For inductive sensing, the I_{LIM} pin voltage should be set based on the inductor's maximum resistance (R_{LMAX}). The design must consider



NOTE: At full load the peak−to−peak voltage ripple on the COMP pin should be less than 20 mV for a well−tuned/stable controller. Higher COMP voltage ripple will contribute to output voltage jitter.

Figure 41. COMP Ripple for a Stable System

the inductor's resistance increase due to current heating and ambient temperature rise. Also, depending on the current sense points, the circuit board may add additional resistance. In general, the temperature coefficient of copper is +0.393% per °C. If using a current sense resistor (R_{SENSE}), the I_{LIM} pin voltage should be set based on the maximum value of the sense resistor. To set the level of the I_{LIM} pin,

$$V_{ILIM} = (I_{OUT,LIM} + \Delta I_{Lo}/2) \cdot R \cdot G_{ILIM} \quad (34)$$

where

$I_{OUT,LIM}$ is the current limit threshold of the converter,
$\Delta I_{Lo}/2$ is half the inductor ripple current,
R is either (R_{LMAX} + R_{PCB}) or R_{SENSE},
G_{ILIM} is the current sense to I_{LIM} gain.

For the overcurrent protection to work properly, the current sense time constant (RC) should be slightly larger than the RL time constant. If the RC time constant is too fast, during step load changes the sensed current waveform will appear larger than the actual inductor current and will probably trip the current limit at a lower level than expected.

10. Overcurrent Timer

The overcurrent timer sets the time the converter will allow hiccup mode operation. Given the capacitance from the C_{OVC} pin to GND, the nominal overcurrent time (t_{OVC}) can be calculated from the following equation.

$$t_{OVC} = C_{OVC} \cdot (OVC_{THRESH} - OVC_{MIN})/I_{OVC} \quad (35)$$
$$= C_{OVC} \cdot (3.0\ V - 0.25\ V)/5.0\ \mu A$$
$$= C_{OVC} \cdot 5.5 \times 10^5$$

where

OVC_{THRESH} is the overcurrent timer's shutdown voltage, nominally 3 V,
OVC_{MIN} is the overcurrent timer's starting voltage, nominally 0.25 V,
I_{OVC} is the charge current supplied to the capacitor at the C_{OVC} pin, nominally 5 μA.

11. Soft Start Time

The Soft Start time (t_{SS}) can be calculated from

$$t_{SS} = (V_{COMP} - R_{C1} \cdot I_{COMP}) \cdot C_{C2}/I_{COMP} \quad (36)$$

where

$$V_{COMP} = V_{CORE}\ @\ 0\ A + Channel_Startup_Offset + Int_Ramp + G_{CSA} \cdot Ext_Ramp/2$$

$$Ext_Ramp = D \cdot (V_{IN} - V_{CORE})/(R_{CSx} \cdot C_{CSx} \cdot f_{SW})$$

$$Int_Ramp = 125\ mV \cdot D/0.50$$

I_{COMP} is the COMP source current from the data sheet,
Int_Ramp is the internal ramp value at the corresponding duty cycle,
Ext_Ramp is the peak−to−peak external steady−state ramp at 0 A,
G_{CSA} is the Current Sense Amplifier Gain (nominally 2.0 V/V),
Startup Offset is typically 0.60V.

12. Power Good Delay Time

The power good timer sets the delay time between when V_{CORE} exceeds the C_{PGD} comparator's threshold voltage and when PGD will actually transition high. The PGD delay time can be calculated from

$$t_{PGD} = C_{PGD} \cdot (PGD_{THRESH} - PGD_{MIN})/I_{PGD} \quad (37)$$
$$= C_{PGD} \cdot (3.0\ V - 0.25V)/I_{PGD}$$

where

PGD_{THRESH} is the PGD comparator's threshold voltage, nominally 3 V,
PGD_{MIN} is the PGD timer's starting voltage, nominally 0.25 V,
I_{PGD} is the charge current supplied to the capacitor at the C_{PGD} pin. This current is a function of the R_{OSC} resistor according to I_{PGD} = 0.52 V/R_{OSC}.

Design Example

Typical Design Requirements:

V_{IN} = 12.0 Vdc
V_{CORE} = 1.20 Vdc (nominal)
$V_{OUT,RIPPLE}$ < 20 mV_{PP} max
VID Range: 0.800 Vdc − 1.550 Vdc
$I_{O,MAX}$ = 52 A at full−load
$I_{OUT,LIM}$ = 72 Adc
dI_{IN}/dt = 0.50 A/μs max
f_{SW} = 200 kHz
η = 80% min at full−load
$T_{A,MAX}$ = 55°C
$T_{J,MAX}$ = 120°C
t_{SS} = 6.0 ms (Soft Start time)
t_{OVC} = 120 ms (Overcurrent time)
t_{PGD} = 6.0 ms (PGD Delay time)
ΔV_{CORE} at no−load (static) =
−25 mV from VID setting = 1.225 Vdc
ΔV_{CORE} at full−load (static) =
–37 mV from VID setting = 1.163 Vdc
ΔV_{CORE} transient loading from 3.0 A to 25 A =
−50 mV from VID setting = 1.150 Vdc

1. Output Capacitor Selection

First, choose a low−cost, low−ESR output capacitor such as the Rubycon 16MBZ1000M10X16: 16 V, 1000 μF, 2.55 A_{RMS}, 19 mΩ, 10 × 16 mm. Calculate the minimum number of output capacitors.

$$N_{OUT,MIN} = ESR\ per\ capacitor \cdot \frac{\Delta I_{O,MAX}}{\Delta V_{O,MAX}} \quad (1)$$
$$= 19\ m\Omega \cdot 22\ A/(1.225\ V - 1.150\ V)$$
$$= 5.6\ or\ 6\ capacitors\ minimum\ (6000\ \mu F)$$

2. Output Inductor Selection

Calculate the minimum output inductance at $I_{O,MAX}$ according to Equation 3 with ±20% inductor ripple current ($\alpha = 0.15$).

$$Lo_{MIN} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{(\alpha \cdot I_{O,MAX} \cdot V_{IN} \cdot f_{SW})} \quad (3)$$
$$= \frac{(12\ V - 1.163\ V) \cdot 1.163\ V}{(0.15 \cdot 52\ A \cdot 12\ V \cdot 200\ kHz)}$$
$$= 673\ nH$$

To minimize core losses, we choose the T50−8B/90 core from Micrometals: 23.0 nH/N^2, 2.50 cm/turn. According to the Micrometals catalog, at 26 A (per phase) the permeability of this core will be approximately 88% of the permeability at 0 A. Therefore, at 0 A we must achieve at least 673 nH/0.88 or 765 nH. Using 6 turns of #16 AWG bifilar (2 mΩ/ft) will produce **828 nH**.

We will need the nominal and worst case inductor resistances for subsequent calculations.

$$R_L = 6\ turns \cdot 2.5\ cm/turn \cdot 0.03218\ ft/cm \cdot 2\ m\Omega/ft$$
$$= 0.965\ m\Omega$$

The inductor resistance will be maximized when the inductor is “hot” due to the load current and the ambient temperature is high. Assuming a 50°C temperature rise of the inductor at full−load and a 35°C ambient temperature rise we can calculate

$$R_{L,MAX} = 0.965\ m\Omega \cdot [1 + 0.39\%/^{\circ}C \cdot (50^{\circ}C + 35^{\circ}C)]$$
$$= 1.28\ m\Omega$$

The output inductance at full−load will be reduced due to the saturation characteristic of the core material.

$$Lo_{52\ A} = 0.88 \times 828\ nH = 729\ nH\ at\ full\ load$$

Next, use Equation 4 to insure the output voltage ripple will satisfy the design goal with the minimum number of output capacitors and the full load output inductance.

$$V_{OUT,P-P} = (ESR\ per\ cap\ /\ N_{OUT,MIN}) \quad (4)$$
$$\cdot \{(V_{IN} - \#Phases \cdot V_{CORE}) \cdot D\ /\ (Lo_{52\ A} \cdot f_{SW})\}$$
$$= (19\ m\Omega/6) \cdot \{(12\ V - 2 \cdot 1.163\ V)$$
$$\cdot (1.163\ V/12\ V)/(729\ nH \cdot 200\ kHz)\}$$
$$= 20\ mV$$

So, the ripple requirement will be satisfied if the minimum number of output capacitors is used. More output capacitors will probably be required to satisfy the transient requirement, which will result in a lower ripple voltage.

3. Input Capacitor Selection

Use Equation 5 to determine the average input current to the converter at full−load.

$$I_{IN,AVG} = I_{O,MAX} \cdot D/\eta \quad (5)$$
$$= 52\ A \cdot (1.163\ V/12\ V)/0.80 = 6.30\ A$$

Next, use Equation 6 to Equation 10 with the full−load inductance value of 729 nH.

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \cdot D/(Lo \cdot f_{SW})$$
$$= (12\ V - 1.163\ V) \cdot \frac{(1.163\ V/12\ V)}{(729\ nH \cdot 200\ kHz)} \quad (10)$$
$$= 7.20\ App$$

$$I_{Lo,MAX} = I_{O,MAX}/2 + \Delta I_{Lo}/2 \quad (8)$$
$$= 52\ A/2 + 7.20\ App/2 = 29.6\ A$$

$$I_{Lo,MIN} = I_{O,MAX}/2 - \Delta I_{Lo}/2 \quad (9)$$
$$= 52\ A/2 - 7.20\ App/2 = 22.4\ A$$

$$I_{C,MAX} = I_{Lo,MAX}/\eta - I_{IN,AVG} \quad (6)$$
$$= 29.6\ A/0.80 - 6.30\ A = 30.7\ A$$

$$I_{C,MIN} = I_{Lo,MIN}/\eta - I_{IN,AVG} \quad (7)$$
$$= 22.4\ A/0.80 - 6.30\ A = 21.7\ A$$

For the two−phase converter, the input capacitor(s) rms current at full−load is as follows. (Note: D = 1.163 V/12 V = 0.097.)

$$I_{CIN,RMS} = [2D \cdot (I_{C,MIN}^2 + I_{C,MIN} \cdot \Delta I_{C,IN} \quad (11)$$
$$+ \Delta I_{C,IN}^2/3) + I_{IN,AVG}^2 \cdot (1 - 2D)]^{1/2}$$
$$= [0.19 \cdot (21.7^2 + 21.7 \cdot 9.0 + 9.0^2/3)$$
$$+ 6.30^2 \cdot (1 - 0.19)]^{1/2}$$
$$= 12.9\ A_{RMS}$$

At this point, the designer must decide between saving board space by using higher−rated/more costly capacitors or saving cost by using more lower−rated/less costly capacitors. To save cost, we choose the MBZ series capacitors by Rubycon. Part number 16MBZ1500M10X20: 1500 μF, 16 V, 2.55 A_{RMS}, 13 mΩ, 10 × 20 mm. This design will require N_{IN} = 12.8 A/2.55 A = 5 capacitors on the input for a cost sensitive design or 6 capacitors for a conservative design.

4. Input Inductor Selection

For the Claw Hammper CPU, the input inductor must limit the input current slew rate to less than 0.5 A/μs during a load transient from 0 to 52 A. A conservative value will be calculated assuming the minimum number of output capacitors (N_{OUT} = 6), five input capacitors (N_{IN} = 5), worst case ESR values for both the input and output capacitors, and a maximum duty cycle at the maximum DAC setting with 25 mV of no−load AVP.

$$D_{MAX} = (1.550\ V + 25\ mV_{AVP})/10.8\ V_{IN} = 0.146$$

First, use Equation 15 to calculate the voltage across the output inductor due to the 52 A load current being shared equally between the two phases.

$$\Delta V_{Lo} = V_{IN} - V_{CORE,NO-LOAD} + (I_{O,MAX}/2) \cdot ESR_{OUT}/N_{OUT} \quad (15)$$
$$= 12\ V - 1.575\ V + 52\ A/2 \cdot 19\ m\Omega/6$$
$$= 10.51\ V$$

Second, use Equation 16 to determine the rate of current increase in the output inductor when the load is applied (i.e., Lo has decreased to 88% due to the dc current).

$$dI_{Lo}/dt = \Delta V_{Lo}/Lo \quad (16)$$
$$= 10.51\ V/729\ nH = 14.4\ V/\mu s$$

Finally, use Equation 17 and Equation 18 to calculate the minimum input inductance value.

$$\Delta V_{Ci} = ESR_{IN}/N_{IN} \cdot dI_{Lo}/dt \cdot D/f_{SW} \quad (17)$$
$$= 13\ m\Omega/5 \cdot 14.4\ V/\mu s \cdot 0.146/200\ kHz$$
$$= 28\ mV$$

$$Li_{MIN} = \Delta V_{Ci} / dI_{IN}/dt_{MAX} \quad (18)$$
$$= 28\ mV/0.50\ A/\mu s = 55\ nH$$

Next, choose the small, cost effective **T30−26** core from Micrometals (33.5 nH/N^2) with #16 AWG. The design requires only 1.28 turns to achieve the minimum inductance value. We allow for inductance "swing" at full−load by using three turns. The input inductor's value will be

$$L_i = 3^2 \cdot 33.5\ nH/N^2 = \mathbf{301\ nH}$$

This inductor is available as part number CTX15−14771 from Coiltronics.

5. MOSFET & Heatsink Selection

For the upper MOSFET we choose two (1) NTD60N03 and for the lower MOSFETs we choose two (2) NTD80N02, both are from ON Semiconductor. The following parameters are derived from the data sheets.

NCP5331 Parameter	Value
Gate Drive Current	1.5 A for 1.0 μs
Upper Gate Voltage	6.5 V
Lower Gate Voltage	11.5 V
Gate Nonoverlap Time	65 ns

Parameter	NTD60N03	NTD80N02
$R_{DS(on)}$	8.0 mΩ @ 6.5 V	5.0 mΩ @ 10 V
Q_{SWITCH}	27 nC	26 nC
Q_{RR}	43 nC	36 nC
Q_{OSS}	12 nC	12 nC
$V_{F,diode}$	0.75 V @ 2.3 A	0.92 V @ 20 A
θ_{JC}	1.65°C/W	1.65°C/W

The rms value of the current in the control MOSFET is calculated from Equation 20 and the previously derived values for D, I_{LMAX}, and I_{LMIN} at the converter's maximum output current.

$$I_{RMS,CNTL} = [D \cdot (I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (20)$$
$$= 0.097 \cdot [(29.6^2 + 29.6 \cdot 22.4 + 22.4^2)/3]^{1/2}$$
$$= 2.53\ A_{RMS}$$

Equation 19 is used to calculate the power dissipation of the control MOSFET but has been modified for one upper and two lower MOSFETs.

$$P_{D,CONTROL} = \{(I_{RMS,CNTL}^2) \cdot R_{DS(on)}\} + (I_{Lo,MAX} \cdot Q_{switch}/I_g \cdot V_{IN} \cdot f_{SW}) + (3 \cdot Q_{oss}/2 \cdot V_{IN} \cdot f_{SW}) + (V_{IN} \cdot Q_{RR} \cdot f_{SW}) \quad (19)$$
$$= \{2.53^2\ A_{RMS} \cdot 8.0\ m\Omega\} + (29.6\ A \cdot 27\ nC/1.5\ A \cdot 12\ V \cdot 200\ kHz) + (3 \cdot 12\ nC/2 \cdot 12\ V \cdot 200\ kHz) + (12\ V \cdot 43\ nC \cdot 200\ kHz)$$
$$= 0.051\ W + 1.28\ W + 0.043\ W + 0.10\ W$$
$$= \mathbf{1.48\ W\ per\ FET}$$

The rms value of the current in the synchronous MOSFET is calculated from Equation 27 and the previously derived values for D, $I_{Lo,MAX}$, and $I_{Lo,MIN}$ at the converter's maximum output current.

$$I_{RMS,SYNCH} = [(1 - D) \cdot (I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (27)$$
$$= (1 - 0.097) \cdot [(29.6^2 + 29.6 \cdot 22.4 + 22.4^2)/3]^{1/2}$$
$$= 23.5\ A_{RMS}\ \text{(shared by two synchronous MOSFETs)}$$

Equation 26 is used to calculate the power dissipation of each synchronous MOSFET. Note: The rms current is shared by the two lower MOSFETs so the total rms current is divided by two in the following equation. Also, during the nonoverlap time, the per−phase current is shared by two body diodes so the full load current is divided between two phases and two forward body diodes per phase.

$$P_{D,SYNCH} = (I_{RMS,SYNCH}^2 \cdot R_{DS(on)}) + (Vf_{diode} \cdot I_{O,MAX}/2 \cdot t_nonoverlap \cdot f_{SW}) \quad (26)$$
$$= \{(23.5/2)^2\ A_{RMS} \cdot 5.0\ m\Omega\} + \{0.92\ V \cdot (52\ A/2/2) \cdot 65\ ns \cdot 200\ kHz\}$$
$$= 0.69\ W + 0.16\ W = \mathbf{0.85\ W\ per\ FET}$$

Equation 28 is used to calculate the heat sink thermal impedances necessary to maintain less than the specified maximum junction temperatures at 55°C ambient.

$$\theta_{CNTRL_{SA}} < (120 - 55^{\circ}C)/1.48\ W - 1.65^{\circ}C/W$$
$$= 42.3^{\circ}C/W$$

$$\theta_{SYNCH_{SA}} < (120 - 55^{\circ}C)/0.85\ W - 1.65^{\circ}C/W$$
$$= 74.8^{\circ}C/W \text{ per MOSFET}$$

or **37.4°C/W per phase** for two MOSFETs/phase

If board area permits, a cost effective heatsink could be formed by using a TO−263 mounting pad of at least 2.0 in^2 (1282 mm^2) for the upper and lower MOSFETs on a single−sided, 1 oz copper PCB. The total required pad area would be slightly less if the area were divided evenly between top and bottom layers with multiple thermal vias joining the two areas. To conserve board space, AAVID offers clip−on heatsinks for TO−220 thru−hole packages. Examples of these heatsinks include #577002 (1″ × 0.75″ × 0.25″, 33°C/W at 2 W) and #591302 (0.75″ × 0.5″ × 0.5″, 29°C/W at 2 W).

6. Adaptive Voltage Positioning

First, to achieve the 200 kHz switching frequency, use Figure 5 to determine that a **51 kΩ** resistor is needed for R_{OSC}. Then, use Figure 6 to find the V_{FB} bias current at the corresponding value of R_{OSC}. In this example, the 51 kΩ R_{OSC} resistor results in a V_{FB} bias current of approximately 7.0 μA. Knowing the V_{FB} bias current, one can calculate the required values for R_{F1} and R_{DRP} using Equation 29 through Equation 31.

The no−load position is easily set using Equation 29.

$$R_{VFBK} = \Delta V_{NO-LOAD}/IBIAS_{VFB} \quad (29)$$
$$= +25\ mV/7.0\ \mu A$$
$$= \mathbf{3.6\ k\Omega}$$

For inductive current sensing, the designer must calculate the inductor's resistance (R_L) and approximate any resistance added by the circuit board (R_{PCB}). We found the inductor's nominal resistance in Section 2 (0.965 mΩ). In this example, we assume **0.2 mΩ** for the circuit board resistance (R_{PCB}). With this information, Equation 30 can be used to calculate the increase at the V_{DRP} pin at full load.

$$\Delta V_{DRP} = I_{O,MAX} \cdot (R_L + R_{PCB}) \cdot G_{VDRP} \quad (30)$$
$$= 52\ A \cdot (0.965\ m\Omega + 0.2\ m\Omega) \cdot 4.2\ V/V$$
$$= 0.254\ mV$$

R_{DRP} can then be calculated from Equation 31.

$$R_{DRP} = \frac{\Delta V_{DRP}}{(IBIAS_{VFB} + \Delta V_{CORE,FULL-LOAD}/R_{F1})} \quad (31)$$
$$= 254\ mV/(7.0\ \mu A + 37\ mV/3.6\ k\Omega)$$
$$= 14.7\ k\Omega$$

7. Current Sensing

Choose the current sense network (R_{Sx}, C_{Sx}, x = 1 or 2) to satisfy

$$R_{Sx} \cdot C_{Sx} = Lo/(R_L + R_{PCB}) \quad (32)$$

Equation 32 will be most accurate for better iron powder core material (such as the −8 from Micrometals). This material is very consistent with dc current and frequency. Less expensive core materials (such as the −52 from Micrometals) change their characteristics with dc current, ac flux density, and frequency. This material will yield acceptable converter performance if the current sense time constant is set lower (longer) than anticipated. As a rule of thumb, start with approximately twice the resistance (R_{Sx}) or twice the capacitance (C_{Sx}) when using the less expensive core material.

The component values determined thus far are L_o = 828 nH, R_L = 0.965 mΩ, and R_{PCB} = 0.2 mΩ. We choose a convenient value for C_{S1} (0.1 μF) and solve for R_{Sx}.

$$R_{Sn} = 828\ nH/(0.965\ m\Omega + 0.2\ m\Omega) \cdot 0.1\ \mu F$$
$$= \mathbf{7.10\ k\Omega}$$

After the circuit is constructed, the values of R_{Sx} and/or C_{Sx} should be tuned to provide a "square−wave" at the V_{DRP} pin with minimal overshoot and fast rise time due to a step change in load current as shown in Figure 35, Figure 36 and Figure 37. This testing has shown that for a 3 to 25 A transient, a value of 10.0 kΩ will produce the desired square wave at V_{DRP}.

8. Error Amplifier Tuning

The error amplifier is tuned by adjusting C_{A1} to provide an acceptable full−load transient response as shown in Figure 38, Figure 39 and Figure 40. After a value for C_{A1} is chosen, the peak−to−peak voltage ripple on the COMP pin is examined under full−load to insure less than 20 mVpp as shown in Figure 41.

9. Current Limit Setting

The maximum inductor resistance, the maximum PCB resistance, and the maximum current−sense gain determine the current limit as shown in Equation 34. The maximum current, $I_{OUT,LIMIT}$, was specified in the design requirements. The maximum inductor resistance occurs at full load and the highest ambient temperature. This value was found in the "Output Inductor Section" (1.28 mΩ). This analysis assumes the PCB resistance only increases due to the change in ambient temperature. Component heating will also increase the PCB temperature but quantifying this effect is difficult. Lab testing should be used to "fine tune" the overcurrent threshold.

$$R_{PCB,MAX} = 0.2\ m\Omega \cdot \{1 + 0.39\%/^{\circ}C$$
$$\cdot (100^{\circ}C - 25^{\circ}C)\}$$
$$= 0.26\ m\Omega$$

$$V_{ILIM} = (I_{OUT,LIM} + \Delta I_{Lo}/2) \cdot (R_{LMAX} + R_{PCB,MAX}) \cdot G_{ILIM}$$
$$= (72\ A + 7.20\ A/2) \cdot (1.28\ m\Omega + 0.26\ m\Omega) \cdot 12\ V/V$$
$$= 1.4\ Vdc$$

Set the voltage at the I_{LIM} pin using a resistor divider from the 5.0 V reference output as shown in Figure 42. If the resistor from I_{LIM} to GND is chosen to be 910 Ω (R_{LIM2}), then the resistor from I_{LIM} to 5.0 V_{REF} can be calculated from

$$R_{LIM1} = (V_{REF} - V_{ILIM})/(V_{ILIM}/R_{LIM2})$$
$$= (5.0\ V - 1.4\ V)/(1.4\ V/910\ \Omega)$$
$$= 2340\ \Omega \text{ or } \mathbf{2.37\ k\Omega}$$

10. Overcurrent Timer

To set the overcurrent timer, solve Equation 35 for C_{OVC} and substitute t_{OVC} = 120 ms.

$$C_{OVC} = t_{OVC}/(5.5 \times 10^5) \quad (35)$$
$$= 120\ ms/(5.5 \times 10^5)$$
$$= 0.218\ \mu F \text{ or } \mathbf{0.22\ \mu F}$$

11. Soft Start Time

To set the Soft Start time, first calculate the external ramp size at a duty−cycle of D = 1.225 V/12 V = 0.102.

$$Ext_Ramp = D \cdot \frac{(V_{IN} - V_{OUT})}{(R_{Sx} \cdot C_{Sx} \cdot f_{SW})}$$
$$= 0.102 \cdot \frac{(12\ V - 1.225\ V)}{(10.0\ k\Omega \cdot 0.1\ \mu F \cdot 200\ kHz)}$$
$$= 5.5\ mV$$

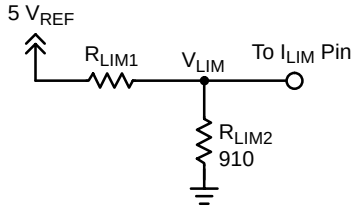


Figure 42. Setting the Current Limit

Then calculate the steady−state COMP voltage.

$$V_{COMP} = V_{OUT} @ 0\ A + Channel_Startup_Offset + Int_Ramp + G_{CSA} \cdot Ext_Ramp/2$$
$$= 1.225\ V + 0.60\ V + 0.102 \cdot 250\ mV + 4.0\ V/V \cdot 5.3\ mV/2$$
$$= 1.86\ V$$

Finally, solve Equation 35 for the soft−start capacitor, C_{C2}, and substitute as required.

$$C_{C2} = (t_{SS} \cdot I_{COMP})/(V_{COMP} - R_{C1} \cdot I_{COMP}) \quad (36)$$
$$= (6\ ms \cdot 30\ \mu A)/(1.86\ V - 7.5\ k\Omega \cdot 30\ \mu A)$$
$$= 0.11\ \mu F \text{ or } \mathbf{0.1\ \mu F}$$

12. Power Good Delay Time

First, use the previously derived value for R_{OSC} to calculate the current that will be supplied to the C_{PGD} capacitor.

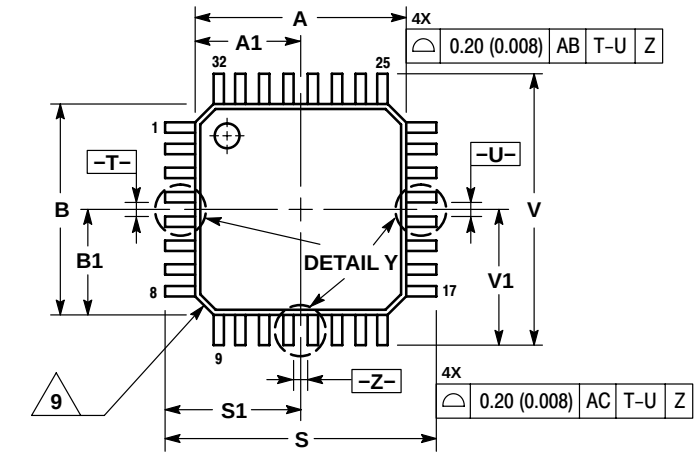
$$I_{PGD} = 0.52\ V/R_{OSC}$$
$$= 0.52\ V/51\ k\Omega$$
$$= 10.2\ \mu A$$

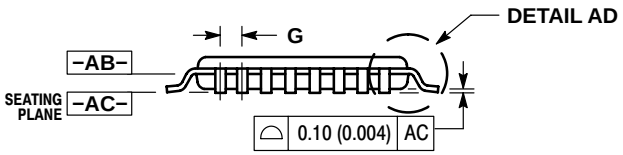
Next, solve equation 37 for C_{PGD} and substitute as required.

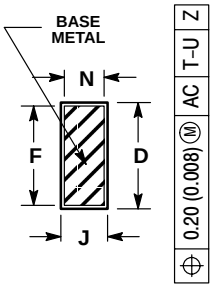
$$C_{PGD} = t_{PGD} \cdot I_{PGD}/(PGD_{THRESH} - PGD_{MIN}) \quad (37)$$
$$= 6\ ms \cdot 10.2\ \mu A/(3.0\ V - 0.25\ V)$$
$$= \mathbf{0.022\ \mu F}$$

PACKAGE DIMENSIONS

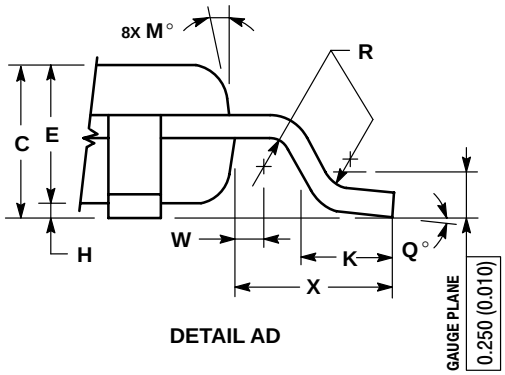
LQFP−32
FT SUFFIX
CASE 873A−02
ISSUE B



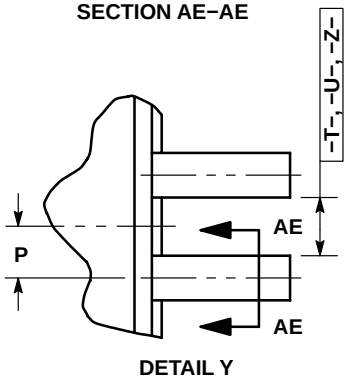




SECTION AE−AE



DETAIL AD



DETAIL Y

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −AB− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS −T−, −U−, AND −Z− TO BE DETERMINED AT DATUM PLANE −AB−.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE −AC−.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −AB−.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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