MAX16813B

Integrated, 4-Channel, High-Brightness LED Driver with High-Voltage DC-DC Controller and Battery Disconnect

General Description

The MAX16813B high-efficiency, high-brightness LED (HB LED) driver provides four integrated LED current-sink channels. An integrated current-mode switching controller drives a DC-DC converter that provides the necessary voltage to multiple strings of HB LEDs. The device accepts a wide 4.75V to 40V input voltage range and withstands direct automotive load-dump events. The wide input range allows powering HB LEDs for small- to medium-sized LCD displays in automotive and general lighting applications.

An internal current-mode switching DC-DC controller supports boost or SEPIC topologies and operates in an adjustable frequency range between 200kHz and 2MHz. An integrated spread-spectrum mode helps reduce EMI. Current-mode control with programmable slope compensation provides fast response and simplifies loop compensation. An adaptive output-voltage control scheme minimizes power dissipation in the LED current-sink paths. The device has a separate p-channel drive (PGATE) pin that is used for output undervoltage protection. Whenever the output falls below the threshold, the external p-MOSFET is latched off, disconnecting the input source. Cycling the EN or the input supply is required to restart the converter. The external p-MOSFET is off when the EN pin is below 0.3V (typ). The shutdown current is 1µA (typ) at an input voltage of 12V.

The device consists of four identical linear current-sink channels, adjustable from 20mA to 150mA with an accuracy of ±3% using a single external resistor. Multiple channels can be connected in parallel to achieve higher current per LED string. The device also features a unique pulsed dimming control through a logic input (DIM), with minimum pulse width as low as 500ns. Protection features include output overvoltage, open-LED detection and protection, programmable shorted-LED detection and protection, output undervoltage detection and protection, and overtemperature protection. The device operates over the -40°C to +125°C automotive temperature range. The MAX16813B is available in 20-pin (6.5mm x 4.4mm) TSSOP and 20-pin (4mm x 4mm) TQFN packages.

Benefits and Features

- 4-Channel Linear LED Current Sinks with Internal MOSFETs Independently Drive Multiple LED Strings
  - Full-Scale LED Current, Adjustable from 20mA to 150mA
  - Drives 1 to 4 LED Strings
  - 10000:1 PWM Dimming at 200Hz
- Flexible Current-Mode Architecture Supports a Wide Range of Applications While Minimizing Interference
  - Boost or SEPIC Current-Mode DC-DC Controller
  - 200kHz to 2MHz Programmable Switching Frequency
  - External Switching-Frequency Synchronization
  - Spread-Spectrum Mode
- Protection Features Enhance Fault Detection and System Reliability
  - Output-to-Ground Undervoltage Protection
  - Open-Drain Fault-Indicator Output
  - Open-LED and LED-Short Detection and Protection
  - Overtemperature Protection
- Adaptive Output-Voltage Optimization to Minimize Power Dissipation
  - Less than 2µA Shutdown Current

Applications

- Automotive Displays LED Backlights
- Automotive RCL, DRL, Front Position, and Fog Lights
- LCD TV and Desktop Display LED Backlights
- Architectural, Industrial, and Ambient Lighting

Ordering Information ***appears at end of data sheet.***

19-100144; Rev 1; 1/18

maxim integrated™

Absolute Maximum Ratings

IN to SGND .....-0.3V to +45V
EN, PGATE to SGND .....-0.3V to (IN + 0.3V)
PGND to SGND.....-0.3V to +0.3V
LEDGND to SGND .....-0.3V to +0.3V
OUT_ to LEDGND.....-0.3V to +45V
V_{CC} to SGND .....-0.3V to the lower of (IN + 0.3V) and +6V
$\overline{FLT}$, DIM, RSDT, OVP to SGND .....-0.3V to +6V
CS, NDRV, RT, COMP, SETI to SGND .... -0.3V to (V_{CC} + 0.3V)
NDRV Peak Current (< 100ns) .....±3A
NDRV Continuous Current.....±100mA
OUT_ Continuous Current.....±175mA
V_{CC} Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C) (Note 1)
20-Pin TQFN (derate 25.6mW/°C above +70°C).....2051mW
20-Pin TSSOP (derate 26.5mW/°C above +70°C)....2122mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....+39°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....+6°C/W

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....+37.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....+2.0°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TSSOP-EP	U20E+6	21-0108	90-0114
20 TQFN-EP	T2044+3	21-0139	90-0037

Electrical Characteristics

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.25kΩ, R_{SETI} = 15kΩ, C_{VCC} = 1µF, NDRV = COMP = OUT_ = PGATE = unconnected, V_{RSDT} = V_{DIM} = V_{CC}, V_{OVP} = 0.7V, V_{CS} = V_{LEDGND} = V_{PGND} = V_{SGND} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLIES						
Operating Voltage Range	V_{IN}		4.75		40	V
Supply Current	I_{IN}	V_{OVP} = 1.266V, all channels on, $V_{OUT_}$ = 0.5V		3.4	5.7	mA
Standby Supply Current	I_{IN_Shdn}	V_{EN} = 0V		1	2	µA
IN Undervoltage Lockout		V_{IN} rising	3.975	4.3	4.625	V
IN UVLO Hysteresis				170		mV

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.25kΩ, R_{SETI} = 15kΩ, C_{VCC} = 1µF, NDRV = COMP = OUT_ = PGATE = unconnected, V_{RSDT} = V_{DIM} = V_{CC}, V_{OVP} = 0.7V, V_{CS} = V_{LEDGND} = V_{PGND} = V_{SGND} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} REGULATOR						
Regulator Output Voltage	V_{CC}	6.5V < V_{IN} < 10V, 1mA < I_{LOAD} < 50mA	4.75	5	5.25	V
		10V < V_{IN} < 40V, 1mA < I_{LOAD} < 10mA	4.75	5	5.25	
Dropout Voltage		V_{IN} - V_{CC}, V_{IN} = 4.75V, I_{LOAD} = 50mA		200	500	mV
Short-Circuit Current Limit	V_{CC_ILIM}	V_{CC} shorted to SGND		100		mA
V_{CC} Undervoltage-Lockout Threshold		V_{CC} rising		4		V
V_{CC} UVLO Hysteresis				125		mV
RT OSCILLATOR						
Switching Frequency Range	f_{SW}	Frequency dithering disabled	200		2000	kHz
Maximum Duty Cycle		f_{SW} = 200kHz to 600kHz	90	94.5	98.5	%
		f_{SW} = 600kHz to 2000kHz	86	90.5	95	
Oscillator Frequency Accuracy		f_{SW} = 200kHz to 2000kHz, frequency dither disabled	-7.5		+7.5	%
Frequency Dither	f_{DITH}	Dither enabled, f_{SW} = from 200kHz to 2000kHz	-5	-7	-9	%
Sync Rising Threshold			4			V
Minimum Sync Frequency			1.1f_{SW}			kHz
PWM COMPARATOR						
PWM Comparator Leading-Edge Blanking				60		ns
PWM-to-NDRV Propagation Delay		Including leading-edge blanking time		90		ns
SLOPE COMPENSATION						
Peak Slope Compensation Current Ramp Magnitude		Current ramp added to the CS input	45	50	55	µA
CURRENT-SENSE COMPARATOR						
Current-Limit Threshold		(Note 3)	396	416	437	mV
CS Limit Comparator to NDRV Propagation Delay		10mV overdrive, excluding leading edge blanking time		10		ns
ERROR AMPLIFIER						
OUT_ Regulation Voltage				1		V
Transconductance	g_M	V_{COMP} = 2V	340	600	880	µS
No-Load Gain		(Note 4)		75		dB
COMP Sink Current		$V_{OUT_}$ = 2.25V, V_{COMP} = 2V	160	375	800	µA
COMP Source Current		$V_{OUT_}$ = 0V, V_{COMP} = 1.0V	160	375	800	µA

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.25kΩ, R_{SETI} = 15kΩ, C_{VCC} = 1µF, NDRV = COMP = OUT_ = PGATE = unconnected, V_{RSDT} = V_{DIM} = V_{CC}, V_{OVP} = 0.7V, V_{CS} = V_{LEDGND} = V_{PGND} = V_{SGND} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSFET DRIVER						
NDRV On-Resistance		I_{SINK} = 100mA (nMOS)		0.9		Ω
		I_{SOURCE} = 50mA (pMOS)		1.1		Ω
Peak Sink Current		V_{NDRV} = 5V		2		A
Peak Source Current		V_{NDRV} = 0V		2		A
Rise Time		C_{LOAD} = 1nF		6		ns
Fall Time		C_{LOAD} = 1nF		6		ns
LED CURRENT SOURCE						
OUT_ Current Sink Range			20		150	mA
Channel-to-Channel Matching		$I_{OUT_}$ = 100mA	-2		+2	%
OUT_ Current		R_{SETI} = 30kΩ, T_A = +25°C	48.25	50	51.75	mA
		R_{SETI} = 30kΩ, T_A = -40°C to +125°C	47.50	50	52.50	
		R_{SETI} = 15kΩ, T_A = +25°C	97	100	103	
		R_{SETI} = 15kΩ, T_A = -40°C to +125°C	96	100	104	
		R_{SETI} = 10kΩ, T_A = +25°C	145.50	150	154.50	
		R_{SETI} = 10kΩ, T_A = -40°C to +125°C	144	150	156	
OUT_ Leakage Current		V_{DIM} = 0V, $V_{OUT_}$ = 40V	-2		+2	µA
LOGIC INPUTS and OUTPUTS						
EN Input Logic-High			2.1			V
EN Input Logic-Low					0.4	V
EN Hysteresis				260		mV
EN Input Current		V_{EN} = 12V		7.5	15	µA
		V_{EN} = 0.3V		100	200	nA
DIM Input Logic-High			2.1			V
DIM Input Logic-Low					0.8	V
DIM Hysteresis				250		mV
DIM Input Current		V_{DIM} = 5V	-2		+2	µA
DIM to LED Turn-On Delay		DIM rising edge to 10% rise in $I_{OUT_}$		150		ns
DIM to LED Turn-Off Delay		DIM falling edge to 10% fall in $I_{OUT_}$		50		ns
$I_{OUT_}$ Rise Time		10% to 90% $I_{OUT_}$		200		ns
$I_{OUT_}$ Fall Time		90% to 10% $I_{OUT_}$		50		ns
$\overline{FLT}$ Output Low Voltage		V_{IN} = 4.75V and I_{SINK} = 5mA			0.4	V
$\overline{FLT}$ Output Leakage Current		$V_{\overline{FLT}}$ = 5.5V	-1		+1	µA
LED Short-Detection Threshold		V_{RSDT} = 2V	6.1	7	7.9	V
Short-Detection Comparator Delay				6.5		µs

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 12.25kΩ, R_{SETI} = 15kΩ, C_{VCC} = 1µF, NDRV = COMP = OUT_ = PGATE = unconnected, V_{RSDT} = V_{DIM} = V_{CC}, V_{OVP} = 0.7V, V_{CS} = V_{LEDGND} = V_{PGND} = V_{SGND} = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

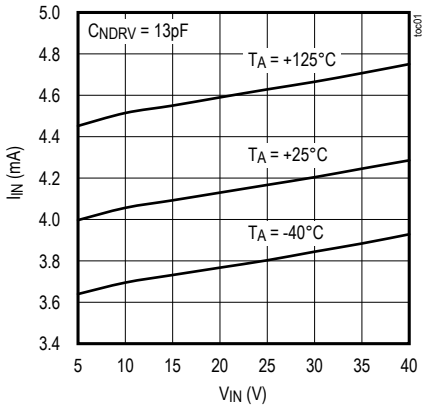
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RSDT Leakage Current		V_{RSDT} = 2.5V	-600		+600	nA
OVP Trip Threshold		OVP rising	1.190	1.228	1.266	V
OVP Hysteresis				70		mV
OVP Leakage Current		V_{OVP} = 1.25V	-200		+200	nA
OVP Undervoltage-Detection Threshold		OVP falling, PGATE latched off	0.485	0.585	0.685	V
OVP Undervoltage-Detection Delay		OVP falling	5	10	20	µs
Thermal-Shutdown Threshold		Temperature rising		165		°C
Thermal-Shutdown Hysteresis				15		°C
PGATE DRIVER						
PGATE On-Resistance	R_{PGATE}	I_{PGATE} = 10mA		100	250	Ω
PGATE Soft-Start Current		Active during PGATE soft-start time	210	350	490	µA
PGATE Soft-Start Time			6.35	10	13.25	ms
PGATE Leakage Current		V_{PGATE} = 12V, V_{EN} = 0V		0.01	1	µA

Note 2: 100% tested at T_A = +25°C. All limits over temperature are guaranteed by design, not production tested.
Note 3: CS threshold includes slope compensation ramp magnitude.
Note 4: Gain = dV_{COMP}/dV_{CS}, 0.05V < V_{CS} < 0.15V.

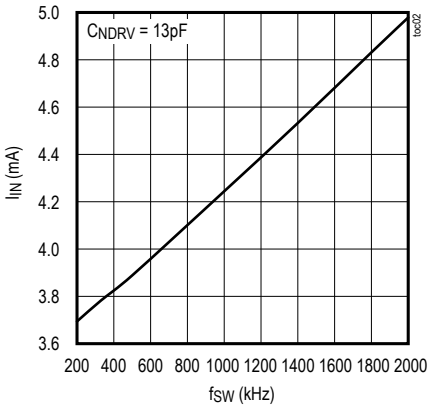
Typical Operating Characteristics

(V_{IN} = V_{EN} = 12V, R_{RT} = 21kΩ, R_{SETI} = 15kΩ, C_{VCC} = 1µF, NDRV = COMP = OUT_ = PGATE = unconnected, V_{OVP} = 0.7V, V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, load = 4 strings of 7 white LEDs, T_A = +25°C, unless otherwise noted.)

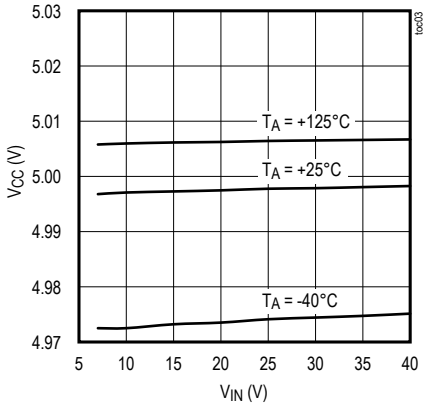
SUPPLY CURRENT vs. SUPPLY VOLTAGE



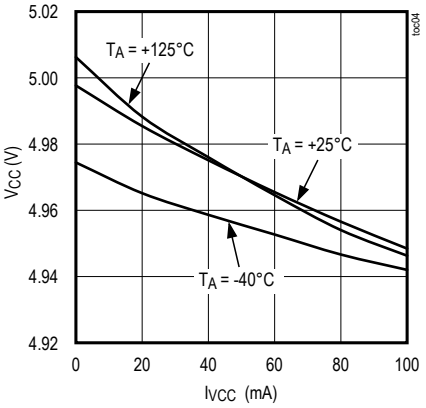
SUPPLY CURRENT vs. SWITCHING FREQUENCY



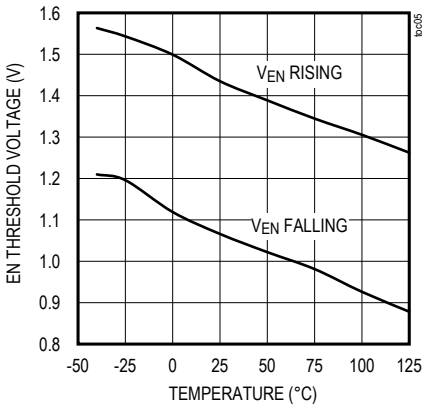
VCC LINE REGULATION



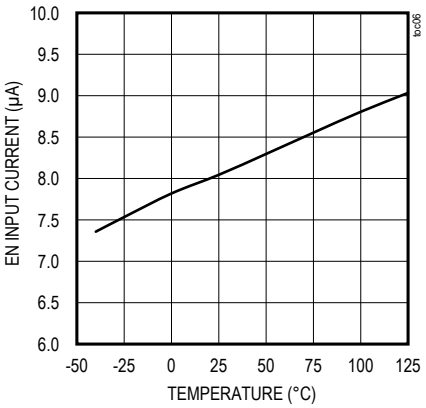
VCC LOAD REGULATION



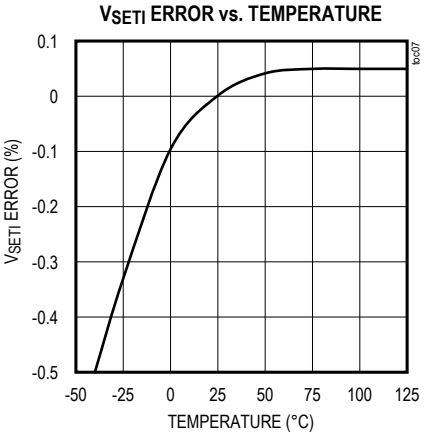
EN THRESHOLD VOLTAGE vs. TEMPERATURE



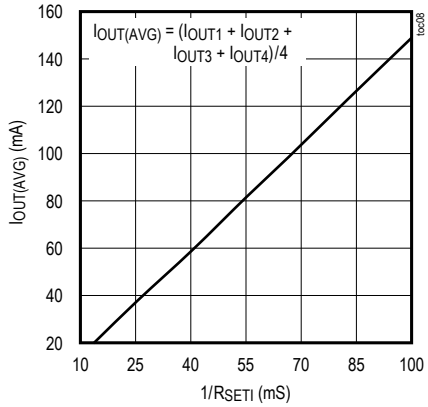
EN INPUT CURRENT vs. TEMPERATURE



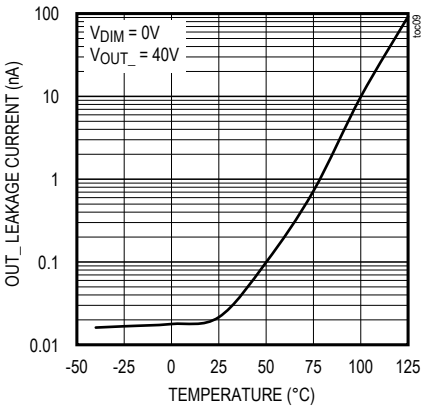
VSETI ERROR vs. TEMPERATURE



IOUT(AVG) vs. 1/RSETI



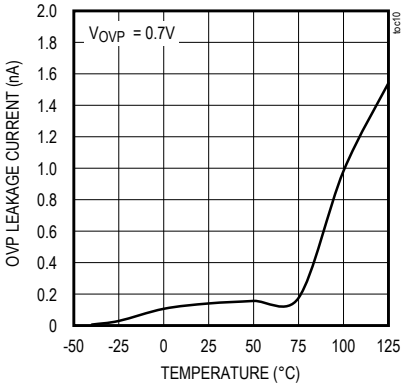
OUT_ LEAKAGE CURRENT vs. TEMPERATURE



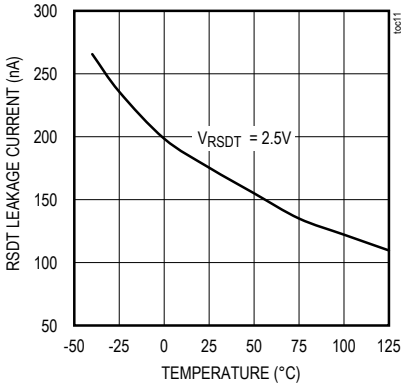
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 21kΩ, R_{SETI} = 15kΩ, C_{VCC} = 1µF, NDRV = COMP = OUT_ = PGATE = unconnected, V_{OVP} = 0.7V, V_{CS} = V_{LEDGND} = V_{DIM} = V_{PGND} = V_{SGND} = 0V, load = 4 strings of 7 white LEDs, T_A = +25°C, unless otherwise noted.)

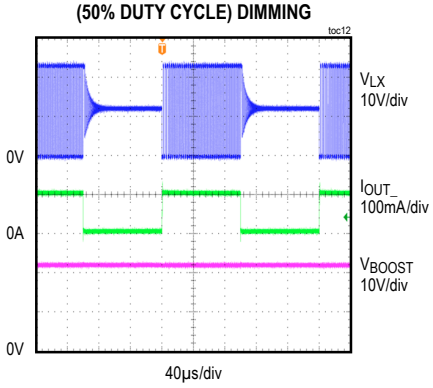
OVP LEAKAGE CURRENT vs. TEMPERATURE



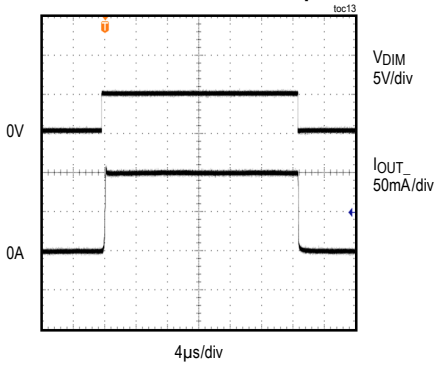
RSDT LEAKAGE CURRENT vs. TEMPERATURE



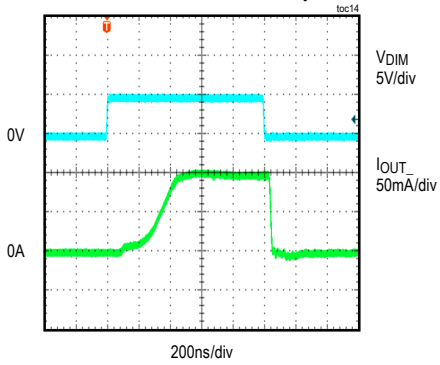
SWITCHING WAVEFORM AT 5kHz (50% DUTY CYCLE) DIMMING



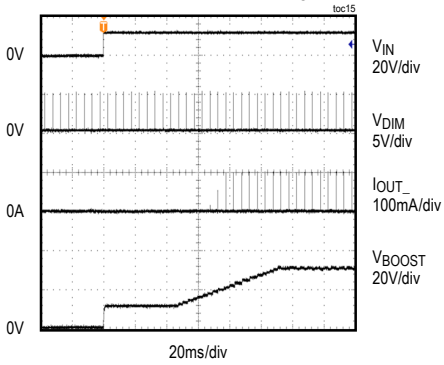
LED CURRENT WAVEFORM WITH DIM ON PULSE WIDTH OF 25µs



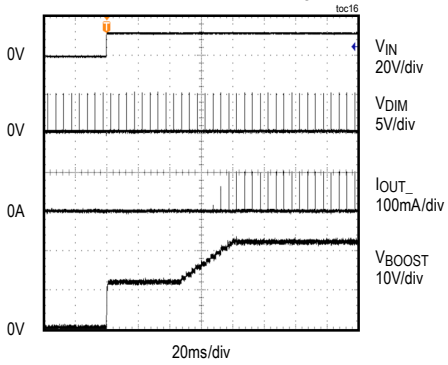
LED CURRENT WAVEFORM WITH DIM ON PULSE WIDTH OF 1µs



STARTUP WAVEFORM WITH DIM ON PULSE WIDTH < 24t_{SW}



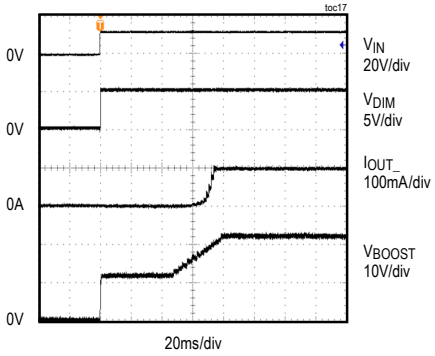
STARTUP WAVEFORM WITH DIM ON PULSE WIDTH ≥ 24t_{SW}



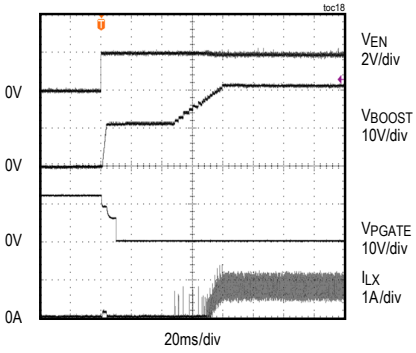
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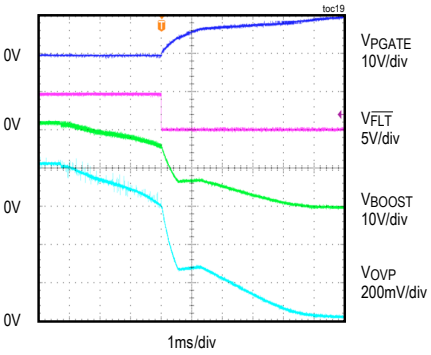
STARTUP WAVEFORM WITH DIM CONTINUOUSLY ON



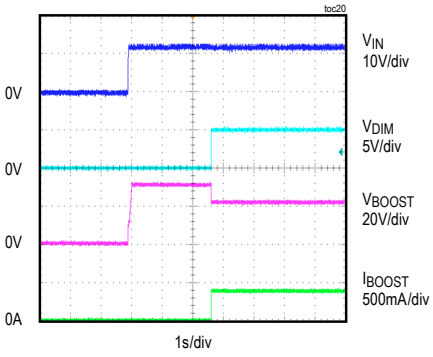
STARTUP WAVEFORM OF PGATE AND INDUCTOR CURRENT WITH DIM CONTINUOUSLY ON



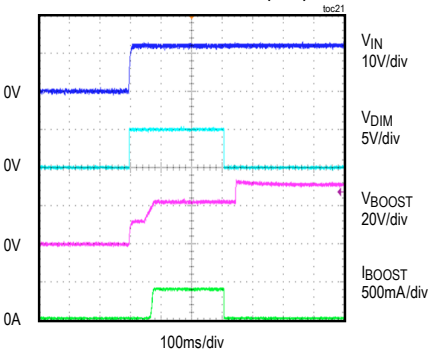
OUTPUT UNDERVOLTAGE FAULT



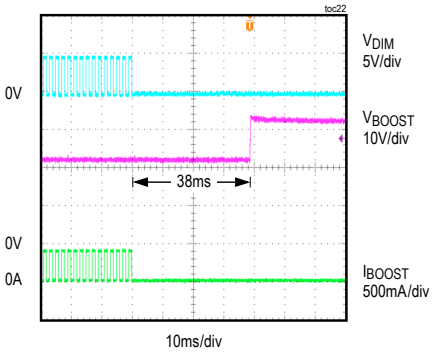
STARTUP WAVEFORMS WITH DELAYED DIM INPUT



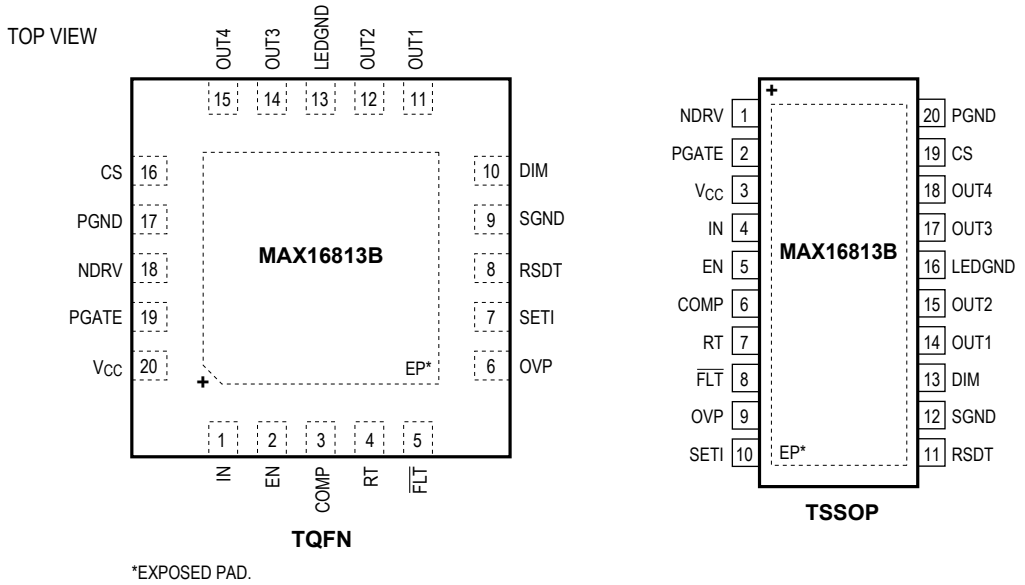
FUNCTIONALITY WITH DIM = 0 FOR DURATION > 38ms (TYP)



DIM LOW DETECTION PERIOD



Pin Configuration



Pin Description

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	4	IN	Bias Supply Input. Connect a 4.75V to 40V supply to IN. Bypass IN to SGND with a ceramic capacitor.
2	5	EN	Enable Input. Connect EN to logic-low to shut down the device. Connect EN to logic-high or IN for normal operation. The EN input should not be left open.
3	6	COMP	Switching Converter Compensation Input. Connect the compensation network from COMP to SGND for current-mode control (see the *Feedback Compensation* section).
4	7	RT	Oscillator Timing Resistor Connection. Connect a timing resistor (R_T) from RT to SGND to program the switching frequency according to the formula $R_T = 7.72 \times 10^9/f_{SW}$. Apply an AC-coupled external clock at RT to synchronize the switching frequency with an external clock. When the oscillator is synchronized with the external clock, the spread spectrum is disabled.
5	8	$\overline{FLT}$	Open-Drain Fault Output. $\overline{FLT}$ asserts low when an open LED, short LED, output undervoltage, or thermal shutdown is detected. Connect a pullup resistor from $\overline{FLT}$ to V_{CC}.
6	9	OVP	Overvoltage/Undervoltage-Threshold Adjust Input. Connect a resistor-divider from the switching converter output to OVP and SGND. The OVP comparator reference is internally set to 1.23V.
7	10	SETI	LED Current-Adjust Input. Connect a resistor (R_{SETI}) from SETI to SGND to set the current through each LED string (I_{LED}), according to the formula $I_{LED} = 1500/R_{SETI}$.
8	11	RSDT	LED Short Detection Threshold-Adjust Input. Connect a resistive divider from V_{CC} to RSDT and SGND to program the LED short detection threshold. Connect RSDT directly to V_{CC} to disable LED short detection.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	TSSOP		
9	12	SGND	Signal Ground. SGND is the current return path connection for the low-noise analog signals. Connect SGND, LEDGND, and PGND at a single point.
10	13	DIM	Digital PWM Dimming Input. Apply a PWM signal to DIM for LED dimming control. Connect DIM to V_{CC} if dimming control is not used.
11	14	OUT1	LED String Cathode Connection 1. OUT1 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT1. OUT1 sinks up to 150mA. If unused, connect OUT1 to LEDGND.
12	15	OUT2	LED String Cathode Connection 2. OUT2 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT2. OUT2 sinks up to 150mA. If unused, connect OUT2 to LEDGND.
13	16	LEDGND	LED Ground. LEDGND is the return path connection for the linear current sinks. Connect SGND, LEDGND, and PGND at a single point.
14	17	OUT3	LED String Cathode Connection 3. OUT3 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT3. OUT3 sinks up to 150mA. If unused, connect OUT3 to LEDGND.
15	18	OUT4	LED String Cathode Connection 4. OUT4 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT4. OUT4 sinks up to 150mA. If unused, connect OUT4 to LEDGND.
16	19	CS	Current-Sense Input. CS is the current-sense input for the switching regulator. A sense resistor connected from the source of the external power MOSFET to PGND sets the switching current limit. A resistor connected between the source of the power MOSFET and CS sets the slope compensation ramp rate (see the *Slope Compensation* section).
17	20	PGND	Power Ground. PGND is the switching current return path connection. Connect SGND, LEDGND, and PGND at a single point.
18	1	NDRV	Switching n-MOSFET Gate-Driver Output. Connect NDRV to the gate of the external switching power MOSFET.
19	2	PGATE	External p-MOSFET Gate connection. Connect a resistor from this pin to the external p-MOSFET gate. Connect PGATE to PGND through a resistor (0 to 10kΩ) if not used.
20	3	V_{CC}	5V Regulator Output. Bypass V_{CC} to SGND with a minimum of 1µF ceramic capacitor as close as possible to the device.
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use EP as the main IC ground connection. EP must be connected to SGND.

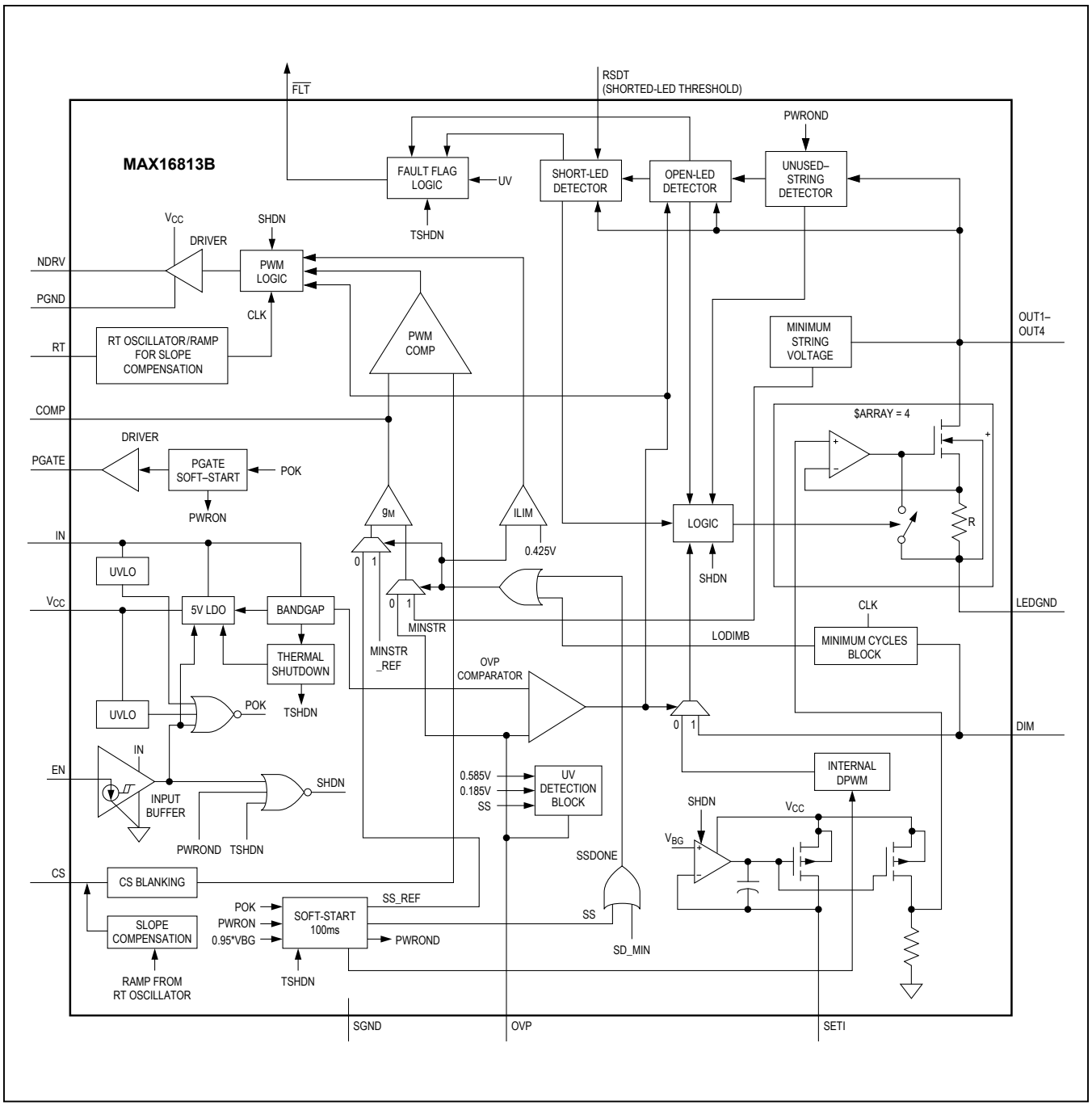


Figure 1. Simplified Functional Diagram

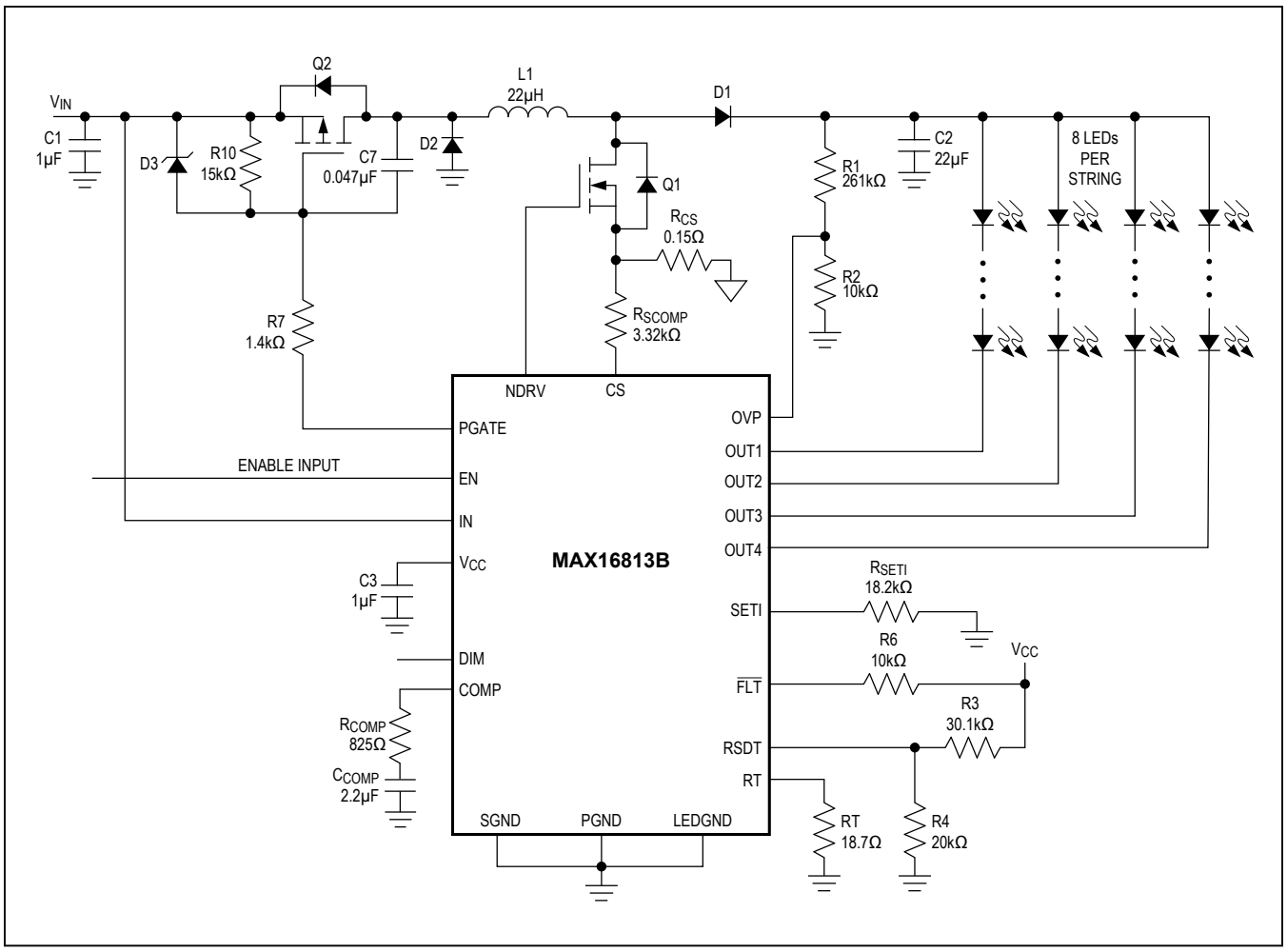


Figure 2. Typical Operating Circuit

Detailed Description

The MAX16813B high-efficiency HB LED driver integrates all the necessary features to implement a high-performance backlight driver to power LEDs in small- to medium-sized displays for automotive as well as general applications. The device provides load-dump voltage protection up to 40V in automotive applications. The device incorporates two major blocks: a DC-DC controller with peak-current-mode control to implement a boost or a SEPIC-type switched-mode power supply and a 4-channel LED driver with 20mA to 150mA constant-current sink capability per channel. Figure 1 is the simplified functional diagram and Figure 2 shows a typical operating circuit.

The device features a constant-frequency peak current-mode control with programmable slope compensation to control the duty cycle of the PWM controller. The high-current FET driver can provide up to 2A of current to the external n-MOSFET. The DC-DC converter implemented using the controller generates the required supply voltage for the LED strings from a wide input supply range. Connect LED strings from the DC-DC converter output to the 4-channel constant-current sink drivers that control the current through the LED strings. A single resistor connected from the SETI input to ground adjusts the forward current through all 4 LED strings.

The device features adaptive voltage control that adjusts the converter output voltage depending on the forward

voltage of the LED strings. This feature minimizes the voltage drop across the constant-current sink drivers and reduces power dissipation in the device. The device includes an internal 5V LDO capable of powering additional external circuitry. A logic input (EN) shuts down the device when pulled low. When the EN pin is pulled below 0.3V (typ), the quiescent input current to the device is less than 1µA (typ).

The device provides a very wide (10000:1) PWM dimming range where a dimming pulse as narrow as 500ns is possible at a 200Hz dimming frequency. This is made possible by a unique feature that detects short PWM dimming input pulses and adjusts the converter feedback accordingly.

Advanced features include detection and string disconnect for open-LED strings, partial or fully shorted strings, and unused strings. Overvoltage protection clamps the converter output voltage to the programmed OVP threshold in the event of an open-LED condition.

Shorted-LED string-detection and overvoltage-protection thresholds are programmable using the RSDT and OVP inputs, respectively. An open-drain $\overline{FLT}$ signal asserts to indicate open-LED, shorted-LED, output undervoltage and overtemperature conditions. Disable individual current sink channels by connecting the corresponding OUT_ to LEDGND. In this case, $\overline{FLT}$ does not assert indicating an open-LED condition for the disabled channel. The device also features an overtemperature protection that shuts down the controller if the die temperature exceeds +165°C.

There are two levels of output undervoltage protection in the device. The first output undervoltage protection is set at 180mV and this is enabled 43ms after power-up. If the OVP pin is lower than 180mV after 43ms, it turns off the converter and disconnects the p-MOSFET from the input. The second undervoltage threshold is activated after the soft-start period of the DC-DC converter. This is set at 585mV. If the OVP pin is below 585mV after the soft-start period of the DC-DC converter, the converter is turned off and the p-MOSFET disconnects the input voltage from the LED driver. See the *Startup Sequence* section for more details.

Current-Mode DC-DC Controller

The peak current-mode controller allows boost or SEPIC-type converters to generate the required bias voltage for the LED strings. The switching frequency can be programmed over the 200kHz to 2MHz range using a resistor connected from RT to SGND. Programmable slope compensation is available to compensate for subharmonic oscillations that occur at above 50% duty cycles in continuous-conduction mode.

The external n-MOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until turned off at the peak current level set by the feedback loop. The peak inductor current is sensed from the voltage across the current-sense resistor (R_{CS}) connected from the source of the external n-MOSFET to PGND. The device features leading-edge blanking to suppress the external n-MOSFET switching noise. A PWM comparator compares the current-sense voltage plus the slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the external n-MOSFET when the voltage at CS exceeds the error amplifier's output voltage. This process repeats every switching cycle to achieve peak-current-mode control.

Error Amplifier

The internal error amplifier compares an internal feedback (FB) with an internal reference (REF) and regulates its output to adjust the inductor current. An internal minimum string detector measures the minimum-current sink voltage with respect to SGND out of the four constant-current sink channels. During normal operation, this minimum OUT_ voltage is regulated to 1V through feedback. The error amplifier takes 1V as the REF and the minimum OUT_ voltage as the FB input. The amplified error at the COMP output controls the inductor peak current to regulate the minimum OUT_ voltage at 1V. The resulting DC-DC converter output voltage is the highest LED string voltage plus 1V.

The converter stops switching when the LED strings are turned off during PWM dimming. The error amplifier is disconnected from the COMP output to retain the compensation capacitor charge. This allows the converter to settle to a steady-state level almost immediately when the LED strings are turned on again. This unique feature provides fast dimming response without having to use large output capacitors.

If the PWM dimming on-pulse is less than or equal to 24 switching cycles, the feedback controls the voltage on OVP so that the converter output voltage is regulated at 95% of the OVP threshold. This mode ensures that narrow PWM dimming pulses are not affected by the response time of the converter. During this mode, the error amplifier remains connected to the COMP output continuously and the DC-DC converter continues switching.

Input and V_{CC} Undervoltage Lockout (UVLO)

The device features two undervoltage lockouts that monitor the input voltage at IN and the output of the internal LDO regulator at V_{CC}. The device turns on after both IN and V_{CC} exceed their respective UVLO thresholds. The UVLO threshold at IN is 4.3V when IN is rising and 4.13V when IN is falling. The UVLO threshold at V_{CC} is 4V when V_{CC} is rising and 3.875V when V_{CC} is falling.

Enable

The device is enabled using the EN logic input pin. The EN input can handle voltages up to IN, providing flexibility in terms of control signals/supplies. To shut down the device, drive the EN pin with a logic-low, which reduces current consumption to 1µA (typ). Connect the EN pin to IN if not used. EN should not be left open.

Startup Sequence

Once EN is driven high, the controller remains off until both IN and V_{CC} trip their rising thresholds.

Once UVLO conditions are satisfied, the driver of the external p-MOSFET is turned on. A constant current of 350µA (typ) flows into the PGATE pin of the device for approximately 10ms (typ). The current flowing into resistor R7 and capacitor C7 (see Figure 2) pulls down the gate of the external p-MOSFET. This capacitor controls the turn-on time of the external p-MOSFET.

After the external p-MOSFET Q2 (Figure 2) is turned on and the 10ms timeout expires, the device detects and then disconnects any unused current sink channels before enabling the converter. Disable the unused current sink channels by connecting the corresponding OUT_ to LEDGND. This avoids asserting the $\overline{FLT}$ output for the unused channels. The detection of unused channels takes approximately 0.7ms (typ).

Once the above phase is completed, the DC-DC converter is enabled and the soft-start is initiated. During soft-start, the DC-DC converter output ramps up as the loop regulates the voltage at the OVP pin to follow an internal ramping voltage. 33ms (typ) after the converter is enabled, the OVP pin is monitored, and if the voltage at the OVP pin is less than 180mV (typ), $\overline{FLT}$ is asserted low, the power converter is turned off, the external p-MOSFET is turned off, and they all stay off until the EN pin or the supply is recycled. If there is no undervoltage, soft-start terminates when the minimum current sink voltage reaches 1V (typ) or when an internal 100ms timeout expires.

After soft-start, the device detects open LED and disconnects any strings with an open LED from the internal minimum OUT_ voltage detector. The converter output discharges to a level where the new minimum OUT_ voltage is 1V and then control is handed over to the internal minimum OUT_ voltage detector.

A second output undervoltage protection is enabled 100ms after the converter is enabled. A fault is detected whenever the OVP pin falls below an internal threshold of 585mV (typ) and the power converter is latched off and PGATE goes high. Cycling the EN pin or the supply is required to start up again, once the fault condition has been removed.

Oscillator Frequency/External Synchronization

The internal oscillator frequency is programmable between 200kHz and 2MHz using a timing resistor (R_T) connected from the RT input to SGND. Use the equation below to calculate the value of R_T for the desired switching frequency (f_{SW}):

$$R_T = \frac{7.72 \times 10^9}{f_{SW}}$$

where f_{SW} is in Hz.

Synchronize the oscillator with an external clock by AC-coupling the external clock to the RT input. The capacitor used for the AC-coupling should satisfy the following relation:

$$C_{SYNC} \le \left(\frac{9.862}{R_T} - 0.144 \times 10^{-3} \right) (\mu F)$$

where R_T is in ohms.

The pulse width for the synchronization pulse should satisfy the following relations:

$$\frac{t_{PW}}{t_{CLK}} V_S < 0.5$$

$$\left(0.8 - \frac{t_{PW}}{t_{CLK}} V_S \right) + V_S > 3.4$$

$$t_{PW} < \frac{t_{CLK}}{t_{CI}} \left(t_{CI} - 1.05 \times t_{CLK} \right)$$

where t_{PW} is the synchronization source pulse width, t_{CLK} is the synchronization clock time period, t_{CI} is the programmed clock period, and V_S is the synchronization pulse voltage level.

Spread-Spectrum Mode

The device includes a unique spread-spectrum mode (SSM) that reduces emission (EMI) at the switching frequency and its harmonics.

The spread spectrum uses a pseudorandom dithering technique where the switching frequency is varied in the range of 93% of the programmed switching frequency, to 100% of the programmed switching frequency set through the external resistor from RT to SGND.

Instead of a large amount of spectral energy present at multiples of the switching frequency, the total energy at the fundamental and each harmonic is spread over a wider bandwidth, reducing the energy peak.

Spread spectrum is only disabled if external synchronization is used.

5V LDO Regulator (V_{CC})

The internal LDO regulator converts the input voltage at IN to a 5V output voltage at V_{CC}. The LDO regulator supplies up to 50mA current to provide power to internal control circuitry and the gate driver. Bypass V_{CC} to SGND with a minimum of 1µF ceramic capacitor as close as possible to the device.

PWM MOSFET Driver

The NDRV output is a push-pull output with the on-resistance of the p-MOSFET (typically 1.1Ω) and the on-resistance of the n-MOSFET (typically 0.9Ω). NDRV swings from PGND to V_{CC} to drive an external n-MOSFET. The driver typically sources 2.0A and sinks 2.0A allowing for fast turn-on and turn-off of high gate-charge MOSFETs.

The power dissipation in the device is mainly a function of the average current sourced to drive the external MOSFET (I_{VCC}) if there are no additional loads on V_{CC}. I_{VCC} depends on the total gate charge (QG) and operating frequency of the converter.

LED Current Control

The device features four identical constant-current sources used to drive multiple HB LED strings. The current through each one of the four channels is adjustable between 20mA and 150mA using an external resistor (R_{SETI}) connected between SETI and SGND. Select R_{SETI} using the following formula:

$$R_{SETI} = 1500/I_{OUT_}$$

where $I_{OUT_}$ is the desired output current for each of the four channels. If more than 150mA is required in an LED string, use two or more of the current source outputs (OUT_) connected together to drive the string, as shown in Figure 3.

LED Dimming Control

The device features LED brightness control using an external PWM signal applied to DIM. A logic-high signal on the DIM input enables all four LED current sources and a logic-low signal disables them.

The duty cycle of the PWM signal applied to DIM also controls the DC-DC converter's output voltage. If the turn-on duration of the PWM signal is less than 24 oscillator clock cycles (DIM pulse width increasing), the boost converter regulates its output based on feedback from the OVP input. While in this mode, the converter output voltage is regulated to 95% of the overvoltage threshold at the OVP pin. If the turn-on duration of the PWM signal is greater than or equal to 24 oscillator clock cycles (DIM pulse width increasing), the converter regulates its output so that the minimum voltage at OUT_ is 1V.

At power-up, if the converter has completed the soft-start period of 100ms (typ) and the PWM signal at the DIM pin is still low, the device regulates the output voltage based on the feedback signal coming from the OVP pin. Once a PWM pulse width greater than 24 oscillator clock cycles is applied, the converter regulates its output so that the minimum voltage at OUT_ is 1V.

The converter output voltage is regulated to 95% of the overvoltage threshold at the OVP pin whenever the PWM signal at the DIM pin is forced low for a duration longer than 38ms (typ).

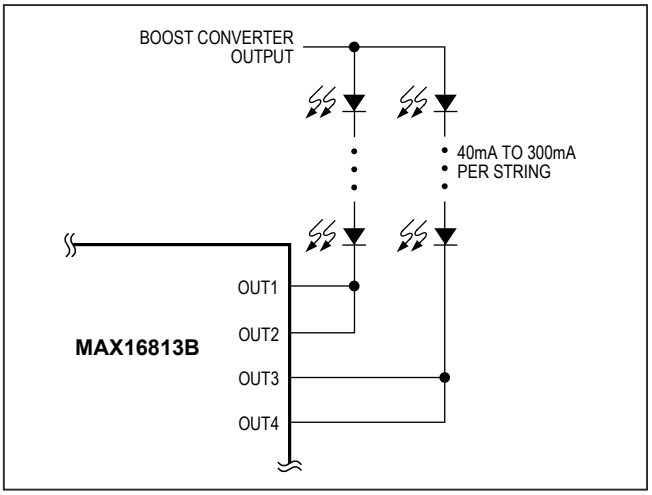


Figure 3. Configuration for Higher LED String Current

Fault Protections

Fault protections in the device include cycle-by-cycle current limiting using the PWM controller, DC-DC converter output overvoltage protection, open-LED detection, short-LED detection and protection, output undervoltage protection, and overtemperature shutdown. An open-drain fault flag output ($\overline{FLT}$) goes low when an open-LED string is detected, a shorted-LED string is detected, an output undervoltage, or during thermal shutdown. $\overline{FLT}$ is cleared when the fault condition is removed during thermal shutdown and shorted LEDs. $\overline{FLT}$ is latched low for an open-LED or output undervoltage condition, and can be reset by cycling power or toggling the EN pin. The thermal-shutdown threshold is +165°C and has +15°C hysteresis.

Open-LED Management and Overvoltage Protection

On power-up, the device detects and disconnects any unused current sink channels before entering the DC-DC converter soft-start. Disable the unused current sink channels by connecting the corresponding OUT_ to LEDGND. This avoids asserting the $\overline{FLT}$ output for the unused channels. After soft-start, the device detects open LED and disconnects any strings with an open LED from the internal minimum OUT_ voltage detector. This keeps the DC-DC converter output voltage within safe limits and maintains high efficiency. During normal operation, the DC-DC converter output regulation loop uses the minimum OUT_ voltage as the feedback input. If any LED string is open, the voltage at the opened OUT_ goes to V_{LEDGND}. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, OVP input, and SGND. The overvoltage-protection threshold at the DC-DC converter output (V_{OVP}) is determined using the following formula:

$$V_{OVP} = 1.23 \times \left(1 + \frac{R1}{R2}\right)$$ (see Figure 2)

where 1.23V (typ) is the OVP threshold. Select R1 and R2 such that the voltage at OUT_ does not exceed the absolute maximum rating. As soon as the DC-DC converter output reaches the overvoltage-protection threshold, the PWM controller is switched off setting NDRV low. Any current sink output with $V_{OUT_}$ < 300mV (typ) is disconnected from the minimum voltage detector. Connect the OUT_ of all channels without LED connections to LEDGND before power-up to avoid OVP triggering at startup. When an open-LED overvoltage condition occurs, $\overline{FLT}$ is latched low. Open-LED detection is disabled when PWM dimming pulse width is less than 24 switching clock cycles.

Short-LED Detection

The device checks for shorted LEDs at each rising edge of DIM. An LED short is detected at OUT_ if the following condition is met:

$$V_{OUT_} > V_{MINSTR} + 3 \times V_{RSDT}$$

where $V_{OUT_}$ is the voltage at OUT_, V_{MINSTR} is the minimum current sink voltage, and V_{RSDT} is the programmable-LED short-detection threshold set at the RSDT input (with V_{RSDT} less than or equal to 2.5V). Adjust V_{RSDT} to a voltage less than or equal to 2.5V using a voltage-divider resistive network connected at the V_{CC} output, RSDT input, and SGND. Once a short is detected on any of the strings, the LED strings with the short are disconnected and the $\overline{FLT}$ output flag asserts until the device detects that the shorts are removed on any of the following rising edges of DIM. Connect RSDT directly to V_{CC} to always disable LED short detection. Short-LED detection is disabled when PWM dimming pulse width is less than 24 switching clock cycles.

Applications Information

DC-DC Converter

Three different converter topologies are possible with the DC-DC controller in the device, which has the ground-referenced outputs necessary to use the constant-current sink drivers. If the LED string forward voltage is always more than the input supply voltage range, use the boost converter topology. If the LED string forward voltage falls within the supply voltage range, use the buck-boost converter topology. Buck-boost topology is implemented using either a conventional SEPIC configuration or a coupled-inductor buck-boost configuration. The latter is basically a flyback converter with 1:1 turns ratio. 1:1-coupled inductors are available with tight coupling suitable for this application. Figure 4 shows the coupled-inductor buck-boost configuration. It is also possible to implement a single inductor converter using the MAX15054 high-side FET driver.

The boost converter topology provides the highest efficiency among the above-mentioned topologies. The coupled-inductor topology has the advantage of not using a coupling capacitor over the SEPIC configuration. Also, the feedback loop compensation for SEPIC becomes complex if the coupling capacitor is not large enough.

Power-Circuit Design

First select a converter topology based on the above factors. Determine the required input supply voltage range, the maximum voltage needed to drive the LED strings including the minimum 1V across the constant LED current sink (V_{LED}), and the total output current needed to drive the LED strings (I_{LED}) as follows:

$$I_{LED} = I_{SRTING} \times N_{SRTING}$$

where I_{SRTING} is the LED current per string in amperes and N_{SRTING} is the number of strings used.

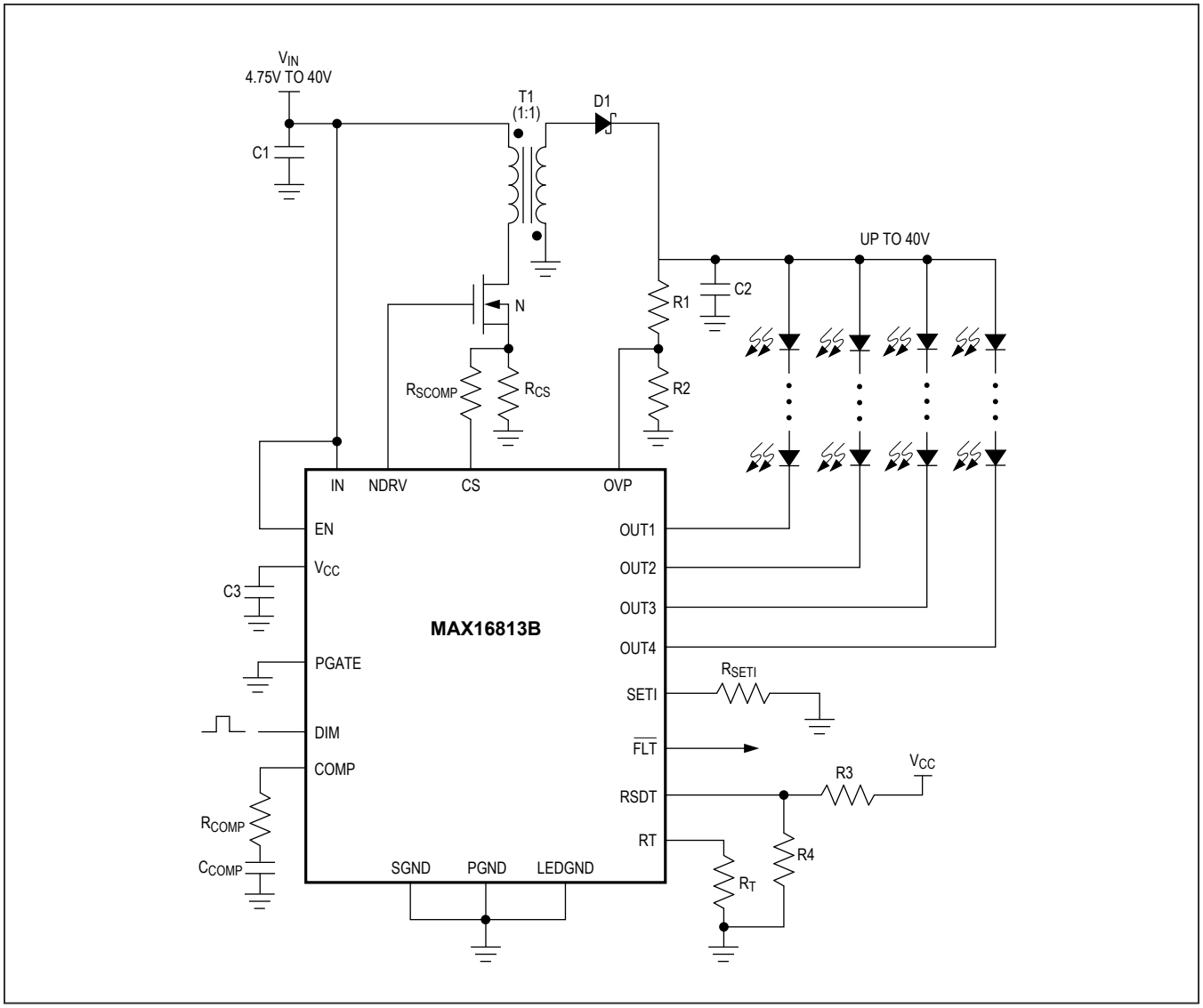


Figure 4. Coupled-Inductor Buck-Boost Configuration

Calculate the maximum duty cycle (D_{MAX}) using the following equations:

For boost configuration:

$$D_{MAX} = \frac{(V_{LED} + V_{D1} - V_{IN_MIN})}{(V_{LED} + V_{D1} - V_{DS} - 0.3V)}$$

For SEPIC and coupled-inductor buck-boost configurations:

$$D_{MAX} = \frac{(V_{LED} + V_{D1})}{(V_{IN_MIN} - V_{DS} - 0.3V + V_{LED} + V_{D1})}$$

where V_{D1} is the forward drop of the rectifier diode in volts (approximately 0.6V), V_{IN_MIN} is the minimum input supply voltage in volts, and V_{DS} is the drain-to-source voltage of the external MOSFET in volts when it is on, and 0.3V is the peak current-sense voltage. Initially, use an approximate value of 0.2V for V_{DS} to calculate D_{MAX}. Calculate a more accurate value of D_{MAX} after the power MOSFET is selected based on the maximum inductor current. Select the switching frequency (f_{SW}) depending on the space, noise, and efficiency constraints.

Boost and Coupled-Inductor Configurations

In all three converter configurations, the average inductor current varies with the input line voltage and the maximum average current occurs at the lowest input line voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum peak-to-peak ripple on the inductor current (ΔIL). The recommended peak-to-peak ripple is 60% of the average inductor current.

Use the following equations to calculate the maximum average inductor current (IL_{AVG}) and peak inductor current (IL_P) in amperes:

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple ΔIL to be ±30% of the average inductor current:

$$\Delta IL = IL_{AVG} \times 0.3 \times 2$$

and

$$IL_P = IL_{AVG} + \frac{\Delta IL}{2}$$

Calculate the minimum inductance value (L_{MIN}) in henries with the inductor current ripple set to the maximum value:

$$L_{MIN} = \frac{(V_{IN_MIN} - V_{DS} - 0.3V) \times D_{MAX}}{f_{SW} \times \Delta IL}$$

where 0.3V is the peak current-sense voltage. Choose an inductor that has a minimum inductance greater than the calculated L_{MIN} and current rating greater than IL_P. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current for boost configuration. For the coupled inductor, the saturation limit of the inductor with only one winding conducting should be 10% higher than IL_P.

SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a conventional design with the output voltage referenced to the input supply voltage. For SEPIC, the output is referenced to ground and the inductor is split into two parts (see Figure 5 for the SEPIC configuration). One of the inductors (L2) takes LED current as the average current and the other (L1) takes input current as the average current.

Use the following equations to calculate the average inductor currents ($IL1_{AVG}$, $IL2_{AVG}$) and peak inductor currents ($IL1_P$, $IL2_P$) in amperes:

$$IL1_{AVG} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a 10% margin to account for the converter losses:

$$IL2_{AVG} = I_{LED}$$

Assuming the peak-to-peak inductor ripple ΔIL is ±30% of the average inductor current:

$$\Delta IL1 = IL1_{AVG} \times 0.3 \times 2$$

and:

$$IL1_P = IL1_{AVG} + \frac{\Delta IL1}{2}$$

$$\Delta IL2 = IL2_{AVG} \times 0.3 \times 2$$

and:

$$IL2_P = IL2_{AVG} + \frac{\Delta IL2}{2}$$

Calculate the minimum inductance values $L1_{MIN}$ and $L2_{MIN}$ in henries with the inductor current ripples set to the maximum value as follows:

$$L1_{MIN} = \frac{(V_{IN_MIN} - V_{DS} - 0.3V) \times D_{MAX}}{f_{SW} \times \Delta IL1}$$

$$L2_{MIN} = \frac{(V_{IN_MIN} - V_{DS} - 0.3V) \times D_{MAX}}{f_{SW} \times \Delta IL2}$$

where 0.3V is the peak current-sense voltage. Choose inductors that have a minimum inductance greater than the calculated $L1_{MIN}$ and $L2_{MIN}$ and current rating greater than $IL1_P$ and $IL2_P$, respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

For simplifying further calculations, consider L1 and L2 as a single inductor with L1 and L2 connected in parallel. The combined inductance value and current is calculated as follows:

$$L_{MIN} = \frac{L1_{MIN} \times L2_{MIN}}{L1_{MIN} + L2_{MIN}}$$

and:

$$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$$

where IL_{AVG} represents the total average current through both the inductors together for SEPIC configuration. Use these values in the calculations for SEPIC configuration in the following sections.

Select coupling capacitor C_S so that the peak-to-peak ripple on it is less than 2% of the minimum input supply voltage. This ensures that the second-order effects created by the series resonant circuit comprising L1, C_S, and L2 do not affect the normal operation of the converter. Use the following equation to calculate the minimum value of C_S:

$$C_S \geq \frac{I_{LED} \times D_{MAX}}{V_{IN_MIN} \times 0.02 \times f_{SW}}$$

where C_S is the minimum value of the coupling capacitor in farads, I_{LED} is the LED current in amperes, and the factor 0.02 accounts for 2% ripple.

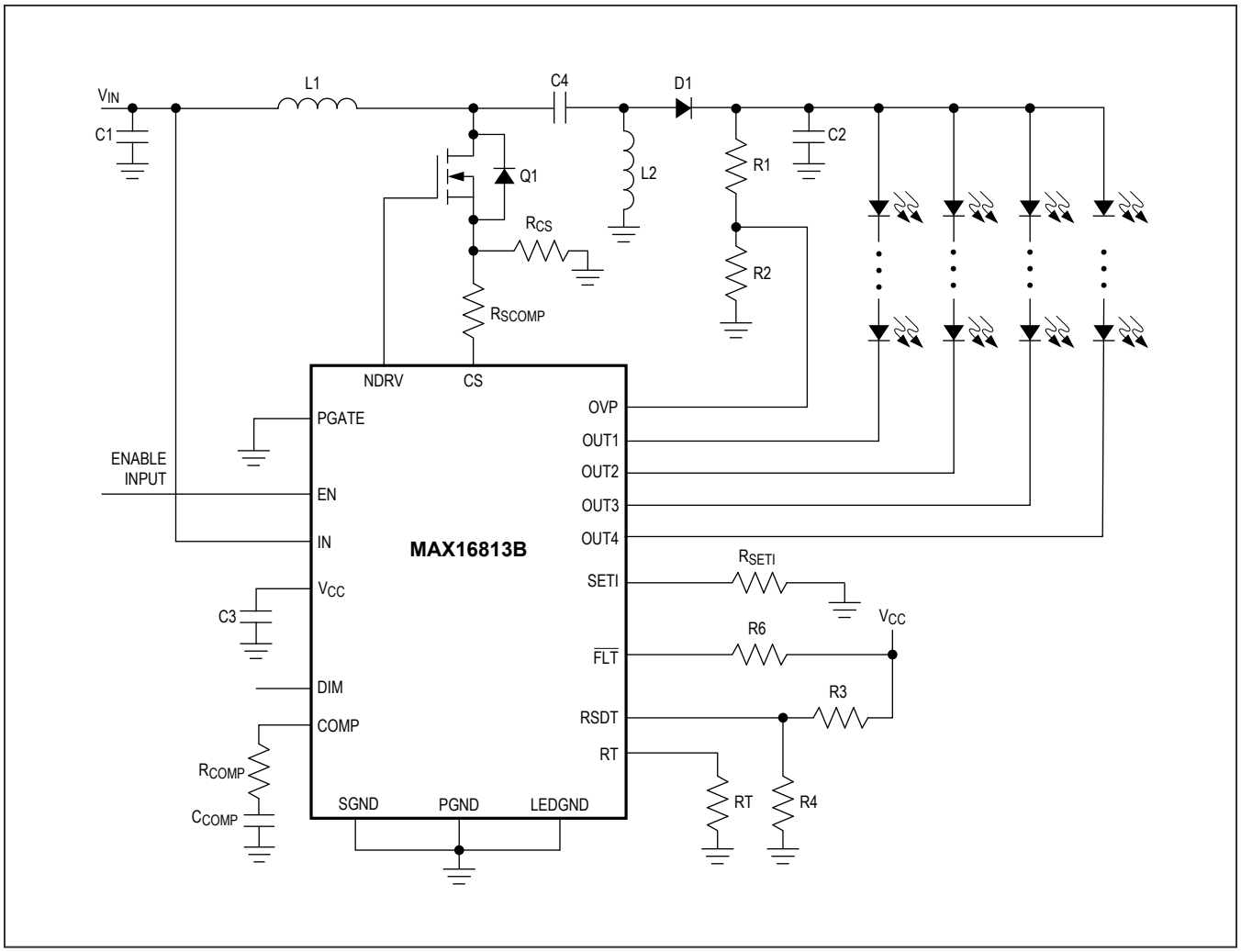


Figure 5. SEPIC LED Driver

Slope Compensation

The device generates a current ramp for slope compensation. This ramp current is in sync with the switching frequency and starts from zero at the beginning of every clock cycle and rises linearly to reach 50µA at the end of the clock cycle. The slope-compensating resistor, (R_{SCOMP}), is connected between the CS input and the source of the external MOSFET. This adds a programmable ramp voltage to the CS input voltage to provide slope compensation.

Use the following equation to calculate the value of slope compensation resistance (R_{SCOMP}):

For boost configuration:

$$R_{SCOMP} = \frac{\left(V_{LED} - 2V_{IN_MIN}\right) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

For SEPIC and coupled inductor:

$$R_{SCOMP} = \frac{\left(V_{LED} - V_{IN_MIN}\right) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

where V_{LED} and V_{IN_MIN} are in volts, R_{SCOMP} and R_{CS} are in ohms, L_{MIN} is in henries, and f_{SW} is in hertz. The value of the switch current-sense resistor, (R_{CS}) can be calculated as follows:

For boost:

$$0.396 \times 0.9 = I_{LP} \times R_{CS} + \frac{\left(D_{MAX} \times \left(V_{LED} - 2V_{IN_MIN}\right) \times R_{CS} \times 3\right)}{4 \times L_{MN} \times f_{SW}}$$

For SEPIC:

$$0.396 \times 0.9 = I_{LP} \times R_{CS} + \frac{\left(D_{MAX} \times \left(V_{LED} - V_{IN_MIN}\right) \times R_{CS} \times 3\right)}{4 \times L_{MN} \times f_{SW}}$$

where 0.396 is the minimum value of the peak current-sense threshold. The current-sense threshold also includes the slope-compensation component. The minimum current-sense threshold of 0.396 is multiplied by 0.9 to take tolerances into account.

Output Capacitor Selection

For all three converter topologies, the output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across constant-current sink outputs because the LED string voltages are stable due to the constant current. For the device, limit the peak-to-peak output-voltage ripple to 200mV to get stable output current.

The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most of the applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming, the amount of ceramic capacitors on the output is usually minimized. In this case, an additional electrolytic or tantalum capacitor provides most of the bulk capacitance.

External Switching-MOSFET Selection

The external switching MOSFET should have a voltage rating sufficient to withstand the maximum output voltage together with the rectifier diode drop and any possible overshoot due to ringing caused by parasitic inductances and capacitances. The recommended MOSFET V_{DS} voltage rating is 30% higher than the sum of the maximum output voltage and the rectifier diode drop.

The recommended continuous-drain current rating of the MOSFET (ID), when the case temperature is at +70°C, is greater than that calculated below:

$$ID_{RMS} = \left(\sqrt{IL_{AVG}{}^2 \times D_{MAX}}\right) \times 1.3$$

The MOSFET dissipates power due to both switching losses and conduction losses. Use the following equation to calculate the conduction losses in the MOSFET:

$$P_{COND} = IL_{AVG}{}^2 \times D_{MAX} \times R_{DS(ON)}$$

where $R_{DS(ON)}$ is the on-state drain-to-source resistance of the MOSFET. Use the following equation to calculate the switching losses in the MOSFET:

$$P_{SW} = \frac{IL_{AVG} \times V_{LED}{}^2 \times C_{GD} \times f_{SW}}{2} \times \left(\frac{1}{I_{GON}} + \frac{1}{I_{GOFF}}\right)$$

where I_{GON} and I_{GOFF} are the gate currents of the MOSFET in amperes when it is turned on and turned off, respectively. C_{GD} is the gate-to-drain MOSFET capacitance in farads.

Rectifier Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a Schottky diode with a voltage rating 20% higher than the maximum boost-converter output voltage and current rating greater than that calculated in the following equation:

$$I_D = IL_{AVG}\left(1 - D_{MAX}\right) \times 1.2$$

Setting RSDT Pin Voltage

As described in the *Short-LED Detection* section, the actual LED short detection threshold depends on the RSDT pin voltage and the minimum current sink (OUT_) voltage.

An optimum choice of RSDT voltage should take into account the maximum voltage at the OUT_ pins when the converter is regulating its output voltage based on the OVP pin.

In particular, it is recommended that the OVP resistor divider be selected to set the output voltage of the converter (when using the OVP input) so that the voltage on the OUT_ pins does not exceed a threshold that depends on the RSDT setting. The plot in Figure 6 shows the relationship between the RSDT voltage and the recommended maximum OUT_ voltage, assuming all the active channels are at the same voltage level.

With higher OUT_ voltages, an erroneous LED short condition can sometimes be detected when the converter output voltage is transitioning from regulation based on the OVP input to regulation based on the OUT_ voltages.

The plot shown here can be used when selecting the OVP resistor divider and the RSDT voltage. It is recommended that the RSDT voltage be chosen to be below the curve. In general, performance is improved when the OVP resistor divider is selected to set a maximum output voltage close to the maximum LED string voltage needed in the application.

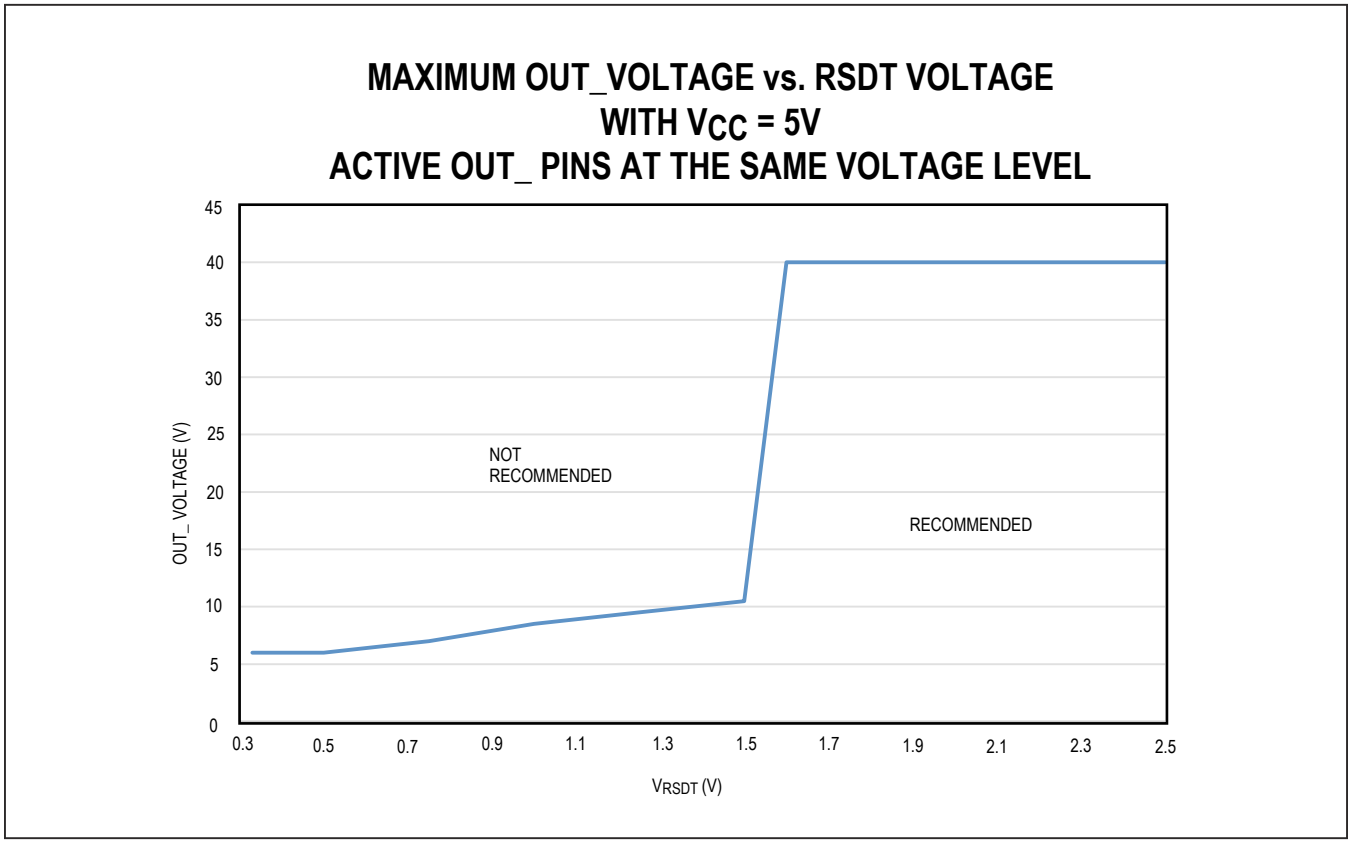


Figure 6. Maximum Output Voltage vs. RSDT Voltage

External Disconnect MOSFET Selection

An external p-MOSFET can be used to disconnect the boost output from the battery in the event of an output overload or short condition. In the case of the SEPIC or buck-boost, this protection is not necessary and in those cases there is no need for the p-MOSFET. Connect the PGATE pin to ground in the case of the SEPIC and buck-boost. If it is necessary to have an output short protection for the boost even at power-up, then the current through the p-MOSFET (Figure 7) has to be sensed. Once the current-sense voltage exceeds a certain threshold, it should limit the input current to the programmed threshold. This threshold should be set at a sufficiently high level so that it never trips at startup or under normal operating conditions. Check the safe operating area of the p-MOSFET so that the current-limit trip threshold and the voltage on the MOSFET do not exceed the limits of the SOA curve of the p-MOSFET at the highest operating temperature. The current-limit protection circuit is active for 33ms before the short trip threshold is triggered in the device, disconnecting the p-MOSFET from the input source. During the 33ms, the p-MOSFET has to sustain the highest input voltage and the programmed current limit.

Overvoltage Protection

The minimum overvoltage-protection threshold at the DC-DC converter output (V_{OVP}) is determined using the following formula:

$$V_{OVPmin} = (1.19 - OVP\ Hysteresis) \times (1 + R1/R2)$$

volts (see Figure 2) where 1.19V is the minimum overvoltage threshold and OVP hysteresis is 70mV. Set this minimum overvoltage threshold so that at 92% of this threshold the circuit can still regulate the current in the LED string when the forward-voltage drop on all the LEDs in the LED string are at the maximum. Use the following formula to calculate the minimum overvoltage-threshold set point:

$$V_{LEDmax} + 1 = 0.92 \times V_{OVPmin}$$

where V_{LEDmax} is the maximum voltage drop that can occur on LED string.

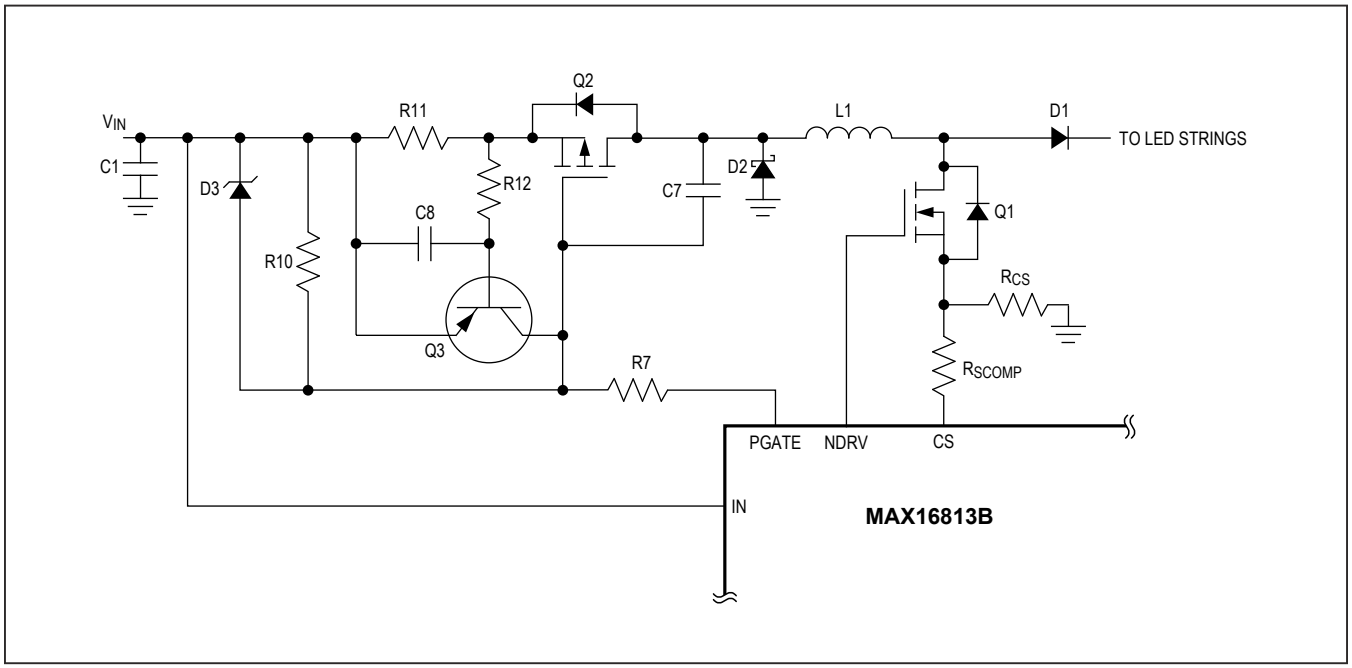


Figure 7. External Disconnect MOSFET

Feedback Compensation

During normal operation, the feedback control loop regulates the minimum OUT_ voltage to 1V when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter and stores the steady-state condition in the form of capacitor voltages, mainly the output filter capacitor voltage and compensation capacitor voltage. When the PWM dimming pulses are less than 24 switching clock cycles, the feedback loop regulates the converter output voltage to 95% of the OVP threshold.

The worst-case condition for the feedback loop is when the LED driver is in normal mode regulating the minimum OUT_ voltage to 1V. The switching converter small-signal transfer function has a right-half plane (RHP) zero for boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

For boost configuration:

$$f_{ZRHP} = \frac{V_{LED}(1-D_{MAX})^2}{2\pi \times L \times I_{LED}}$$

For SEPIC and coupled-inductor buck-boost configurations:

$$f_{ZRHP} = \frac{V_{LED}(1-D_{MAX})^2}{2\pi \times L \times I_{LED} \times D_{MAX}}$$

where f_{ZRHP} is in hertz, V_{LED} is in volts, L is the inductance value of L1 in henries, and I_{LED} is in amperes. A simple way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The switching converter small-signal transfer function also has an output pole. The effective output impedance, together with the output filter capacitance, determines the output pole frequency (f_{P1}) that is calculated as follows:

For boost configuration:

$$f_{P1} = \frac{I_{LED}}{2 \times \pi \times V_{LED} \times C_{OUT}}$$

For SEPIC and coupled-inductor buck-boost configurations:

$$f_{P1} = \frac{I_{LED} \times D_{MAX}}{2 \times \pi \times V_{LED} \times C_{OUT}}$$

where f_{P1} is in hertz, V_{LED} is in volts, I_{LED} is in amperes, and C_{OUT} is in farads. Compensation components (R_{COMP} and C_{COMP}) perform two functions. C_{COMP} introduces a low-frequency pole that presents a -20dB/decade slope to the loop gain. R_{COMP} flattens the gain of the error amplifier for frequencies above the zero formed by R_{COMP} and C_{COMP}. For compensation, this zero is placed at the output pole frequency (f_{P1}) so that it provides a -20dB/decade slope for frequencies above f_{P1} to the combined modulator and compensator response.

The value of R_{COMP} needed to fix the total loop gain at f_{P1}, so that the total loop gain crosses 0dB with -20dB/decade slope at 1/5 the R_{HP} zero frequency, is calculated as follows:

For boost configuration:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1-D_{MAX})}$$

For SEPIC and coupled-inductor buck-boost configurations:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times D_{MAX}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1-D_{MAX})}$$

where R_{COMP} is the compensation resistor in ohms, f_{ZRHP} and f_{P1} are in hertz, R_{CS} is the switch current-sense resistor in ohms, and GM_{COMP} is the transconductance of the error amplifier (600µS).

The value of C_{COMP} is calculated as follows:

$$C_{COMP} = \frac{1}{2\pi \times R_{COMP} \times f_{Z1}}$$

where f_{Z1} is the compensation zero placed at 1/5 of the crossover frequency that is, in turn, set at 1/5 of the f_{ZRHP}. If the output capacitors do not have low ESR, the ESR zero frequency may fall within the 0dB crossover frequency. An additional pole may be required to cancel out this pole placed at the same frequency. This is usually implemented by connecting a capacitor in parallel with C_{COMP} and R_{COMP}. Figure 5 shows the SEPIC configuration and Figure 4 shows the coupled-inductor buck-boost configuration.

Design Verification

The following criteria must be satisfied before the design can go into production:

1) The chosen inductor must not saturate at the lowest input line voltage and the maximum output current condition. The inductor must not saturate at the highest operating case temperature. Adequate margin should be provided.

2) Verify that the slope compensation is adequate. Inadequate slope compensation can cause subharmonic oscillation. For more information on selecting the proper slope-compensation resistor, see the *SSlope Compensation* section.
3) At the lowest input line voltage and the maximum power condition, the signal on the CS pin should be close to the current-limit voltage on the CS pin.
4) Select Schottky diodes, MOSFETs, and resistors that meet the power and voltage ratings.
5) Select input and output capacitors that meet ripple-voltage and ripple-current requirements.
6) Set the overvoltage at the appropriate point.
7) After the compensation values are designed, verify the design by measuring the loop stability.

Loop-Stability Verification

To verify the loop stability, it is a good idea to use a loop analyzer to study the closed-loop gain and phase with frequency. To check the closed-loop gain, connect the test and reference probes of the analyzer, as shown in Figure 8.

Check the voltages on the OUT_ pins with dimming at 100% duty cycle. Then insert a diode and the injection resistor in the string where the OUT_ voltage is closest to 1V. The added diode in series with the LED string keeps the string where the injection resistor is added as the string that controls the output voltage. Use an injection transformer to insert the injection voltage from test to ref. The loop analyzer can plot the gain and phase of the closed loop where the loop gain is T_{JW}/R_{JW}. The crossover frequency occurs at the frequency where the gain is 0db. The phase margin at that frequency should exceed 45° for guaranteed stable operation. The optimum phase margin should exceed 60°. An example of the closed-loop gain and phase margin on a MAX16813B boost is shown in Figure 9. This measurement was done on the typical application shown in Figure 2 at an input voltage of 12V.

The crossover frequency (f_C) in the design is 12kHz and the phase margin is 74°. It is important to verify the loop stability and phase margin before the design goes into production. The typical crossover frequency should be in the range of $f_{SW}/10 > f_C > f_{SW}/20$ where f_C is the crossover frequency. The phase margin should exceed 60° if possible. It is also important to check the performance of the design at the transition point from low dim to high dim and vice versa. When the device is switching over from low DIM mode to normal DIM mode, the output voltage on the boost will change. The boost output voltage drops when there is a transition from low dim to normal dim made. If the closed-loop phase margin is less than 45°, the output voltage might ring when the transition from LO dim to normal dim occurs. This can cause flicker of the LEDs and this flicker needs to be prevented by increasing the phase margin. If the flicker is still present even when the phase margin exceeds 60°, it may be necessary to increase the output capacitor.

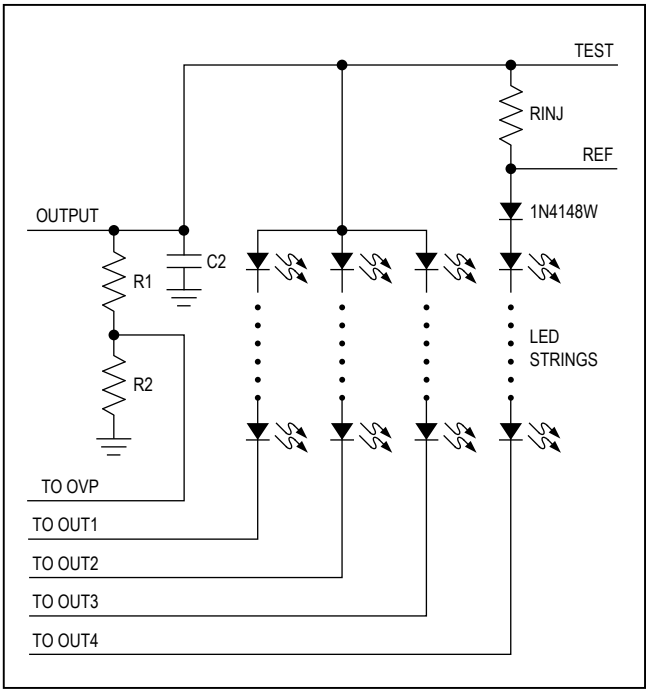


Figure 8. Loop Analyzer Connection to MAX16813B Circuit

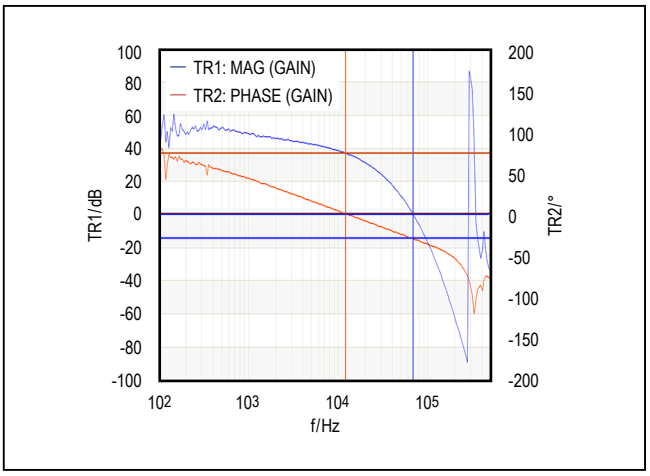


Figure 9. Closed-Loop Gain and Phase Margin

Analog Dimming Using External Control Voltage

Connect a resistor (R_{SETI2}) to the SETI input as shown in Figure 10 for controlling the LED string current using an external control voltage. The device applies a fixed 1.23V bandgap reference voltage at SETI and measures the current through SETI. This measured current multiplied by a factor of 1220 is the current through each one of the four constant-current sink channels. Adjust the current through SETI to get analog dimming functionality by connecting the external control voltage to SETI through the resistor (R_{SETI2}). The resulting change in the LED current with the control voltage is linear and inversely proportional. The LED current control range remains between 20mA to 150mA.

Use the following equation to calculate the LED current set by the control voltage applied:

$$I_{OUT} = \frac{1500}{R_{SETI}} + \frac{(1.23 - V_C)}{R_{SETI2}} \times 1220$$

PCB Layout Considerations

LED driver circuits based on the MAX16813B device use a high-frequency switching converter to generate the voltage for LED strings. Take proper care while laying out the circuit to ensure proper operation. The switching-converter part of the circuit has nodes with very fast voltage changes that could lead to undesirable effects on the sensitive parts of the circuit. Follow the guidelines below to reduce noise as much as possible:

1) Connect the bypass capacitor on V_{CC} as close as possible to the device and connect the capacitor ground to the analog ground plane using vias close to the capacitor terminal. Connect SGND of the device to the analog ground plane using a via close to SGND. Lay the analog ground plane on the inner layer, preferably next to the top layer. Use the analog ground plane to cover the entire area under critical signal components for the power converter.
2) Have a power ground plane for the switching-converter power circuit under the power components (input filter capacitor, output filter capacitor, inductor, MOSFET, rectifier diode, and current-sense resistor). Connect PGND to the power ground plane as close as possible to PGND. Connect all other ground connections to the power ground plane using vias close to the terminals.
3) There are two loops in the power circuit that carry high-frequency switching currents. One loop is when the MOSFET is on (from the input filter capacitor positive terminal, through the inductor, the internal MOSFET, and the current-sense resistor, to the input capacitor negative terminal). The other loop is when the MOSFET is off (from the input capacitor positive terminal, through the inductor, the rectifier diode, output filter capacitor, to the input capacitor negative terminal). Analyze these two loops and make the loop areas as small as possible. Wherever possible, have a return path on the power ground plane for the switching currents on the top-layer copper traces, or through power components. This reduces the loop area considerably and provides a low-inductance path for the switching currents. Reducing the loop area also reduces radiation during switching.
4) Connect the power ground plane for the constant-current LED driver portion of the circuit to LEDGND as close as possible to the device. Connect SGND to PGND at the same point.

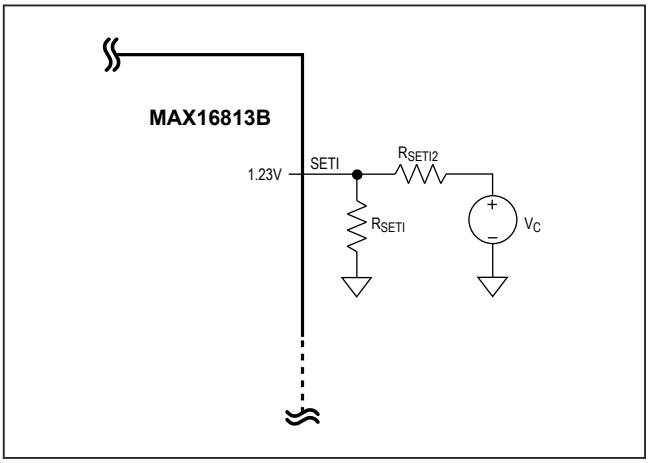


Figure 10. Analog Dimming with External Control Voltage

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16813BATP/V+	-40°C to +125°C	20 TQFN-EP*
MAX16813BAUP/V+	-40°C to +125°C	20 TSSOP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/17	Initial release	—
1	1/18	Removed future product status from MAX16813BAUP/V+ in *Ordering Information*	26

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