PIC24FJ256GA412/GB412 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ256GA412/GB412 family devices that you have received conform functionally to the current Device Data Sheet (DS30010089**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ256GA412/GB412 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 8, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ256GA412/GB412 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A2			A2
PIC24FJ256GA412	6112h	0010h	PIC24FJ256GB412	6116h	0010h
PIC24FJ128GA412	610Ah		PIC24FJ128GB412	610Eh	
PIC24FJ64GA412	6102h		PIC24FJ64GB412	6106h	
PIC24FJ256GA410	6111h		PIC24FJ256GB410	6115h	
PIC24FJ128GA410	6109h		PIC24FJ128GB410	610Dh	
PIC24FJ64GA410	6101h		PIC24FJ64GB410	6105h	
PIC24FJ256GA406	6110h		PIC24FJ256GB406	6114h	
PIC24FJ128GA406	6108h		PIC24FJ128GB406	610Ch	
PIC24FJ64GA406	6100h		PIC24FJ64GB406	6104h	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC24FJ256GA412/GB412 Family Flash Programming Specification"* (DS30010073) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A2
POR/BOR	Reset	1.	If the Brown-out Reset (BOR) is disabled, the part may fail to come out of the Reset state during the VDD power-down and the subsequent power-up condition.	X
POR/BOR	Reset	2.	If the Brown-out Reset (BOR) is disabled, the part may not start at the minimum VDD specification.	X
POR/BOR	Reset	3.	The POR bit may get set at temperatures below 0ºC when BOR occurs.	X
Reset	Trap Conflict	4.	The TRAPR bit is not getting set when a hard trap conflict occurs.	X
I^2C	Slave Mode	5.	While AHEN = 1, a slave interrupt may be asserted after an address mismatch if the data byte matches the device slave address.	X
I^2C	Slave Mode	6.	In 10-Bit Addressing Slave mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence.	X
MCCP/SCCP (Output Compare)	Single Edge Event	7.	The Single Edge Compare Event Status (SCEVT) bit is not setting for MOD[3:0] = 0010.	X
SPI	Slave Mode	8.	In Slave mode, the RX watermark interrupt does not wake the device from Sleep, which causes loss of the first few receive bytes.	X
SPI	Audio PCM/DSP	9.	SPI module follows Right Justified mode of transmission and reception in PCM/DSP mode.	X
SPI	Slave Mode Audio L/R Justified	10.	In Slave mode, the Most Significant bit (MSb) is missed in Left and Right Justified modes.	X
SPI	Slave Mode Audio L/R Justified	11.	At start-up, the Idle state of the SDOx pin will be the same as the Most Significant bit of the first data packet loaded when in Slave mode and configured for Left Justified or Right Justified mode.	X
SPI	Master Mode	12.	While operating in Master mode (MSTEN = 1), the transmit watermark interrupt is not asserted if there is more than one entry in the FIFO buffer.	X
Primary XT and HS Oscillator (POSC)	Primary Oscillator Start-up Timer (OST)	13.	The OST may indicate the oscillator is ready for use too early.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: POR/BOR

If Brown-out Reset (BOR) is disabled, the part may fail to come out of the Reset state during the VDD power-down and the subsequent power-up condition.

When BOR is disabled, in extremely rare cases, the part remains in the Reset state during the VDD power-down (not until VSS), followed by the subsequent power-up condition.

Work around

There are three known work arounds for this issue:

- Always enable BOR by setting the Configuration Fuse bit, BOREN (FPOR[0]) = 1.
- Use an external voltage supervisor chip on the MCLR pin to hold the MCLR low when the power supply voltage is between 1.4V and 2.0V. Release MCLR after the VDD is in the operating range.
- Make sure that VDD goes all the way to VSS before powering on.

Affected Silicon Revisions

A2							
X							

2. Module: POR/BOR

When BOR is disabled, the part may not start at the minimum VDD specification.

Work around

There are two known work arounds for this issue:

- Always enable BOR by setting the Configuration Fuse bit, BOREN (FPOR[0]) = 1.
- For initial start-up, make sure that the minimum VDD is more than 2.2V. Once the device is powered, it will operate down to the minimum VDD voltage specified in the data sheet specifications. This is a typical battery-operated application with a fully charged battery installed into the application. The part will continue to operate to the data sheet specifications.

Affected Silicon Revisions

A2							
X							

3. Module: POR/BOR

The POR Reset flag bit (RCON[0]) may get set in addition to the BOR Reset flag bit (RCON[1]) when a BOR Reset occurs at temperatures below 0ºC.

Work around

None.

Affected Silicon Revisions

A2							
X							

4. Module: Reset

If a lower priority address error trap occurs while a higher priority oscillator failure trap is being processed, the TRAPR bit (RCON[15]) is not set. A Trap Conflict Reset does not occur as expected and the device may stop executing code.

Work around

None. However, a MCLR/POR/WDT Reset will recover the device.

Affected Silicon Revisions

A2							
X							

5. Module: I²C

When the device is operating as an I²C slave with multiple slaves on the I²C bus, and if the master is communicating with another slave and a transmitted data byte matches the slave address of the device, the device may generate an unexpected slave interrupt.

Work around

User application should ignore the extra interrupt until a Stop condition is seen on the data bus.

Affected Silicon Revisions

A2							
X							

6. Module: I²C

In I²C Slave 10-Bit Addressing mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status (ACKTIM) bit (I2CxSTAT[13]) is not asserted during an Acknowledgment sequence.

The issue is not seen during the reception of the lower address byte (A7 to A0) and data bytes. The hardware asserts the ACKTIM bit on the falling edge of the eighth clock and deasserts on the rising edge of the ninth clock. In this case, ACKTIM is not asserted on the upper address byte reception. When AHEN (I2CxCONH[1]) = 1, the clock is stretched after the 8th falling edge and the ACKTIM bit is asserted until the clock is released. If AHEN = 0, the clock is not stretched and ACKTIM is asserted during the Acknowledgment sequence, which is of a very short duration. Therefore, the user application can see this issue of the ACKTIM bit not getting asserted when AHEN = 1.

Work around

Instead of polling for ACKTIM to be asserted, poll for the RBF flag (I2CxSTAT[1]).

Affected Silicon Revisions

A2							
X							

7. Module: MCCP/SCCP (Output Compare)

The Single Edge Compare Event Status (SCEVT) bit (CCPxSTATL[3]) may not set for Single Edge mode, drive output low on match (MOD[3:0] = 0010). In this case, the comparator output is still driven low on the first CCPxRA match, but will not be reset by writing '0' to the SCEVT bit.

All MCCPs/SCCPs are affected.

Work around

This mode may be used to trigger a single event before the module must be reinitialized by clearing and setting CCPON (CCPxCON1L[15]).

The Capture/Compare Interrupt Flag (CCPxIF) still occurs on a match with CCPxRA, and can be used to update the user that a compare event has been triggered and the module needs to be reset.

Affected Silicon Revisions

A2							
X							

8. Module: SPI

The RX watermark interrupt is not asserted for the first few bytes in Sleep mode when the SPI slave is configured for Enhanced Buffer 8, 16 or 32-Bit mode (MSTEN = 0, ENHBUF = 1).

The interrupt does not get asserted for any value of buffer mask (RXMSK[5:0]). For 8-bit mode, interrupt after 32; for 16-bit mode, interrupt after 16; for 32-bit mode, interrupt after 8.

Work around

Tie the SPI clock pin to the external interrupt in the Slave device. This work around has a limitation on SPI speed of 5 MHz.

Affected Silicon Revisions

A2							
X							

9. Module: SPI

The SPI module, irrespective of master or slave configured for PCM/DSP mode, follows the Right Justified mode of transmission and reception.

Work around

None.

Affected Silicon Revisions

A2							
X							

10. Module: SPI

In Slave Left Justified or Right Justified modes, the Most Significant bit of the data is missed.

Work around

None.

Affected Silicon Revisions

A2							
X							

11. Module: SPI

When the SPI is a slave and is configured for Left Justified or Right Justified mode at start-up, the Idle state of the SDOx pin will be the same as the Most Significant bit (MSb) of the first data packet loaded to the buffer.

For example:

1. If the first data loaded to the buffer is 0xA5A5 (where the MSb is '1'), then at start-up, the Idle state of SDOx will be HIGH.
2. If the first data loaded to the buffer is 5A5A (where the MSb is '0'), then at start-up, the Idle state of SDOx will be LOW.

Work around

None.

Affected Silicon Revisions

A2							
X							

12. Module: SPI

While operating in Master mode (MSTEN = 1), the transmit watermark interrupt is not asserted if there is more than one entry in the FIFO buffer.

This means, for various modes, that the interrupt is not asserted for:

- More than one byte to be transmitted in 8-bit mode;
- More than one word to be transmitted in 16-bit mode; or
- More than one double word to be transmitted in 32-bit mode.

Work around

None.

Affected Silicon Revisions

A2							
X							

13. Module: Primary XT and HS Oscillator (POSC)

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early.

Clocking the device before the oscillator is ready may result in incorrect execution and exceptions.

This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize POSC.
3. Switch to the POSC source.

Example 1 shows a work around for the device power-on and Example 2 explains the work around when the device wakes from Sleep.

EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma config FNOSC = FRCDIV          // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
void    main()
{
// configure REFO to request POSC
REFOCONLbits.ROSEL = 2;                // POSC = 2
REFOCONLbits.ROOUT = 0;                // disable output
REFOCONLbits.ROEN =  1;                // enable module
// wait for POSC stable clock
// this delay may vary depending on different application conditions
// such as voltage, temperature, layout, XT or HS mode and components
{ // 9 ms delay
unsigned short delay = (unsigned short)(0.009*8000000/2);
asm     volatile ("repeat %0 \n nop" : : "r"(delay));
}
// switch to POSC = 2
__builtin_write_OSCCONH(0x02);         // 2 = PRIMARY OSC
__builtin_write_OSCCONL(OSCCON | 0x01);
// Wait for Clock switch to occur
while   (OSCCONbits.OSWEN==1);
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

EXAMPLE 2: USING POSC WHEN WAKING FROM SLEEP

```
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD

- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
__builtin_write_OSCCONH(0x02);           // 2 = PRIMARY OSC
__builtin_write_OSCCONL(OSCCON | 0x01);
// Wait for Clock switch to occur
while   (OSCCONbits.OSWEN== 1);
// enter sleep mode
Sleep();
// configure REFO to request POSC
REFOCONLbits.ROSEL = 2;                  // POSC = 2
REFOCONLbits.ROOUT = 0;                  // disable output
REFOCONLbits.ROEN =  1;                  // enable module
// wait for POSC stable clock
// this delay may vary depending on different application conditions
// such as voltage, temperature, layout, XT or HS mode and components
{ // 9 ms delay
unsigned short delay = (unsigned short)(0.009*8000000/2);
asm     volatile ("repeat %0 \n nop" : : "r"(delay));
}
// switch to POSC = 2
__builtin_write_OSCCONH(0x02);           // 2 = PRIMARY OSC
__builtin_write_OSCCONL(OSCCON | 0x01);
// Wait for Clock switch to occur
while   (OSCCONbits.OSWEN== 1);
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

Affected Silicon Revisions

A2							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30010089**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (7/2015)

Initial release of this document; issued for silicon revision A2.

Rev B Document (6/2016)

Adds silicon issues **8. Module: "SPI"**, **9. Module: "SPI"**, **10. Module: "SPI"**, **11. Module: "SPI"**, **12. Module: "SPI"** and **13. Module: "Primary XT and HS Oscillator (POSC)"**.

Rev C Document (12/2016)

Updates the Device Data Sheet reference to the current revision D (DS30010089**D**) and adds additional content for PIC24FJ256GA412 family devices.

Adds data sheet clarifications **1. Module: "Memory Organization"** and **2. Module: "Electrical Characteristics"**.

Rev D Document (11/2019)

Updates the Device Data Sheet reference to the current revision E (DS30010089**E**).

Updates silicon issue **4. Module: "Reset"**.

Removes data sheet clarifications **1. Module: "Memory Organization"** and **2. Module: "Electrical Characteristics"**, since these issues have been corrected in the current Device Data Sheet revision E.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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