GaAs, pHEMT, MMIC, Low Noise Amplifier, 0.3 GHz to 20 GHz

Enhanced Product

HMC1049SCPZ-EP

FEATURES

- Low noise figure: 2 dB
- P1dB output power: 15 dBm
- P_{SAT} output power: 17 dBm
- High gain: 14 dB
- Output IP3: 23 dBm
- Supply voltage: V_{DD} = 7 V at 70 mA
- 50 Ω matched I/O
- 32-lead, 5 mm × 5 mm LFCSP package: 25 mm^2

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended industrial temperature range: −55°C to +105°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Radars
- Military communications
- Very small aperture terminals (VSATs) and satellite communications (SATCOM)
- Unmanned systems

FUNCTIONAL BLOCK DIAGRAM

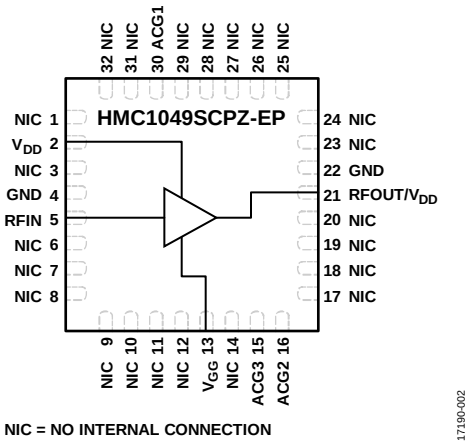

Figure 1.

GENERAL DESCRIPTION

The HMC1049SCPZ-EP is a Gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), low noise amplifier (LNA) that operates between 0.3 GHz and 20 GHz. This LNA provides 14 dB of small signal gain, 2 dB noise figure, and an IP3 output of 23 dBm, yet requires only 70 mA from a 7 V supply. The P1dB output power of 15 dBm enables the LNA to function as a local oscillator (LO) driver for balanced, inphase/quadrature (I/Q), or image rejection mixers. V_{DD} can also be applied to Pin 21, although Pin 21 requires a bias tee with V_{DD} = 4 V. The HMC1049SCPZ-EP amplifier input/outputs (I/Os) are internally matched to 50 Ω, and the device is supplied in a compact, leadless 5 mm × 5 mm LFCSP package.

Additional application and technical information can be found in the HMC1049LP5E data sheet.

Rev. 0

Document Feedback

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REVISION HISTORY

1/2019—Revision 0: Initial Version

SPECIFICATIONS

0.3 GHZ TO 1 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 7 V, I_{DD} = 70 mA, 50 Ω system.

Table 1.

Parameter[1]	Min	Typ	Max	Unit
FREQUENCY RANGE	0.3		1	GHz
GAIN	13.5	16		dB
Gain Variation over Temperature		0.006		dB/°C
NOISE FIGURE		2.5	3.5	dB
RETURN LOSS				
Input		15		dB
Output		8		dB
OUTPUT				
Output Power for 1 dB Compression (P1dB)		16		dBm
Saturated (P_{SAT})		18		dBm
Output Third-Order Intercept (IP3)[2]		25		dBm
TOTAL SUPPLY CURRENT		70		mA

[1] Adjust V_{GG} between −2 V and 0 V to achieve I_{DD} = 70 mA typical.
[2] Measurement taken at output power (P_{OUT}) per tone = 8 dBm.

1 GHZ TO 14 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 7 V, I_{DD} = 70 mA, 50 Ω system.

Table 2.

Parameter[1]	Min	Typ	Max	Unit
FREQUENCY RANGE	1		14	GHz
GAIN	12	14		dB
Gain Variation over Temperature		0.019		dB/°C
NOISE FIGURE		2	3	dB
RETURN LOSS				
Input		13		dB
Output		15		dB
OUTPUT				
Output Power for 1 dB Compression (P1dB)		15		dBm
Saturated (P_{SAT})		17		dBm
Output Third-Order Intercept (IP3)[2]		23		dBm
TOTAL SUPPLY CURRENT		70		mA

[1] Adjust V_{GG} between −2 V and 0 V to achieve I_{DD} = 70 mA typical.
[2] Measurement taken at P_{OUT} per tone = 8 dBm.

14 GHZ TO 20 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 7 V, I_{DD} = 70 mA, 50 Ω system.

Table 3.

Parameter[1]	Min	Typ	Max	Unit
FREQUENCY RANGE	14		20	GHz
GAIN	10	12		dB
Gain Variation over Temperature		0.017		dB/°C
NOISE FIGURE		3.0	4.5	dB
RETURN LOSS				
Input		14		dB
Output		13		dB
OUTPUT				
Output Power for 1 dB Compression (P1dB)		13		dBm
Saturated (P_{SAT})		15		dBm
Output Third-Order Intercept (IP3)[2]		18		dBm
TOTAL SUPPLY CURRENT		70		mA

[1] Adjust V_{GG} between −2 V and 0 V to achieve I_{DD} = 70 mA typical.
[2] Measurement taken at P_{OUT} per tone = 8 dBm.

Table 4. Typical Supply Current vs. V_{DD}

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Supply Current, I_{DD}[1]	V_{DD} = 5 V		70		mA
	V_{DD} = 6 V		70		mA
	V_{DD} = 7 V		70		mA

[1] Adjust V_{GG} to achieve I_{DD} = 70 mA.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Drain Bias Voltage (V_{DD})	10 V
Drain Bias Voltage (RFOUT/V_{DD})	7 V
RF Input Power	18 dBm
Gate Bias Voltage (V_{GG})	−2 V to +0.2 V
Junction Temperature (T_J)	175°C
Continuous Power Dissipation, P_{DISS}[1]	
T_{CASE} = 85°C	3.34 W
T_{CASE} = 105°C	2.60 W
Peak Reflow Temperature	260°C
Temperature	
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +105°C
ESD Sensitivity, Human Body Model (HBM)	Class 1A

[1] For maximum power dissipation vs. case temperature, see Figure 2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-32-29	61.1	8.9	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.
[2] Thermal impedance simulated values are based on a JEDEC 1S0P thermal test board. See JEDEC JESD51.

POWER DERATING CURVES

Figure 2 shows the maximum power dissipation vs. case temperature.

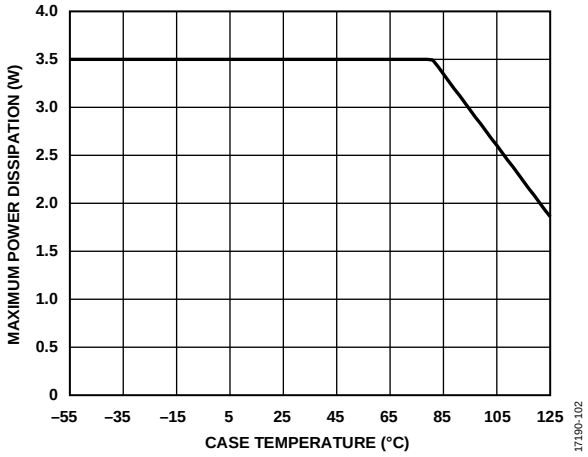


Figure 2. Maximum Power Dissipation vs. Case Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

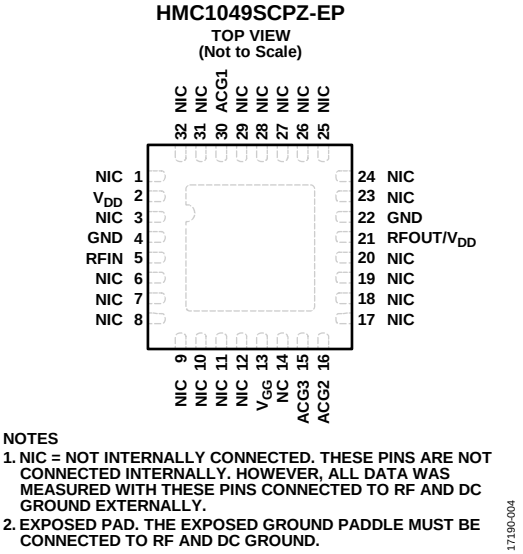


Figure 3. Pin Configuration Diagram

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description[1]
1, 3, 6 to 12, 14, 17 to 20, 23 to 29, 31, 32	NIC	Not Internally Connected. These pins are not connected internally. However, all data was measured with these pins connected to RF and dc ground externally (see the Typical Performance Characteristics section for data plots).
2	V_{DD}	Power Supply Voltage for the Amplifier. External bypass capacitors (100 pF and 0.01 µF) are required.
4, 22	GND	Ground. Connect Pin 4 and Pin 22 to RF and dc ground.
5	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω.
13	V_{GG}	Gate Control for Amplifier. Adjust the voltage to achieve I_{DD} = 70 mA. External bypass capacitors of 100 pF, 0.01 µF, and 4.7µF are required.
15, 16	ACG2, ACG3	Low Frequency Termination. External bypass capacitors of 100 pF are required.
21	RFOUT/V_{DD}	RF Output/Alternate Power Supply Voltage for the Amplifier. An external bias tee is required when used as alternative V_{DD}. This pin is dc-coupled and matched to 50 Ω.
30	ACG1	Low Frequency Termination. An external bypass capacitor of 100 pF is required.
	EP	Exposed Pad. The exposed ground paddle must be connected to RF and dc ground.

[1] See the Interface Schematics section for pin interfaces.

INTERFACE SCHEMATICS

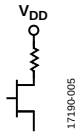


Figure 4. V_{DD} Interface

Figure 5. GND Interface

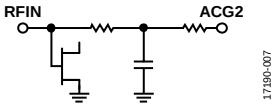


Figure 6. RFIN Interface

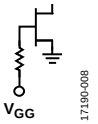


Figure 7. V_{GG} Interface

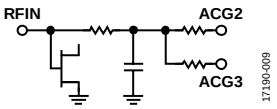


Figure 8. ACG2 and ACG3 Interface

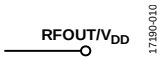


Figure 9. RFOUT/V_{DD} Interface

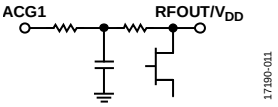


Figure 10. ACG1 Interface

TYPICAL PERFORMANCE CHARACTERISTICS

Data taken with V_{DD} applied to Pin 2, V_{DD} = 7 V.

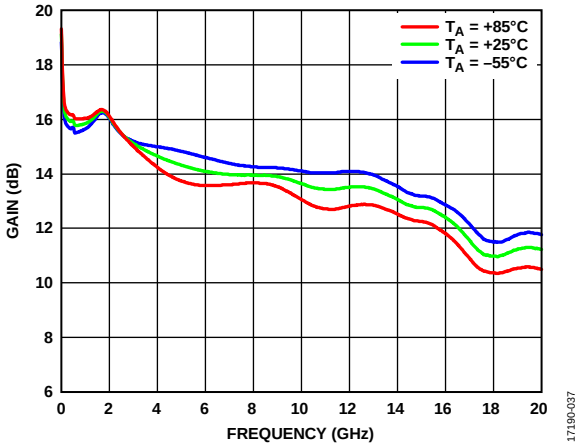


Figure 11. Gain vs. Frequency at Various Temperatures

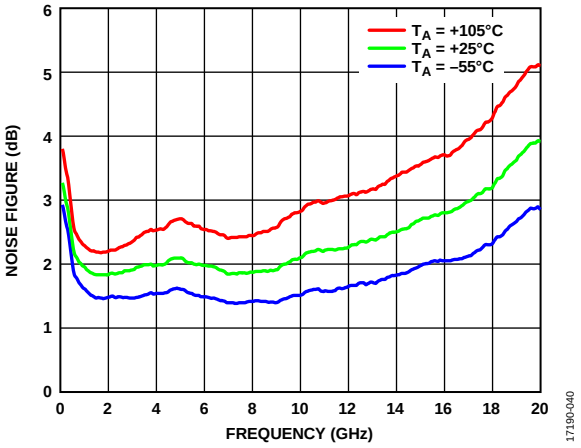


Figure 14. Noise Figure vs. Frequency at Various Temperatures

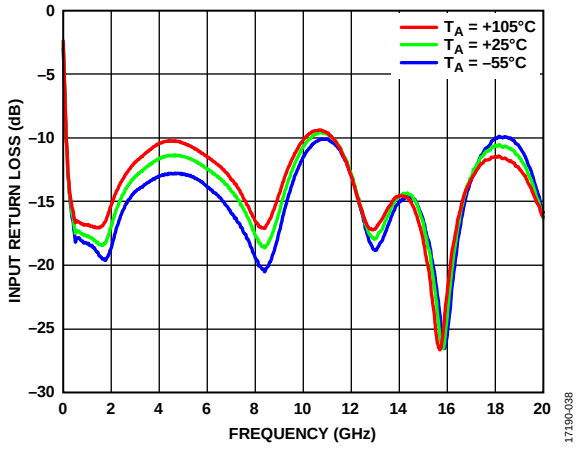


Figure 12. Input Return Loss vs. Frequency at Various Temperatures

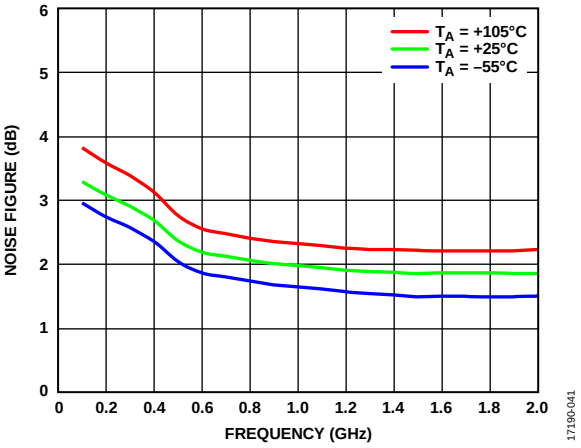


Figure 15. Noise Figure vs. Frequency at Various Temperatures, Low Frequency

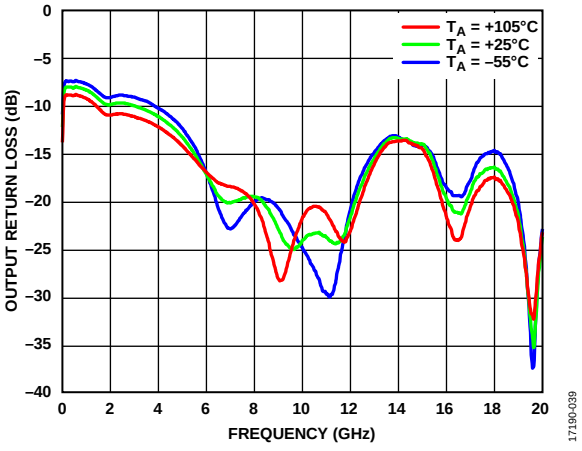


Figure 13. Output Return Loss vs. Frequency, at Various Temperatures

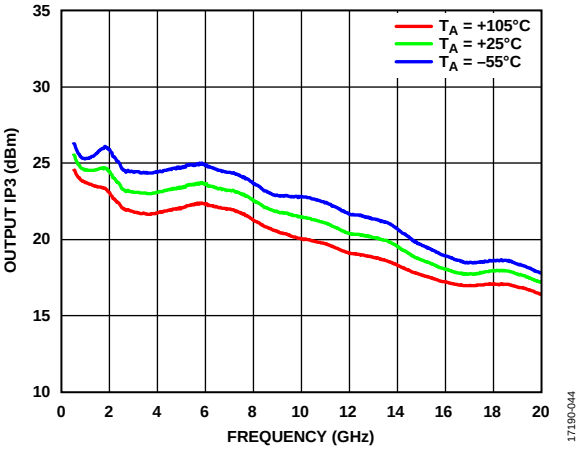


Figure 16. Output IP3 vs. Frequency at Various Temperatures

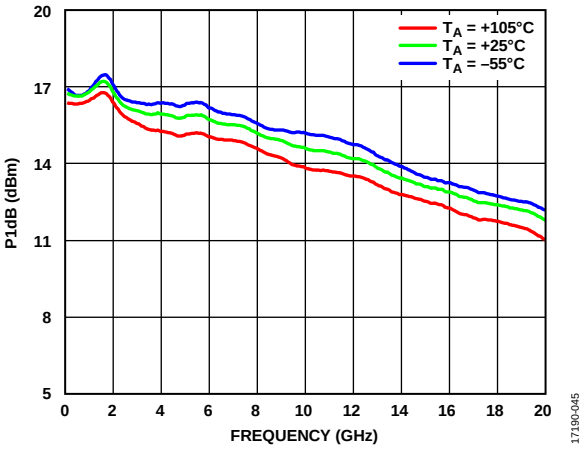


Figure 17. P1dB vs. Frequency at Various Temperatures

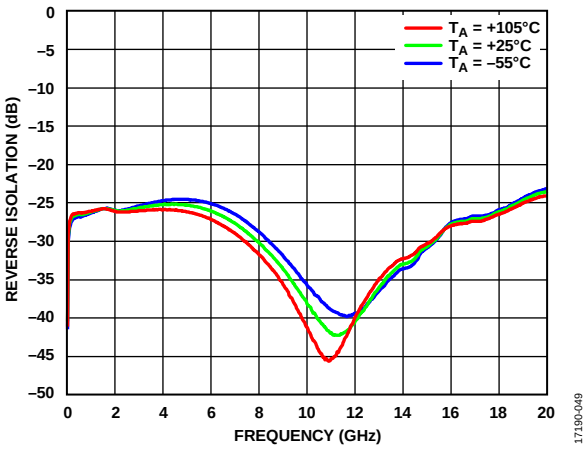


Figure 19. Reverse Isolation vs. Frequency at Various Temperatures

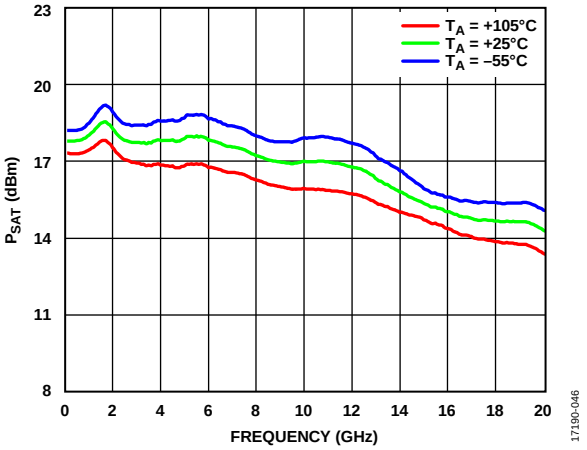
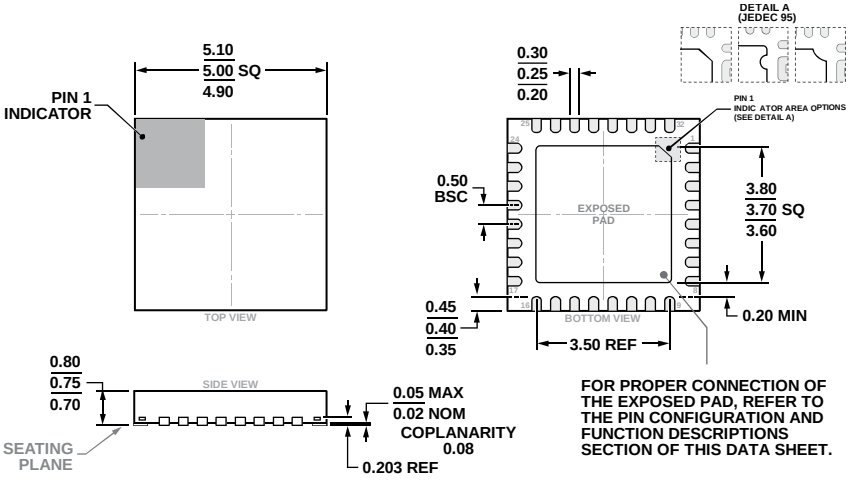


Figure 18. P_{SAT} vs. Frequency at Various Temperatures

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-4

Figure 20. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm and 0.75 mm Package Height
(CP-32-29)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Lead Finish	Package Description	Package Option
HMC1049SCPZ-EP-R7	−55°C to +105°C	Nickel/palladium/gold (NiPdAu)	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-29

[1] Z = RoHS Compliant Part.