AN_652X_041 March 2009

Design for EMC

1 INTRODUCTION

Design for electromagnetic compatibility (EMC) must be a top priority from the very beginning of the meter design cycle. Routine EMC/EMI tests for metering products typically include:

- Conducted and Radiated Emissions tests
- RF Immunity tests with and without load
- Electrostatic Discharge (ESD) tests
- Electrical Fast transient (EFT) tests

Successfully passing these tests depends on many factors, including:

- Schematic design and component selection
- Printed circuit board (PCB) topology, component placement, PCB design
- Input connections and wiring of the sensing elements to the meter
- Firmware code

The methods presented in this document are incorporated into the TERIDIAN Demo Boards, enhancing EMI compatibility without affecting accuracy performance of the meter.

Following the recommendations outlined in this document in the initial phase of schematic and PCB design helps generating EMI/EMC compliant designs up front, avoiding potential rework of PCBs.

Note: Reference designators are given in a generalized form and do not necessarily relate to the reference designators used on actual TERIDIAN Demo Boards.

2 SCHEMATIC DESIGN

2.1 Pure LCD Pins (SEG Pins)

These pins cannot be configured and are dedicated LCD driver pins. In some designs, restrictions on the choice for *LCD_NUM* may require that some DIO/SEG pins are configured as LCD pins. If not connected to an LCD pin, these unused SEG pins should be terminated to DGND with 22 pF capacitors as shown in Figure 1.

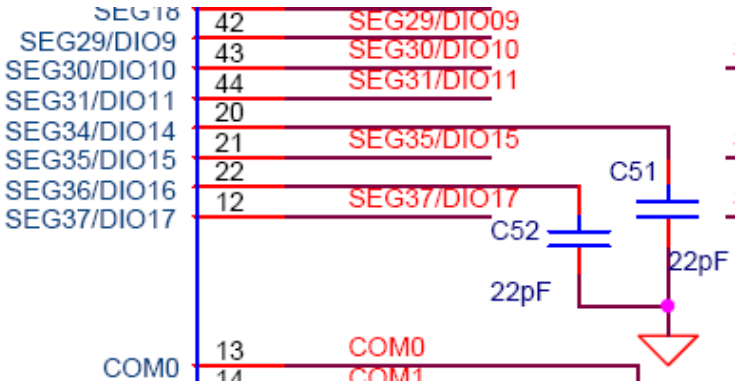

Figure 1: Termination for Unused LCD Pins

If no LCD is used in the design, the pure segment pins can also be tied to DGND. *LCD_E* must be set to zero (power-up default), otherwise current will be drawn from the pins.

2.2 Pure DIO Pins

These pins cannot be configured for other functions and are dedicated DIO pins.

- If pins are left open they should be configured as outputs and set to 0 (low).
- If pins are connected to V3P3 or GND they should be configured as inputs.

2.3 DIO/SEG Pins

These pins can be configured as LCD drivers or DIO.

- If possible, configure as DIO and treat as pure DIO pins (see 2.2).
- If pin cannot be configured as DIO, treat as LCD pin (see 2.1).

2.4 Crystal Oscillator

The crystal oscillator is a very critical component of the meter. It controls basic metering parameters such as accumulation interval, display updates, and sampling rates, but also the RTC. The XOUT and XIN pins on the 71M6521 are connected to high-impedance circuitry which makes them potentially very sensitive to component selection and layout.

- Both capacitors at the crystal should be ceramic capacitors with 27 pF capacitance.
- The crystal should be a 32-kHz type with a load capacitance of 12.5 pF

The crystal body (if a metal-can crystal is used) and the capacitors should have a separate ground, as shown in Figure 2 (blue lines). This ground should be connected to the board ground (GNDD) with a ferrite bead.

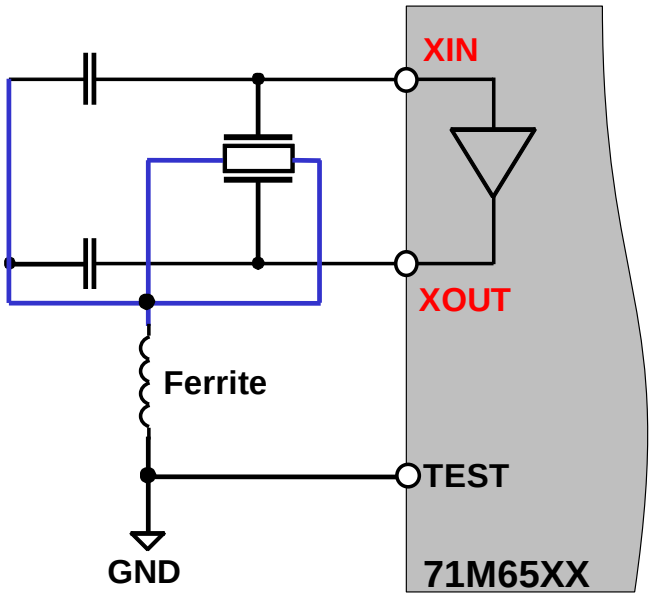

Figure 2: Connecting a Crystal to XIN/XOUT

2.5 V1 Pin

The V1 input pin detects power faults and provides a means to disable the hardware watchdog timer for debugging purposes. When the voltage at the V1 pin falls below +1.6 VDC (VBIAS), the device enters its power-down mode (brownout mode). The firmware decides whether to proceed from there to LCD or sleep mode or whether the IC stays in brownout mode.

Since the hardware watchdog timer (WDT) is automatically disabled when the ICE_E pin is pulled high, the V1 pin need not have a jumper to V3P3 to disable the WDT for emulator connection.

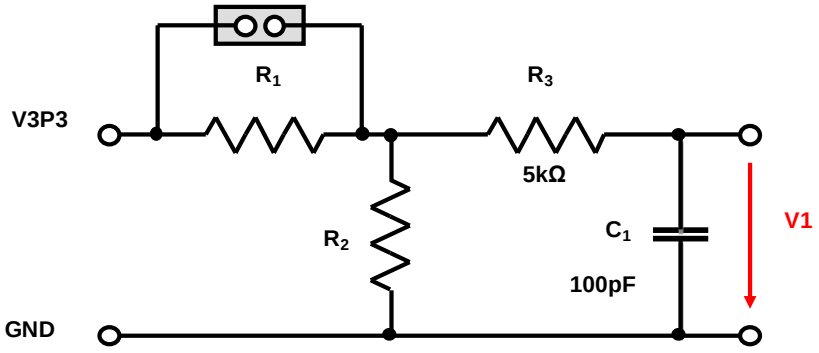

Figure 3: V1 Circuit

The R1 (16.9 kΩ) and R2 (20 kΩ) component values are selected to provide a prompt response to a loss of line power (V1 = 54% of V3P3SYS). That way, V1 crosses VBIAS (1.6 VDC) when V3P3SYS falls below the safe operating voltage of 3.0 VDC, as shown in Figure 4. This figure shows the voltage at V1 following V3P3 in linear fashion, i.e. without hysteresis.

On closer inspection, the development of the voltage at V1 is a little more complex than what Figure 4 shows. The IC itself loads V1 with 1 µA nominal if V1 < VBIAS, and with close to 0 µA if V1 > VBIAS. This is shown in Figure 5. The voltage drop in R3 will cause a hysteresis of R3 * 1 µA, and an additional voltage drop will be created in R1. Combined, the hysteresis current will cause the IC to transition to brownout mode at a slightly lower supply voltage when system/board power is moving down, whereas the transition from brownout to mission mode still happens at the supply voltage determined by the resistor divider ratio formed by R1 and R2. This creates the narrow voltage band shown in yellow in Figure 6 that guarantees that the IC is not rapidly transitioning in between power modes when the V1 voltage stays close to 1.6 VDC.

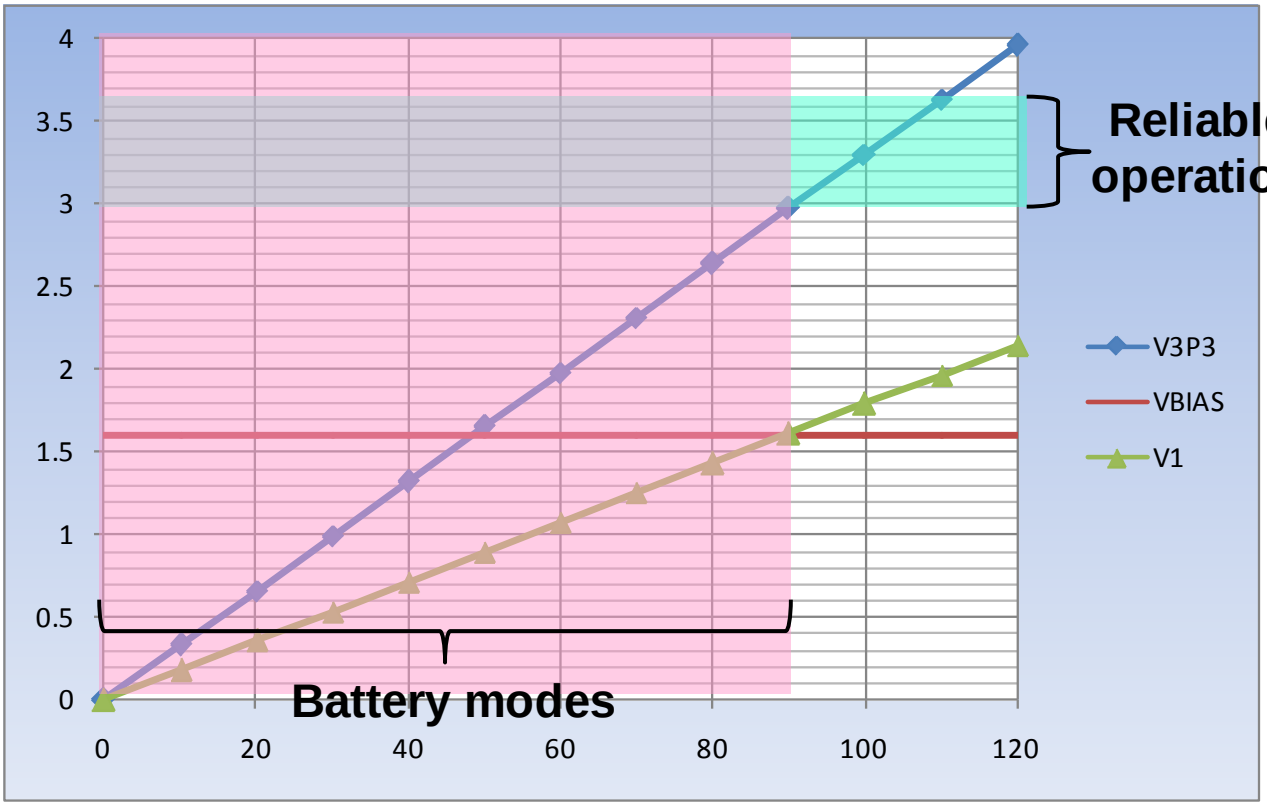

Figure 4: Operation Modes Controlled by the V1 Pin

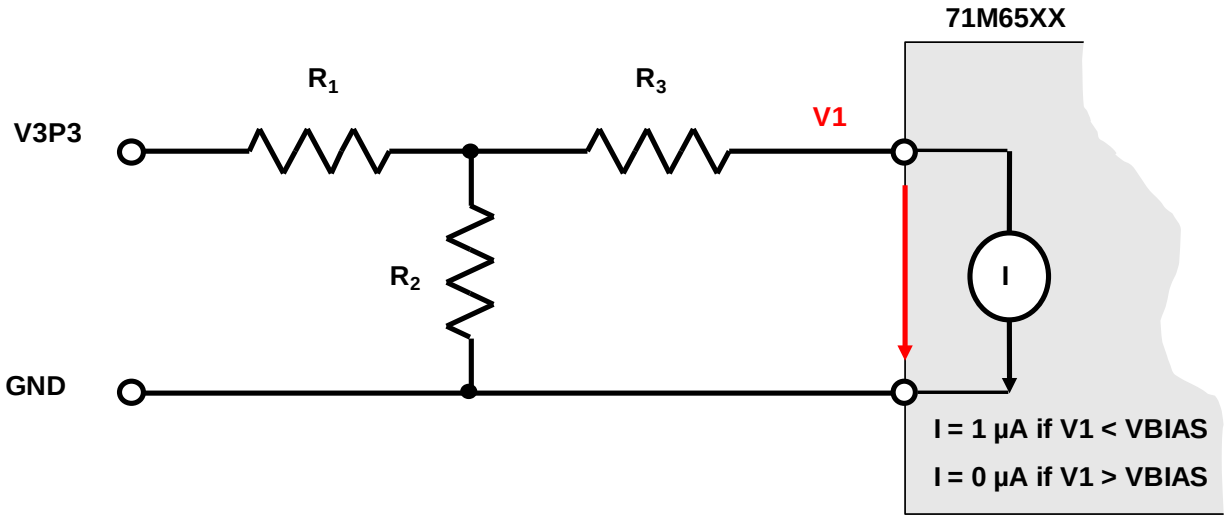

Figure 5: Generation of Hysteresis at the V1 Pin

It is important to note that the capacitor at V1 (C1) must not be allowed to be large. A large capacitor will form a low-pass filter with R1 and R3 causing a delay between V3P3 and V1. In extreme cases this could mean that V1 signals a voltage above VBIAS (mission mode) while V3P3 is in reality at a low (unsafe) voltage.

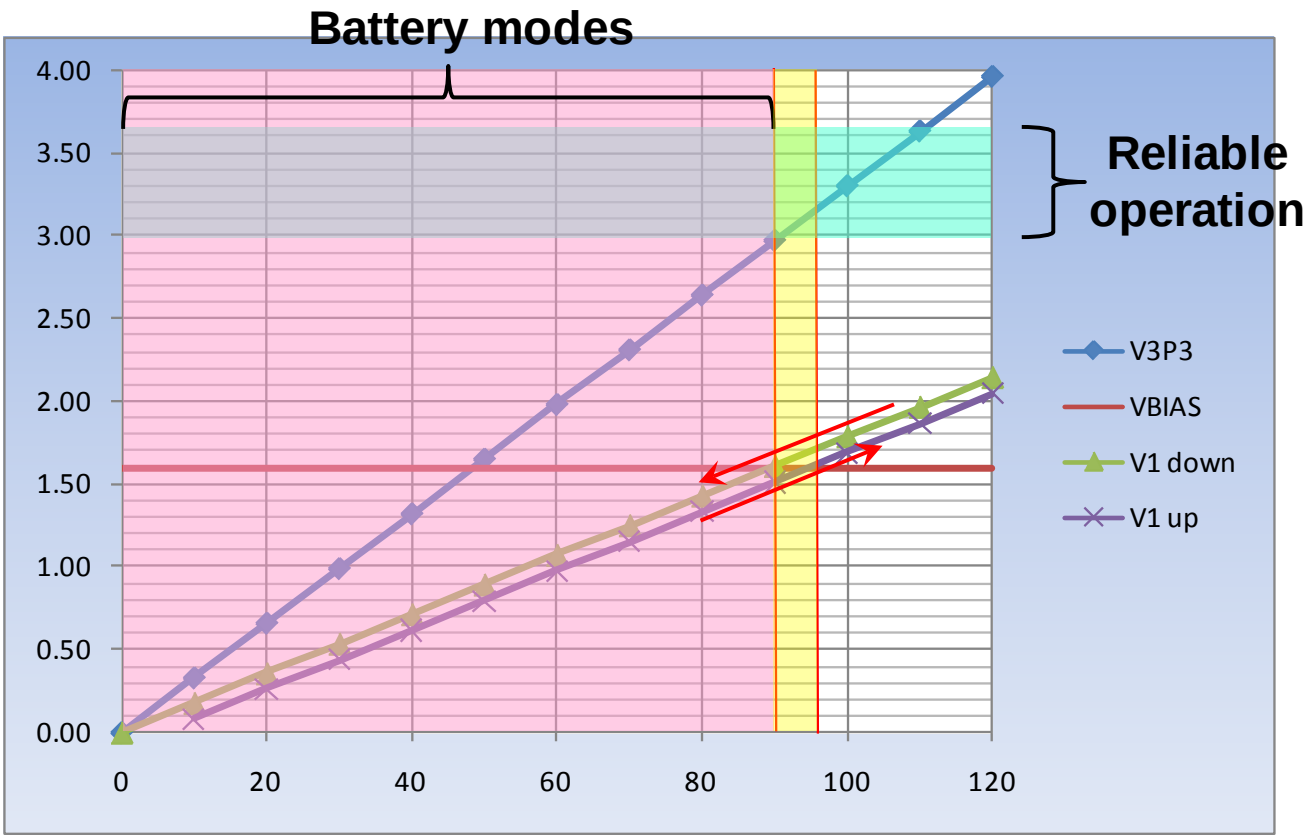

Figure 6: Hysteresis at the V1 Pin

2.6 VREF Pin

The VREF pin can be connected to the internal reference voltage of the ADC. For best EMC performance:

- Leave the VREF pin open.
- Disable/disconnect the pin in firmware (*VREF_DIS* = 0 and *VREF_CAL* = 0)

2.7 VBAT Pin

Noise at the VBAT pin could affect the contents of the RTC registers used for time-keeping. It is recommended to protect the VBAT pin with the components shown in Figure 7

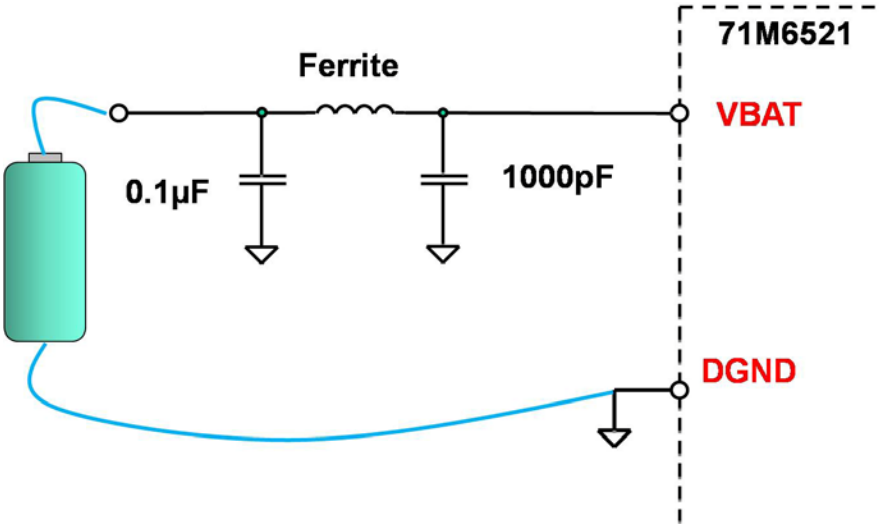

Figure 7: Components for the VBAT Pin

2.8 Serial Port (UART) Pins

The pins TX, RX, OPT_TX, and OPT_RX provide access to the internal UARTs (general-purpose UART0 and optical port UART1). Spurious transitions on the RX and OPT_RX pins should be avoided because they could trigger firmware activity and garbled serial data. Configure the pins OPT_TX, OPT_RX, TX and RX as outputs when not used.

- Unused pins: Terminate to GNDD or V3P3SYS
- Used receive pins RX, OPT_RX: Use a combination of 10 kΩ resistor and 100 pF capacitor to GND

2.9 PB Pin

This pin causes a transition from sleep or LCD mode to brownout mode and should therefore be protected from spurious signals:

- Use a combination of a 10 kΩ resistor and 100 pF capacitor to GND

2.10 Reset Pin

Since the 71M6521 generates its own reset signal on power-up, the reset pin is only required for prototyping. For best rejection of EMI the reset pin should be grounded, as shown in Figure 8

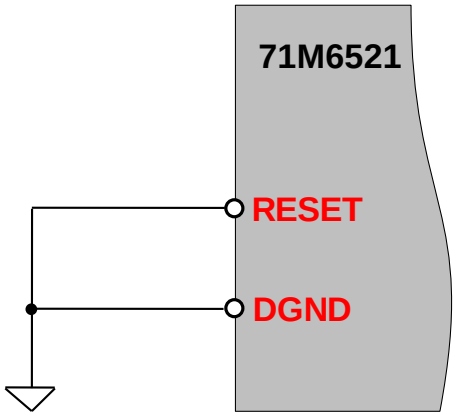

Figure 8: Reset Pin

2.11 ICE-Interface

Figure 9 shows the recommended connections for the ICE-interface. The E_RST and E_RXTX pins should be blocked by 22 pF capacitors to ground. The ICE_E pin should be pulled down to GNDD with a resistor in the range of 200 Ω.

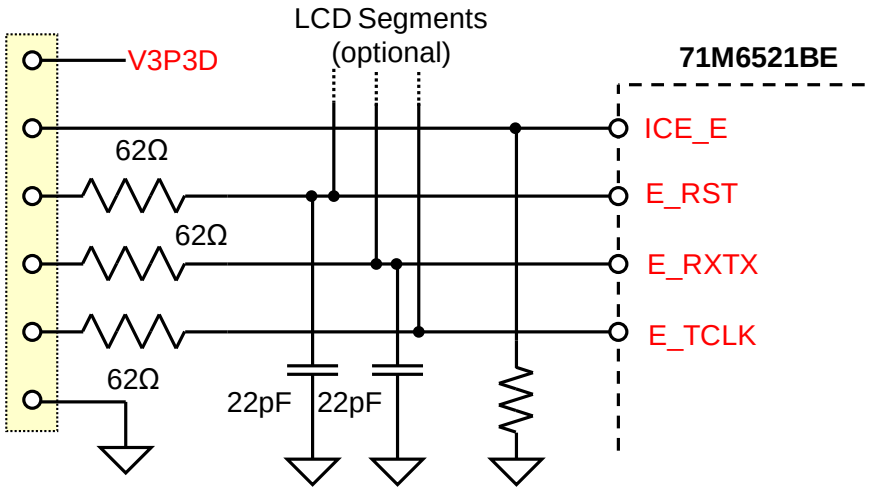

Figure 9: ICE-Interface

It is useful to bring out the ICE_E signal to the programming connector. This is useful when the 71M6521 is programmed with the TFP2 flash programmer. In some situations, the TFP-2 can implement the proper sequence for erasing and programming the 71M6521. When the *SECURE* bit is set, and reprogramming is required on a meter board that utilizes a battery, the following sequence is used by the TFP-2:

- TFP-2 erases flash using ICE_E = high
- TFP-2 then pulls ICE_E = low → a watchdog reset occurs
- TFP-2 pulls ICE_E = high
- TFP-2 programs the 71M6521

2.12 Connecting Other IC Pins

All signals to and from the 71M652X IC must be examined carefully for EMC/EMI susceptibility.

The following list of precautions detail design considerations for the IC pins not mentioned above:

1. Terminate all unused current and voltage inputs (**IA, IB, VA, VB**) to V3P3.
2. A 10 µF tantalum capacitor must decouple the power and ground star points. The **V3P3A** pin and ground pin of the IC must have a clean and direct connection to the star points.
3. The V3P3SYS, V3P3A should be fed from the Star point as described.
4. The GNDD and GNDA pins should also be fed from the GND star point.
5. Place a 0.1µF capacitor adjacent to the **V2P5** pin between the V2P5 pin and ground.
6. CKTEST/SEG19 can be terminated with 22 pF as a dummy SEG load if this pin is not used for clock output.
7. Connect the **VBAT** pin to V3P3 when no battery is used.
8. Connect the **X4MHZ** pin directly to ground.
9. V3P3D should not be loaded by more than a 0.1 µF capacitor.

3 SENSOR INTERFACE

The interfaces to sensors such as CTs, shunt resistors and resistive voltage dividers are very critical for the EMC performance of a meter. Accurate display and recording of energy under EMI conditions depends on the design of the current and voltage inputs. Improper design may lead to erroneous measurements or resets.

The input signal conditioning circuit depends on the type of current sensor used. Each of the current sensor types are individually discussed in this section.

3.1 Current Transformers

Figure 10 shows the recommended input signal conditioning circuit.

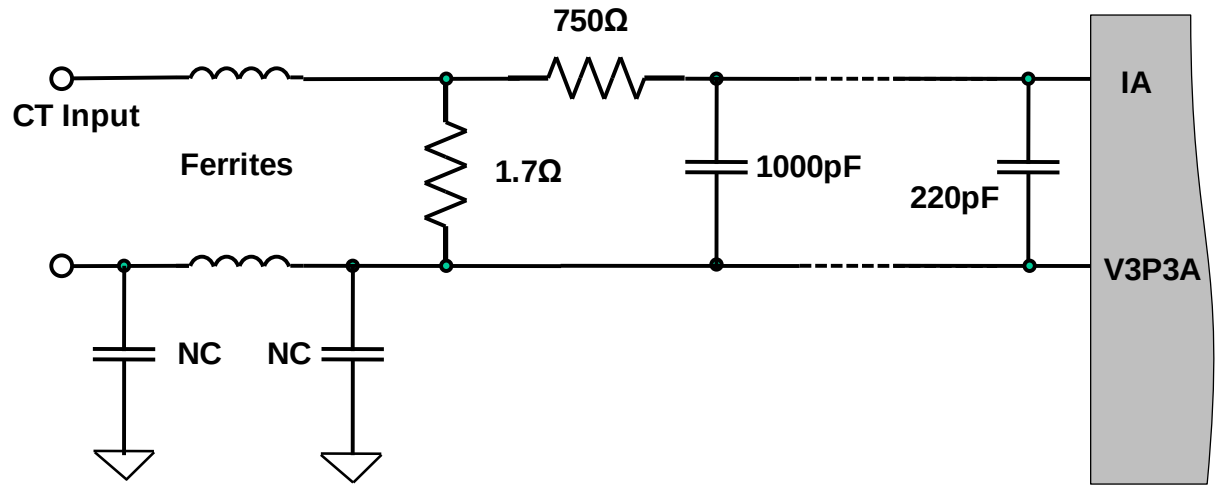

Figure 10: CT Input Signal Processing Circuit

Key recommendations for the CT input signal conditioning circuit are:

1. Ferrite beads at the CT input provide 600 Ω impedance for common mode signals above 100 MHz (use TDK MMZ2012S601A or equivalent).
2. The combination of the 750 Ω resistor and the 1000 pF capacitor provides a low-pass filter for differential signals with a cutoff frequency of 212 kHz. Depending on the length of the sensor cable harness, the value of this capacitor may vary, but it is not advisable to make it greater than 1000pF.
3. It is useful to provide a third pin for an optional GND connection at the CT terminal. Connect this pin to the shield of the CT cable (if available) to minimize high-frequency noise entering through the sensor cable.
4. The two capacitors labeled NC eliminate high-frequency noise spikes on the analog reference signal V3P3. The values of these capacitors may have to be modified based on the desired filtering frequencies.
5. A 100 pF to 220 pF capacitor between IA and V3P3A positioned right at the IA pin of the 71M6521 helps eliminate false readings caused by noise pick-up on long signal traces.

3.2 Voltage Dividers

The most common way to attenuate the mains voltage to the levels acceptable to the 71M6521 IC is to use a resistive voltage divider. The recommended circuit is shown in Figure 11.

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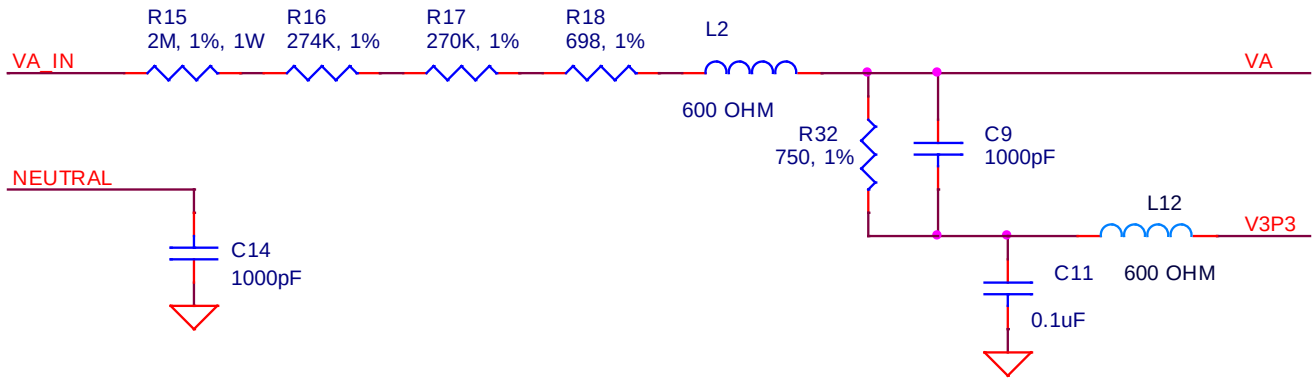

Figure 11: Voltage Input Circuit for CT

The recommendations for the design of the CT input signal conditioning circuit with respect to EMC/EMI testing are:

1. L2 and L12 are Ferrite beads that provide 600-Ohm impedance for common mode signals above 100 MHz (e.g. TDK MMZ2012S601A).
2. R15+R16+R17+R18 and C9 provide a low-pass filter for differential signals.
3. The highest value of the resistor ladder (in this case R15) should be placed directly at the voltage input terminal. This component experiences the highest voltage drop. Consequently, the voltages at R16, R17, etc. will be in a safer range and precautions for leakage or arching need only be taken for R15.
4. C11 filters EMI noise on the Neutral connection.

3.3 Current Shunt Resistor

The current shunt configuration is the most critical in terms of accuracy and EMC performance. Due to the usually very low resistances of the shunts, the achievable signal amplitude is very low at low currents and sometimes close to the noise floor. In addition, the meter is galvanically connected to the mains voltage which invites EMC issues.

Designing a meter that uses shunts but that is still accurate and passes EMC tests requires more than proper component selection: Shunt wiring, circuit topology, component selection and layout techniques are all factors that have to be considered.

It helps to understand some basics about the supply topology used for the 71M6521: This IC has single-ended analog inputs, and measurements are taken with V3P3A as the reference. The 71M6521 has two different V3P3 networks, V3P3SYS (corresponding to the V3P3D net on the first-generation 71M651X ICs) and V3P3A. V3P3SYS powers all digital circuits inside the IC. V3P3A is the net that powers all internal analog circuits and acts as the reference for measurements. As stated in the Teridian datasheets, the V3P3A and V3P3SYS nets should be seen as almost the same for the device, i.e. DC voltage differences between these nets should be very low. This does not mean that V3P3A and V3P3SYS are interchangeable and that these nets should be routed indiscriminately. On the contrary: As we will see, V3P3A and V3P3SYS must be separated for the most part.

Regarding the ground pins, there is no such distinction. GNDD and GNDA should be connected to the same ground plane or large ground copper structure.

A summary of proper techniques when designing a shunt meter is listed below:

1) The V3P3A net is the reference for measurements and also the supply for the analog parts of the 71M6521 IC. This means that V3P3A must be kept as noise-free as possible and well bypassed with capacitors. All digital nets and power supplies to unrelated components should be removed from this net, allowing only the filters for the analog inputs and the V3P3A IC pin to be part of V3P3A. This way, the only current loading V3P3A is the 71M6521 IC itself. A star-point topology should be used for all the connections for this network. The star point must be as close as possible to the 71M6521.

2) V1 is considered an analog signal and its connections should be part of the star-point.
3) Another very important issue is the impedance for the V3P3A net. All vias should be large, and traces should be wide in order to minimize impedance.
4) Decoupling of the V3P3A net to ground should be done as closely as possible to the V3P3A pin with several capacitors, preferably with 10 µF, 100 nF, and 1nF capacitors placed in this order, so that the lower capacitor value is closer to the V3P3A pin.
5) All longer V3P3A traces, for instance the ones connected to channel B, should be decoupled to ground at several locations, in order to reduce noise.
6) Care must be taken to avoid low-voltage TVSs ("Tranzorbs") for the V3P3A net, since these components tend to generate leakage currents that have negative effects on low-current accuracy.
7) The V3P3A net should be connected to V3P3SYS right at the shunt resistor. This is the preferred arrangement (see Figure 12). If this is not possible, the two nets should be joined as soon as they enter the PCB. V3P3A and V3P3SYS should only be connected at one point and otherwise always routed separately (see Figure 13).
8) Analog inputs should have wide traces and large vias in order to minimize impedance.
9) Shunt resistors with three tabs (terminals) should be used (see Figure 12). Commercially available shunt resistors have two tabs on one side and one tab on the opposing side.
10) Using ferrite beads at the sensor inputs brings good results, but care must be taken regarding the impedance of the V3P3A net. Using ferrite beads with high DC resistance decreases low-current accuracy. Even a resistance as low as 0.3 Ω can cause inaccuracy at low currents. Therefore, ferrites with the lowest possible DC resistance should be used. These ferrites are usually of larger size (2220 and larger). A ferrite that works well is the HI2220R181R-10 by Steward/Laird Technologies.
11) A common problem with accuracy is low capacity of the power supply capacitors. Relatively low power supply ripple can result in significant reduction of accuracy and/or repeatability. This makes adding a large electrolytic capacitor at the 3.3 VDC output of the power supply advisable.

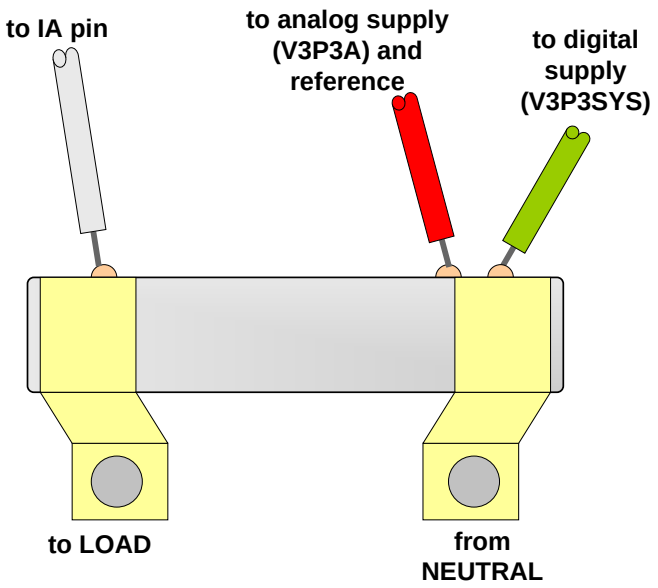

Figure 12: Shunt Connections

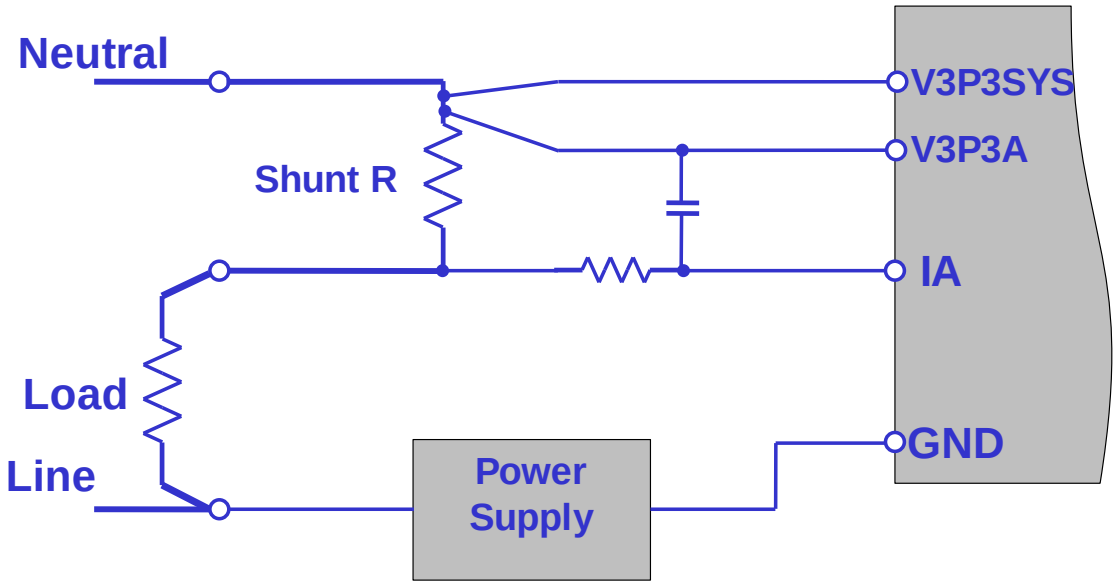

Figure 13: Current Shunt Circuit Topology

Figure 14 shows the recommended input signal conditioning circuit.

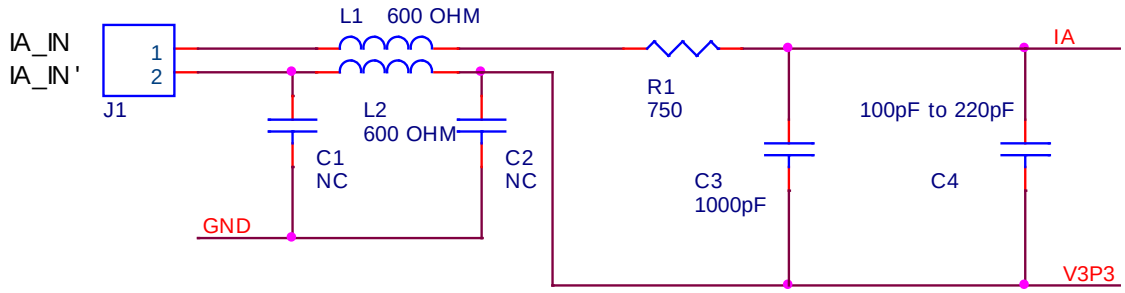

Figure 14: Current Shunt Input Signal Processing Circuit

Key recommendations for passing EMC/EMI testing for the current shunt input signal conditioning circuit:

1. L1 and L2 are ferrite beads with very low DC resistance.
2. R1 and C3 provide a low-pass filter for differential signals with a cutoff frequency of around 212 kHz. Depending on the length of the sensor cable harness, the value of C3 may vary. It is not advisable to make C3 greater than 1000pF.
3. The connector to the shunt resistor should have a third pin for a GND connection. Connect pin 3 of J1 to the shield of the shunt cable (if available) to minimize high-frequency noise entering through the shunt sensor plate and the sensor cables.
4. The combination of C1, L2, and C2 eliminates high-frequency noise spikes (EFT) on the analog reference signal V3P3. The value of C1 and C2 can be modified based on the desired filtering characteristics. The larger the value, the better EFT rejection will be. However, large values for C1 and C2 affect low-current accuracy. Good starting values for C1 and C2 are 330 pF.
5. A 10 kΩ resistor may be used in parallel with C2 to dampen EMI noise.
6. C4 is used to eliminate noise picked up by longer circuit traces causing accuracy issues. C4 should be located very close to the IA pin of the 71M652X IC.

3.4 Sensor Wiring

The following precautions apply to the sensor wiring:

1. Sensor wires may be shielded. Shielded wires are recommended for use with current shunts due to their low-level signals. Use twisted pair wiring for internal wiring harnesses with or without shielding (STP or UTP).
2. When available, connect the cable shields to the board GND.
3. If cable shielding is not used, use unshielded twisted pair wire (UTP). The tighter the twist, the better the rejection of common-mode noise.
4. Keep sensor wires as short as possible.
5. It is possible to use ferrite clamps on sensor wiring to reduce common-mode noise.

3.5 Other Circuit Elements

3.5.1 Power Supply Circuit

Figure 15 shows the recommended circuit for the standard capacitive power supply, as used on most 6521 Demo Boards. In general, transformer-based power supplies will provide better EMC/EMI test results.

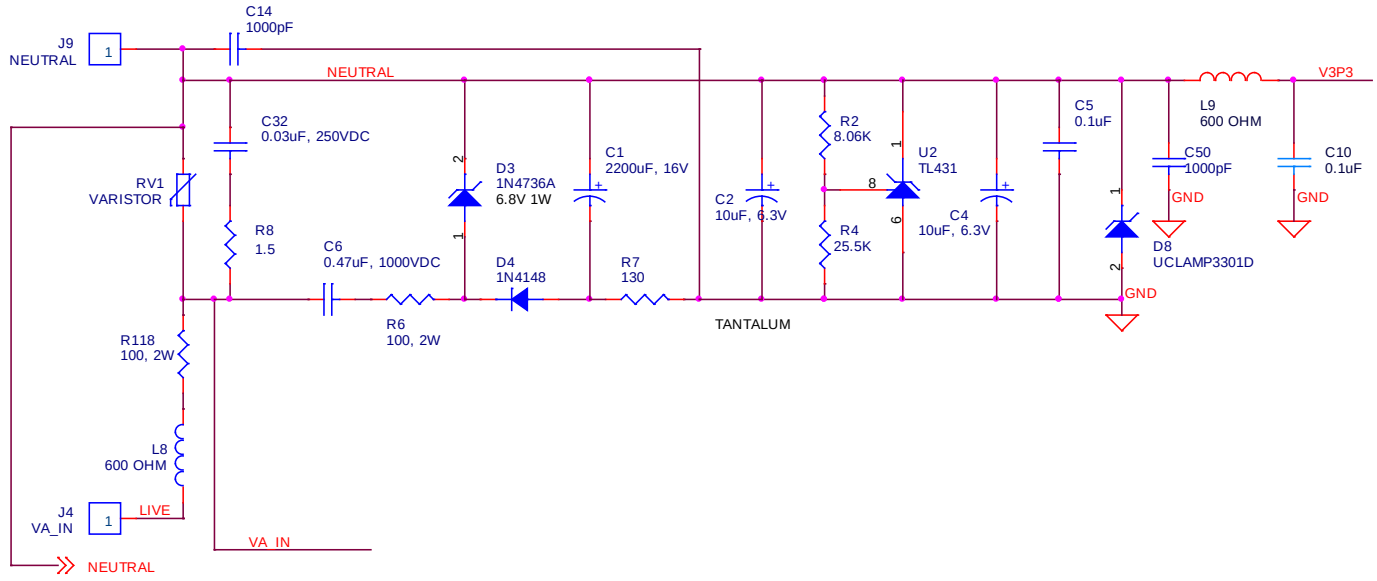

Figure 15: Power Supply Circuit

Key recommendations for the power supply circuit are:

1. The ferrite bead L9 at the V3P3 output minimizes high-frequency EMI noise.
2. A TVS (Transient Voltage Suppressor, or “Tranzorb”, D8) is added to clamp the V3P3 supply voltage to 3.3 V. This device may be a bi-directional clamping device to prevent high voltage peaks from entering the circuit, e.g. the SEMTECH UCLAMP3301D.
3. The resistor R118 is added in series to the varistor (MOV) to limit the surge current. This resistor will cause a voltage drop that helps to protect both the varistor and the meter circuitry. Use a flame-proof type 100 Ω resistor rated 2W to 5W.
4. The high-voltage capacitor C32 is added in parallel to the varistor to suppress high-frequency EMI noise. The series resistor R8 (1.5 Ω) dampens oscillations that may occur due to the effective impedance of the power supply.
5. C50 and C10 suppress high-frequency EMI noise.
6. Improved EFT immunity is achieved by replacing C2 and C4 with ceramic type capacitors of values between 10 µF to 47 µF (even though the Demo Board utilizes Tantalum).

4 LAYOUT PRECAUTIONS

4.1 Copper Layers

Four-layer printed circuit boards provide optimum performance with fastest time to market. The two internal layers are partitioned for ground and V3P3/V3P3SYS.

A two-layer board structure demands careful attention to the ground and V3P3A/3P3SYS signal integrity. Excessive copper voids and copper discontinuities will cause signal interference resulting in poor measurement accuracy and poor EFT/EMC performance. For two-layer boards:

- Allocate the bottom layer for ground to maximize the ground surface under the device.
- Use the top layer for signal routing and for additional GND structures, as shown in Figure 18.
- "Stitch" gaps in the GND structures to GND bridges on the other PCB side, as shown in Figure 16.

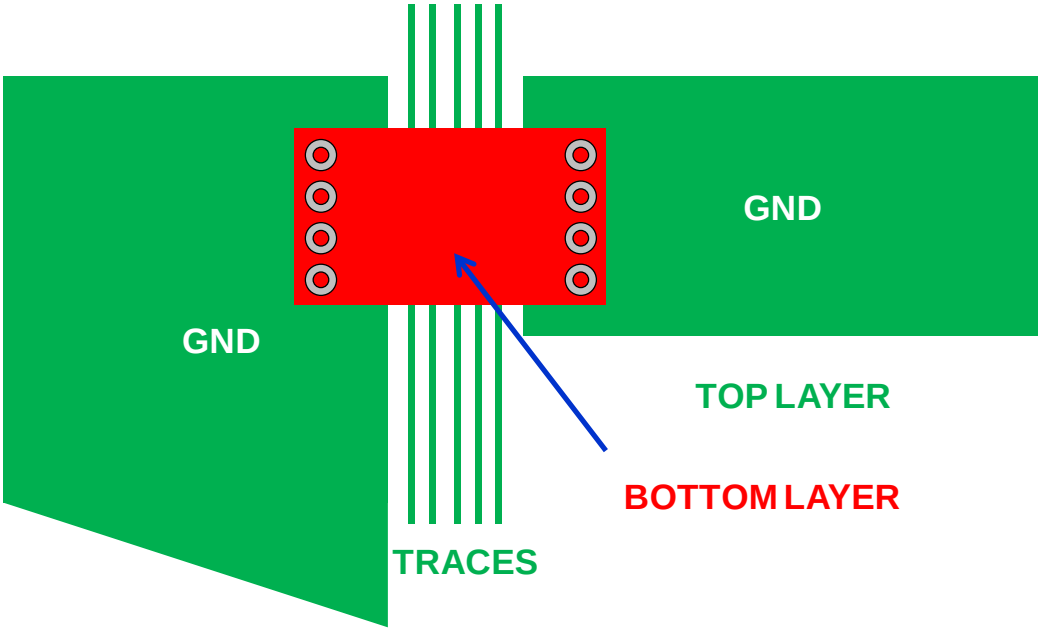

Figure 16: "Stitching" of Copper Structures

4.2 Component Placement

Good layout starts with proper component placement. It is useful to physically separate the high-voltage and low-voltage sections of the board and to bundle the functional groups into well-defined clusters of components. Where necessary, use PCB cutouts to eliminate stray currents and arching.

All critical signal paths should be as short as possible, which dictates component placement. This applies especially to the traces connecting the crystal (pins XIN, XOUT), the analog current inputs, and other sensitive signals such as V1, RESET, ICE_E, TEST, and X4MHZ.

Place sensitive components, such as crystal, current input signal conditioning circuits, etc. away from magnetic components or high-frequency signals, such as switching power supplies.

When placing bypass capacitors for V3P3SYS and V3P3A, the smaller capacitor values should be placed closer to the 71M6521 than the larger ones.

An example for component placement is shown in Figure 17

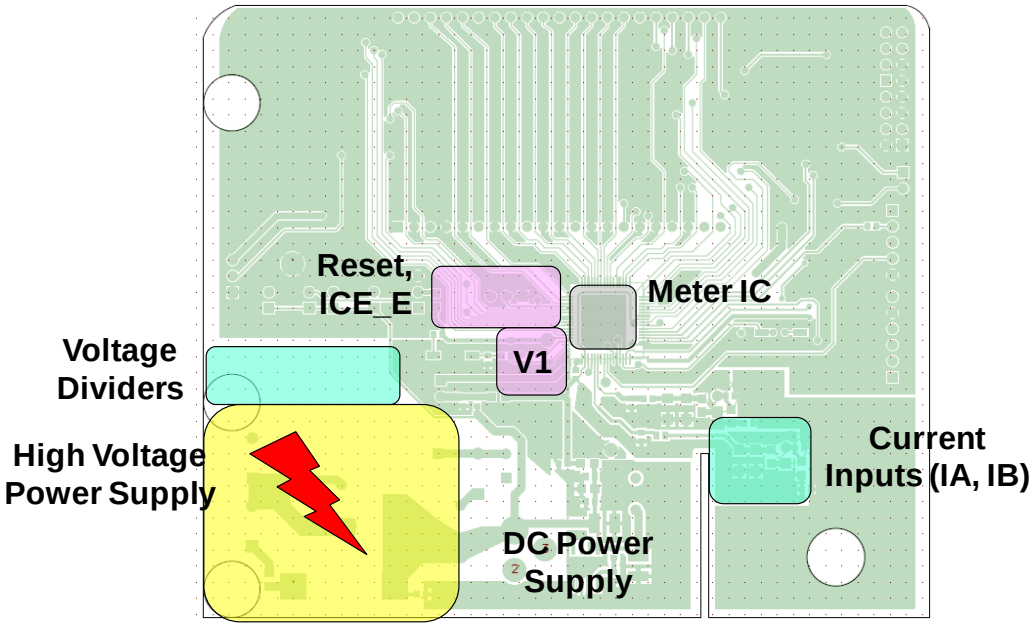

Figure 17: Component Placement

4.3 General Recommendations

1. Widen ground and V3P3 traces (using copper pour techniques) to create virtual planes. Use multiple free vias to "stitch" together top layer ground copper fills to the bottom layer ground plane structure.
2. Create a wide V3P3A plane structure to provide a stable reference for the measurement signals. Meter measurement performance is improved with wider V3P3A copper structures (see Figure 21).
3. Utilize a star point connection structure ("Kelvin" junction) on the top layer placed close to the V3P3A pin of the IC to bring together all analog circuits connected to V3P3A, including V1 (see Figure 20).
4. Utilize a ground star point on the bottom side of the board for connecting the grounds from power supply, voltage and current input circuits. Place one 10 µF capacitor across the ground and V3P3 star points.
5. The crystal and its load capacitors should be positioned adjacent to the 71M652X IC. Placing the crystal and its load capacitors on the bottom side of the board results in the shortest trace lengths. The crystal should have its own ground structure, as shown in Figure 19.
6. The trace for E_TCLK should be routed separate from the sensitive crystal traces.
7. Whether directly connected or terminated through a resistor, the ground connections for the digital input signals RESET, PB, X4MHZ, ICE_E and TEST tie directly to the bottom layer ground structure.
8. The V1 pin of the 71M6521 is sensitive to RF noise. Long signal traces connecting the various components to the V1 pin must be avoided. Locate components R1, R2, R3, and C1 (see Figure 3) adjacent to the V1 pin. C1 is recommended as a provisional noise filter. Usage of additional components is dependent on the printed circuit board routing of the V3P3A signal.
9. Since the V3P3D net supplies all DIO pins internally and is used as a net for pull-up resistors for a variety of board signals, it should be implemented as a solid copper structure (see Figure 22).
10. Unrelated to EMI, the 68-pin version of the 71M6521 incorporates an exposed ground pad on the bottom side of the device. Do not route traces or place vias under the device.

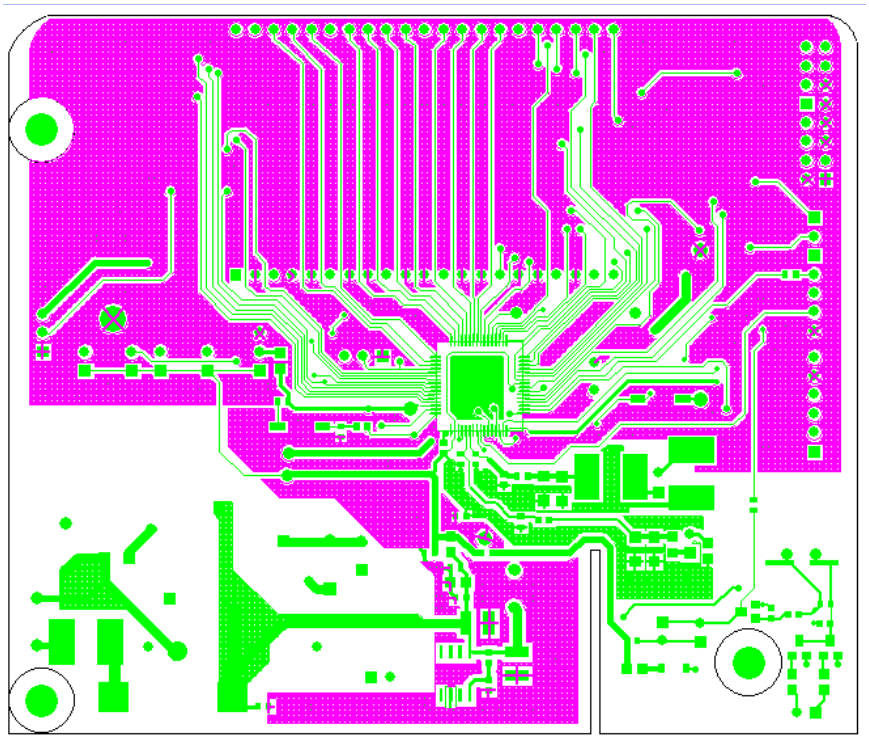

Figure 18: GND Copper on Top (Purple)

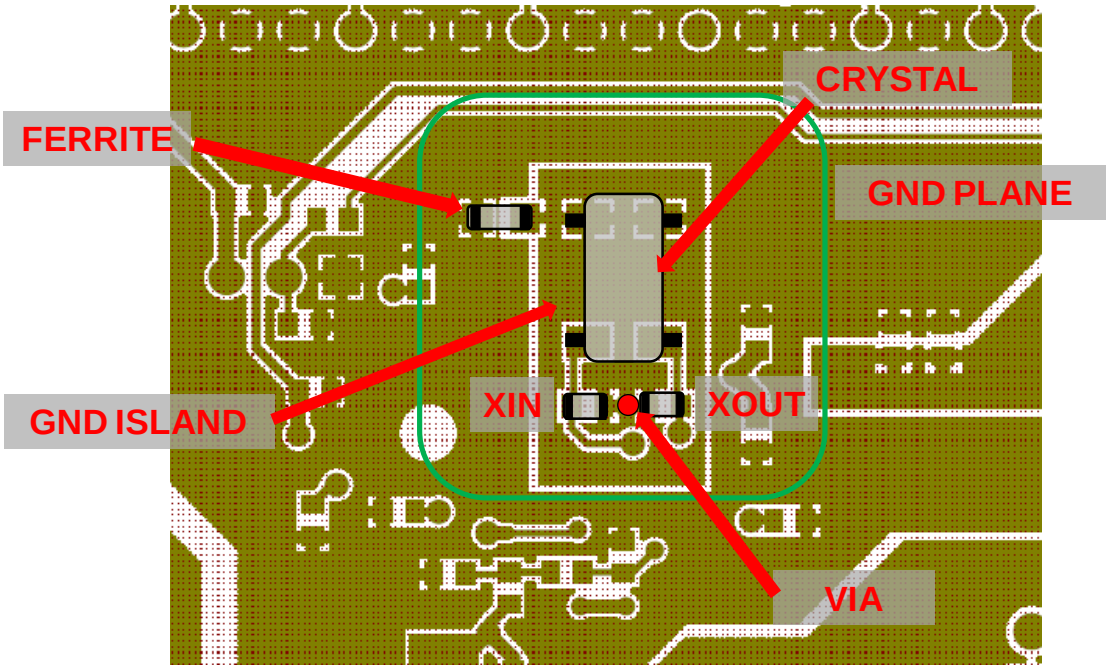

Figure 19: Separate GND Structure for the Crystal

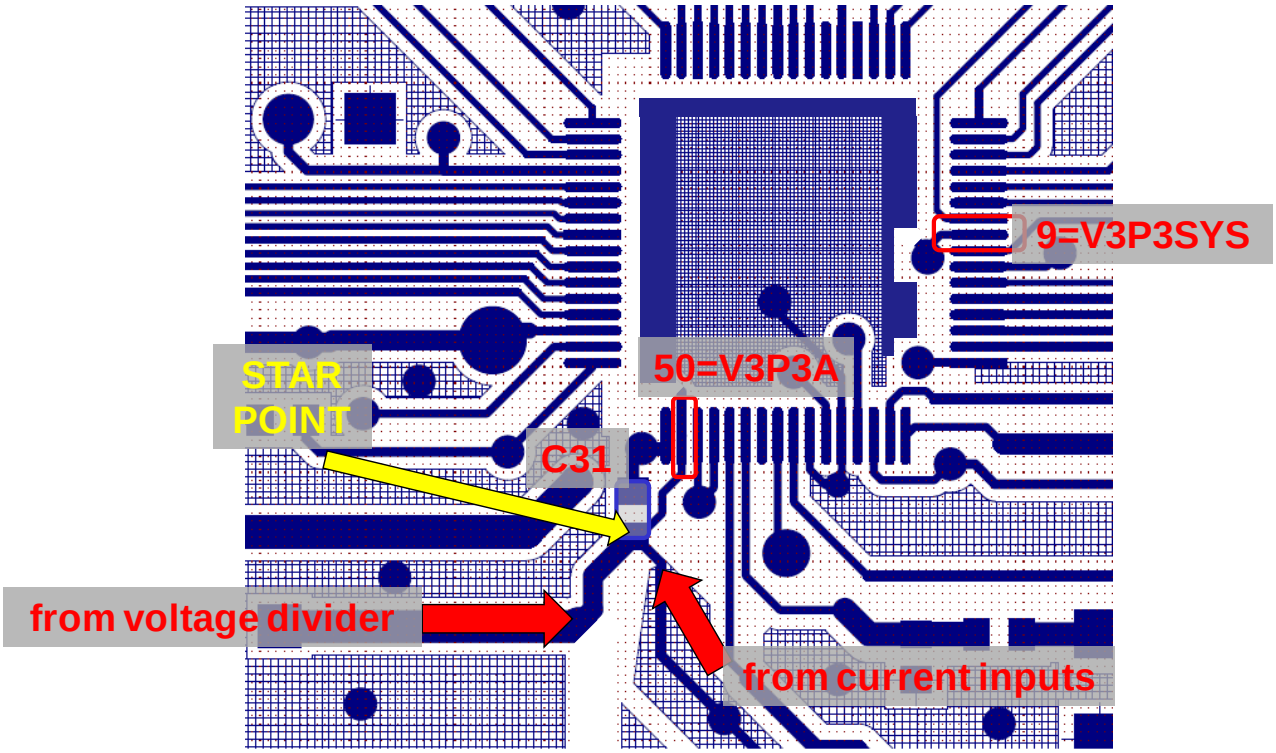

Figure 20: V3P3A Star Point

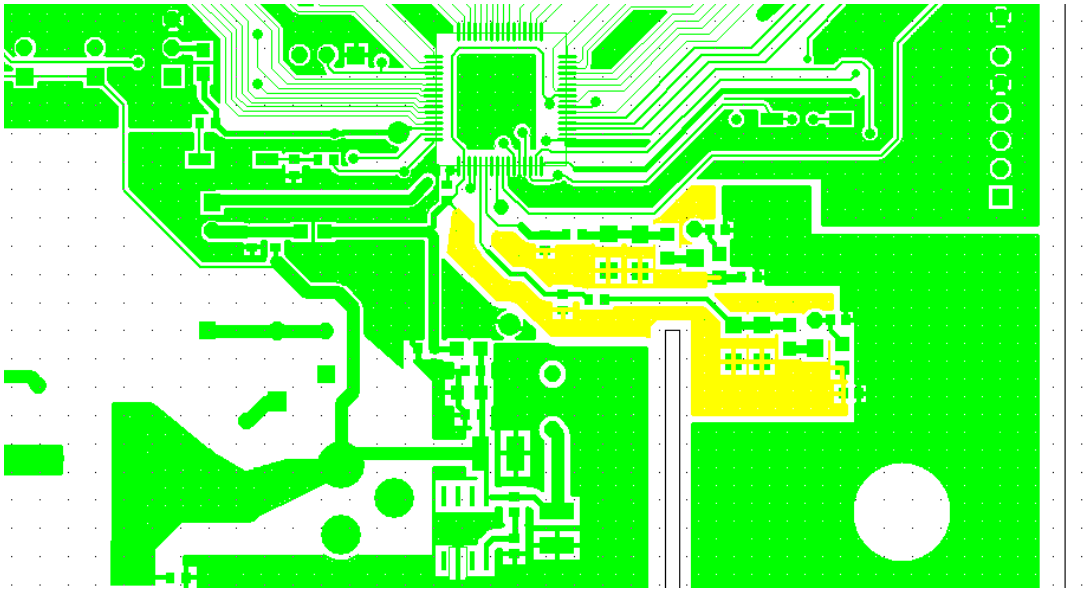

Figure 21: V3P3A Structures for IA and IB

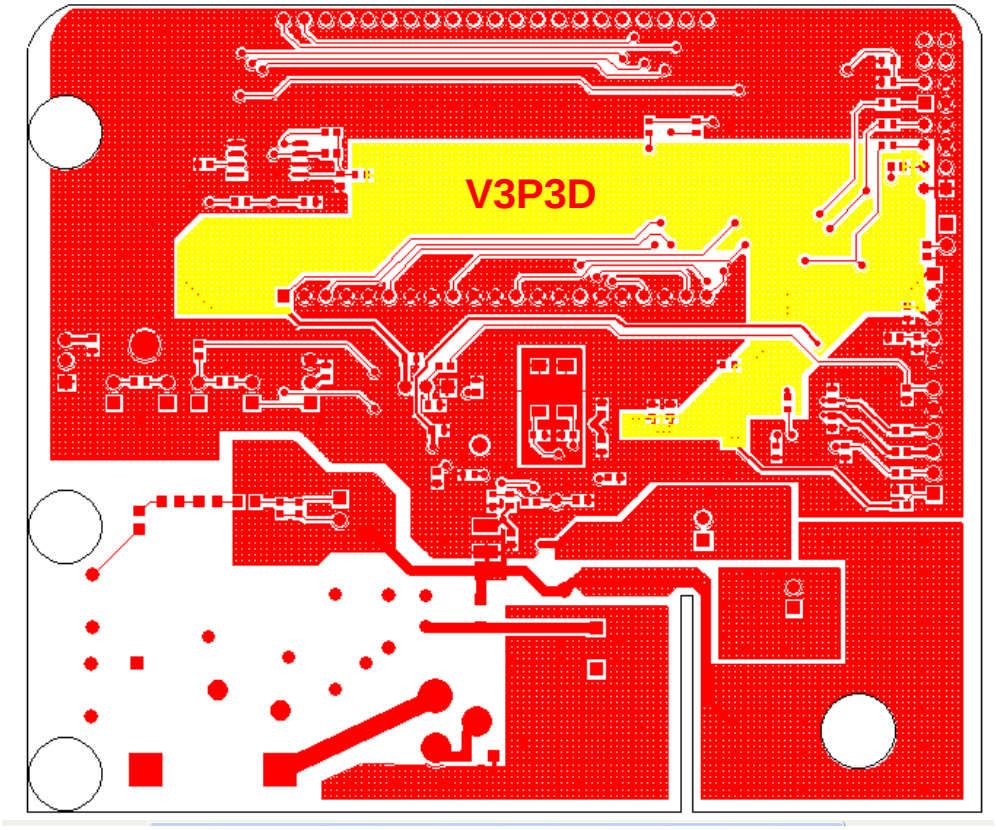

Figure 22: Copper Structure for V3P3D

5 FIRMWARE RECOMMENDATIONS

1. Configure all unused DIO pins as outputs. This prevents unwanted signals from entering the IC.
2. Disable the emulator clock by disabling the emulator port (ICE_E pin pulled low). No firmware instructions are required for this.
3. Disable the CKTEST clock output (by configuring *CKOUT_DIS* to 1) if not in use.
4. Place dummy interrupt service routines containing a RETI instruction at all locations pointed to by unused interrupt vectors.
5. All interrupt service routines (ISRs) are to be as short as possible and must minimize any memory manipulation operations.

6 EXTERNAL COMPONENTS

After all recommendations of this Application Note have been incorporated into the meter design, there should not be any issue passing EMC tests. If the meter still fails to produce the desired results, the addition of external ferrite components to the sensor and power wires may be required.

The current shunt configuration is the most difficult application due to the direct connection of the NEUTRAL wire to the V3P3 nets of the board. External clamp-on ferrites or external toroid ferrites on the following wires provide additional noise suppression:

1. NEUTRAL power entry wire
2. Second NEUTRAL power entry wire
3. Current shunt sensor wires

7 REVISION HISTORY

Revision	Date	Description
Rev. 1.0	3/13/2007	First publication.
Rev. 1.1	3/13/2007	Added figures showing emulator interface signals.
Rev. 1.2	3/14/2007	Deleted references to Rogowski coils. Added alternative connection for reset button and button connected to PB. Added information on components at XIN and XOUT pins.
Rev. 2.0	10/01/2008	Completely revised to reflect latest Demo Board design techniques. Integrated many graphs from EMC web presentation.
Rev. 2.1	10/01/2008	Updated reference designator in description to Figures 8 and 12.
Rev. 2.2	12/10/2008	Added note on pure SEG pins in designs where no LCD is used. Added explanation of hysteresis at V1.

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