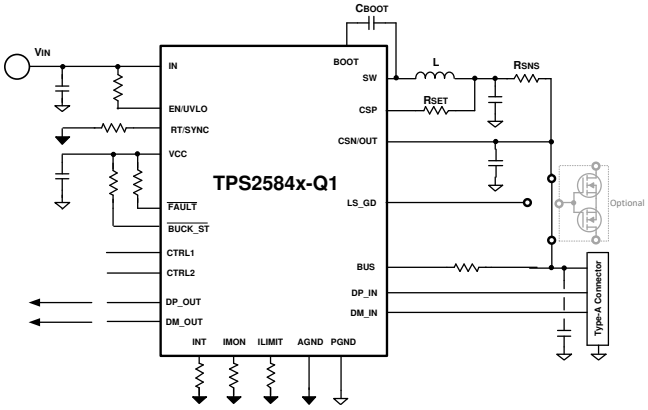
TPS2584x-Q1 USB Type-A BC1.2 5-V 3.5-A Output, 36-V Input Synchronous Buck With Cable Compensation

1 Features

- AEC-Q100 Qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - HBM ESD Classification level H2
  - CDM ESD Classification level C5
- Synchronous Buck DC/DC regulator
  - Input voltage range: 4.5 V to 36 V
  - Output current: 3.5 A
  - 5.1-V Output voltage with ±1% accuracy
  - Current mode control
  - Adjustable frequency: 300 kHz to 2.2 MHz
  - Frequency synchronization to external clock
  - FPWM with Spread-spectrum dithering
  - Internal compensation for ease of use
- Compliant to USB-IF standards
  - CDP/SDP Mode per USB BC1.2
- Optimized for USB power and communication
  - User-Programmable USB current limit
  - Cable Droop compensation up to 1.5 V
  - High bandwidth data switches on DP and DM
  - Client mode for system update
- Integrated protection
  - V_{BUS} Short-to-V_{BAT} protection
  - DP_IN and DM_IN Short-to-V_{BAT} (TPS25840-Q1 Only)
  - DP_IN and DM_IN Short-to-V_{BUS}
  - DP_IN, DM_IN IEC 61000-4-2 Rated
    - ±8kV Contact and ±15kV air discharge
- Fault flag reports
- 32 Pin QFN package with Wettable Flank

Simplified Schematic TPS2584x-Q1



2 Applications

- Automotive Infotainment
- USB Media Hubs
- USB Charger Ports

3 Description

The TPS2584x-Q1 is a USB Type-A BC1.2 charging solution that includes a synchronous DC/DC converter. With cable droop compensation, the Vbus voltage remains constant regardless of load current, ensuring connected portable devices are charged at optimal current and voltage even under heavy loads.

The TPS2584x-Q1 includes high bandwidth analog switches for DP and DM pass-through.

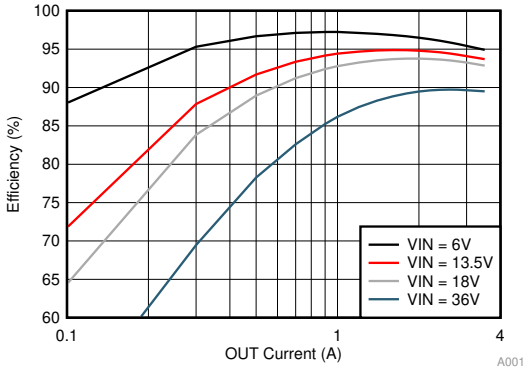
The TPS25840-Q1 also integrates short to battery protection on V_{BUS}, DM_IN and DP_IN pins. These pins can withstand voltage up to 18 V. While TPS25842-Q1 don't support data line (Dx) short to VBAT protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25840-Q1	VQFN (32)	5.00 mm x 5.00 mm
TPS25842-Q1	VQFN (32)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet

Buck Efficiency vs Output Current fsw = 400kHz



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2019) to Revision A	Page
• Changed Layout description for clarity	47

5 Description (Continued)

The synchronous buck regulator operates with current mode control and is internally compensated to simplify design. A resistor on the RT pin sets the switching frequency between 300 kHz and 2.2 MHz. Operating below 400 kHz results in better system efficiency. Operation above 2.1 MHz avoids the AM radio bands and allows for use of a smaller inductor.

The TPS2584x-Q1 integrates electrical signatures necessary for legacy devices which utilize USB data lines to determine charging configuration.

A precision current sense amplifier is included for user programmable cable droop compensation and current limit tuning. Cable compensation aids portable devices in charging at optimum current and voltage under heavy loads by changing the buck regulator output voltage linearly with load current to counteract the voltage drop due to wire resistance in automotive cabling. The VBUS voltage measured at a connected portable device remains approximately constant, regardless of load current, allowing the portable device's battery charger to work optimally.

The USB specifications require current limiting of USB charging ports, but give system designers reasonable flexibility to choose overcurrent protection levels based on system requirements. The TPS2584x-Q1 uses a novel two-threshold current limit circuit allowing system designers to either program average current limit protection of the buck regulator, or optionally, current limit using an external NMOS between the CSN/OUT and BUS pins. The NFET implementation enables the TPS2584x-Q1 buck regulator to supply a 5-V output for other loads during an overcurrent condition on the USB port.

Protection features include cycle-by-cycle current limit, hiccup short-circuit protection, undervoltage lockout, VBUS overvoltage and overcurrent, data line (Dx) short to VBUS, and die overtemperature protection.

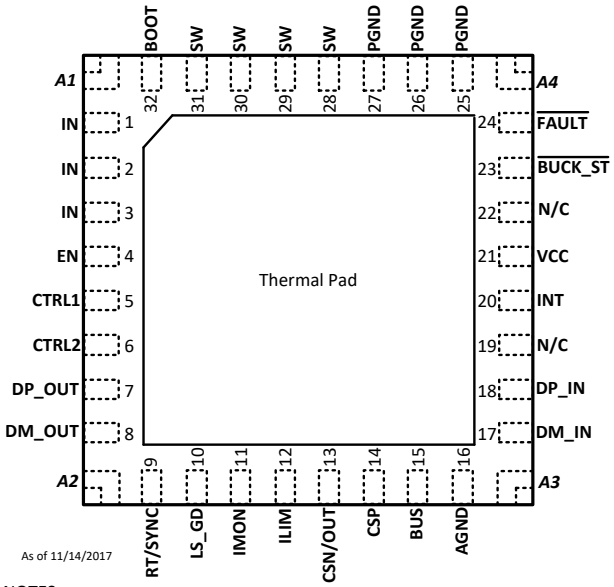
The TPS25840-Q1 includes high bandwidth analog switches for DP and DM pass-through, and support data line (Dx) short to VBAT protection. TPS25842-Q1 don't support data line (Dx) short to VBAT protection.

6 Device Comparison Table

PART NUMBER	PACKAGE	DCP AUTO	DP AND DM SWITCHES	NTC INPUT	DP/DM Short to BAT
TPS25840-Q1	VQFN (32)	No	Yes	No	Yes
TPS25842-Q1	VQFN (32)	No	Yes	No	No

7 Pin Configuration and Functions

TPS25840/2-Q1 RHB Package
32-Pin (VQFN)
Top View



NOTES:
1) A1, A2, A3, and A4 are corner anchors for enhanced package stress performance.
2) A1, A2, A3, and A4 are electrically connected to the thermal pad.
3) A1, A2, A3, and A4 PCB lands should be electrically isolated or electrically connected to thermal pad and PGND.

Pin Functions

PIN		TYPE(1)	I/O	DESCRIPTION
NAME	NO.			
AGND	16	G	-	Analog ground terminal. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB.
BOOT	32	P		Boot-strap capacitor connection for HS FET driver. Connect a high quality 100-nF capacitor from this pin to the SW pin.
BUS	15	A	I	VBUS discharge input. Connect to VBUS on USB Connector.
CSN/OUT	13	P	I	Negative input of current sense amplifier, also buck output for internal voltage regulation
CSP	14	P	I	Positive input of current sense amplifier.
CTRL1	5	A	I	Logic-level control inputs for device/system configuration. (See Table 6)
CTRL2	6	A	I	Logic-level control inputs for device/system configuration. (See Table 6)
DM_IN	17	A		DM data line. Connect to USB connector.
DM_OUT	8	A		DM data line. Connect to USB host controller.
DP_IN	18	A		DP data line. Connect to USB connector.
DP_OUT	7	A		DP data line. Connect to USB host controller.

(1) A = Analog, P = Power, G = Ground.

Pin Functions (continued)

PIN		TYPE(1)	I/O	DESCRIPTION
NAME	NO.			
EN/UVLO	4	A		Enable pin. Do not float. High = on, Low = off. Can be tied to VIN. Precision enable input allows adjustable UVLO by external resistor divider.
$\overline{\text{FAULT}}$	24	A	O	Active LOW open-drain output. Asserted during fault conditions. (See Table 4)
ILIMIT	12	A		External resistor used to set the current-limit threshold. (See Table 2)
IMON	11	A		External resistor used to set the max cable comp voltage at full load current.
IN	1, 2, 3	P	I	Input Supply to regulator. Connect a high-quality bypass capacitor(s) directly to this pin and PGND.
$\overline{\text{BUCK\_ST}}$	23	A	O	Active Low open-drain output. After $\overline{\text{BUCK\_ST}}$ assert, Buck converter begin to start up. At the same time, DP and DM data switch will turn on accordingly.
LS_GD	10	A		External NMOS gate driver. If TPS2584x-Q1 configured under average current limit mode, LS_GD pin must be pulled up through 2.2kΩ resistor. (See *Current Limit Setting using R_{ILIMIT}*)
PGND	25, 26, 27	G		Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces.
N/C	19, 22	-		Make no electrical connection.
RT/SYNC	9	A		Resistor Timing or External Clock input. An internal amplifier holds this terminal at a fixed voltage when using an external resistor to ground to set the switching frequency. If the terminal is pulled above the PLL upper threshold, a mode change occurs and the terminal becomes a synchronization input. The internal amplifier is disabled and the terminal is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
SW	28, 29, 30, 31	P		Switching output of the regulator. Internally connected to source of the HS FET and drain of the LS FET. Connect to power inductor.
INT	20	A		For internal circuit, must connect a 5.1K resistor to AGND.
VCC	21	P		Output of internal bias supply. Used as supply to internal control circuits. Connect a high quality 2.2 µF capacitor from this pin to GND.

8 Specifications

8.1 Absolute Maximum Ratings

Voltages are with respect to GND (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Input voltage	IN to PGND	–0.3	40	V
	OUT to PGND	–0.3	20	
	EN to AGND	–0.3	VIN + 0.3	
	CSP to AGND	–0.3	20	
	CSN to AGND	–0.3	20	
	BUS to AGND	–0.3	18	
	RT/SYNC to AGND	–0.3	6	
	CTRL1 or CTRL2 to AGND	–0.3	6	
	AGND to PGND	–0.3	0.3	
Output voltage	SW to PGND	–0.3	VIN + 0.3	V
	SW to PGND (less than 10 ns transients)	–3.5	40	
	BOOT to SW	–0.3	6	
	VCC to AGND	–0.3	6	
	LS_GD	–0.3	18	
Voltage range	**TPS25840-Q1**: DP_IN, DM_IN to AGND	–0.3	18	V
	TPS25842-Q1: DP_IN, DM_IN to AGND	–0.3	7	
	DP_OUT, DM_OUT to AGND	–0.3	6	
	$\overline{\text{FAULT}}$, $\overline{\text{BUCK\_ST}}$, INT to AGND	–0.3	6	
	ILIMIT or IMON to AGND	–0.3	6	
Pin positive source current, I_{VCC}	VCC Source Current		5	mA
Pin positive sink current, I_{SNK}	$\overline{\text{FAULT}}$, $\overline{\text{BUCK\_ST}}$		Internally Limited	A
I/O current	DP_IN to DP_OUT, or DM_IN to DM_OUT in SDP, CDP, or Client Mode	–100	100	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000(2)	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, 17, 25 and 32)	±750(3)	
			Other pins	±750(3)	
		IEC 61000-4-2 contact discharge	DP_IN, DM_IN pins	±8000(4)	
		IEC 61000-4-2 air-gap discharge	DP_IN, DM_IN pins	±15000(4)	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5
(4) Surges per IEC61000-4-2, 1999 applied between DP_IN, DM_IN and output ground of the TPS2584x-Q1 evaluation module.

8.3 Recommended Operating Conditions

Voltages are with respect to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage	IN to PGND	4.5		36	V
		EN	0		VIN	
		VCC when driven from external regulator	0		5.5	
		DP_IN, DM_IN	0		3.6	
		DP_OUT, DM_OUT	0		3.6	
		CTRL1, CTRL2	0		VCC	
		RT/SYNC when driven by external clock	0		VCC	
V_{PU}	Pull up voltage	$\overline{FAULT}$, $\overline{BUCK\_ST}$	0		VCC	
V_O	Output voltage	CSN/OUT	0		6.5	
I_O	Output current	Buck regulator output current	0		3.5	A
		DP_IN to DP_OUT or DM_IN to DM_OUT Continuous current in SDP, CDP or Client Mode	–30		30	mA
I_{SNK}	Sink current	$\overline{FAULT}$, $\overline{BUCK\_ST}$			10	
I_I	Input current	Continuous current into the CSP pin			200	µA
R_{EXT}	External resistnace	R_{IMON}, R_{ILIMIT}	0		100	kΩ
T_J		Operating junction temperature	–40		125(1)	°C

(1) Operating at junction temperatures greater than 125°C is possible, however lifetime will be degraded.

8.4 Thermal Information

THERMAL METRIC(1)		TPS2584x-Q1 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTATE (IN PIN)						
V_{IN}	Operating input voltage range		4.5		36	V
I_Q	Operating quiescent current (non switching)	$V_{EN/UVLO}$ = V_{IN}, CTRL1 = CTRL2 = V_{CC}, V_{CSN} = 8V, INT pull down resistance = 5.1kΩ		700	990	µA
I_{SD}	Shutdown quiescent current; measured at IN pin.	EN= 0		10	16	µA
ENABLE and UVLO (EN/UVLO PIN)						
$V_{EN/UVLO\_VCC\_H}$	EN/UVLO input level required to turn on internal LDO	$V_{EN/UVLO}$ rising threshold			1.14	V
$V_{EN/UVLO\_VCC\_L}$	EN/UVLO input level required to turn off internal LDO	$V_{EN/UVLO}$ falling threshold	0.3			V
$V_{EN/UVLO\_H}$	EN/UVLO input level required to turn on state machine	$V_{EN/UVLO}$ rising threshold	1.140	1.200	1.260	V
$V_{EN/UVLO\_HYS}$	Hysteresis	$V_{EN/UVLO}$ falling threshold		90		mV
$I_{LKG\_EN/UVLO}$	Enable input leakage current	$V_{EN/UVLO}$ = 3.3 V		0.5		uA
INTERNAL LDO						
V_{BOOT_UVLO}	Bootstrap voltage UVLO threshold			2.2		V
V_{CC}	Internal LDO output voltage appearing on VCC pin	6 V ≤ V_{IN} ≤ 36 V	4.75	5	5.25	V
$V_{CC\_UVLO\_R}$	Rising UVLO threshold		3.4	3.6	3.8	V
$V_{CC\_UVLO\_HYS}$	Hysteresis			600		mV
CURRENT LIMIT VOLTAGE (CSP - CSN/OUT PINS) TO ACTIVATE BUCK AVG CURRENT LIMITING						
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage buck regulator control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	43.5	46	48.5	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage buck regulator control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	42.5	46	49.5	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage buck regulator control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 26.1 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	20	22.5	25	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage buck regulator control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 26.1 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	19	22.5	26	mV
CURRENT LIMIT VOLTAGE (CSP - CSN/OUT PINS) TO ACTIVATE EXTERNAL NFET CURRENT LIMITING						

Electrical Characteristics (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 6.8 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	40	43	46	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 6.8 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	38.5	43	47.5	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13.7 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	18	21	24	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13.7 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	17	21	25	mV
CURRENT LIMIT - BUCK REGULATOR PEAK CURRENT LIMIT						
$I_{L-SC-HS}$	High-side current limit		4.6	5.4	6.2	A
$I_{L-SC-LS}$	Low-side current limit		3.5	4	4.5	A
$I_{L-NEG-LS}$	Low-side negative current limit		–3.1	–2.1	–1.3	A
CABLE COMPENSATION VOLTAGE						
V_{IMON}	Cable compensation voltage	(V_{CSP} – V_{CSN}) = 46 mV, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ	0.935	1	1.065	V
V_{IMON}	Cable compensation voltage	(V_{CSP} – V_{CSN}) = 23 mV, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ	0.435	0.5	0.565	V
V_{IMON}	Cable compensation voltage (internal clamp)	(V_{CSP} –V_{CSN}) = 46 mV, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = open		1.8		V
BUCK OUTPUT VOLTAGE (CSN/OUT PIN)						
$V_{CSN/OUT}$	Output voltage	INT pulldown resistance = 5.1kΩ, R_{IMON} = 0 Ω, R_{ILIMIT} = 0 Ω	5.05	5.10	5.15	V
$V_{CSN/OUT}$	Output voltage accuracy	INT pulldown resistance = 5.1kΩ, R_{IMON} = 0 Ω, R_{ILIMIT} = 0 Ω	–1		1	%
V_{CSN/OUT_OV}	Overvoltage level on CSN/OUT pin which buck regulator stops switching	$V_{CSN/OUT}$ rising	7.1	7.5	7.9	V
V_{CSN/OUT_OV_HYS}	Hysteresis			500		mV
V_{HC}	CSN / OUT pin voltage required to trigger short circuit hiccup mode			2		V
V_{DROP}	Dropout voltage (V_{IN}-V_{OUT})	V_{IN} = V_{OUT} + V_{DROP}, V_{OUT} = 5.1V, I_{OUT} = 3A		150		mV
BUCK REGULATOR INTERNAL RESISTANCE						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	Load = 3 A, T_J = 25°C		40	45	mΩ
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	Load = 3 A, -40°C ≤ T_J ≤ 125°C		40	68	mΩ
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	Load = 3 A, -40°C ≤ T_J ≤ 150°C		40	75	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	Load = 3 A, T_J = 25C		35	41	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	Load = 3 A, -40°C ≤ T_J ≤ 125°C		35	60	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	Load = 3 A, -40°C ≤ T_J ≤ 150°C		35	68	mΩ
NFET GATE DRIVE (LS_GD PIN)						
V_{LS_GD}	NFET gate drive output voltage	$V_{CSN/OUT}$ = 5.1 V, C_G = 1000 pF (see Figure 27)	9.5	11	12.5	V
$I_{LS\_DR\_SRC}$	NFET gate drive output source current	$V_{CSN/OUT}$ = 5.1 V, C_G = 1000 pF	2	3	4	µA
$I_{LS\_DR\_SNK}$	NFET gate drive output sink current	$V_{CSN/OUT}$ = 5.1 V, C_G = 1000 pF	20	35	50	µA
$V_{LS\_GD\_UVLO\_R}$	$V_{CSN/OUT}$ rising threshold for LS_GD operation	$V_{CSN/OUT}$ rising	2.85	3	3.15	V

Electrical Characteristics (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LS\_GD\_UVLO\_HYS}$	Hysteresis			80		mV
BUS DISCHARGE (BUS PIN)						
V_{BUS_OV}	Rising threshold for BUS pin overvoltage protection	V_{BUS} rising	6.6	7	7.3	V
$V_{BUS\_OV\_HYS}$	Hysteresis			180		mV
$R_{BUS\_DCHG\_18V}$	Discharge resistance for BUS	V_{BUS} = 18V, measure leakage current		29		kΩ
$R_{BUS\_DCHG\_8V}$	Discharge resistance for BUS	V_{BUS} = 8V, measure leakage current		35		kΩ
$\overline{\text{FAULT}}$, $\overline{\text{BUCK\_ST}}$						
V_{OL}	FAULT Output low voltage	I_{SNK_PIN} = 0.5 mA			250	mV
I_{OFF}	FAULT Off-state leakage	V_{PIN} = 5.5 V			1	µA
V_{OL}	$\overline{\text{BUCK\_ST}}$ Output low voltage	I_{SNK_PIN} = 0.5 mA			250	mV
I_{OFF}	$\overline{\text{BUCK\_ST}}$ Off-state leakage	V_{PIN} = 5.5 V			1	µA
CTRL1, CTRL2 - LOGIC INPUTS						
V_{IH}	Rising threshold voltage			1.48	2	V
V_{IL}	Falling threshold voltage		0.85	1.30		V
V_{HYS}	Hysteresis			180		mV
I_{IN}	Input current		–1		1	µA
DP_IN AND DM_IN OVERVOLTAGE PROTECTION						
$V_{Dx\_IN\_OV}$	Rising threshold for Dx_IN overvoltage protection	DP_IN or DM_IN rising	3.7	3.9	4.15	V
	Hysteresis			100		mV
$R_{Dx\_IN\_DCHG\_18V}$	Discharge resistance for Dx_IN	VDx_IN = 18V, measure leakage current		94		kΩ
$R_{Dx\_IN\_DCHG\_5V}$	Discharge resistance for Dx_IN	VDx_IN = 5V, measure leakage current		416		kΩ
HIGH-BANDWIDTH ANALOG SWITCH						
R_{DS_ON}	DP and DM switch on-resistance	V_{DP_OUT} = V_{DM_OUT} = 0 V, I_{DP_IN} = I_{DM_IN} = 30 mA		3.4	6.3	Ω
R_{DS_ON}	DP and DM switch on-resistance	V_{DP_OUT} = V_{DM_OUT} = 2.4 V, I_{DP_IN} = I_{DM_IN} = –15 mA		4.3	7.7	Ω
$\lvert\Delta R_{DS\_ON}\rvert$	Switch resistance mismatch between DP and DM channels	V_{DP_OUT} = V_{DM_OUT} = 0 V, I_{DP_IN} = I_{DM_IN} = 30 mA		0.05	0.15	Ω
$\lvert\Delta R_{DS\_ON}\rvert$	Switch resistance mismatch between DP and DM channels	V_{DP_OUT} = V_{DM_OUT} = 2.4 V, I_{DP_IN} = I_{DM_IN} = –15 mA		0.05	0.15	Ω
C_{IO_OFF}	DP/DM switch off-state capacitance	V_{EN} = 0 V, V_{DP_IN} = V_{DM_IN} = 0.3 V, Vac = 0.03 V_{PP} , f = 1 MHz		6.7		pF
C_{IO_ON}	DP/DM switch on-state capacitance	V_{DP_IN} = V_{DM_IN} = 0.3 V, Vac = 0.03 V_{PP}, f = 1 MHz		10		pF
O_{IRR}	Off-state isolation	V_{EN} = 0 V, f = 250 MHz		9		dB
X_{TALK}	On-state cross-channel isolation	f = 250 MHz		29		dB
$I_{lkg(OFF)}$	Off-state leakage current, DP_OUT and DM_OUT	V_{EN} = 0 V, V_{DP_IN} = V_{DM_IN} = 3.6 V, V_{DP_OUT} = V_{DM_OUT} = 0 V, measure I_{DP_OUT} and I_{DM_OUT}		0.1	1.5	µA
BW	Bandwidth (–3 dB)	R_L = 50 Ω		800		MHz
CHARGING DOWNSTREAM PORT (CDP) DETECT						
V_{DM_SRC}	DM_IN CDP output voltage	V_{DP_IN} = 0.6 V, –250 µA < I_{DM_IN} < 0 µA	0.5	0.6	0.7	V

Electrical Characteristics (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DAT_REF}	DP_IN rising lower window threshold for V_{DM_SRC} activation		0.36	0.38	0.4	V
V_{DAT_REF}	Hysteresis			50		mV
V_{LGC_SRC}	DP_IN rising upper window threshold for VDM_SRC deactivation		0.8	0.84	0.88	V
$V_{LGC\_SRC\_HYS}$	Hysteresis			100		mV
I_{DP_SINK}	DP_IN sink current	V_{DP_IN} = 0.6 V	40	70	100	µA
RT/SYNC THRESHOLD (RT/SYNC PIN)						
$V_{IH\_RT/SYNC}$	RT/SYNC high threshold for external clock synchronization	Amplitude of SYNC clock AC signal (measured at SYNC pin)	3.5			V
$V_{IL\_RT/SYNC}$	RT/SYNC low threshold for external clock synchronization	Amplitude of SYNC clock AC signal (measured at SYNC pin)			0.8	V
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown	Shutdown threshold		160		°C
		Recovery threshold		140		°C

8.6 Timing Requirements

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

			MIN	NOM	MAX	UNIT
SYNC (RT/SYNC PIN) WITH EXTERNAL CLOCK						
f_{SYNC}	Switching frequency using external clock on RT/SYNC pin		300		2300	kHz
T_{SYNC_MIN}	Minimum SYNC input pulse width	f_{SYNC} = 400kHz, $V_{RT/SYNC} > V_{IH\_RT/SYNC}$, $V_{RT/SYNC} < V_{IL\_RT/SYNC}$		100		ns
T_{LOCK_IN}	PLL lock time			100		µs

8.7 Switching Characteristics

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
T_{SS}	Internal soft-start time	The time of internal reference to increase from 0 V to 1.0 V	3	5	7	ms
HICCUP MODE						
N_{OC}	Number of cycles that LS current limit is tripped to enter Hiccup mode			128		Cycles
T_{OC}	Hiccup retry delay time			118		ms
SW (SW PIN)						
T_{ON_MIN}	Minimum turnon-time			105		ns
T_{ON_MAX}	Maximum turnon-time, HS timeout in dropout			7.5		µs
T_{OFF_MIN}	Minimum turnoff time			80		ns

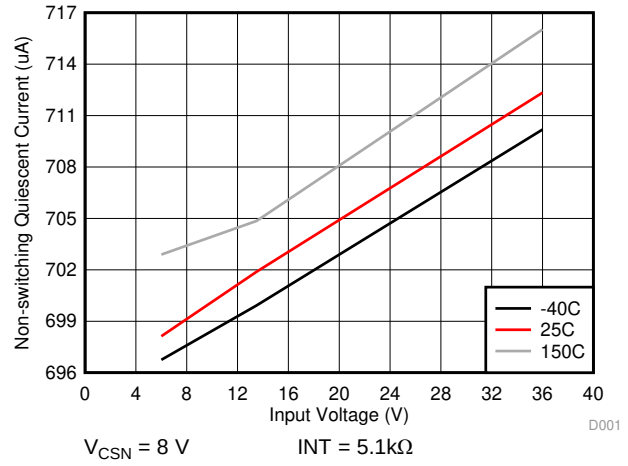
Switching Characteristics (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D_{max}	Maximum switch duty cycle			98		%
TIMING RESISTOR AND INTERNAL CLOCK						
f_{SW_RANGE}	Switching frequency range using RT mode		300		2300	kHz
f_{SW}	Switching frequency	R_T = 49.9 kΩ	360	400	440	kHz
	Switching frequency	R_T = 8.87 kΩ	1953	2100	2247	kHz
FS_{SS}	Frequency span of spread spectrum operation			±6		%
NFET DRIVER						
t_r	V_{LS_DR} rise time	VOUT = 5.1V, NFET = CSD87502Q2, time from LS_GD 10% to 90%		1000		µs
t_f	V_{LS_DR} fall time	VOUT = 5.1V, NFET = CSD87502Q2, time from LS_GD time 90% to 10%		100		µs
CURRENT LIMIT - EXTERNAL NFET CONNECTED BETWEEN CSN/OUT AND BUS, LS_GD CONNECTED TO FET GATE						
$t_{OC\_HIC\_ON}$	ON-time during hiccup mode			2		ms
$t_{OC\_HIC\_OFF}$	OFF-time during hiccup mode			263		ms
$\overline{\text{FAULT}}$ DUE TO VBUS OC, VBUS OV, DP OV, DM OV						
t_{DEGLA}	Asserting deglitch time		5.5	8.2	11.5	ms
t_{DEGLD}	De-asserting deglitch time		5.5	8.2	11.5	ms
$\overline{\text{BUCK\_ST}}$						
t_{DEGLA}	Asserting deglitch time		88	150	220	ms
HIGH-BANDWIDTH ANALOG SWITCH						
t_{pd}	Analog switch propagation delay			0.14		ns
t_{SK}	Analog switch skew between opposite transitions of the same port (t_{PHL} – t_{PLH})			0.02		ns
t_{OV_Dn}	DP_IN and DM_IN overvoltage protection response time			2		µs
$t_{ST\_DEG\_Dn}$	Deglitch time from Vcc > 4V to DP / DM data switch turn on		88	150	220	ms

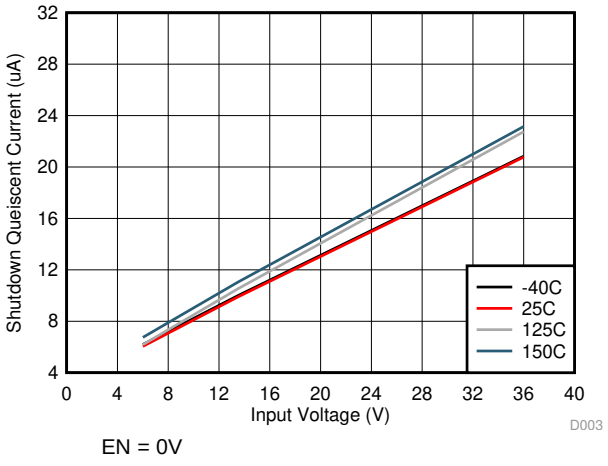
8.8 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.



V_{CSN} = 8 V INT = 5.1kΩ

Figure 1. Non-Switching Quiescent Current



EN = 0V

Figure 2. Shutdown Quiescent Current

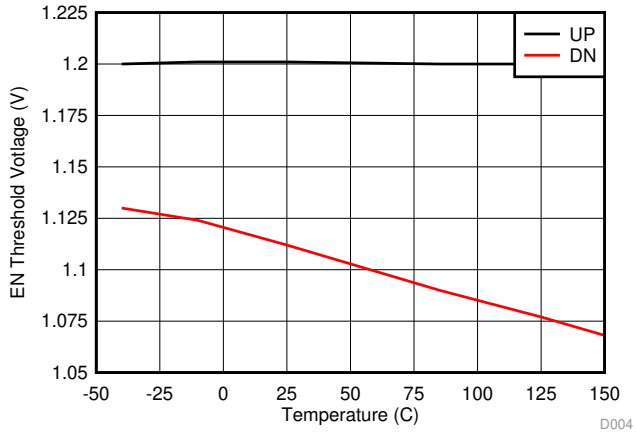


Figure 3. Precision Enable Threshold

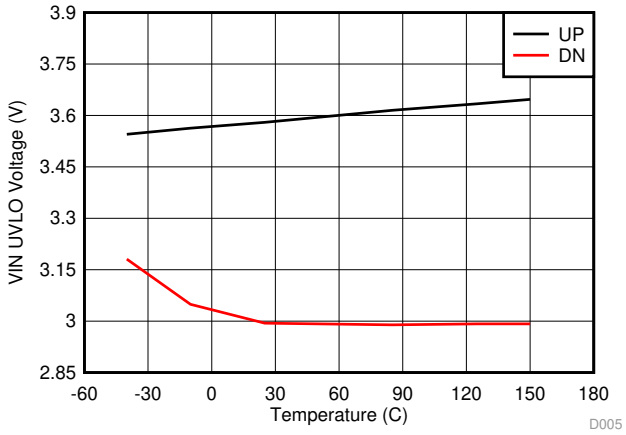


Figure 4. VIN UVLO Threshold

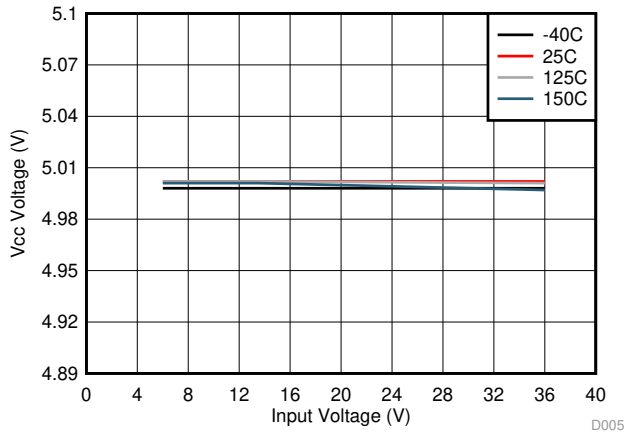
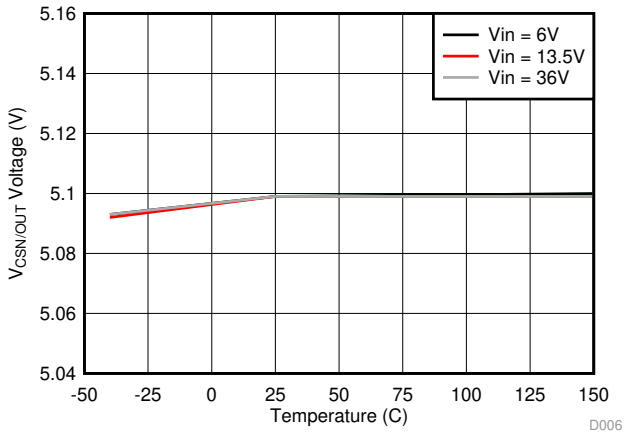


Figure 5. VCC vs Input Voltage



R_{IMON} = 0Ω

Figure 6. $V_{CSN/OUT}$ Voltage vs Junction Temperature

Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

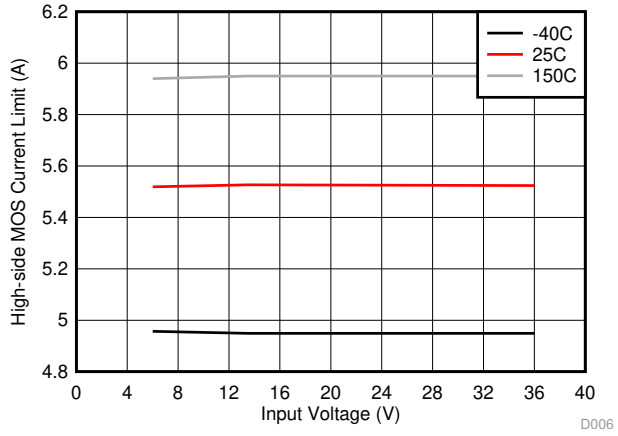


Figure 7. High-side Current Limit vs Input Voltage

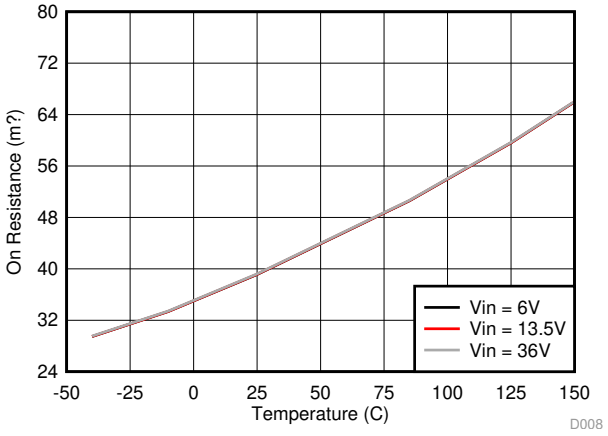


Figure 8. High-side MOSFET on Resistance vs Junction Temperature

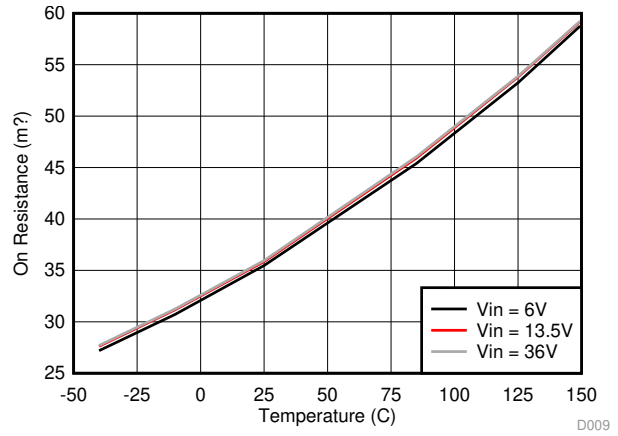
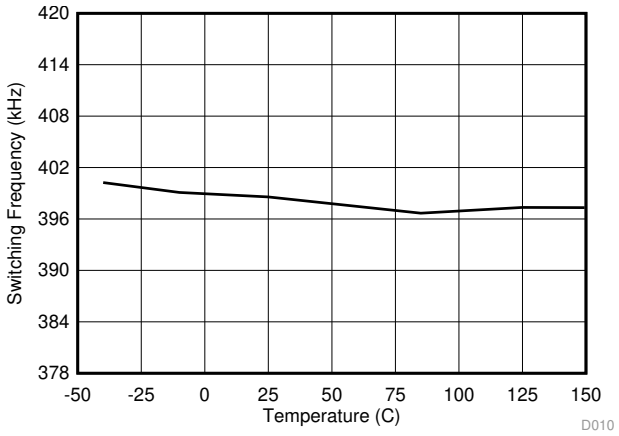
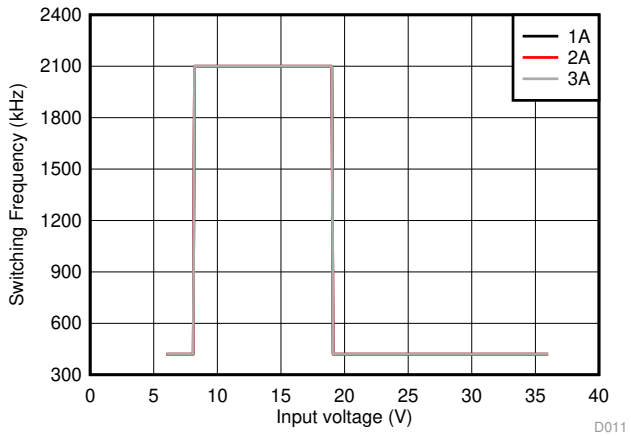


Figure 9. Low-side MOSFET on Resistance vs Junction Temperature



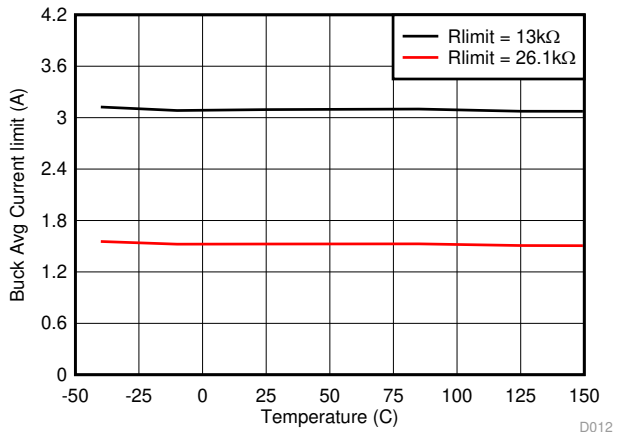
R_T = 49.9kΩ

Figure 10. Switching Frequency vs Junction Temperature



R_T = 8.87kΩ

Figure 11. Switching Frequency vs VIN Voltage

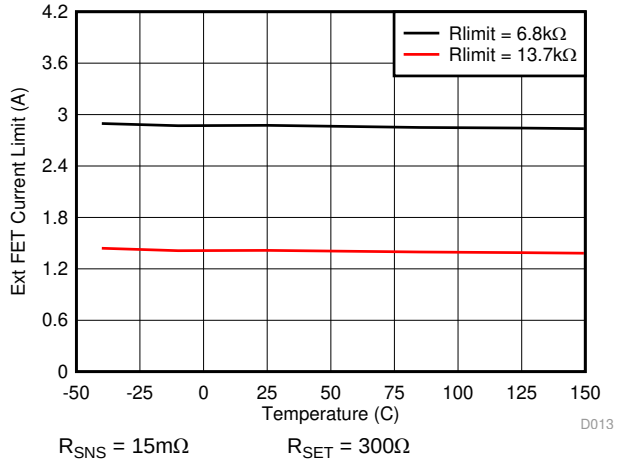


R_{SNS} = 15mΩ R_{SET} = 300Ω

Figure 12. Buck Average Current Limit vs Junction Temperature

Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.



R_{SNS} = 15mΩ R_{SET} = 300Ω

Figure 13. External FET Current Limit vs Junction Temperature

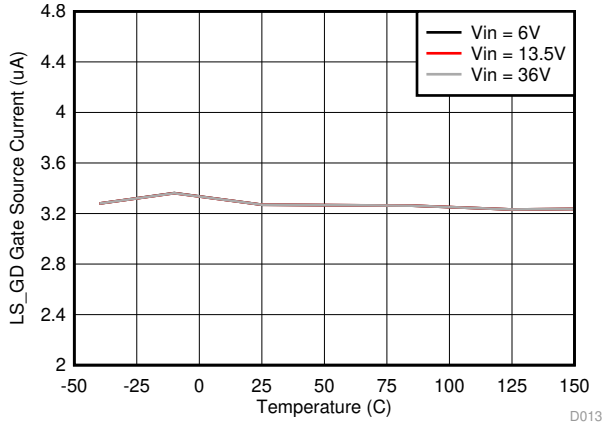
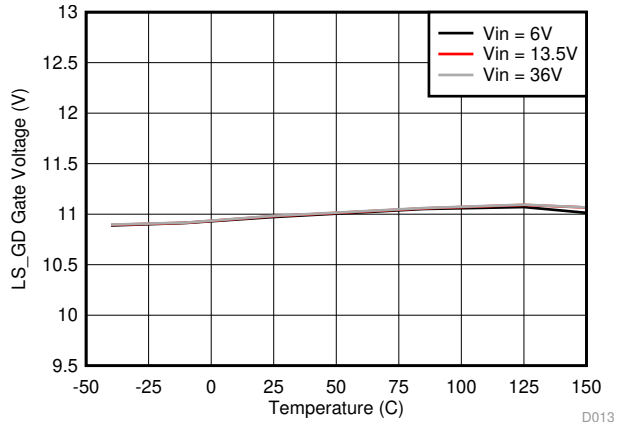
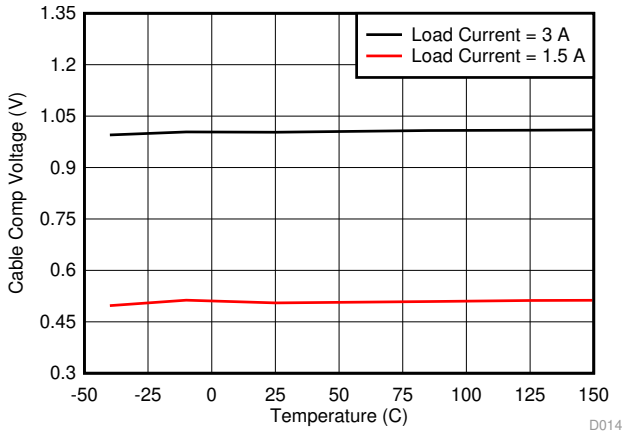


Figure 14. LS_GD Gate Source Current vs Junction Temperature



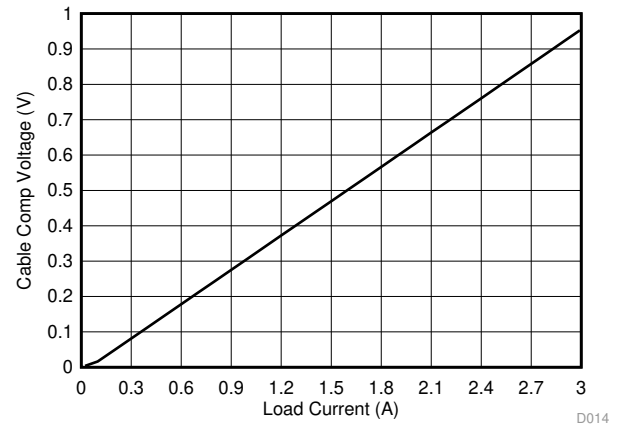
$V_{CSN/OUT}$ = 5.1V R_{IMON} = 0kΩ

Figure 15. LS_GD Gate Voltage vs Junction Temperature



R_{SNS} = 15mΩ R_{SET} = 300Ω R_{IMON} = 13kΩ

Figure 16. Cable Compensation Voltage vs Junction Temperature



R_{SNS} = 15mΩ R_{SET} = 300Ω R_{IMON} = 13kΩ

Figure 17. Cable Compensation Voltage vs Load Current

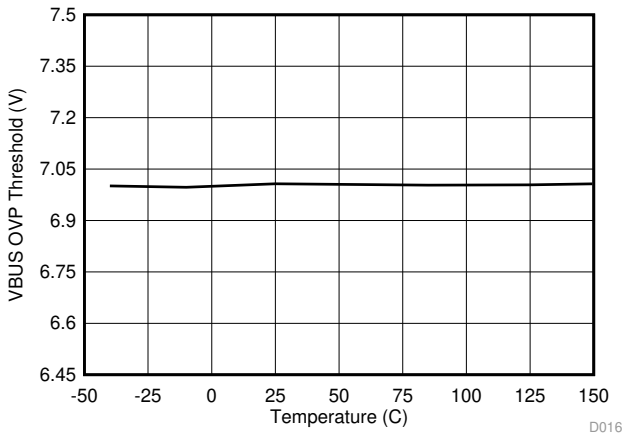


Figure 18. V_{BUS} Overvoltage Protection Threshold vs Junction Temperature

Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

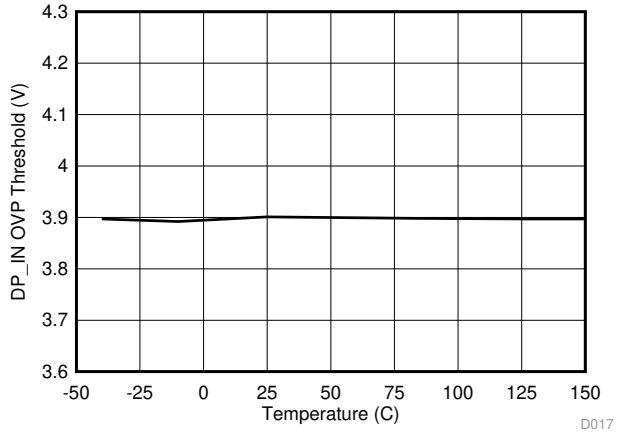


Figure 19. DP_IN Overvoltage Protection Threshold vs Junction Temperature

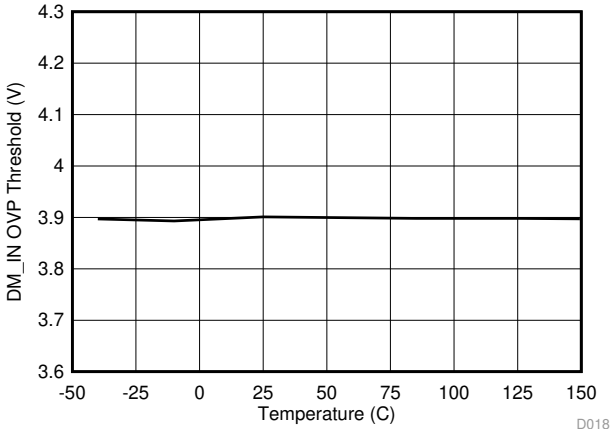
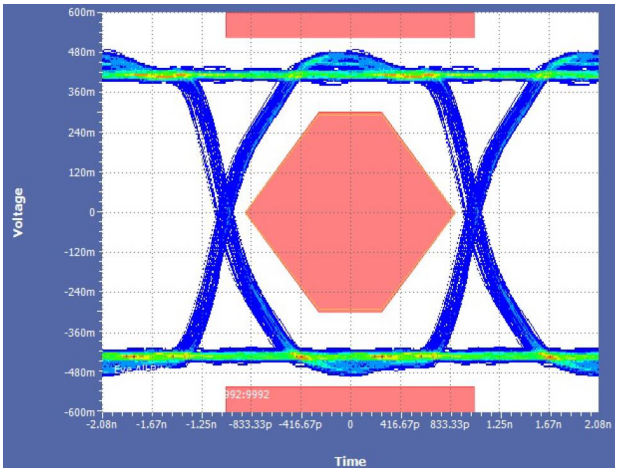
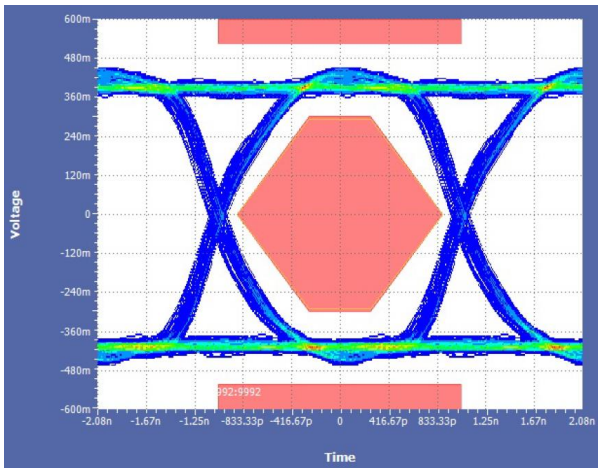


Figure 20. DM_IN Overvoltage Protection Threshold vs Junction Temperature



Measured Source with 10-cm cable

Figure 21. Bypassing the TPS2584x-Q1 Data Switch



Measured on TPS25830-Q1 EVM with 10-cm cable

Figure 22. Through the TPS2584x-Q1 Data Switch

Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

Figure 23. Data Transmission Characteristics vs Frequency

Figure 24. Off-State Data-Switch Isolation vs Frequency

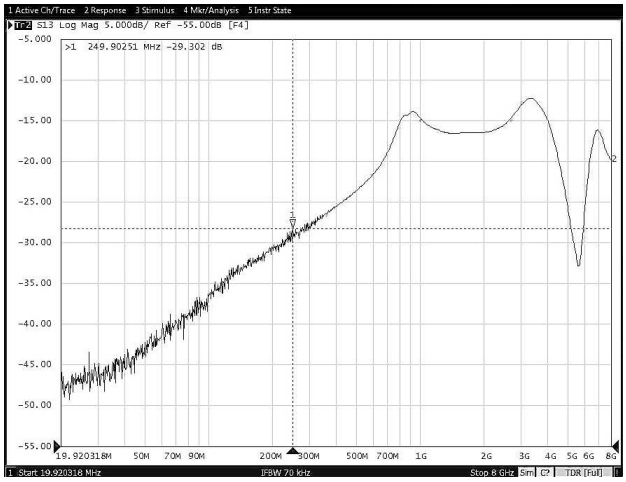


Figure 25. On-State Cross-Channel Isolation vs Frequency

9 Parameter Measurement Information

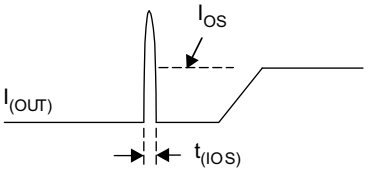


Figure 26. Short-Circuit Parameters

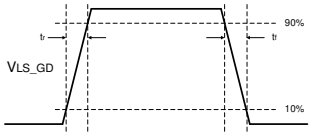


Figure 27. NFET Gate Drive Rise and Fall Time

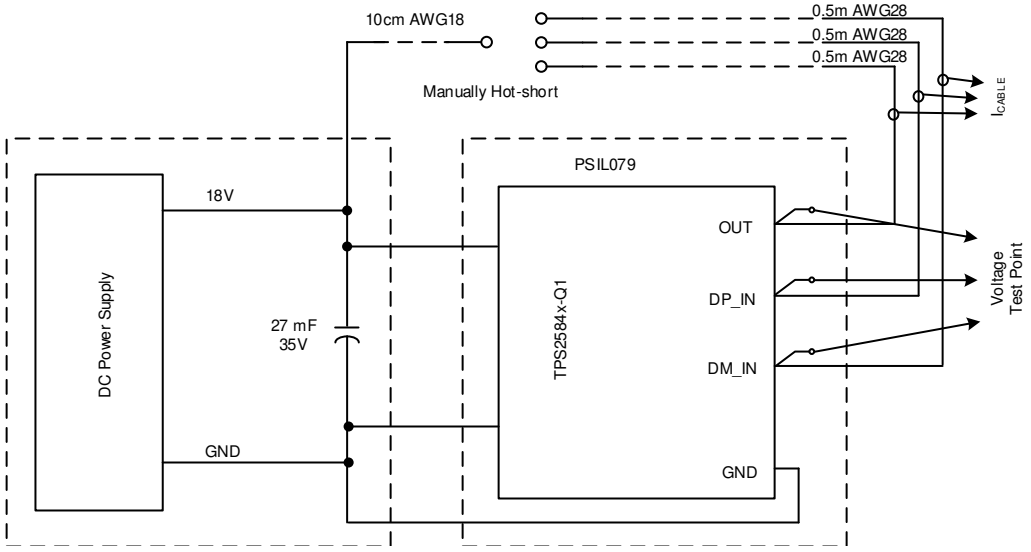


Figure 28. Short-to-Battery System Test Setup

10 Detailed Description

10.1 Overview

The TPS2584x-Q1 devices are full-featured solutions for implementing a compact USB charging port with support for Type-A BC1.2 standards. Both devices contain an efficient 36-V buck regulator power source capable of providing up to 3.5 A of output current at 5.10 V (nominal). System designers can optimize efficiency or solution size through careful selection of switching frequency over the range of 300 to 2200 kHz with sufficient margin to operate above or below the AM radio frequency band. In all versions the buck regulator operates in forced PWM mode ensuring fixed switching frequency regardless of load current. Spread-spectrum feature aid reducing harmonic peaks of the switching frequency potentially simplifying EMI filter design and easing compliance.

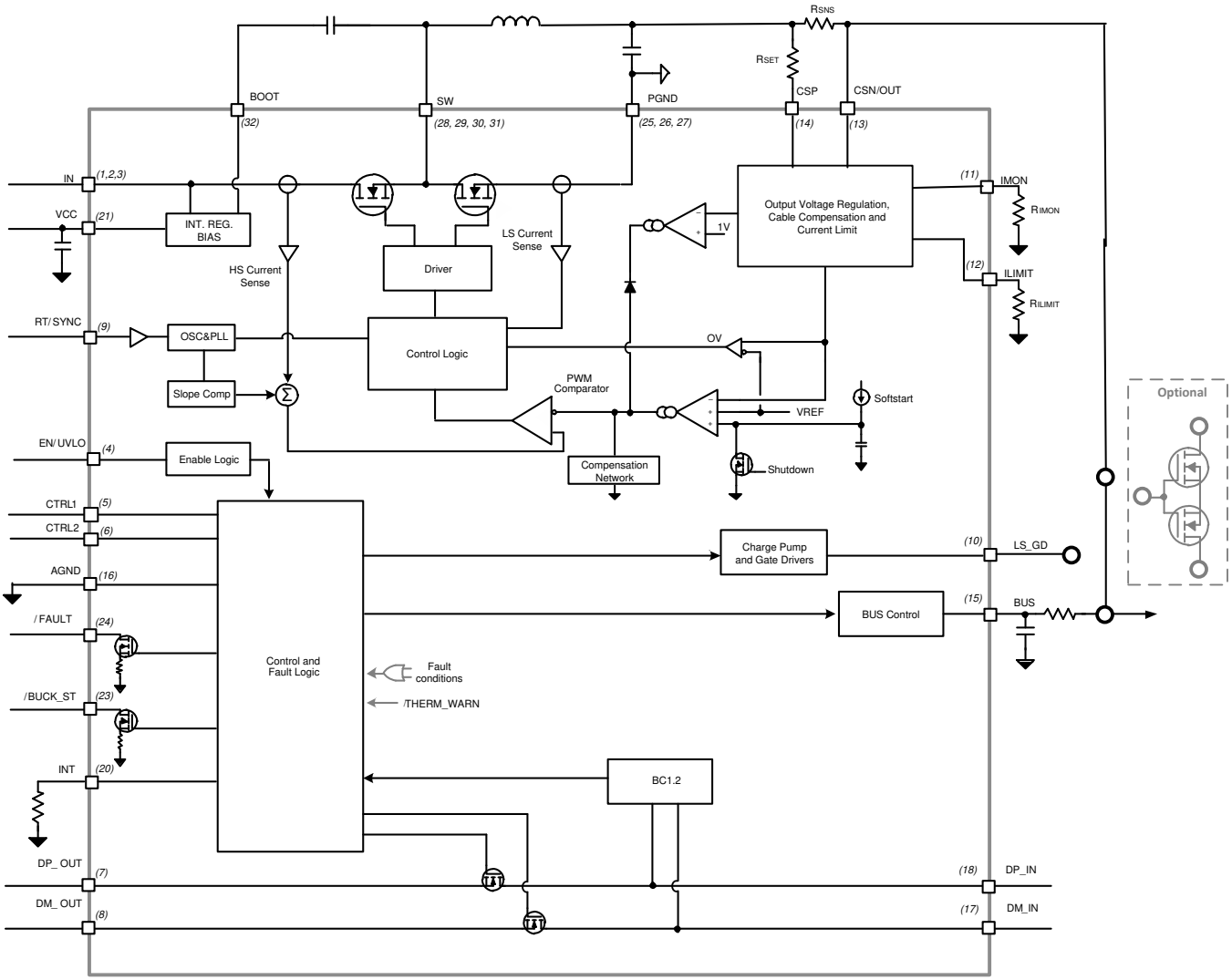
Current sensing via a precision high-side current sense amplifier enables an accurate, user programmable overcurrent limit setting; and programmable linear cable compensation to overcome IR losses when powering remote USB ports.

The CTRL1 and CTRL2 pins set the operating mode for the TPS2584x-Q1 device. The device can support CDP, SDP or Client configurations.

The TPS25840-Q1 integrates high band-width (800 MHz) USB switches, includes short to V_{BAT} and short to V_{BUS} protection as well as IEC61000-4-2 electrostatic discharge clamps to protect the host from potentially damaging overvoltage conditions.

The TPS25842-Q1 integrates high band-width (800 MHz) USB switches, includes short to V_{BUS} protection as well as IEC61000-4-2 electrostatic discharge clamps, but does not support short to V_{BAT} protection.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Buck Regulator

The following operating description of the TPS2584x-Q1 will refer to the *Functional Block Diagram* and the waveforms in Figure 29. TPS2584x-Q1 is a step-down synchronous buck regulator with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The TPS2584x-Q1 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current i_L increase with linear slope ($V_{IN} – V_{OUT}$) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the LS switch with a slope of $–V_{OUT}$ / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

Feature Description (continued)

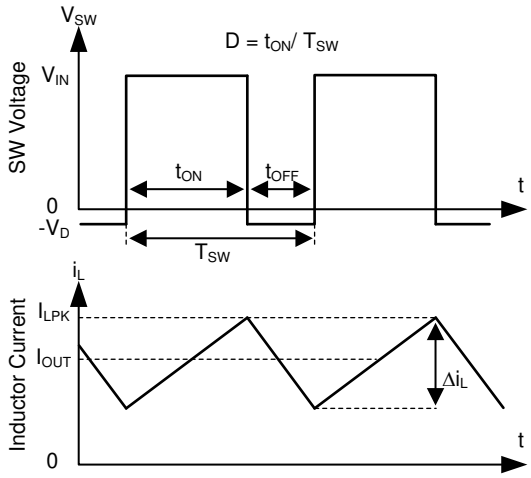


Figure 29. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The TPS2584x-Q1 employs fixed frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. TPS2584x-Q1 operates in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

10.3.2 Enable/UVLO

The voltage on the EN/UVLO pin controls the ON or OFF operation of TPS2584x-Q1. An EN/UVLO pin voltage higher than $V_{EN/UVLO-VOUT-H}$ is required to start the internal regulator (Assume 5.1k pull down resister on INT pin). The EN/UVLO pin is an input and can not be left open or floating. The simplest way to enable the operation of the TPS2584x-Q1 is to connect the EN to V_{IN}. This allows self-start-up of the TPS2584x-Q1 when V_{IN} is within the operation range.

Feature Description (continued)

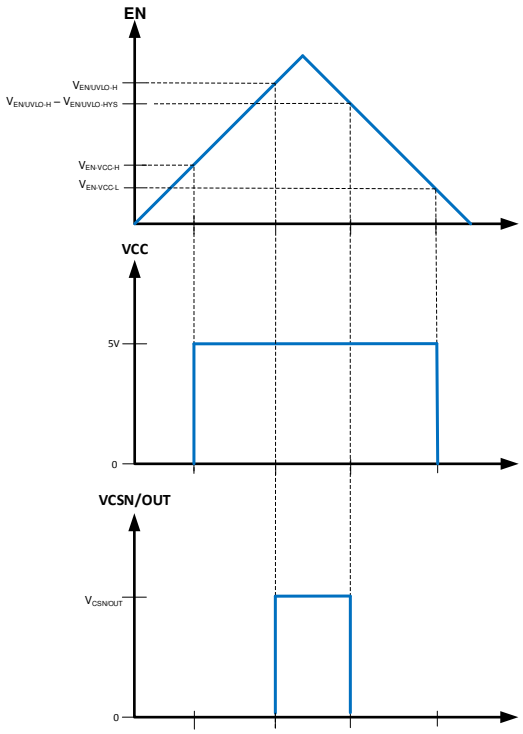


Figure 30. Precision Enable Behavior

Many applications will benefit from the employment of an enable divider R_{ENT} and R_{ENB} (Figure 31) to establish a precision system UVLO level for the TPS2584x-Q1. System UVLO can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery discharge level. To ensure the USB port V_{BUS} is within the 5-V operating range as required for USB compliance (refer to *USB.org* for the latest USB specifications and requirements), it is suggested that the R_{ENT} and R_{ENB} resistors be chosen such that the TPS2584x-Q1 enables when V_{IN} is approximately 6 V. Considering the drop out voltage of the buck regulator and IR loses in the system, 6 V provides adequate margin to maintain V_{BUS} within USB specifications. If system requirements such as a warm crank (start) automotive scenario require operation with V_{IN} < 6 V, the values of R_{ENT} and R_{ENB} can be calculated assuming a lower V_{IN}. An external logic signal can also be used to drive EN/UVLO input when a microcontroller is present and it is desirable to enable or disable the USB port remotely for other reasons.

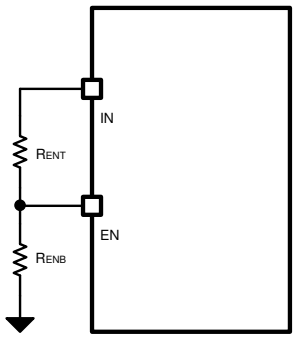


Figure 31. System UVLO by Enable Divider

UVLO configuration using external resistors is governed by the following equations:

Feature Description (continued)

$$R_{ENT} = (\frac{V_{IN(ON)}}{V_{EN/UVLO\_H}} - 1) \times R_{ENB} \quad (1)$$

$$V_{IN(OFF)} = V_{IN(ON)} \times (1 - \frac{V_{EN/UVLO\_HYS}}{V_{EN/UVLO\_H}}) \quad (2)$$

Example:

$V_{IN(ON)}$ = 6 V (user choice)

R_{ENB} = 5 kΩ (user choice)

R_{ENT} = [($V_{IN(ON)}$ / $V_{EN/UVLO\_H}$) - 1] × R_{ENB}= 19.6 kΩ. Choose standard 20 kΩ.

Therefore, $V_{IN(OFF)}$ = 6 V x [1 - (0.09 V / 1.2 V)] = 5.55 V

A typical start-up waveform is shown in Figure 32. The rise time of DCDC VBUS voltage is about 5 ms.

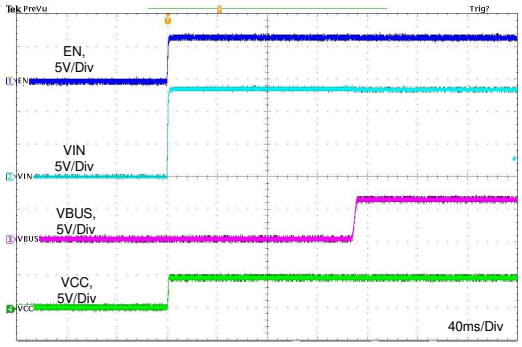


Figure 32. Typical Start-up Behavior, V_{IN} = 13.5 V, R_{IMON} = 12.6 kΩ

For TPS2584x-Q1, the pin voltage must meet the requirement below during startup, see Figure 33.

- V_{BUS} < 0.8 V (typical)
- V_{DX_OUT} < 2.2 V (typical)
- V_{DX_IN} < 1.5 V (typical)

After the 150-ms deglitch time, no additional requirement on these pins. In real application, $\overline{\text{BUCK\_ST}}$ pin can be used to configure the timing sequence.

Feature Description (continued)

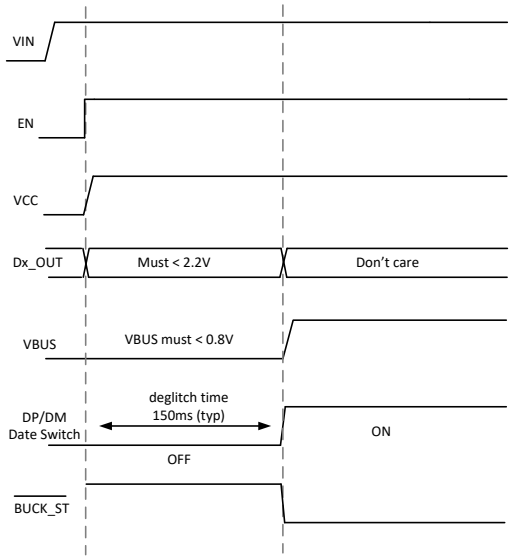


Figure 33. TPS2584x-Q1 Pin Voltage Requirement During Startup

10.3.3 Switching Frequency and Synchronization (RT/SYNC)

The switching frequency of the TPS2584x-Q1 can be programmed by the resistor R_T from the RT/SYNC pin and GND pin. To determine the RT resistance, for a given switching frequency, use Equation 3.

$$R_{RT}(k\Omega) = 26660 \times {f_{sw}}^{-1.0483}(kHz) \quad (3)$$

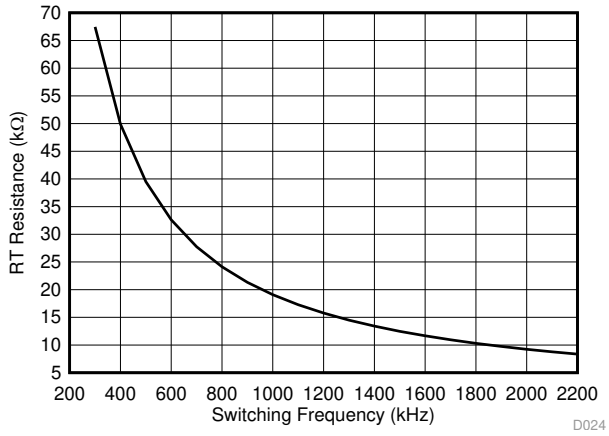


Figure 34. RT Set Resistor vs Switching Frequency

Typical RT resistors value are listed in Table 1.

Table 1. Setting the Switching Frequency with RT

RT (kΩ)	SWITCHING FREQUENCY (kHz)
68.1	300
49.9	400
39.2	500
19.1	1000
12.4	1500

Feature Description (continued)

Table 1. Setting the Switching Frequency with RT (continued)

RT (kΩ)	SWITCHING FREQUENCY (kHz)
9.31	2000
8.87	2100
8.45	2200

TPS2584x-Q1 switching action can be synchronized to an external clock from 300 kHz to 2.3 MHz. The RT/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive edge into the RT/SYNC pin. The AC coupled peak-to-peak voltage at the RT/SYNC pin must exceed the SYNC amplitude threshold of 3.5 V (typical) to trip the internal synchronization pulse detector, and the minimum SYNC clock ON and OFF time must be longer than 100 ns (typical). When using a low impedance signal source, the frequency setting resistor R_T is connected in parallel with an AC coupling capacitor C_{COUP} to a termination resistor R_{TERM} (for example: 50 Ω). The two resistors in series provide the default frequency setting resistance when the signal source is turned off. A 10 pF ceramic capacitor can be used for C_{COUP}. Figure 35 show the device synchronized to an external clock.

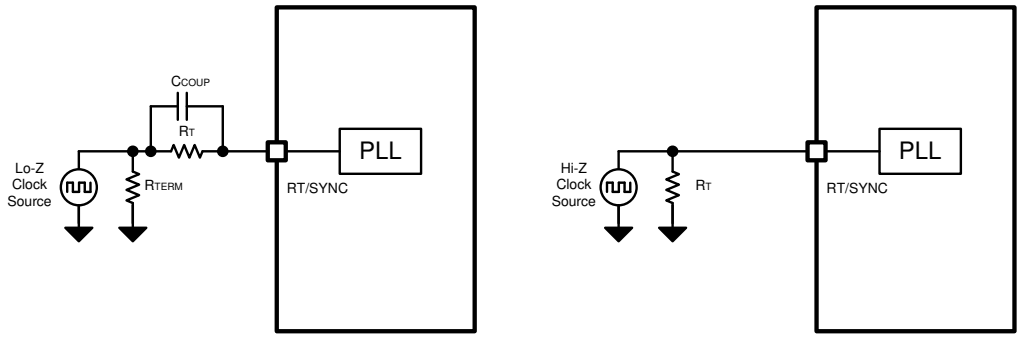


Figure 35. Synchronize to External Clock

In order to avoid AM radio frequency brand and maintain proper regulation when minimum ON-time or minimum OFF-time is reached, the TPS2584x-Q1 implement frequency foldback scheme depends on VIN voltage, refer to Figure 10.

- When 8 V < VIN ≤ 19 V, the switching frequency of TPS2584x-Q1 is determined by R_T resistor or external sync clock.
- When VIN ≤ 8 V, the switching frequency of TPS2584x-Q1 is set to default 420kHz, regardless of R_T resistor setting or external sync clock.
- When VIN > 19 V, the switching frequency of TPS2584x-Q1 is set to default 420kHz, regardless of R_T resistor setting or external sync clock.

Figure 36, Figure 37 and Figure 38 show the device switching frequency and behavior under different VIN voltage and R_T = 8.87kΩ.

Figure 39, Figure 40 and Figure 41 show the device switching frequency and behavior under different VIN voltage and synchronized to an external 2.1M system clock.

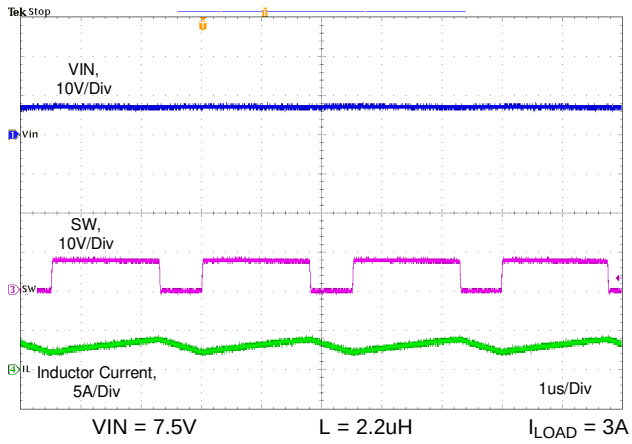


Figure 36. Switching Frequency when R_T = 8.87 kΩ

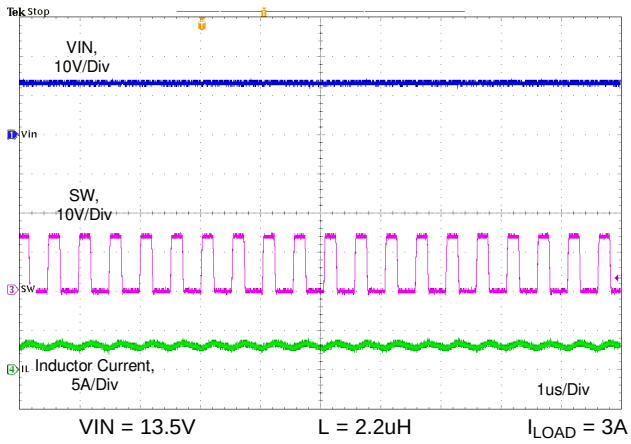


Figure 37. Switching Frequency when R_T = 8.87 kΩ

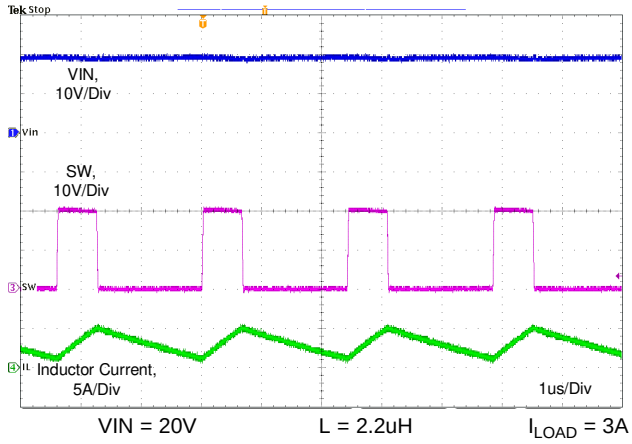


Figure 38. Switching Frequency when R_T = 8.87 kΩ

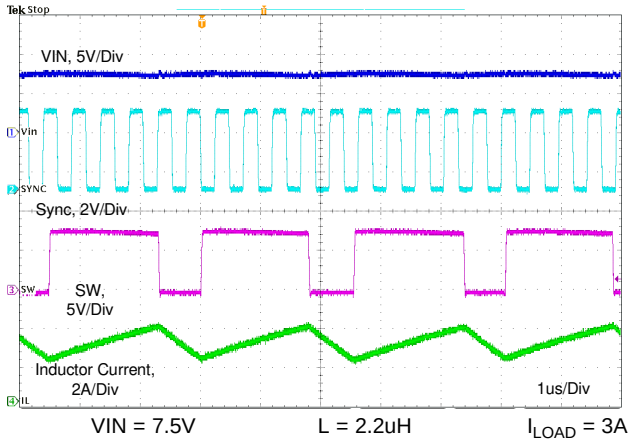


Figure 39. Synchronizing to External 2.1 MHz Clock

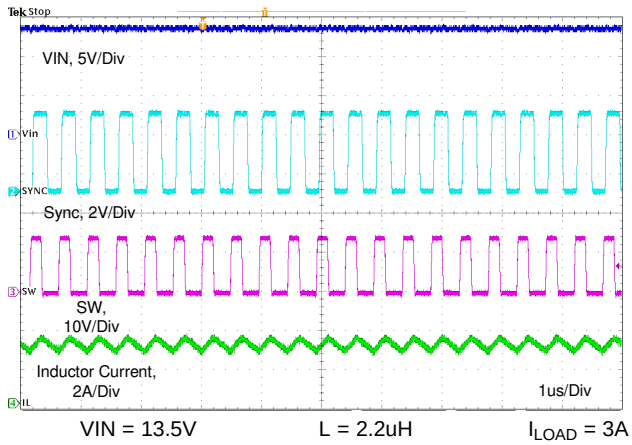


Figure 40. Synchronizing to External 2.1 MHz Clock

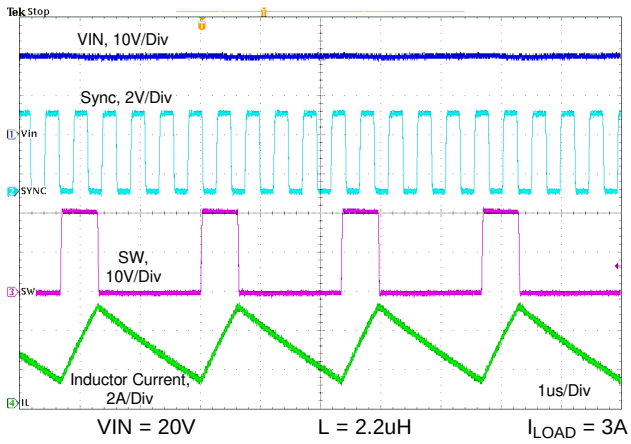


Figure 41. Synchronizing to External 2.1 MHz Clock

10.3.4 Spread-Spectrum Operation

In order to reduce EMI, the TPS2584x-Q1 introduce frequency spread spectrum. The spread spectrum is used to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. In most systems, low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The TPS2584x-Q1 devices use ±6% spread of switching frequencies with 1/256 swing frequency.

The spread spectrum function is only available when using the TPS2584x-Q1 internal oscillator. If the RT/SYNC pin is synchronized to an external clock, the spread spectrum function will be turn off.

10.3.5 VCC, VCC_UVLO

The TPS2584x-Q1 integrates an internal LDO to generate V_{CC} for control circuitry and MOSFET drivers. The nominal voltage for V_{CC} is 5 V. The V_{CC} pin is the output of an LDO and must be properly bypassed. A high quality ceramic capacitor with a value of 2.2 µF to 4.7 µF, 10 V or higher rated voltage should be placed as close as possible to VCC and grounded to the PGND ground pin. The V_{CC} output pin should not be loaded with more than 5 mA, or shorted to ground during operation. Shorting V_{CC} to ground during operation may cause damage to the TPS2584x-Q1.

10.3.6 Minimum ON-time, Minimum OFF-time

Minimum ON-time, T_{ON_MIN}, is the smallest duration of time that the HS switch can be on. T_{ON_MIN} is typically 105 ns in the TPS2584x-Q1. Minimum OFF-time, T_{OFF_MIN}, is the smallest duration that the HS switch can be off. T_{OFF_MIN} is typically 80 ns in the TPS2584x-Q1. In CCM (FPWM) operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given a selected switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON\_MIN} \times f_{sw} \tag{4}$$

And the maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{sw} \tag{5}$$

Given fixed T_{ON_MIN} and T_{OFF_MIN}, the higher the switching frequency the narrower the range of the allowed duty cycle.

10.3.7 Internal Compensation

The TPS2584x-Q1 is internally compensated as shown in Figure 42. The internal compensation is designed such that the loop response is stable over the specified operating frequency and output voltage range. The TPS2584x-Q1 is optimized for transient response over the range 300 kHz ≤ fsw ≤2300 kHz.

10.3.8 Bootstrap Voltage (BOOT)

The TPS2584x-Q1 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the BOOT capacitor is 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance overtemperature and voltage.

10.3.9 R_{SNS}, R_{SET}, R_{ILIMIT} and R_{IMON}

The programmable current limit threshold and full-scale cable compensation voltage are determined by the values of the R_{SNS}, R_{SET}, R_{ILIMIT} and R_{IMON} resistors. Refer to Figure 42.

- R_{SNS} is the current sense resistor. The recommended voltage across R_{SNS} under current limit should be approximately 50 mV as a compromise between accuracy and power dissipation. For example, if current limiting is desired for $I_{OUT(MAX)}$ ≥ 3.3 A, then R_{SNS} = 0.05 V / 3.3 A = 0.01515 Ω. Choose a standard value of 15 mΩ.
- R_{SET} determines the input current to the transconductance amplifier and current mirror. The amplifier

balances the voltage to be equal to that across R_{SNS}. Choose a R_{SET} value to produce an I_{SET} current between 75 - 180 µA at the desired $I_{OUT(MAX)}$. Considering 50 mV across R_{SET}, a value of 300 Ω will provide approximately 166 µA of I_{SET} current to the amplifier and mirror circuit. Care should be taken to limit the I_{SET} current below 200 µA to avoid saturating the internal amplifier circuit.

- R_{ILIMIT} inconjuction with the 0.5 x I_{SET} current produces a voltage on the ILIMIT pin which is proportional to the load current flowing in R_{SNS}. See *Current Limit Setting using R_{ILIMIT}* for details on setting the current limit.
- R_{IMON} inconjuction with the 0.5 x I_{SET} current produces a voltage on the IMON pin which is proportional to the load current flowing in R_{SNS}. See *Cable Compensation* for details on setting the current limit.

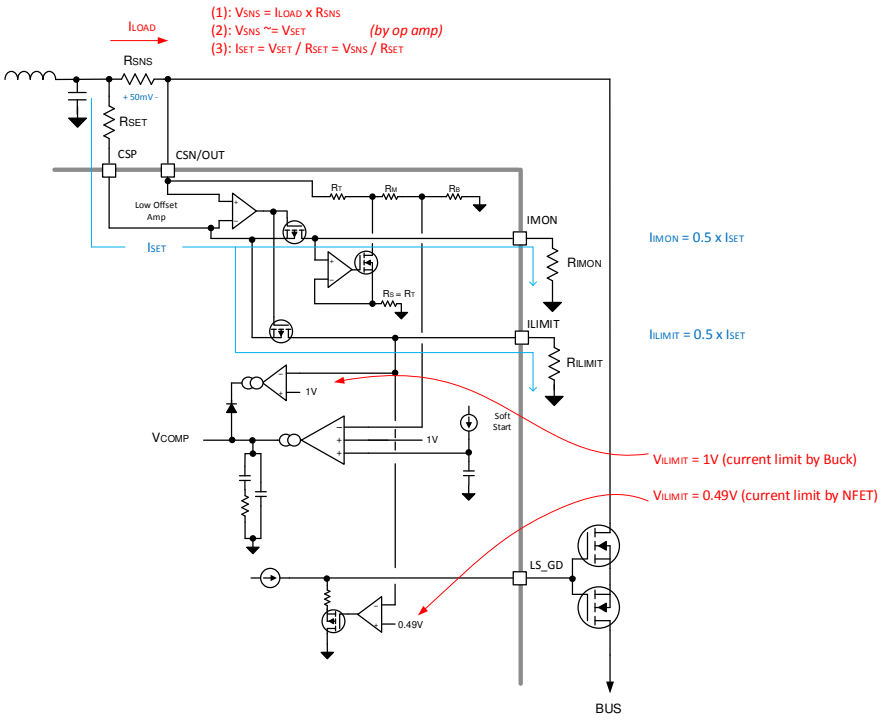


Figure 42. Current Limit and Cable Compensation Circuit

10.3.10 Overcurrent and Short Circuit Protection

For maximum versatility, TPS2584x-Q1 includes both a precision, programmable current limit as well cycle-by-cycle current limit to protect the USB port from extreme overload conditions. In most applications the R_{ILIMIT} resistor in conjunction with the selection of R_{SNS} and R_{SET} will determine the overload threshold. The cycle-by-cycle current limit will serve as a backup means of protection in the event R_{ILIMIT} is shorted to ground disabling the programmable current limit function.

In some application, the setting of TPS2584x-Q1 over-current need meet MFi requirement, pls refer to How to Pass MFi Overcurrent Protection Test With USB Charger and Switch Device for more details.

10.3.10.1 Current Limit Setting using R_{ILIMIT}

Refer to Figure 42. The TPS2584x-Q1 can establish current limit by two methods.

- Using external a single or back-to-back N-Channel MOFETs between CSN/OUT and BUS: A voltage of 0.49 V on the ILIMIT pin initiates current limiting using the external MOSFET by decreasing the LS_GD voltage causing the FET to operate in the saturation region. To protect the MOSFETs from damage a hiccup timer limits the duty cycle to prevent thermal runaway. Refer to the *Specifications* for MOSFET hiccup timing.
- Buck average current limit: No MOSFET, CSN/OUT connected to BUS. The LS_GD must be pulled up through 2.2-kΩ resistor. In this configuration a voltage of 1 V across R_{ILIMIT} on the ILIMIT pin initiates average current limiting of the buck regulator.

The two level current limit is described below:

- With external MOSFET Figure 43:

Isolating a fault on the USB port from other loads connected to the CSP output of the TPS2584x-Q1. In some applications, it may be useful to power additional circuitry (for example: USB HUB) from the output of the TPS2584x-Q1 and maintain operation of these circuits in the event of a short circuit downstream of the BUS pin. To prevent triggering the MOSFET current limit below the programmed ILIMIT threshold, external circuits should be supplied after the inductor and before the current sense resistor, R_{SNS}.

After R_{SNS} and R_{SET} are determined and the full load I_{SET} current is known, the resistor value R_{ILIMIT} can be determined by:

$$R_{ILIMIT} = \frac{0.49 \times R_{SET}}{0.5 \times (I_{LIMIT} \times R_{SNS} + 0.0007)} \quad (6)$$

In most cases, the recommended voltage across R_{SNS} under current limit should be approximately 50 mV as a compromise between accuracy and power dissipation. While in some application, R_{ILIMIT} is the only resistor that can be changed to achieve different current limit. Typical R_{ILIMIT} resistors value are listed in Table 2 given the condition R_{SNS} = 15 mΩ and R_{SET} = 300 Ω

Table 2. Setting the Current Limit with R_{ILIMIT}

Current-Limit Threshold (mA)	R_{ILIMIT} (kΩ)	
	With External MOSFET	Without External MOSFET
700	26.1	53.6
1500	12.7	26.1
1700	11.3	22.6
2700	7.15	14.7
3000	6.49	13
3400	5.62	11.5
3800	5.11	10.5

- Buck Average Current Limit Figure 44:

  CSN/OUT connected directly to BUS, LS_GD must be pulled up through 2.2-kΩ resistor. The TPS2584x-Q1 can operate as a stand-alone USB charging port. In this configuration, the internal buck regulator operates with average current limiting as programmed by the ILIMIT pin, potentially producing less heat compared to N-channel MOSFET current limiting

  After R_{SNS} and R_{SET} are determined and the full load I_{SET} current is known, the resistor value R_{ILIMIT} can be determined by:

$$R_{ILIMIT} = \frac{1 \times R_{SET}}{0.5 \times (I_{LIMIT} \times R_{SNS} + 0.0007)} \quad (7)$$

  Typical R_{ILIMIT} resistors value are listed in Table 2 given the condition R_{SNS} = 15 mΩ and R_{SET} = 300 Ω

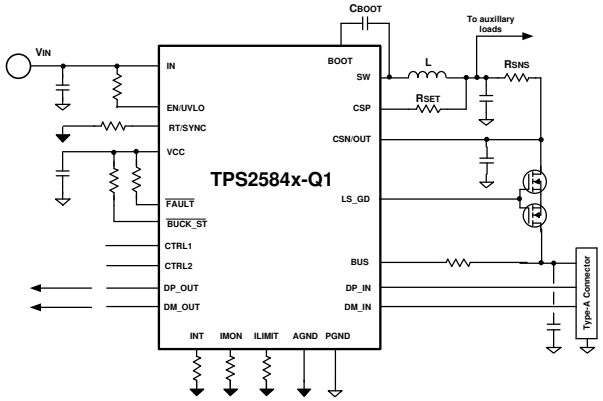


Figure 43. Current Limit with External MOSFET

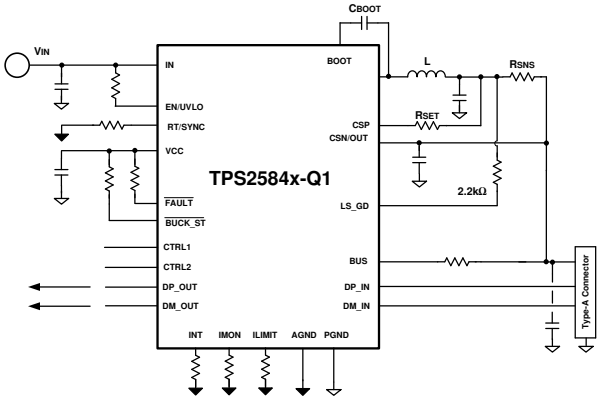


Figure 44. Buck Average Current Limit

10.3.10.2 Buck Average Current Limit Design Example

To start the procedure, the $I_{LOAD(MAX)}$, R_{SNS} and R_{SET}, must be known.

1. Determine I_{LIMIT}, usually chose I_{LIMIT}= $I_{LOAD(MAX)}$ / (1 - 10%).
2. Determine R_{SNS} to achieve 50 mV at current limit. For 3-A load current, choose I_{LIMIT} = 3.3A. R_{SNS} = (0.05 V / 3.3 A) = 15 mΩ.
3. Choose R_{SET} = 300 Ω
4. According to Equation 7, R_{LIMIT} = 300 / (0.5 x (3.3 X 0.015 + 0.0007)) = 11.95 kΩ.
5. Choose standard 11.8 kΩ.

10.3.10.3 External MOSFET Gate Drivers

The TPS2584x-Q1 has integrated NFET gate drivers, and can support current limit with external NFET. Refer to Figure 43.

The LS_GD pin of TPS2584x-Q1 can source 3 uA (typical) current to enhance the external MOSFET. A 6.2-V clamp between LS_GD and CSN/OUT pin limits the gate-to-source voltage. During DCDC start up, the LS_GD gate drivers begin to source current after $V_{CSN/OUT}$ reach 3V. If the $V_{CSN/OUT}$ > 7.5 V or V_{BUS} > 7 V under overvoltage condition, the LS_GD will turn off immediately with 35 uA (typical) sink current.

If load current above NFET current limit threshold, LS_GD will also turn off the NFET after 2 ms (typical) and enter hiccup mode to protect NFET from thermal issue. Refer to Figure 73 for application waveform.

In real application, if V_{BUS} short to V_{BAT} function is needed, 20 V back-to-back NFET is suggested in circuit design.

10.3.10.4 Cycle-by-Cycle Buck Current Limit

The buck regulator cycle-by-cycle current limit on both the peak and valley of the inductor current. Hiccup mode will be activated if a fault condition persists to prevent over-heating.

High-side MOSFET overcurrent protection is implemented by the nature of the Peak Current Mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. Refer to the *Functional Block Diagram* for more details. The peak current of HS switch is limited by a clamped maximum peak current threshold I_{HS_LIMIT} which is constant. So the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The current going through LS MOSFET is also sensed and monitored. When the LS switch turns on, the inductor current begins to ramp down. The LS switch will not be turned OFF at the end of a switching cycle if its current is above the LS current limit I_{LS_LIMIT}. The LS switch will be kept ON so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit I_{LS_LIMIT}. Then the LS switch will be turned OFF and the HS switch will be turned on after a dead time. This is somewhat different than the more typical peak current limit, and results in Equation 8 for the maximum load current.

$$I_{OUT\_MAX} = 0.5 \times (I_{LS\_LIMIT} + I_{HS\_LIMIT}) \tag{8}$$

If $V_{CSN/OUT}$ < 2-V typical due to a short circuit for 128 consecutive cycles, hiccup current protection mode will be activated. In hiccup mode, the regulator will be shut down and kept off for 118 ms typically, then TPS2583x-Q1 go through a normal re-start with soft start again. If the short-circuit condition remains, hiccup will repeat until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, prevents over-heating and potential damage to the device and serves as a backup to the programmable current limit see *Current Limit Setting using R_{ILIMIT}*. Once the output short is removed, the hiccup delay is passed, the output voltage recovers normally as shown in Figure 70.

10.3.11 Overvoltage, IEC and Short to Battery Protection

The TPS25840-Q1 integrates OVP and short to battery protection on VBUS, DM_IN and DP_IN pins. These pins can withstand voltage up to 18 V, and can protect upstream processor or Hub data line when overvoltage or short to battery condition occurs. Refer to Figure 28 for the short to battery test setup.

The TPS2584x-Q1 also integrates IEC ESD cell on DP_IN and DM_IN pins.

For more detailed TPS2584x-Q1 Short to Battery consideration and test report, pls refer to TPS2583x-Q1 and TPS2584x-Q1 Short-to- Battery Application.

10.3.11.1 V_{BUS} and $V_{CSN/OUT}$ Overvoltage Protection

The TPS25840-Q1 integrates overvoltage protection on both BUS and CSN/OUT pin, to meet different application requirement.

BUS pin can withstand up to 18 V, and the OVP threshold is 7-V typical. Once overvoltage is detected on BUS pin, the LS_GD will turn off immediately, also $\overline{\text{FAULT}}$ asserts after 8-ms deglitch time. Once the excessive voltage is removed, the LS_GD will turn on again and $\overline{\text{FAULT}}$ deasserts.

CSN/OUT pin can withstand up to 20 V, and the OVP threshold is 7.5-V typical. Once overvoltage is detected on CSN/OUT pin, the buck converter will stop regulation, also LS_GD will turn off immediately. Once the excessive voltage is removed, the buck converter will resume and the LS_GD will turn on again.

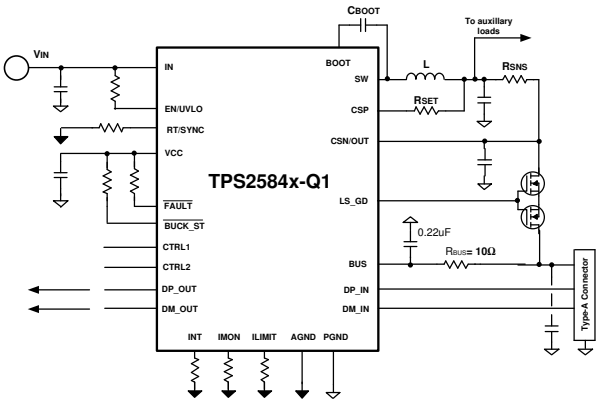


Figure 45. Current Limit with External MOSFET

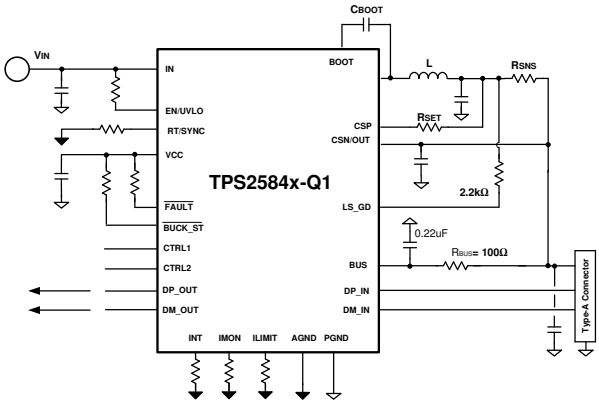


Figure 46. Buck Average Current Limit

As shown in Figure 45, TPS25840-Q1 is configured in external FET current limit mode. When short to battery occurs on BUS_Connector, the external MOSFET will be turn off immediately after BUS pin detect over voltage. The $\overline{\text{FAULT}}$ signal will assert after 8-ms deglitch time, see Figure 77. With Back-to-back FET, the TPS2583x-Q1 can withstand short to battery event even when Vin is off. A 10-Ω 0805 resistor is recommended between BUS pin and BUS_Connector.

As shown in Figure 46, TPS25840-Q1 is configured in buck average current limit mode. When short to battery occurs on BUS_Connector, the buck regulator will stop switching after CSN/OUT pin detect overvoltage. The $\overline{\text{FAULT}}$ signal will also assert after 8-ms deglitch time. A 100-Ω 0805 resistor is recommended between BUS pin and BUS_Connector in buck average current limit mode.

10.3.11.2 DP_IN and DM_IN Protection

DP_IN and DM_IN protection consists of IEC ESD and overvoltage protection.

The DP_IN and DM_IN pins integrate an IEC ESD cell to provide ESD protection up to ±15 kV air discharge and ±8 kV contact discharge per IEC 61000-4-2 (See the *ESD Ratings* section for test conditions). The IEC ESD performance of the TPS2584x-Q1 device depends on the capacitance connected from BUS pin to GND. A 0.22 µF capacitor placed close to the BUS pin is recommended.

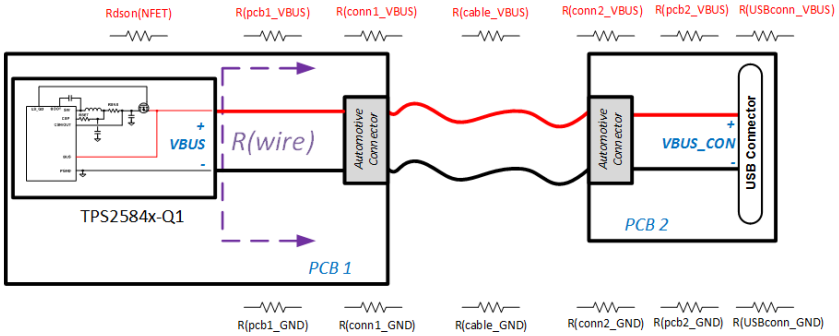
The ESD stress seen at DP_IN and DM_IN is impacted by many external factors like the parasitic resistance and inductance between ESD test points and the DP_IN and DM_IN pins. For air discharge, the temperature and humidity of the environment can cause some difference, so the IEC performance should always be verified in the end-application circuit.

Overvoltage protection (OVP) is provided for short-to-V_{BUS} or short-to-battery conditions in the vehicle harness, preventing damage to the upstream USB transceiver or hub. When the voltage on DP_IN or DM_IN exceeds 3.9 V (typical), the TPS25840-Q1 device immediately turn off DP/DM switch, and responds to block the high-voltage reverse connection to DP_OUT and DM_OUT. $\overline{\text{FAULT}}$ signal will assert after 8-ms deglitch time, see Figure 79.

For DP_IN and DM_IN, when OVP is triggered, the device turns on an internal discharge path with 416-kΩ resistance to ground. On removal of the overvoltage condition, the pin automatically turns off this discharge path and returns to normal operation by turning on the previously affected analog switch.

10.3.12 Cable Compensation

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. Cable droop compensation linearly increases the voltage at the CSN/OUT pin of TPS2584x-Q1 as load current increases with the objective of maintaining V_{BUS_CON} (the bus voltage at the USB connector) at 5 V, regardless of load conditions. Most portable devices charge at maximum current when 5 V is present at the USB connector. Figure 47 provides an example of resistor drops encountered when designing an automotive USB system with a remote USB connector location.



R(wire) = R(pcb1_VBUS) + R(conn1_VBUS) + R(cable_VBUS) + R(conn2_VBUS) + R(pcb2_VBUS) + R(USBconn_VBUS) + R(USBconn_GND) + R(pcb2_GND) + R(conn2_GND) + R(cable_GND) + R(conn1_GND) + R(pcb1_GND)

Figure 47. Automotive USB Resistances

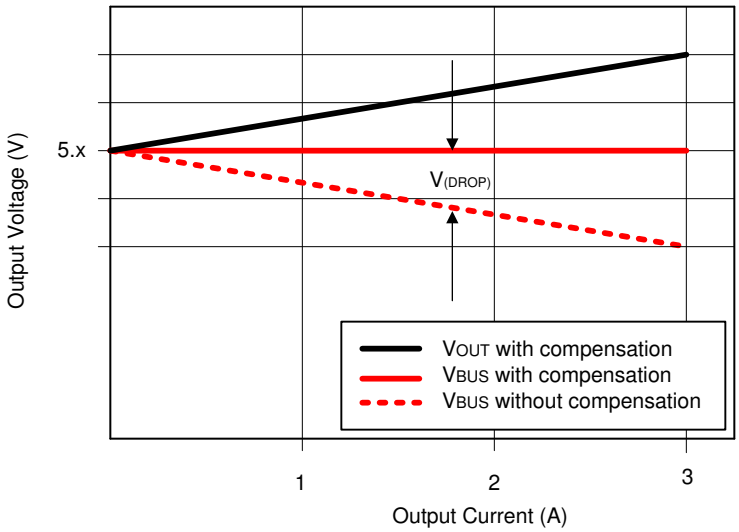


Figure 48. Voltage Drop

The TPS2584x-Q1 detects the load current and increases the voltage at the CSN/OUT pin to compensate the IR drop in the charging path according to the gain set by the R_{SNS}, R_{SET}, and R_{IMON} resistors as described in *R_{SNS}, R_{SET}, R_{ILIMIT} and R_{IMON}*.

The amount of cable droop compensation required can be estimated by the following equation $\Delta V_{OUT} = (R_{SNS} + R_{DSON\_NFET} + R_{WIRE}) * I_{BUS}$. R_{IMON} is then chosen by $R_{IMON} = (\Delta V_{OUT} * R_{SET} * 2) / (I_{BUS} * R_{SNS})$, Where ΔV_{OUT} is the desired cable droop compensation voltage at full load.

In most cases, the recommended voltage across R_{SNS} should be 50 mV, see the *R_{SNS}, R_{SET}, R_{ILIMIT} and R_{IMON}* section. In type-C application, typical R_{IMON} resistors value are listed in Table 3 given the condition full load current = 3 A, R_{SNS} = 15 mΩ and R_{SET} = 300 Ω.

Table 3. Setting the Cable Compensation Voltage with R_{IMON}

Cable Compensation Voltage at 3-A Full Load (V)	R_{IMON} (kΩ)
0.3	4.02
0.6	8.06
0.9	12.1
1.2	16.2
1.5	20

NOTE

The maximum cable compensation voltage in TPS2584x-Q1 is 1.5 V.

10.3.12.1 Cable Compensation Design Example

To start the procedure, the R_{SNS}, R_{DSON_NFET} and wire resistance R_{WIRE}, must be known.

1. Determine R_{SNS} to achieve 50 mV at full current. For 3.3 A (3-A load current plus at approximately 10% for overcurrent threshold). R_{SNS} = (0.05 V / 3.3 A) = 15 mΩ.
2. R_{DSON_NFET} = 50 mΩ
3. R_{WIRE} = 200 mΩ
4. $\Delta V_{OUT} = (R_{SNS} + R_{DSON\_NFET} + R_{WIRE}) \times I_{BUS} = (0.015 + 0.05 + 0.2) \times 3 = 0.795$ V
5. Choose R_{SET} = 300 Ω
6. $R_{IMON} = (\Delta V_{OUT} * R_{SET} \times 2) / (I_{BUS} \times R_{SNS}) = (0.795 \times 300 \times 2) / (3 \times 0.015) = 10.6$ kΩ

10.3.13 USB Port Control

The TPS25840-Q1 and TPS25842-Q1 include DP_IN, DM_IN pins for automatic or host facilitated USB port power management of a Type-A downstream facing connector. See *Device Functional Modes* for details on configuring the TPS2584x-Q1.

10.3.14 FAULT Response

The device features an active-low, open-drain fault output. Connect a 100-kΩ pullup resistor from $\overline{\text{FAULT}}$ to VCC or other suitable I/O voltage. $\overline{\text{FAULT}}$ can be left open or tied to GND when not used.

Table 4 summarizes the conditions that generate a fault and actions taken by the device.

Table 4. Fault and Warning Conditions

EVENT	CONDITION	ACTION
Overcurrent on OUT	NFET or Buck average current limit implemented, see *Current Limit Setting using R_{ILIMIT}*. $I_{CSN/OUT}$ > programmed I_{SNS}.	The device regulates current at I_{SNS} either by external NFET or by the buck regulator control loop. When current limiting by external NFET, there is NO fault indicator assertion under minor overload conditions. When current limiting by buck average current, there is NO fault indicator assertion under minor overload conditions. Hard shorts during average buck current limiting may trigger buck hiccup operation. The $\overline{\text{FAULT}}$ indicator asserts immediately after N_{OC} cycles in and persists for T_{OC} as specified in *Cycle-by-Cycle Buck Current Limit*.
Overvoltage on BUS	$V_{BUS} > V_{BUS\_OV}$	The device turns on the BUS discharge path in the event of an overvoltage conditions, and turn off the LS_GD immediately. The $\overline{\text{FAULT}}$ indicator asserts and de-asserts with a 8-ms deglitch.
Overvoltage on the data lines	DP_IN or DM_IN > $V_{Dx\_IN\_OV}$	The device immediately shuts off the USB data switches. The $\overline{\text{FAULT}}$ indicator asserts and de-asserts with a 8-ms deglitch.

10.3.15 USB Specification Overview

Universal Serial Bus specifications provide critical physical and electrical requirements to electronics manufacturers of USB capable equipment. Adherence to these specifications during product development coupled with standardized compliance testing assures very high degrees of interoperability amongst USB products in the market. Since its inception in the mid 1990s, USB has undergone a number of revisions to enhance utility and extend functionality. For the most up to date standards, please consult the USB Implementers Forum (USB-IF).

All USB ports are capable of providing a 5-V output making them a convenient power source for operating and charging portable devices. USB specification documents outline specific power requirements to ensure interoperability. In general, a USB 2.0 port host port is required to provide up to 500 mA; a USB 3.0 or USB 3.1 port is required to provide up to 900 mA; ports adhering to the USB Battery Charging 1.2 Specification provide up to 1500 mA; and newer Type-C ports can provide up to 3000 mA. Though USB standards governing power requirements exist, some manufacturers of popular portable devices created their own proprietary mechanisms to extend allowed available current beyond the 1500 mA maximum per BC 1.2. While not officially part of the standards maintained by the USB-IF, these proprietary mechanisms are recognized and implemented by manufacturers of USB charging ports.

The TPS2584x-Q1 device supports the most-common USB-charging schemes BC1.2 in popular hand-held media and cellular devices.

The BC1.2 specification includes three different port types:

- Standard downstream port (SDP, supported)
- Charging downstream port (CDP, supported)
- Dedicated charging port (DCP, NOT supported)

BC1.2 defines a charging port as a downstream-facing USB port that provides power for charging portable equipment. Under this definition, CDP and DCP are defined as charging ports.

Table 5 lists the difference between these port types.

Table 5. Operating Modes Table

PORT TYPE	SUPPORTS USB2.0 COMMUNICATION	MAXIMUM ALLOWABLE CURRENT DRAWN BY PORTABLE EQUIPMENT (A)
SDP (USB 2.0)	YES	0.5
SDP (USB 3.0 and 3.1)	YES	0.9
CDP	YES	1.5
DCP	NO	1.5

10.3.16 Device Power Pins (IN, CSN/OUT, and PGND)

The IN pins are the input power path to the TPS2584x-Q1 devices. The internal LDO and buck regulator high side switch are supplied from the IN pins. The CSN/OUT pin connects to the negative terminal of the current sense amplifier and the internal voltage feedback network. This pin must be connected to the output LC filter for proper operation. PGND is the power ground return. For optimum performance, ensure the IN pin is properly bypassed to PGND with adequate bulk and high-frequency bypass capacitance located as close to these pins as possible.

10.3.17 Thermal Shutdown

The device has an internal overtemperature shutdown threshold, T_{SD} to protect the device from damage and overall safety of the system. When device temperature exceeds T_{SD}, the LD_GD pin is pulled low, and the buck regulator stops switching. The device attempts to power-up when die temperature decreases by approximately 20°C.

10.4 Device Functional Modes

10.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPS2584x-Q1. When V_{EN} is below 1.2 V (typical), the device is in shutdown mode. The TPS2584x-Q1 also employs VIN and VCC undervoltage lock out protection. If V_{IN} or V_{CC} voltage is below their respective UVLO level, the regulator will be turned off.

10.4.2 Active Mode

The TPS2584x-Q1 is in Active Mode when V_{EN} is above the precision enable threshold, V_{IN} and V_{CC} are above their respective UVLO levels. The simplest way to enable the TPS2584x-Q1 is to connect the EN pin to VIN pin. This allows self startup when the input voltage is in the operating range: 3.8 V to 36 V and a UFP detection is made. Refer to *VCC, VCC_UVLO* and *Enable/UVLO* for details on setting these operating levels.

In Active Mode, the TPS2584x-Q1 buck regulator operates with forced pulse width modulation (FPWM), also referred to as forced continuous conduction mode (FCCM). This ensures the buck regulator switching frequency remains constant under all load conditions. FPWM operation provides low output voltage ripple, tight output voltage regulation, and constant switching frequency. Built-in spread-spectrum modulation aids in distributing spectral energy across a narrow band around the switching frequency programmed by the RT/SYNC pin. Under light load conditions the inductor current is allowed to go negative. A negative current limit of I_{L_NEG} is imposed to prevent damage to the regulator's low side FET. During operation the TPS2584x-Q1 will synchronize to any valid clock signal on the RT/SYNC input.

10.4.3 Device Truth Table (TT)

The device truth table (Table 6) lists all valid combinations for the two control pins (CTRL1 and CTRL2). The TPS2584x-Q1 devices monitor the CTRL inputs and transitions to whichever charging mode it is commanded.

Table 6. Truth Table

DEVICE(S)	CTRL1	CTRL2	CURRENT LIMIT SETTING	USB MODES	BUCK REGULATOR	LS_GD
TPS2584x-Q1	0	0	Buck Hiccup Only	Client Mode(1)	ON	OFF
	0	1	Buck Hiccup Only	Client Mode(1)	ON	OFF
	1	0	See *Current Limit Setting using R_{ILIMIT}*	SDP Mode	ON	
	1	1		CDP Mode	ON	

(1) TPS2584x-Q1: USB data switches ON during client mode.

10.4.4 USB Port Operating Modes

10.4.4.1 Standard Downstream Port (SDP) Mode — USB 2.0, USB 3.0, and USB 3.1

An SDP is a traditional USB port that follows USB 2.0, USB 3.0 or USB 3.1 protocol. A USB 2.0 SDP supplies a minimum of 500 mA per port and supports USB 2.0 communications. A USB 3.x SDP supplies a minimum of 900 mA per port and supports USB 3.0 or USB 3.1 communications. For both types, the host controller must be active to allow charging.

10.4.4.2 Charging Downstream Port (CDP) Mode

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5 A per port. A CDP provides power and meets the USB 2.0 requirements for device enumeration. USB-2.0 communication is supported, and the host controller must be active to allow charging. The difference between CDP and SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP handshaking process occurs in two steps. During step one, the portable equipment outputs a nominal 0.6-V output on the D+ line and reads the voltage input on the D– line. The portable device detects the connection to an SDP if the voltage is less than the nominal data-detect voltage of 0.3 V. The portable device detects the connection to a CDP if the D– voltage is greater than the nominal data detect voltage of 0.3 V and optionally less than 0.8 V.

The second step is necessary for portable equipment to determine whether the equipment is connected to a CDP or a DCP. The portable device outputs a nominal 0.6-V output on the D– line and reads the voltage input on the D+ line. The portable device concludes the equipment is connected to a CDP if the data line being read remains less than the nominal data detects voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3 V.

10.4.4.3 Client Mode

The TPS2584x-Q1 device integrates client mode as shown in Figure 49. The external MOSFET power switch is OFF and only the data analog switch is ON. This mode can be used by automotive USB system manufacturers and OEMs for factory-only software programming via the USB port.

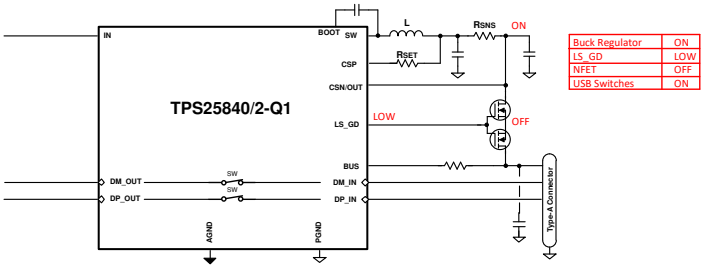


Figure 49. Client-Mode Equivalent Circuit

10.4.5 High-Bandwidth Data-Line Switches

The TPS2584x-Q1 device passes the D+ and D– data lines through the device to enable monitoring and handshaking while supporting the charging operation. A wide-bandwidth signal switch allows data to pass through the device without corrupting signal integrity. The data-line switches are turned on in any of the CDP, SDP, or client operating modes. The EN input must be at logic high for the data line switches to be enabled.

For more detailed USB2.0 data line consideration and eye diagram test report, pls refer to How to improve USB2.0 Eye Diagram using long USB cable.

NOTE

- While in CDP mode, the data switches are ON, even during CDP handshaking.
- The data line switches are OFF if EN/UVLO is low.
- The data line switches are OFF during External FET Current limit conditions.
- The data switches are only for a USB-2.0 differential pair. In the case of a USB-3.0 host, the super-speed differential pairs must be routed directly to the USB connector without passing through the TPS2584x device.

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The TPS2584x-Q1 is a step down DC-to-DC regulator and USB charge port controller. It is typically used in automotive systems to convert a DC voltage from the vehicle battery to 5-V DC with a maximum output current of 3 A. The following design procedure can be used to select components for the TPS2584x-Q1.

11.2 Typical Application

The TPS2584x-Q1 only requires a few external components to convert from a wide voltage range supply to a 5-V output for powering USB devices. Figure 50 shows a basic schematic.

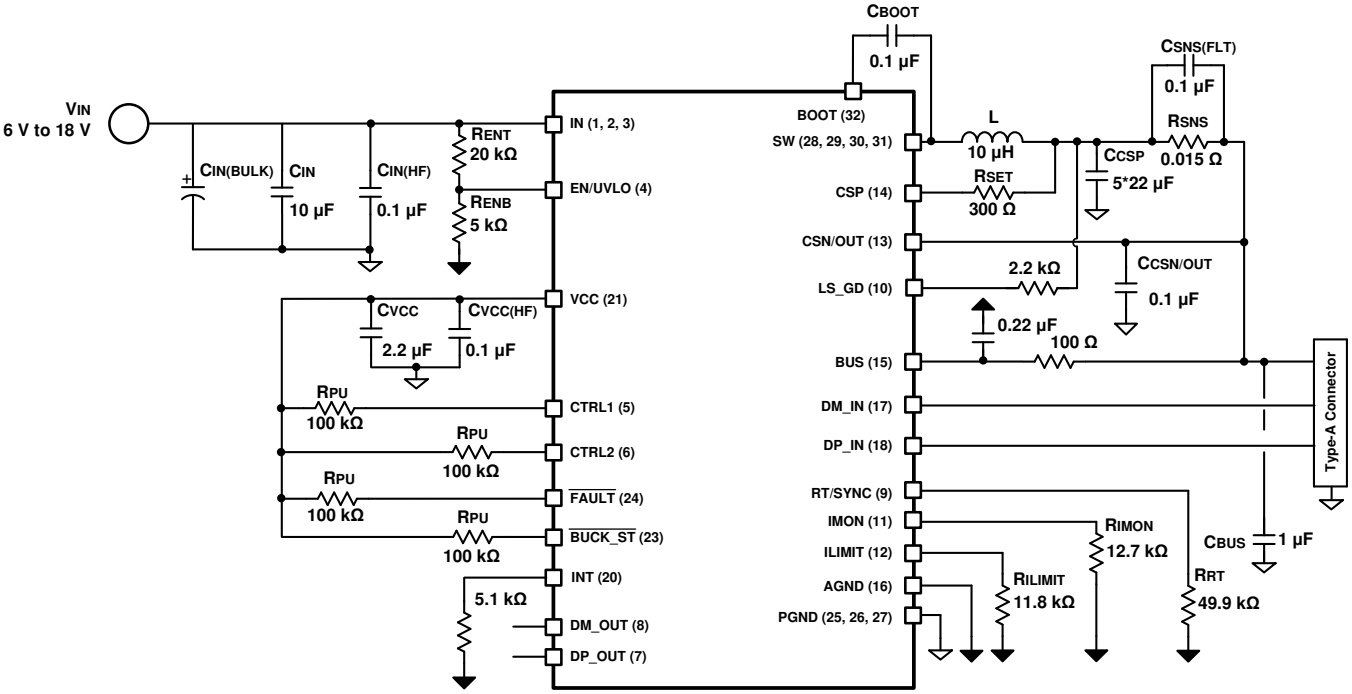


Figure 50. Application Circuit

The integrated buck regulator of TPS2584x-Q1 is internally compensated and optimized for a reasonable selection of external inductance and capacitance. The external components have to fulfill the needs of the application, but also the stability criteria of the device's control loop. Table 8 can be used to simplify the output filter component selection.

11.2.1 Design Requirements

To begin the design process, a few parameters must be known:

- Cable compensation: Total resistance including cable resistance, contact resistance of connectors, TPS2584x-Q1 current sense resistor and external NFET $r_{DS(on)}$ (if used). Refer to Figure 47 for examples of resistance in an automotive application.
- The maximum continuous output current for the charging port. The minimum current-limit setting of TPS2584x-Q1 device must be higher than this current.

Typical Application (continued)

For this example, use the parameters listed in Table 7 as the input parameters.

Table 7. Design Example Parameters

PARAMETER	VALUE
Input Voltage, V_{IN}	13.5-V typical, range from 6 V to 18 V
Output Voltage, V_{OUT}	5.1 V
Maximum Output Current $I_{OUT(MAX)}$	3.0 A
Transient Response 0.3 A to 3 A	5%
Output Voltage Ripple	50 mV
Input Voltage Ripple	400 mV
Switching Frequency f_{SW}	400 kHz
Cable Resistance for Cable Compensation	300 mΩ
Current Limit by Buck Average	3.3 A

Table 8. L, and C_{OUT} Typical Values

f_{SW}	V_{OUT} without Cable Compensation	C_{IN} + C_{HF}	L	Current Limit	C_{CSP}	$C_{CSN/OUT}$	C_{BUS}
400 kHz	5.10 V	1 x 10 µF + 1 x 100 nF	10 µH	Buck Avg	5 x 22 µF	100 nF	1 to 4.7 µF
400 kHz	5.10 V	1 x 10 µF + 1 x 100 nF	10 µH	Ext. NFET	5 x 22 µF	100 nF	1 to 4.7 µF
2100 kHz	5.10 V	1 x 10 µF + 1 x 100 nF	2.2 µH	Buck Avg	2 x 22 µF	100 nF	1 to 4.7 µF

1. Inductance value is calculated based on V_{IN} = 18 V.
2. All the C_{OUT} values are after derating.

11.2.2 Detailed Design Procedure

11.2.2.1 Output Voltage

The output voltage of TPS2584x-Q1 is internally fixed at 5.10 V. Cable compensation can be used to increase the voltage on the CSN/OUT pin linearly with increasing load current. Refer to *Cable Compensation* for more details on output voltage variation versus load current. If cable compensation is not desired, use a 0-Ω R_{IMON} resistor.

11.2.2.2 Switching Frequency

The recommended switching frequency of the TPS2584x-Q1 is in the range of 300-400 kHz for best efficiency. Choose R_{RT} = 49.9 kΩ for 400 kHz operation. To choose a different switching frequency, refer to Table 1.

11.2.2.3 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current and the rated current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 10 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} should be 20% to 40%. During an instantaneous short or over current operation event, the RMS and peak inductor current can be high. The inductor current rating should be higher than the current limit of the device.

$$\Delta i_L = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times L \times f_{SW}} \quad (9)$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (10)$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that over current protection at the full load could be falsely triggered. It also generates more conduction loss and inductor core loss. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.3, the minimum inductor value is calculated to be 8.7 µH. Choose the nearest standard 10 µH ferrite inductor with a capability of 4 A RMS current and 6-A saturation current.

11.2.2.4 Output Capacitor Selection

The value of the output capacitor, and its ESR, determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. Equation 11 can be used to estimate a lower bound on the total output capacitance, and an upper bound on the ESR, required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[1+K+\frac{K^2}{12} \cdot \left(1+\frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = Ripple factor from *Inductor Selection* (11)

Once the output capacitor and ESR have been calculated, Equation 12 can be used to check the peak-to-peak output voltage ripple; V_r.

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}} \quad (12)$$

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

For this example we require a ΔV_{OUT} of ≤ 250 mV for an output current step of ΔI_{OUT} = 2.7 A. Equation 11 gives a minimum value of 86 µF and a maximum ESR of 0.08 Ω. Assuming a 20% tolerance and a 10% bias de-rating, we arrive at a minimum capacitance of 110 µF. This can be achieved with a bank of 5 × 22-µF, 10-V, ceramic capacitors in the 1210 case size. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases an aluminum electrolytic capacitor can be placed in parallel with the ceramics to help build up the required value of capacitance.

In practice the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and Bode plots are the best way to validate any given design and should always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help to reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing voltage spikes on the output caused by inductor and board parasitics.

The maximum value of total output capacitance should be limited to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

11.2.2.5 Input Capacitor Selection

The TPS2584x-Q1 device requires high frequency input decoupling capacitor(s) and a bulk input capacitor, depending on the application. A high-quality ceramic capacitor type X5R or X7R with sufficient voltage ratings are recommended. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. The bulk capacitance selection depends upon a number of factors: long leads from the automotive battery to the IN pin of TPS2584x-Q1, cold or warm engine crank requirements and so forth. The bulk capacitor is used to dampen voltage spike due to the lead inductance of the cable or the trace. For this design, one 10 µF, 50 V, X7R ceramic capacitors are used. A 0.1 µF for high-frequency filtering and place it as close as possible to the device pins. Consider adding additional bulk capacitance for operation through low V_{IN} warm-crank profiles is required by the vehicle OEM.

11.2.2.6 Bootstrap Capacitor Selection

Every TPS2584x-Q1 design requires a bootstrap capacitor (C_{BOOT}). The recommended capacitor is 0.1 µF and rated 10 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

11.2.2.7 VCC Capacitor Selection

The VCC pin is the output of an internal LDO for TPS2584x. The LDO supplies gate charge to the LS buck switch and is the supply to the digital state-machine and analog USB circuitry. To insure stability of the device, place a minimum of 2.2 µF, 10 V, X7R capacitor from this pin to ground. In addition a 0.1 µF high frequency decoupling capacitor is highly recommended.

11.2.2.8 Enable and Under Voltage Lockout Set-Point

The system enable and undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The EN/UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. The following equations can be used to determine the $V_{IN(ON)}$ and $V_{IN(OFF)}$ levels.

$$R_{ENT} = \left(\frac{V_{IN(ON)}}{V_{EN/UVLO\_H}} - 1\right) \times R_{ENB} \tag{13}$$

$$V_{IN(OFF)} = V_{IN(ON)} \times \left(1 - \frac{V_{EN/UVLO\_HYS}}{V_{EN/UVLO\_H}}\right) \tag{14}$$

$V_{IN(ON)}$ = 6 V (user choice)

R_{ENB} = 5 kΩ (user choice)

R_{ENT} = [($V_{IN(ON)}$ / ($V_{EN/UVLO\_H}$) – 1] × R_{ENB}

R_{ENB} = [(6 V / 1.2 V) - 1] x 5 kΩ = 20 kΩ. Choose standard 20 kΩ.

Therefore $V_{IN(OFF)}$ = 6 V × [1 - (0.09 V / 1.2 V)] = 5.55 V

11.2.2.9 Current Limit Set-Point

The TPS2584x-Q1 provides an accurate current limit to protect the USB port from overload based upon the values of R_{SNS}, R_{SET} and R_{ILIMIT}. The design process is the same regardless of whether buck average current limiting or external NFET current limiting is chosen. The only difference is the current limit threshold voltage on the ILIMIT pin.

- R_{SNS} is the current sense resistor. The recommended voltage across R_{SNS} under current limit should be approximately 50 mV as a compromise between accuracy and power dissipation. For example, if current limiting is desired for $I_{OUT(MAX)}$ ≥ 3.3 A, then R_{SNS} = 0.05 V / 3.3 A = 0.01515 Ω. Choose a standard value of

15 mΩ.

- R_{SET} determines the input current to the transconductance amplifier and current mirror. The amplifier balances the voltage to be equal to that across R_{SNS}. Choose a R_{SET} value to produce an I_{SET} current between 75 - 180 µA at the desired $I_{OUT(MAX)}$. Considering 50 mV across R_{SET}, a value of 300 Ω will provide approximately 166 µA of I_{SET} current to the amplifier and mirror circuit. Care should be taken to limit the I_{SET} current below 200 µA to avoid saturating the internal amplifier circuit.
- Buck average current limiting occurs when V_{ILIMIT} = 1 V. R_{ILIMIT} is calculated as 1 V x 300 Ω / [0.5 x (3.3 A x 15 mΩ + 0.7 mV)] = 11.95 kΩ. A standard 11.8 kΩ value is chosen.

11.2.2.10 Cable Compensation Set-Point

From Table 7 the total cable resistance to be accounted for is 300 mΩ.

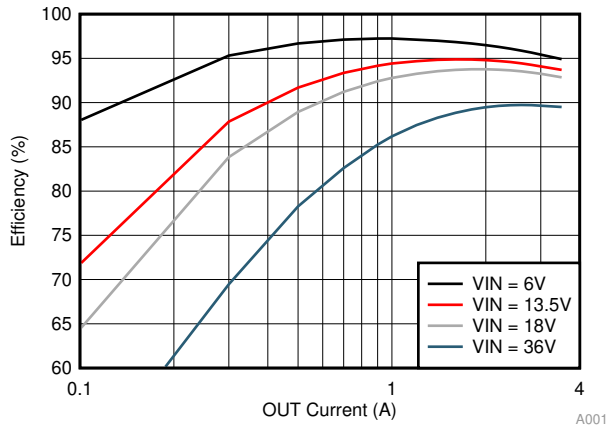
1. From *Current Limit Set-Point* R_{SNS} and R_{SET} have been determined as 15 mΩ and 300 Ω, respectively.
2. R_{WIRE} = 300 mΩ
3. $\Delta V_{OUT} = (R_{SNS} + R_{WIRE}) \times I_{BUS} = (0.015 + 0.3) \times 3 = 1.0395$ V
4. $R_{IMON} = (\Delta V_{OUT} \times R_{SET} \times 2) / (I_{BUS} \times R_{SNS}) = (1.0395 \times 300 \times 2) / (3.3 \times 0.015) = 12.6$ kΩ. A standard value of 12.7 kΩ is selected.

11.2.2.11 $\overline{FAULT}$ Resistor Selection

The $\overline{FAULT}$ pins are open-drain output flags. They can be connected to the TPS2584x-Q1 VCC pin with 100 kΩ resistors, or connected to another suitable I/O voltage supply if actively monitored by a USB HUB or MCU. They can be left floating if unused.

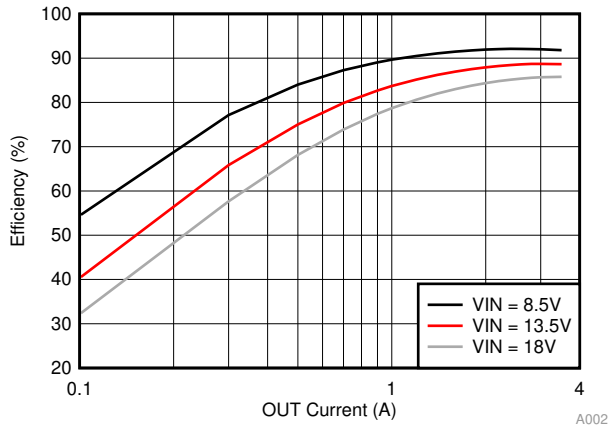
11.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.



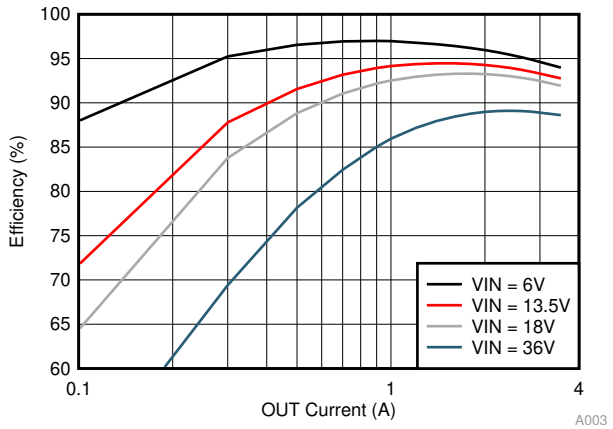
V_{OUT} = 5.1 V f_{SW} = 400 kHz

Figure 51. Buck Only Efficiency



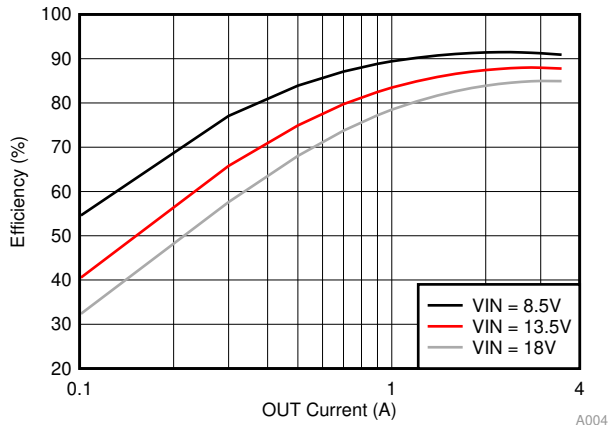
V_{OUT} = 5.1 V f_{SW} = 2100 kHz

Figure 52. Buck Only Efficiency



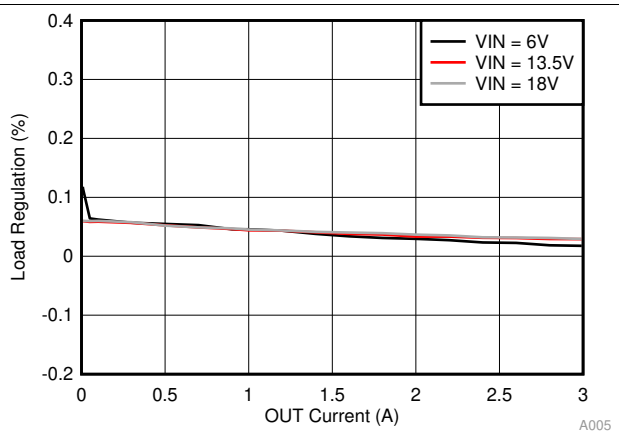
V_{OUT} = 5.1 V f_{SW} = 400 kHz R_{SENS} = 15 mΩ

Figure 53. Efficiency With Sense Resistor



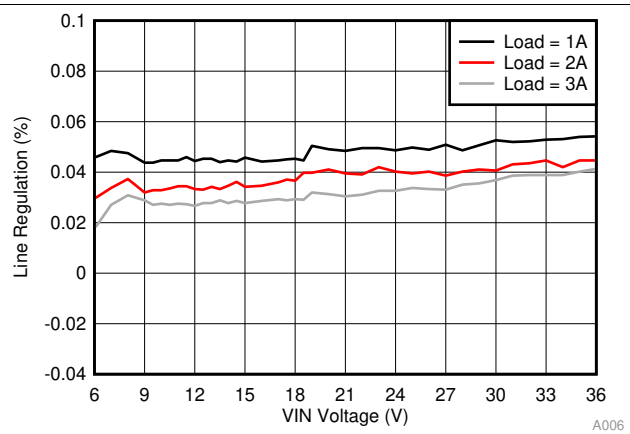
V_{OUT} = 5.1 V f_{SW} = 2100 kHz R_{SENS} = 15 mΩ

Figure 54. Efficiency With Sense Resistor



V_{OUT} = 5.1 V f_{SW} = 400 kHz

Figure 55. Load Regulation



V_{OUT} = 5.1 V f_{SW} = 400 kHz

Figure 56. Line Regulation

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

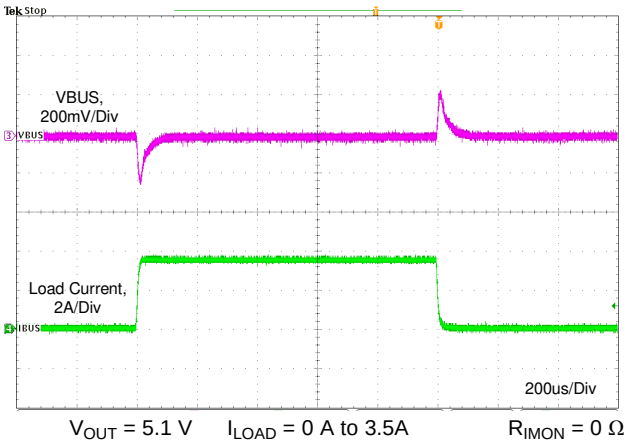


Figure 57. Load Transient Without Cable Compensation

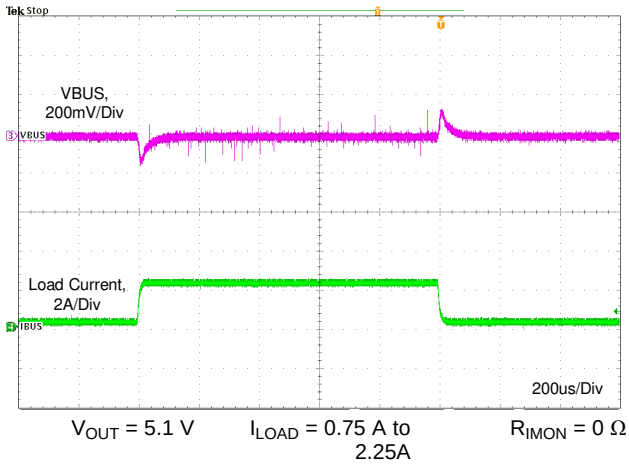


Figure 58. Load Transient Without Cable Compensation

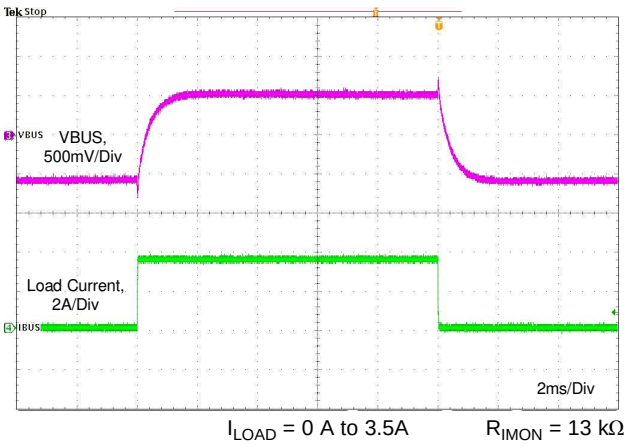


Figure 59. Load Transient With Cable Compensation

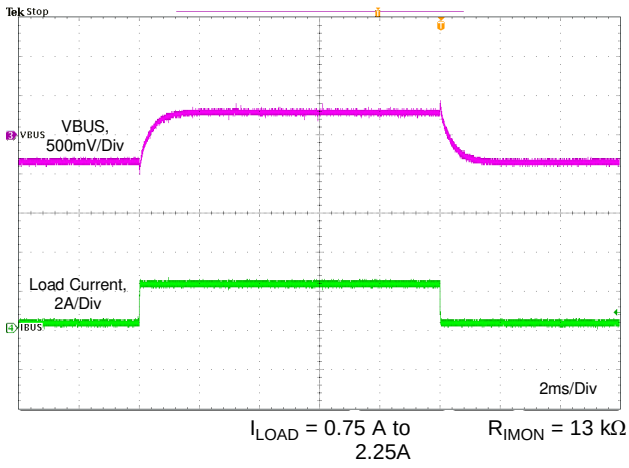


Figure 60. Load Transient With Cable Compensation

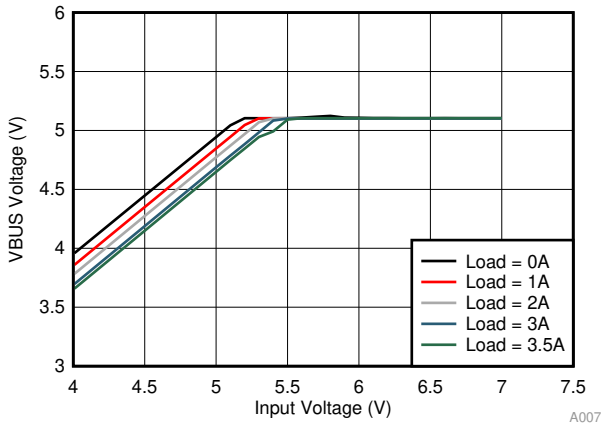


Figure 61. Dropout Characteristic

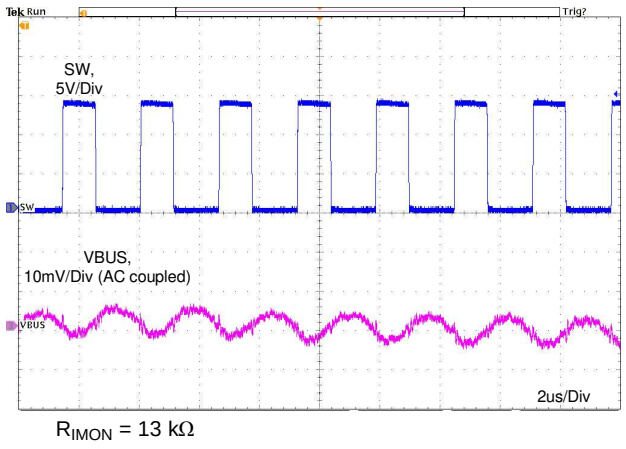


Figure 62. 3.5-A Output Ripple

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

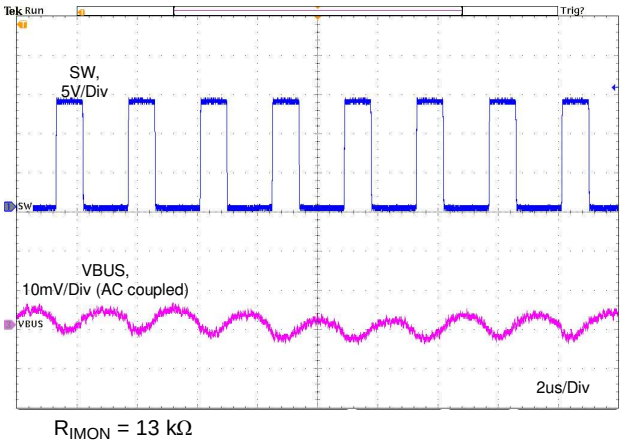


Figure 63. 100-mA Output Ripple

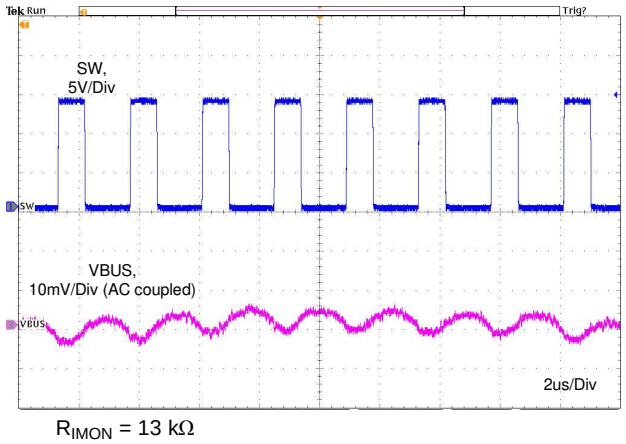


Figure 64. No Load Output Ripple

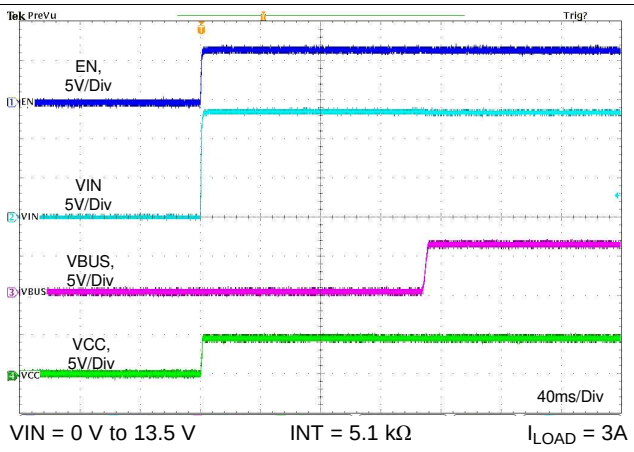


Figure 65. Startup Relate to VIN

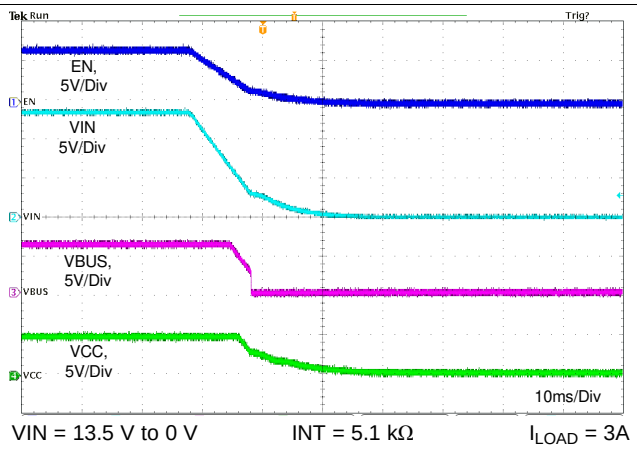


Figure 66. Shutdown Relate to VIN

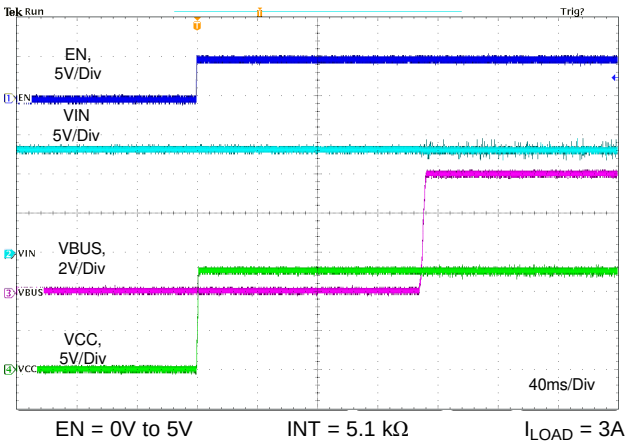


Figure 67. Startup Relate to EN

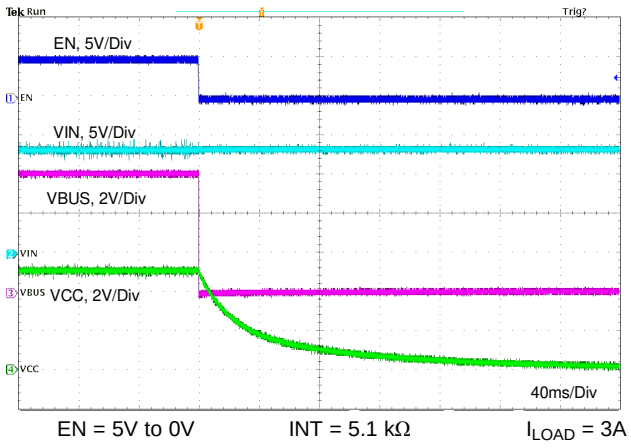


Figure 68. Shutdown Relate to EN

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

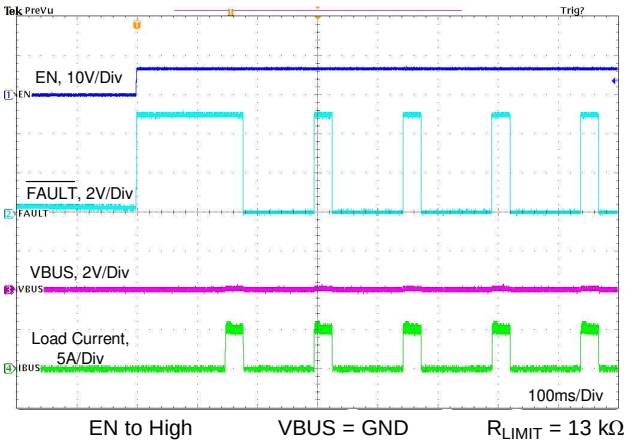


Figure 69. Enable into Short Without External FET

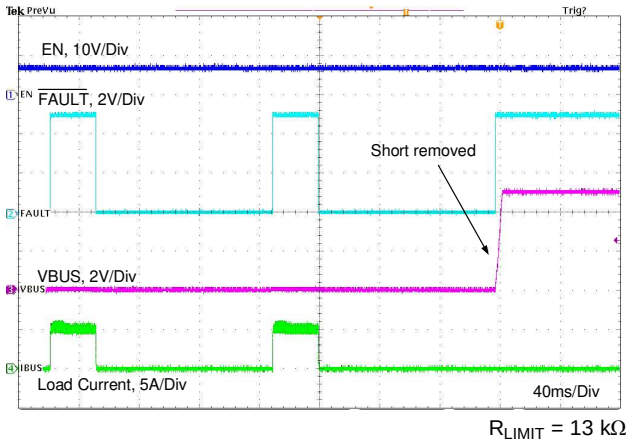


Figure 70. Short Circuit Recovery Without External FET

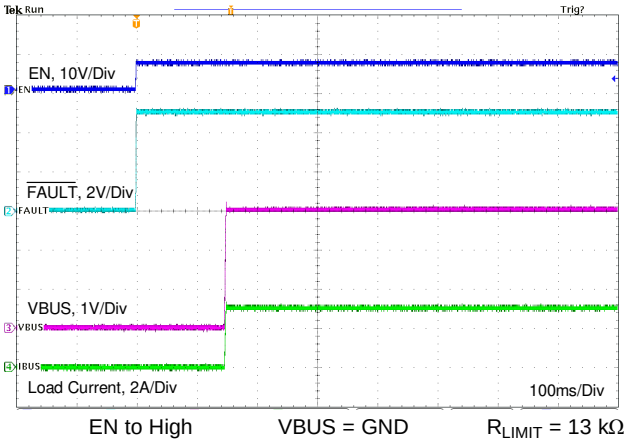


Figure 71. Enable Into 1-Ω Load Without External FET

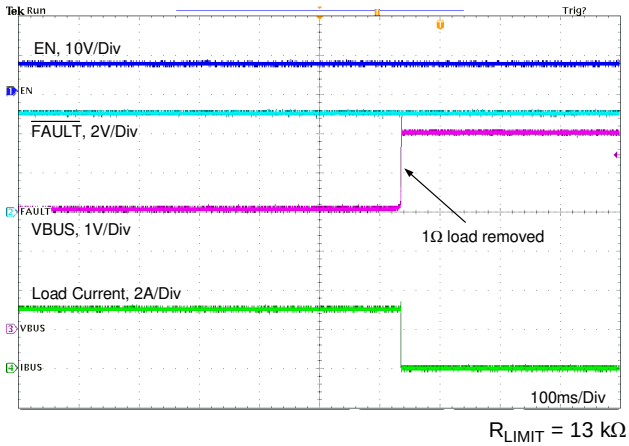


Figure 72. 1-Ω Load Recovery Without External FET

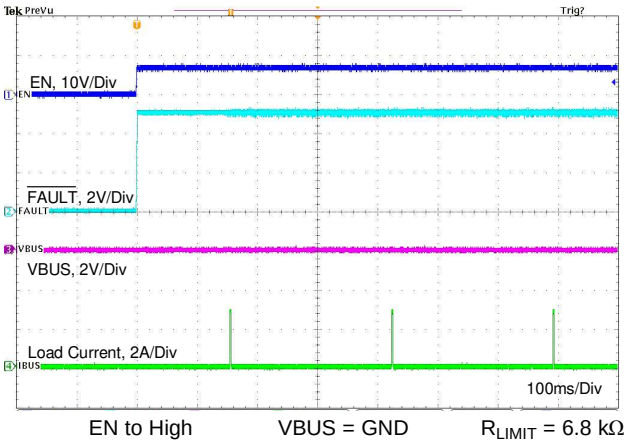


Figure 73. Enable Into Short With External FET

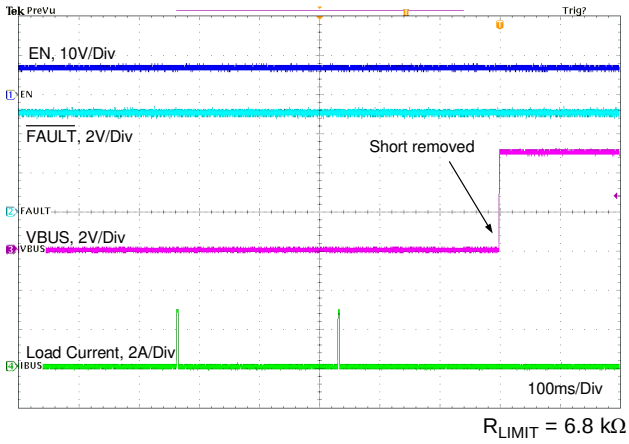


Figure 74. Short Circuit Recovery With External FET

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 10 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

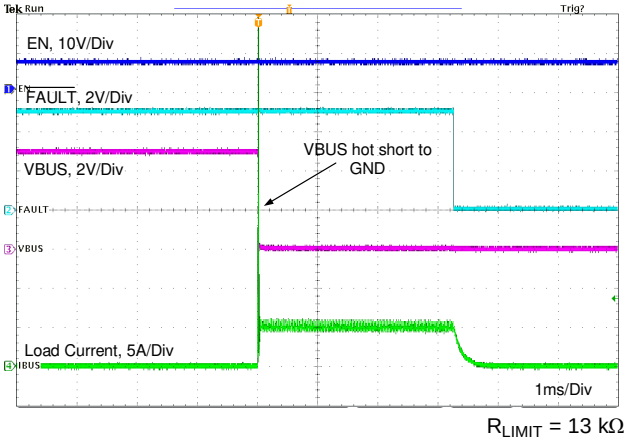


Figure 75. VBUS Hot Short to GND Without External FET

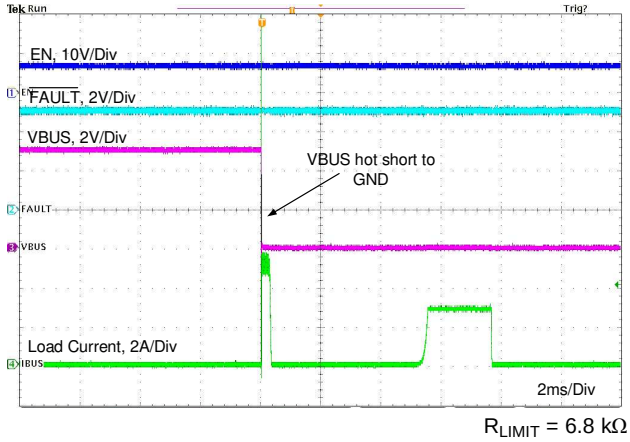


Figure 76. VBUS Hot Short to GND With External FET

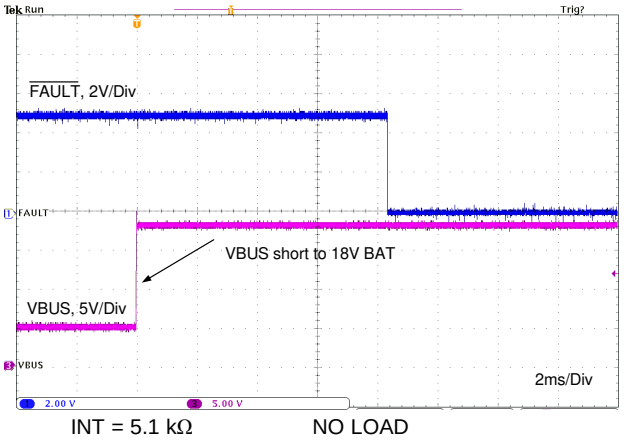


Figure 77. VBUS Short to BAT With External FET

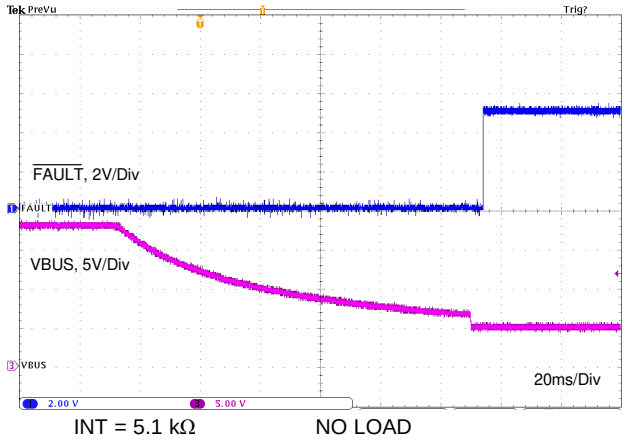


Figure 78. VBUS Short to BAT Recovery With External FET

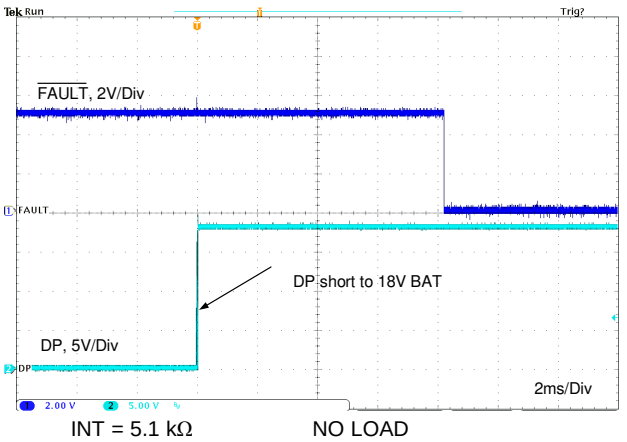


Figure 79. DP Short to BAT

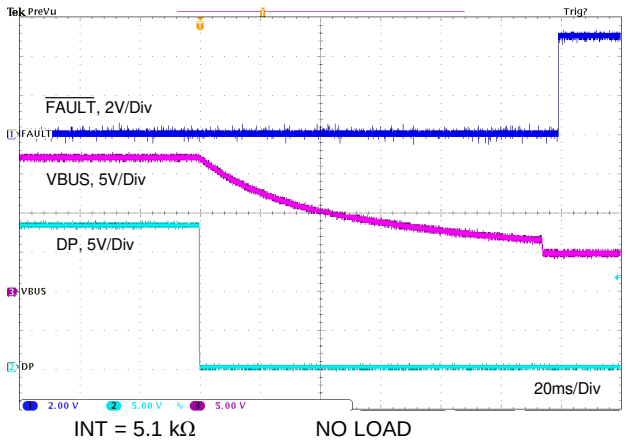


Figure 80. DP Short to BAT Recovery

12 Power Supply Recommendations

The TPS2584x-Q1 is designed to operate from an input voltage supply range between 6 V and 36 V. This input supply should be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the TPS2584x-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the TPS2584x-Q1, additional bulk capacitance may be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47 μF or 100 μF electrolytic capacitor is a typical choice.

13 Layout

13.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI. For more detailed EMC design consideration and test report, please see PCB Layout and Parameters Recommendation for TPS2583X EMC Performance

1. ***Input capacitor:*** The input bypass capacitor C_{IN} must be placed as close as possible to the IN and PGND pins. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the PGND pin and PAD. A combination of different values and packages of capacitors can help improve the EMC performance (for example: 10μF + 0.1 μF + 2.2nF). Besides, the distance between the input filter section and the output power section must be at least 15mm to prevent the output high-frequency signal from coupling into the input filter. A 10-μF cap cross V_{IN} and PGND pin on top of SW is suggested for TPS2584x-Q1.
2. ***V_{CC} bypass capacitor:*** Place bypass capacitors for V_{CC} close to the VCC pin and ground the bypass capacitor to device ground.
3. Use a ground plane in one of the middle layers as noise shielding and heat dissipation path.
4. Connect the thermal pad to the ground plane. The QFN package has a thermal pad (PAD) connection that must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection. The integrity of this solder connection has a direct bearing on the total effective $R_{\theta JA}$ of the application.
5. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
6. Provide enough PCB area for proper heat sinking. As stated in the section, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. Use an array of heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
7. The SW pin connecting to the inductor should be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) will bring a high current conduction capacity to minimize parasitic resistance, but it will also cause a larger parasitic capacitance. Thus a balance should be found between smaller parasitic resistance and larger parasitic capacitance. And the current path should be kept straight forward to the inductor, otherwise the L-shaped or T-shaped path will make a sudden change of the impedance which causes signal reflection and impacts the performance of EMC. The output capacitors should be placed close to the V_{OUT} end of the inductor and closely grounded to PGND pin and exposed PAD. Besides, do not punch vias on SW lines. Using shielded inductors or molded inductors to reduce high-frequency radiation.
8. ***Sense and Set Resistors:*** The R_{SNS} and R_{SET} resistors connect to the current sense amplifier inputs at the CSP and CSN/OUT pins. For best current limit and cable compensation accuracy; short, parallel traces give the best performance. If it is not possible to place R_{SNS} and R_{SET} near the CSP and CSN/OUT pins, it is recommended that the traces from sense resistor be routed in parallel and of similar lengths. A small filter capacitor in parallel with R_{SNS} and a small filter capacitor from CSN/OUT to AGND help decouple noise.
9. R_{ILIMIT} and R_{IMON} resistors should be placed as close as possible to the ILIMIT and IMON pins and connected to AGND. If needed, these components can be placed on the bottom side of the PCB with signals routed through small vias.

Layout Guidelines (continued)

10. Trace routing of DP_IN, DM_IN, DP_OUT, and DM_OUT: Route these traces as micro-strips with nominal differential impedance of 90 Ω. Minimize the use of vias in the high-speed data lines. Keep the reference GND plane devoid from cuts or splits above the differential pairs to prevent impedance discontinuities.
11. $\overline{\text{FAULT}}$ are open-drain outputs. They can be connected to the VCC pin via pull-up resistors. Suggested resistor value is 100 kΩ.
12. The area enclosed by current loop of input side and output side should be as small as possible; the area enclosed by the BOOT circuit should be as small as possible.
13. Power ground PGND and the signal ground AGND should be separated in the actual PCB layout.

13.2 Ground Plane and Thermal Considerations

It is recommended to use one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The PGND pins should be connected to the ground plane using vias right next to the bypass capacitors. PGND pin is connected to the source of the internal LS switch. The PGND net contains noise at switching frequency and may bounce due to load variations. PGND trace, as well as VIN and SW traces, should be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and should be used for sensitive routes. AGND and PGND should be connected under the QFN package PAD.

It is recommended to provide adequate device heat sinking by utilizing the PAD of the IC as the primary thermal path. Use a minimum 2 row, 2 column "+" array of 12 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias should be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top of, 2 oz / 1 oz / 1 oz / 2 oz. Four layer boards with enough copper thickness provide low current conduction impedance, proper shielding and lower thermal resistance.

The thermal characteristics of the TPS2584x-Q1 are specified using the parameter θ_{JA}, which characterize the junction temperature of silicon to the ambient temperature in a specific system. Although the value of θ_{JA} is dependent on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \times \theta_{JA} + T_A \quad (15)$$

where

T_J = Junction temperature in °C

$P_D = V_{IN} \times I_{IN} \times (1 - \text{Efficiency}) - 1.1 \times I_{OUT}^2 \times \text{DCR}$ in Watt

DCR = Inductor DC parasitic resistance in Ω

θ_{JA} = Junction to ambient thermal resistance of the device in °C/W

T_A = Ambient temperature in °C

θ_{JA} is highly related to PCB size and layout, as well as environmental factors such as heat sinking and air flow.

13.3 Layout Example

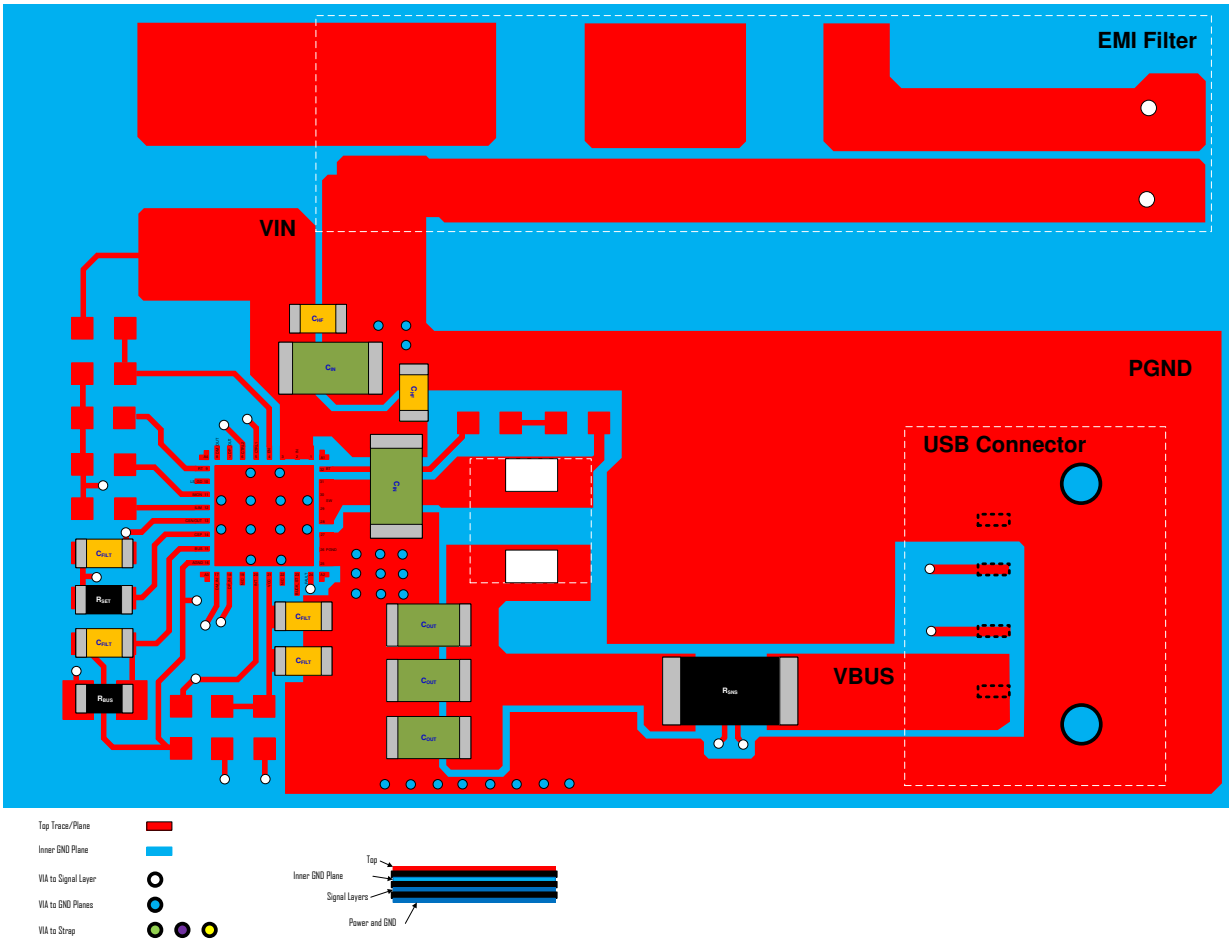


Figure 81. Layout Example

14 Device and Documentation Support

14.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 9. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS25840-Q1	Click here	Click here	Click here	Click here	Click here
TPS25842-Q1	Click here	Click here	Click here	Click here	Click here

14.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

14.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25840QWRHBRQ1	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	T25840	Samples
TPS25840QWRHBTQ1	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	T25840	Samples
TPS25842QWRHBRQ1	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	T25842	Samples
TPS25842QWRHBTQ1	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	T25842	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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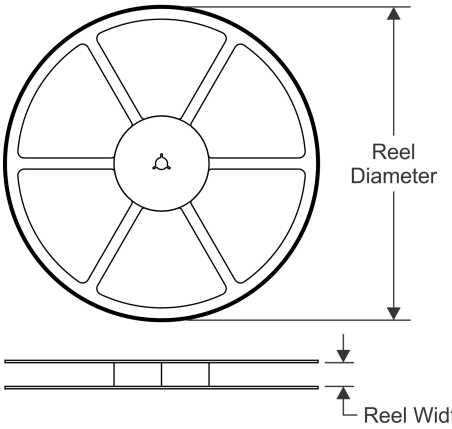
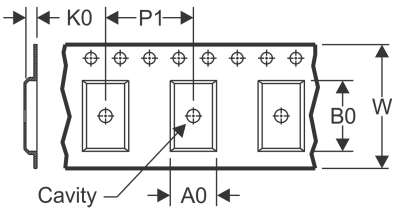
TAPE AND REEL INFORMATION

REEL DIMENSIONS

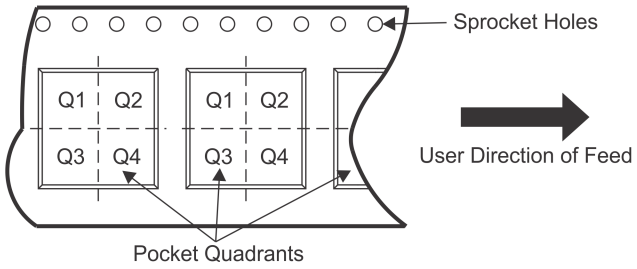


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

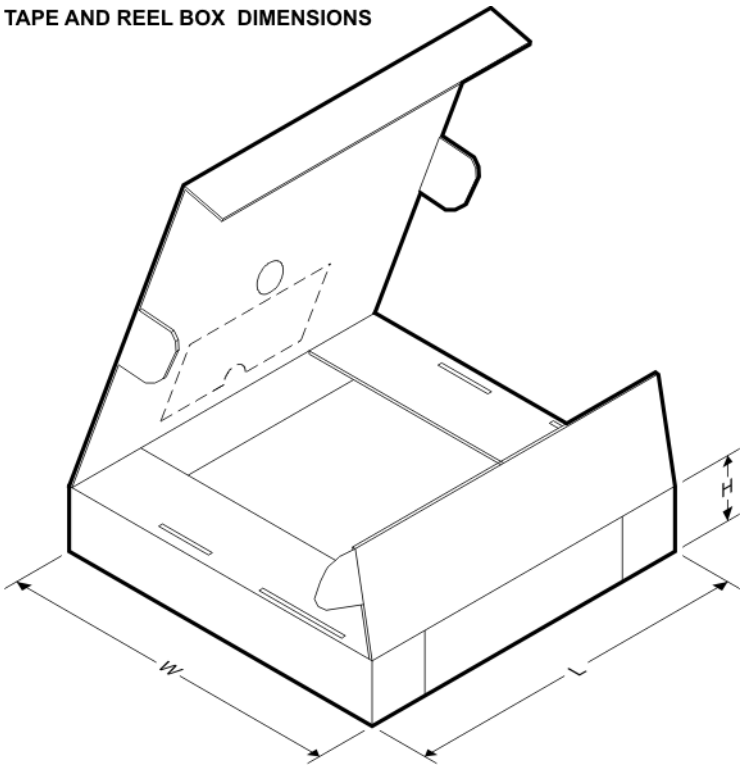
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25840QWRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS25840QWRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS25842QWRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS25842QWRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25840QWRHBRQ1	VQFN	RHB	32	3000	370.0	355.0	55.0
TPS25840QWRHBTQ1	VQFN	RHB	32	250	195.0	200.0	45.0
TPS25842QWRHBRQ1	VQFN	RHB	32	3000	370.0	355.0	55.0
TPS25842QWRHBTQ1	VQFN	RHB	32	250	195.0	200.0	45.0

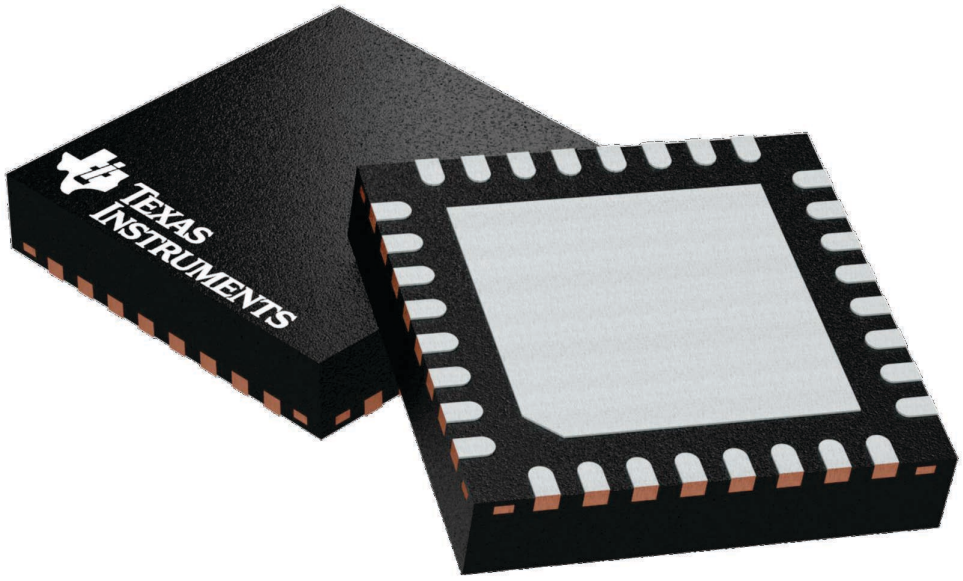
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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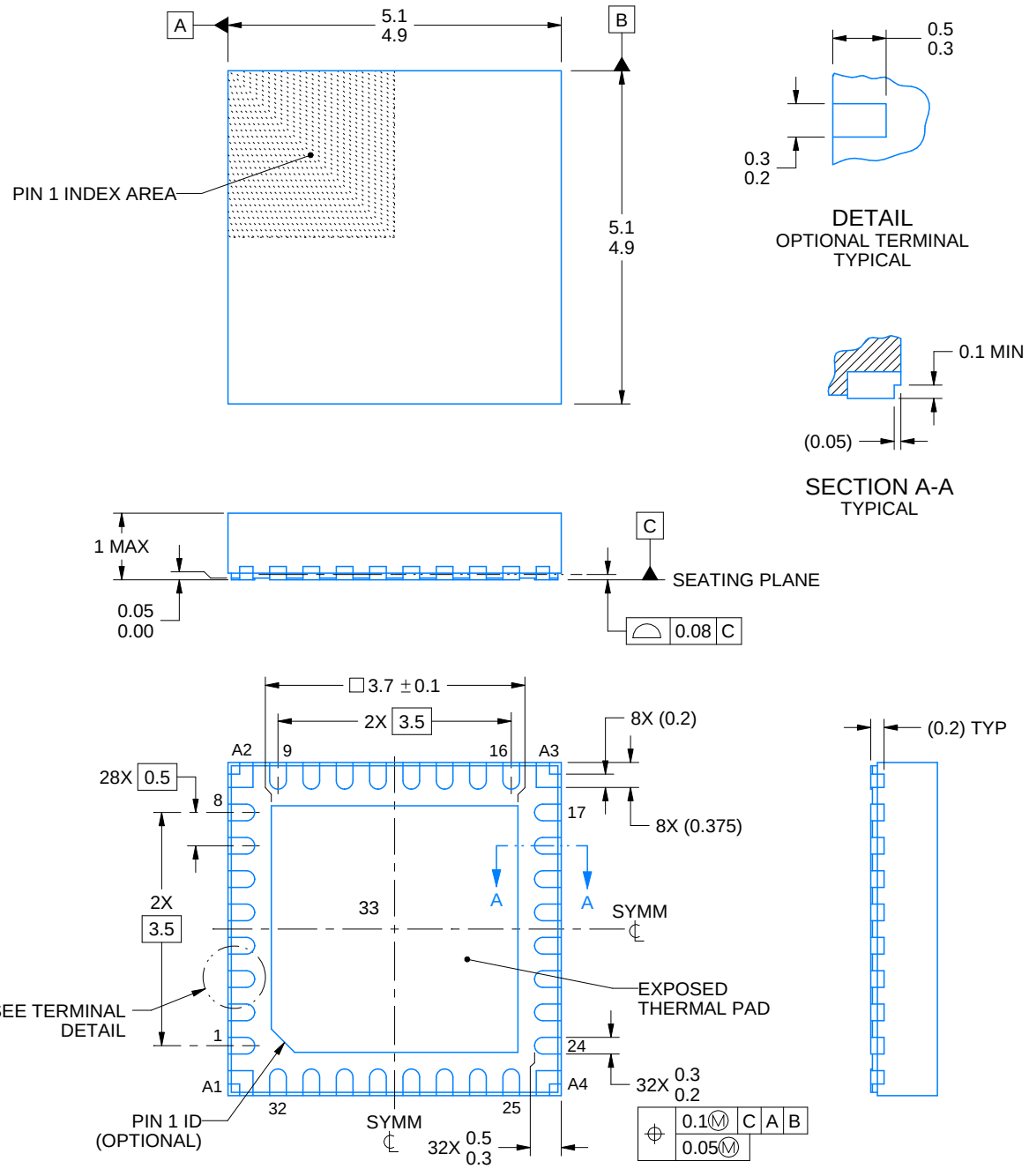
PACKAGE OUTLINE

RHB0032R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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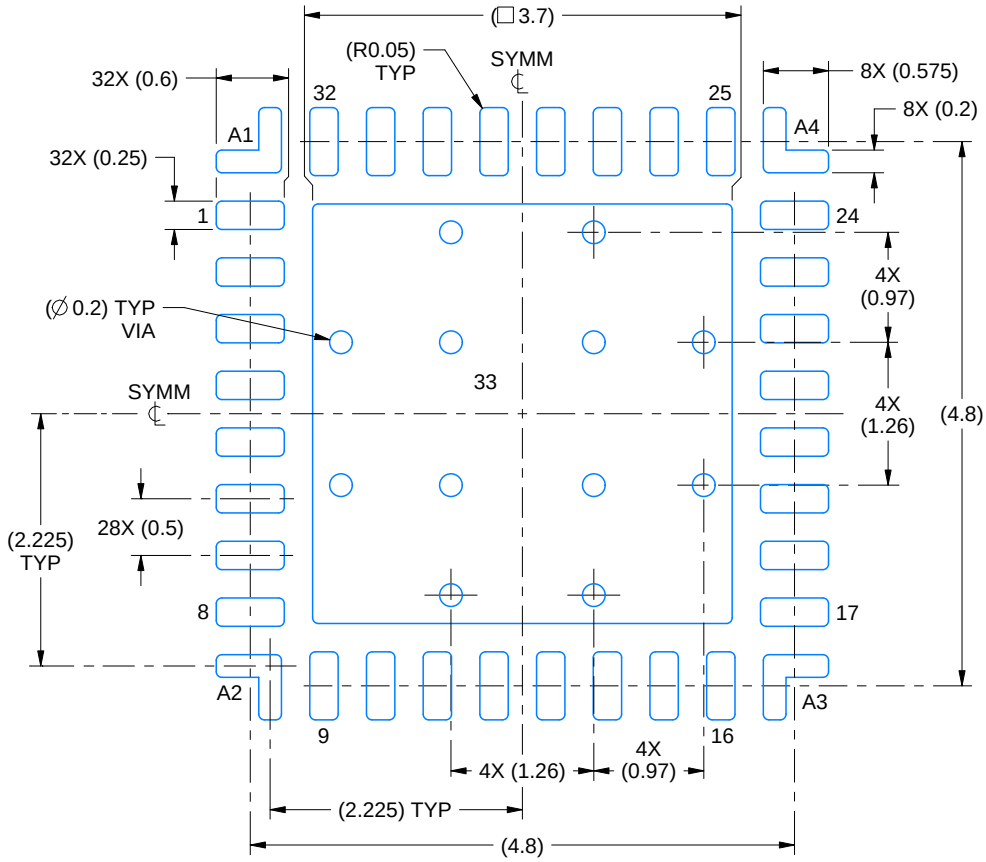
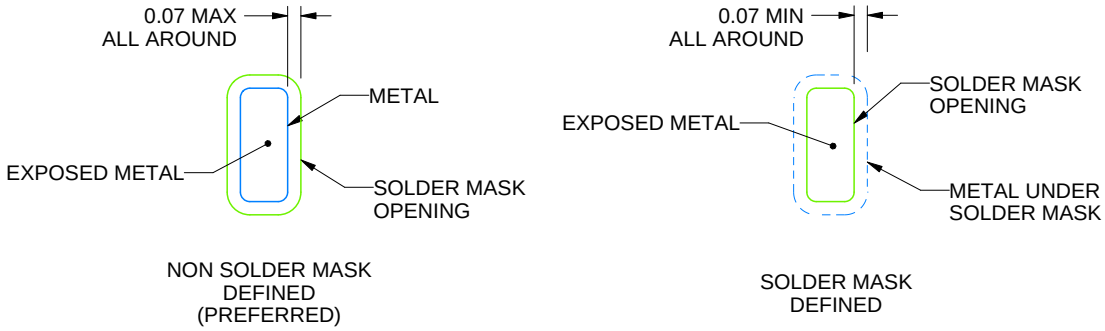
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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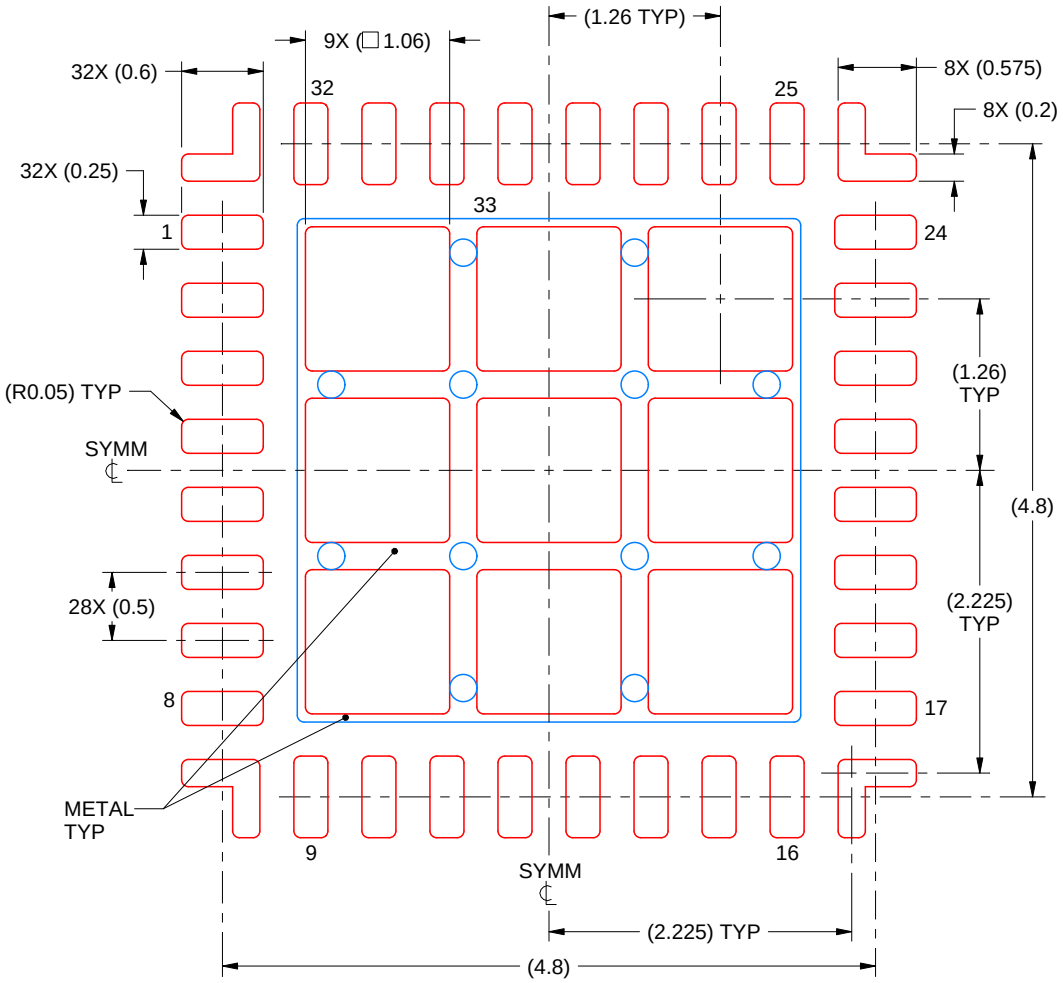
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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