

Wide Operating Range, Valley Mode,
No R_{SENSE}^{TM} Synchronous Step-Down Controller

DESCRIPTION

Demonstration circuit 947 is a Wide Operating Range, Valley Mode, No R_{SENSE}^{TM} Synchronous Step-Down Controller featuring the LT3740EDHC. It produces 1.8VDC for loads up to 10A from an input range of 3-15VDC, switching at a fixed frequency of 300KHz.

In order to operate from an input voltage as low as 3V, the circuit must provide adequate voltage to drive the external power MOSFETs. To this end, the LT3740 includes an on-chip step-up converter to provide a bias about 7V above the input voltage to power the top MOSFET gate driver. The stock configuration of DC947 also uses this bias to power the bottom gate drive circuit, but pads have been added to the circuit board to power the bottom gate drive from another source.

The LT3740 is equipped with an external reference input that allows the user to override the 0.8V internal reference with any lower value, allowing full

control of the output voltage during operation, output voltage tracking or soft-start.

In addition, the LT3740 has three current limit levels that can be chosen by connecting the RANGE pin to ground, leaving it open circuit, or tying to the input.

DC947 is equipped with jumpers that allow the user to select among soft-start options and reference voltage sources. Unpopulated pads have been added to DC947 in order to facilitate input voltages higher than 15V and No R_{SENSE}^{TM} operation.

**Design files for this circuit board are available.
Call the LTC factory.**

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PERFORMANCE SUMMARY Specifications are at $T_A = 25^{\circ}\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Range		3.0		15.0	V
V_{OUT}	Output Voltage Range	$V_{IN} = 3.0 - 15.0\text{V}$, $I_{LOAD} = 0-10\text{A}$	1.76		1.84	V
I_{OUT}	Output current	$V_{IN} = 3.0 - 15.0\text{V}$, $V_{OUT} = 1.8\text{V}$	0		10.0	A
V_{RIPPLE}	Output Ripple	$V_{IN} = 3.0 - 15.0\text{V}$, $I_{LOAD} = 0-10\text{A}$			20	mV

QUICK START PROCEDURE

Demonstration circuit 947 is easy to set up to evaluate the performance of the LT3740EDHC.

Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

LT3740EDHC

NOTE. When measuring the output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the Vin or Vout and GND terminals. See Figure 2 for proper scope probe technique.

1. Place jumpers in the following positions:

JP1 Up (Internal Reference)

JP2 Up (Voltage_SS ON)

JP3 Down (Current_SS ON)

2. With power off, connect the input power supply to Vin and GND.

3. Connect the 0-10A load.

4. Turn on the power at the input. Make sure that the input voltage is between 3 and 15V.

NOTE. Make sure that the input voltage does not exceed 15V.

5. Check for the proper output voltages. Vout should be 1.8V, nominal. If there is no output, temporarily disconnect the load to make sure that the load is not set too high.

6. Once the proper output voltages are established, adjust the loads within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

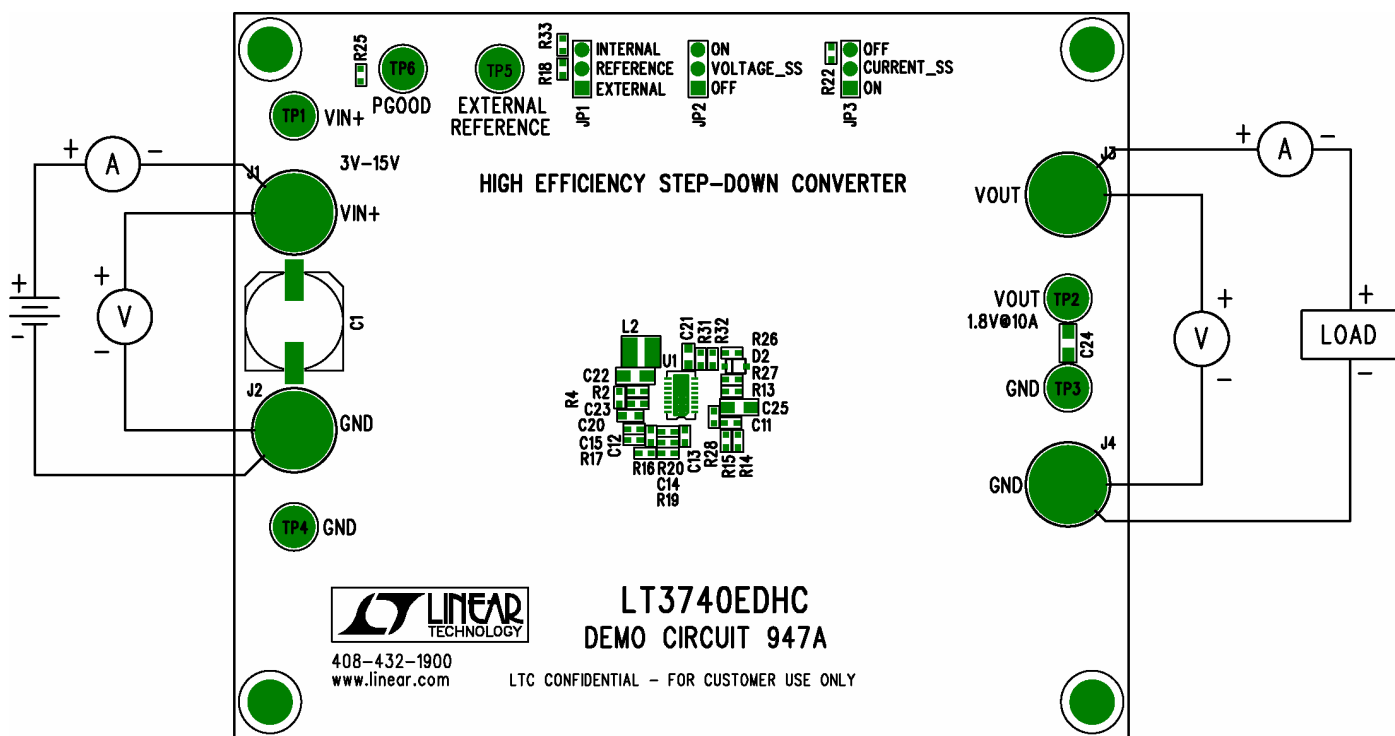


Figure 1. Proper Measurement Equipment Setup

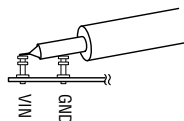


Figure 2. Measuring Input/Output Ripple

OPERATION

The LT3740 is a current-mode synchronous buck controller that can accept input voltages as low as 2.2V, and as high as 22V, but still provides at least 7V for the MOSFET gate drives through an internal boost regulator. It is equipped for No Rsense™ operation to maximize efficiency and features three user selectable current limit ranges and a flexible soft-start system capable of output tracking.

To close the current loop, the LT3740 reads the switching current through the bottom MOSFET “on” resistance. The chip features three user selectable current limit thresholds to optimize efficiency: 45mV, 75mV and 105mV. DC947 uses the middle setting, but unpopulated pads are available for selecting the other two settings.

In the interest of making the board able to handle a wide variety of input and output voltage combinations, DC947 does not use the No Rsense™ feature, but has been configured so that it is easy to do so. This is accomplished by shorting out the R1 sense resistor and moving the zero ohm resistor at location R14 to location R13. Change R28 to 1 ohm. Other component changes unique to the desired output voltage, input voltage range and frequency compensation may be necessary.

DC947 is configured such that the bottom gate drive power (BGDP) pin is connected directly to the output of the on-chip boost regulator (BIAS) through R32. This is what allows the circuit to provide sufficient power MOSFET gate drive when the input is as low as 3V.

If the design is not required to operate at input voltages below 7V, the BGDP pin can be tied to Vin to reduce the loading on the boost converter

and thus save power. To do this, move the zero ohm resistor at location R32 to R31 and add a 1uF ceramic capacitor at location C25. Also, implement the UVLO circuit by removing R30 and populating the circuitry made up of D3, Q3, and R29.

The LT3740 has an active high, open collector power good signal. On the demo board, it is pulled up to the 1.8V output through a 100K resistor, and can be conveniently read at TP6. Note that this pull-up voltage may not be compatible with all voltage systems. Please refer to the data sheet for a detailed description of the PGOOD signal.

A 0-0.8V external reference may be applied to the LT3740 at TP5. This is used to over-ride the internal 0.8V reference, giving control of the DC947 output voltage to an external signal source. Use of this function must first be enabled by setting JP1 (REFERENCE) to the EXTERNAL position. For further details about the external reference function, please refer to the XREF function described in the LT3740 data sheet.

JP2 (VOLTAGE_SS) and JP3 (CURRENT_SS) must both be set to their respective ON positions in order for the DC947 output to power up. If either of these jumpers is set to the OFF position, the output will not turn on. JP2 (VOLTAGE_SS) is associated with the XREF input, while JP3 (CURRENT_SS) ties into the SHDN input. For further details about the LT3740 soft-start operation, please refer to the data sheet.

On the DC947 demo board, the signals applied to both of the soft-start inputs are generated by simple RC circuits. The RC time constant of the CURRENT_SS soft-start is much longer than that of the VOLTAGE_SS, so the CURRENT_SS will

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dominate the behavior of the demo board output. To observe the behavior of the output when under VOLTAGE_SS control, simply change the RC time constant of R18 and C15 to make it longer than that of R22 and C20. Make sure that JP1 is set to INTERNAL.

DC947A is equipped with many optional components to facilitate the implementation of many optional functions. A simplified schematic of essential components is shown in figure 3, while a full schematic of the board is given in at the end of this document.

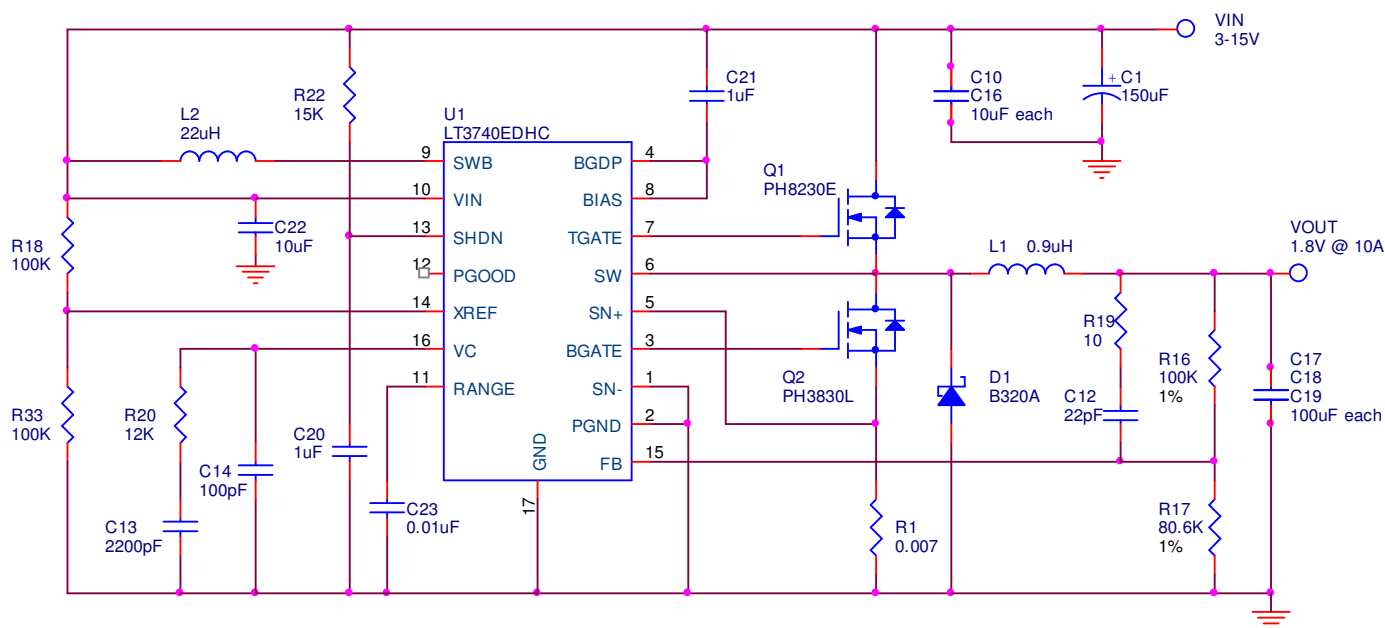
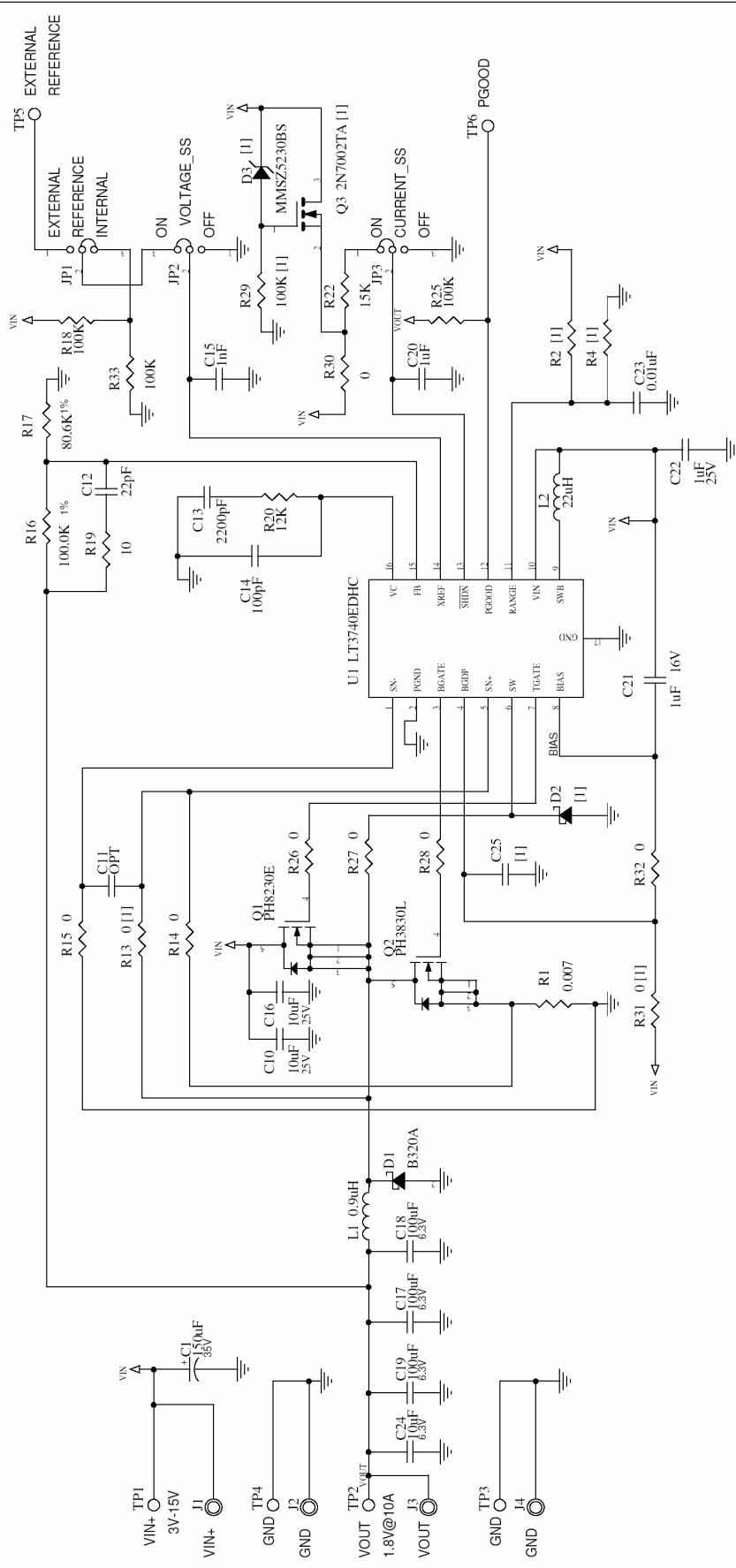


Figure 3. Simplified Schematic showing only essential components.

This circuit is proprietary to Linear Technology and supplied for use with Linear Technology parts.

Customer Notice: Linear Technology has made a best effort to design a circuit that meets customer-supplied specifications; however, it remains the customer's responsibility to verify proper and reliable operation in the actual application. Component substitution and printed circuit board layout may significantly affect circuit performance or reliability. Contact Linear Applications Engineering for assistance.

REVISION HISTORY			
ECO	REV	DESCRIPTION	DATE
	5	PROD	05/24/06



CONTRACT NO.		APPROVALS		DATE	
DRAWN MEI		CHECKED		07/19/05	
		APPROVED			
ENGINEER D. Ng		DESIGNER			
Wednesday, September 20, 2006		SCALE: NONE		FILENAME: 947A-5.DSN	
		SIZE		CAGE CODE	
		DWG NO		DC947A	
		REV		5	
		SHEET		1	
		OF		1	

NOTE: UNLESS OTHERWISE SPECIFIED, [1] OPTIONAL.

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LINEAR TECHNOLOGY

TITLE
SCH, LT3740EDHC, HIGH EFFICIENCY STEP-DOWN CONVERTER