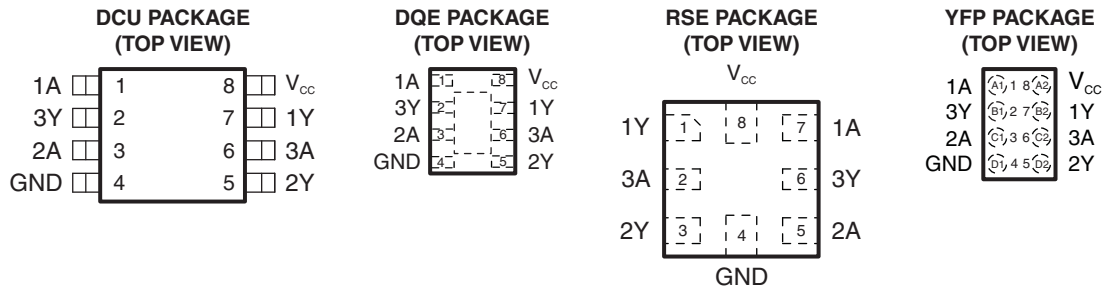


## LOW-POWER TRIPLE INVERTER GATE

Check for Samples: [SN74AUP3G04](#)

### FEATURES

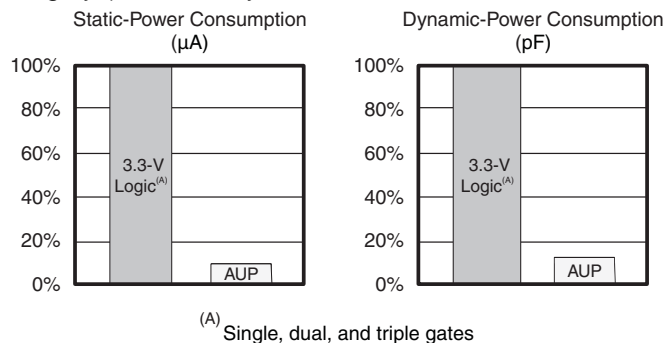
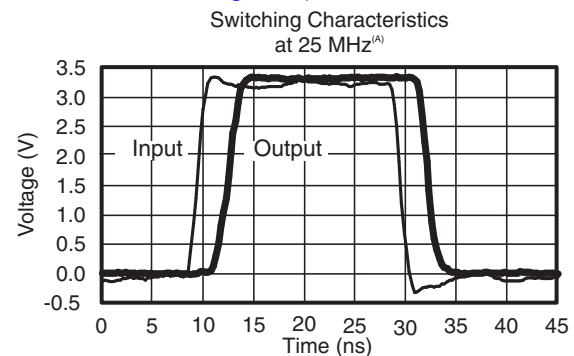
- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ( $I_{CC} = 0.9 \mu A$  Maximum)
- Low Dynamic-Power Consumption ( $C_{pd} = 4.3 \text{ pF Typ at } 3.3 \text{ V}$ )
- Low Input Capacitance ( $C_i = 1.5 \text{ pF Typical}$ )
- Low Noise – Overshoot and Undershoot <10% of  $V_{CC}$
- $I_{off}$  Supports Live Insertion, Partial PowerDown Mode, and Back Drive Protection
- Wide Operating  $V_{CC}$  Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.3 \text{ ns Maximum at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

### DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire  $V_{CC}$  range of 0.8 V to 3.6 V, resulting in increased battery life (see [Figure 1](#)). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in [Figure 2](#)).


**Figure 1. AUP – The Lowest-Power Family**

(A) SN74AUP3Gxx data at  $C_L = 15 \text{ pF}$ .

**Figure 2. Excellent Signal Integrity**


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

The SN74AUP3G04 performs the Boolean function  $Y = A$  in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION<sup>(1)</sup>

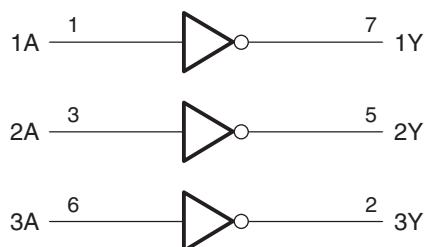
$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP3G04YFPR	__ _ H C _
	uQFN – DQE	Reel of 5000	SN74AUP3G04DQER	T9
	QFN – RSE	Reel of 5000	SN74AUP3G04RSE	T9
	SSOP – DCU	Reel of 3000	SN74AUP3G04DCUR	H04_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.  
YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

### FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

### LOGIC DIAGRAM (POSITIVE LOGIC)



- (1) Pin numbers shown are for the DCU and DQE packages.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		–0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		–0.5	4.6	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		–0.5	4.6	V
V <sub>O</sub>	Output voltage range in the high or low state <sup>(2)</sup>		–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50	mA
I <sub>O</sub>	Continuous output current			±20	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	DCU package		220	°C/W
		DQE package		261	
		RSE package		253	
		YFP package		132	
T <sub>stg</sub>	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

RECOMMENDED OPERATING CONDITIONS			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		0.8	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub>		V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.65 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 0.8 V		0	V
		V <sub>CC</sub> = 1.1 V to 1.95 V		0.35 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 3 V to 3.6 V		0.9	
V <sub>I</sub>	Input voltage		0	3.6	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 0.8 V		−20	μA
		V <sub>CC</sub> = 1.1 V		−1.1	mA
		V <sub>CC</sub> = 1.4 V		−1.7	
		V <sub>CC</sub> = 1.65		−1.9	
		V <sub>CC</sub> = 2.3 V		−3.1	
		V <sub>CC</sub> = 3 V		−4	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 0.8 V		20	μA
		V <sub>CC</sub> = 1.1 V		1.1	mA
		V <sub>CC</sub> = 1.4 V		1.7	
		V <sub>CC</sub> = 1.65 V		1.9	
		V <sub>CC</sub> = 2.3 V		3.1	
		V <sub>CC</sub> = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 0.8 V to 3.6 V		200	ns/V
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>		I <sub>OH</sub> = –20 μA	0.8 V to 3.6 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1		V
		I <sub>OH</sub> = –1.1 mA	1.1 V	0.75 × V <sub>CC</sub>			0.7 × V <sub>CC</sub>		
		I <sub>OH</sub> = –1.7 mA	1.4 V	1.11			1.03		
		I <sub>OH</sub> = –1.9 mA	1.65 V	1.32			1.3		
		I <sub>OH</sub> = –2.3 mA	2.3 V	2.05			1.97		
		I <sub>OH</sub> = –3.1 mA		1.9			1.85		
		I <sub>OH</sub> = –2.7 mA	3 V	2.72			2.67		
		I <sub>OH</sub> = –4 mA		2.6			2.55		
V <sub>OL</sub>		I <sub>OL</sub> = 20 μA	0.8 V to 3.6 V	0.1			0.1		V
		I <sub>OL</sub> = 1.1 mA	1.1 V	0.3 × V <sub>CC</sub>			0.3 × V <sub>CC</sub>		
		I <sub>OL</sub> = 1.7 mA	1.4 V	0.31			0.37		
		I <sub>OL</sub> = 1.9 mA	1.65 V	0.31			0.35		
		I <sub>OL</sub> = 2.3 mA	2.3 V	0.31			0.33		
		I <sub>OL</sub> = 3.1 mA		0.44			0.45		
		I <sub>OL</sub> = 2.7 mA	3 V	0.31			0.33		
		I <sub>OL</sub> = 4 mA		0.44			0.45		
I <sub>I</sub>	A or B input	V <sub>I</sub> = GND to 3.6 V	0 V to 3.6 V	0.1			0.5	μA	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V	0.2			0.6	μA	
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V to 0.2 V	0.2			0.6	μA	
I <sub>CC</sub>		V <sub>I</sub> = GND or (V <sub>CC</sub> to 3.6 V), I <sub>O</sub> = 0	0.8 V to 3.6 V	0.5			0.9	μA	
ΔI <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> – 0.6 V <sup>(1)</sup> , I <sub>O</sub> = 0	3.3 V	40			50	μA	
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	0 V	1.5				pF	
			3.6 V	1.5					
C <sub>o</sub>		V <sub>O</sub> = GND	0 V	3				pF	

(1) One input at V<sub>CC</sub> – 0.6 V, other input at V<sub>CC</sub> or GND

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C<sub>L</sub> = 5 pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	0.8 V	18					ns
			1.2 V ± 0.1 V	2.6	7.3	12.8	2.1	15.6	
			1.5 V ± 0.1 V	1.4	5.2	8.7	0.9	10.3	
			1.8 V ± 0.15 V	1	4.2	6.6	0.5	8.2	
			2.5 V ± 0.2 V	1	3	4.4	0.5	5.5	
			3.3 V ± 0.3 V	1	2.4	3.5	0.5	4.3	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 10$  pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		21				ns
			1.2 V $\pm$ 0.1 V	1.5	8.5	14.7	1	17.2	
			1.5 V $\pm$ 0.1 V	1	6.2	10	0.5	11.3	
			1.8 V $\pm$ 0.15 V	1	5	7.7	0.5	9	
			2.5 V $\pm$ 0.2 V	1	3.6	5.2	0.5	6.1	
			3.3 V $\pm$ 0.3 V	1	2.9	4.2	0.5	4.7	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 15$  pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		24				ns
			1.2 V $\pm$ 0.1 V	3.6	9.9	16.3	3.1	19.9	
			1.5 V $\pm$ 0.1 V	2.3	7.2	11.1	1.8	13.2	
			1.8 V $\pm$ 0.15 V	1.6	5.8	8.7	1.1	10.6	
			2.5 V $\pm$ 0.2 V	1	4.3	5.9	0.5	7.3	
			3.3 V $\pm$ 0.3 V	1	3.4	4.8	0.5	5.9	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 30$  pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

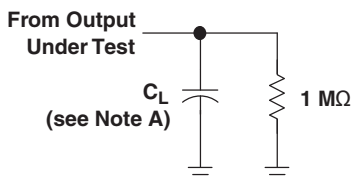
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		32.8				ns
			1.2 V $\pm$ 0.1 V	4.9	13.1	20.9	4.4	25.5	
			1.5 V $\pm$ 0.1 V	3.4	9.5	14.2	2.9	16.9	
			1.8 V $\pm$ 0.15 V	2.5	7.7	11	2	13.5	
			2.5 V $\pm$ 0.2 V	1.8	5.7	7.6	1.3	9.4	
			3.3 V $\pm$ 0.3 V	1.5	4.7	6.2	1	7.5	

## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

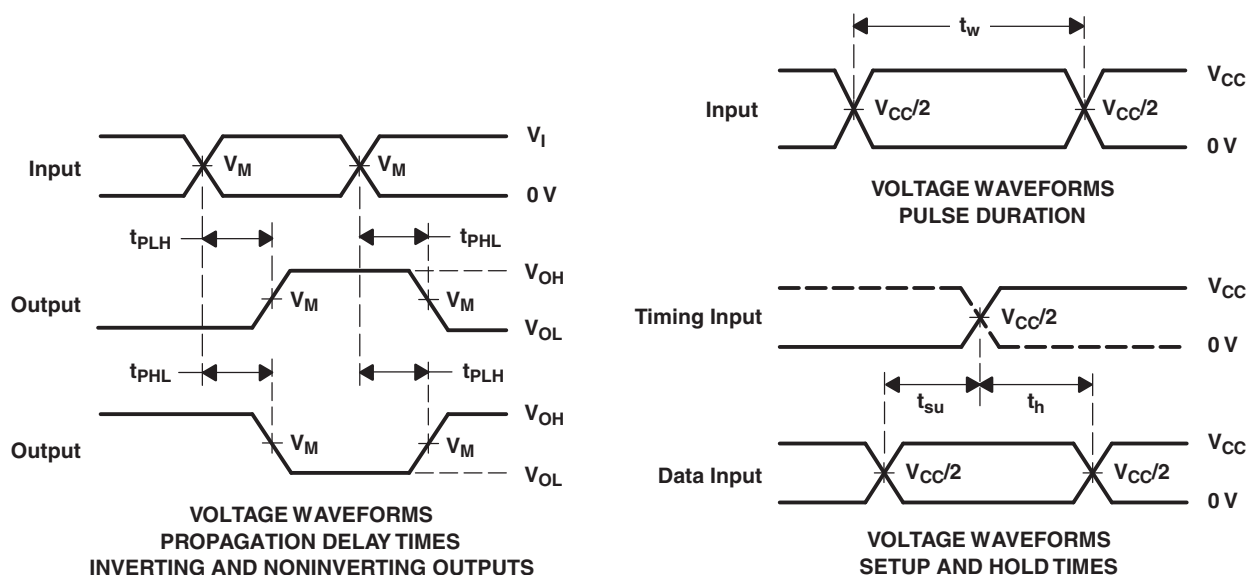
PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$f = 10$ MHz	0.8 V	4	pF
			1.2 V $\pm$ 0.1 V	4	
			1.5 V $\pm$ 0.1 V	4	
			1.8 V $\pm$ 0.15 V	4	
			2.5 V $\pm$ 0.2 V	4.1	
			3.3 V $\pm$ 0.3 V	4.3	

## PARAMETER MEASUREMENT INFORMATION (Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

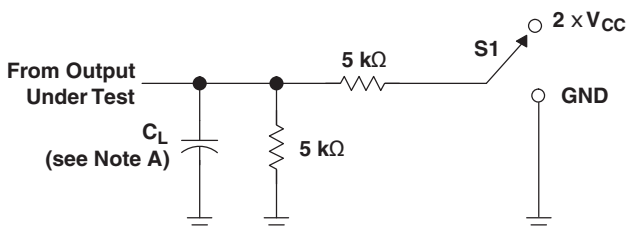
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$



- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , for propagation delays  $t_r/t_f = 3 \text{ ns}$ , for setup and hold times and pulse width  $t_r/t_f = 1.2 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

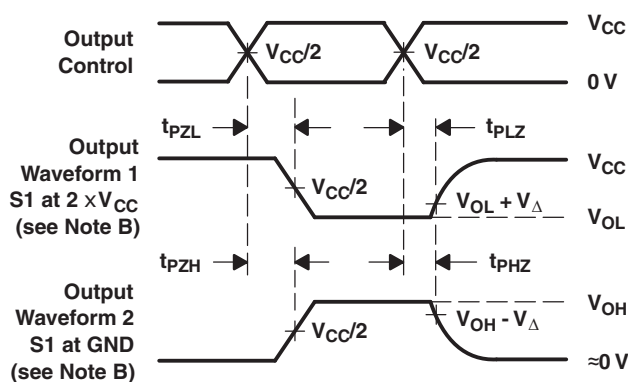
## PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



LOAD CIRCUIT

TEST	S1
$t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PZH}$	$2 \times V_{CC}$ GND

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_{\Delta}$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 3 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit and Voltage Waveforms**



## REVISION HISTORY

Changes from Revision B (March 2010) to Revision C	Page
• Added Live Insertion and Back Drive Protection to Features. ....	<a href="#">1</a>

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP3G04DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H04R	<a href="#">Samples</a>
SN74AUP3G04DQER	ACTIVE	X2SON	DQE	8	5000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	T9	<a href="#">Samples</a>
SN74AUP3G04RSER	ACTIVE	UQFN	RSE	8	5000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	T9	<a href="#">Samples</a>
SN74AUP3G04YFPR	ACTIVE	DSBGA	YFP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HCN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP3G04DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP3G04DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP3G04RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
SN74AUP3G04YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP3G04DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP3G04DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP3G04RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP3G04YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0

DCU (R-PDSO-G8)

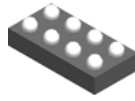
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



## NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

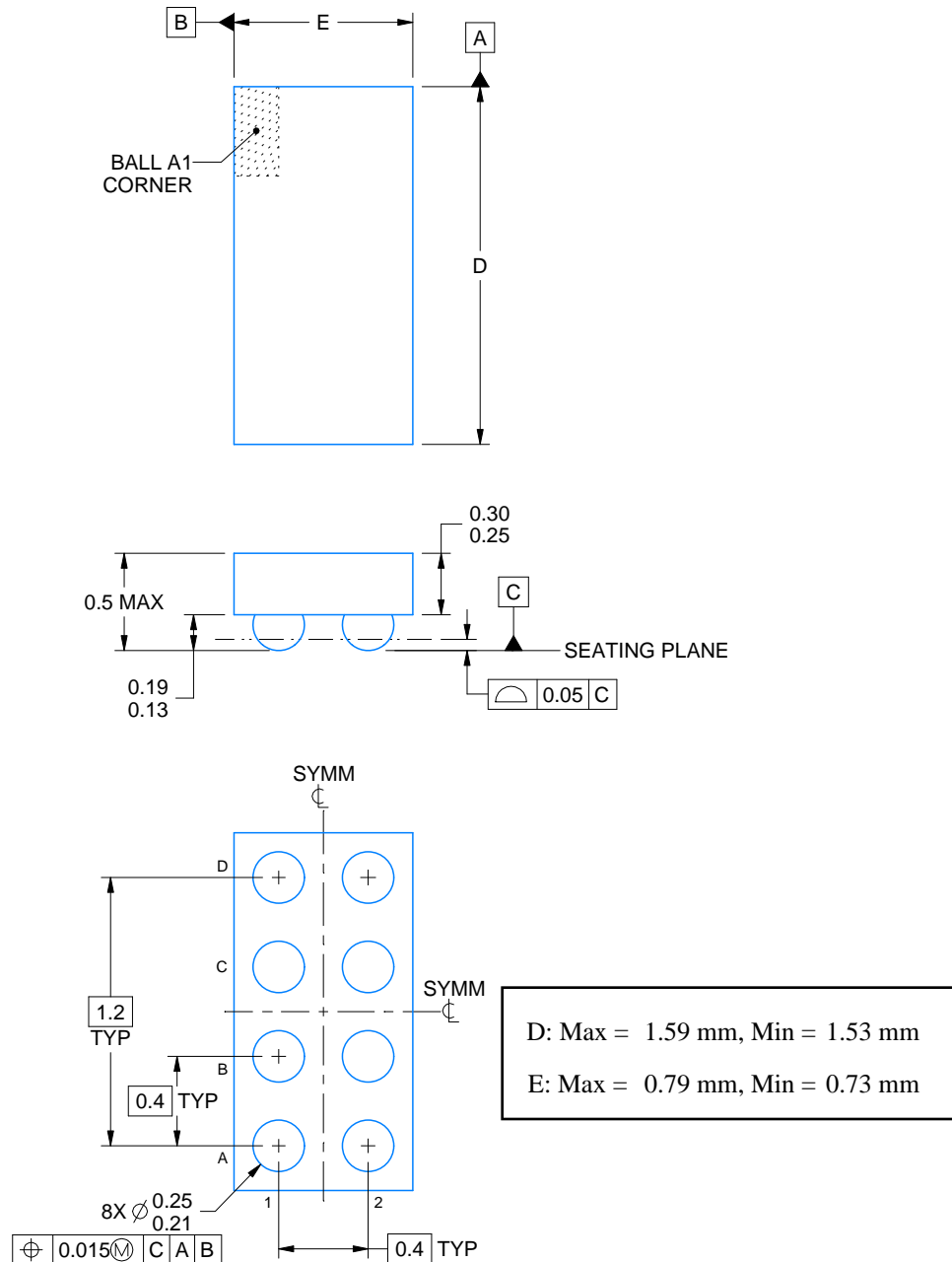
YFP0008



# PACKAGE OUTLINE

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4225242/A 08/2019

### NOTES:

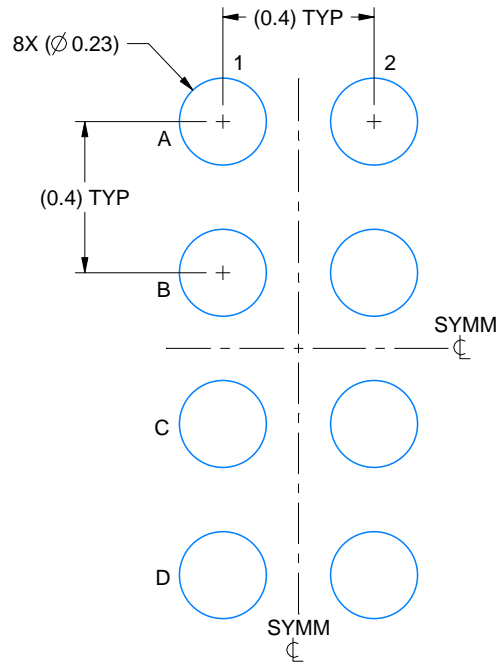
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

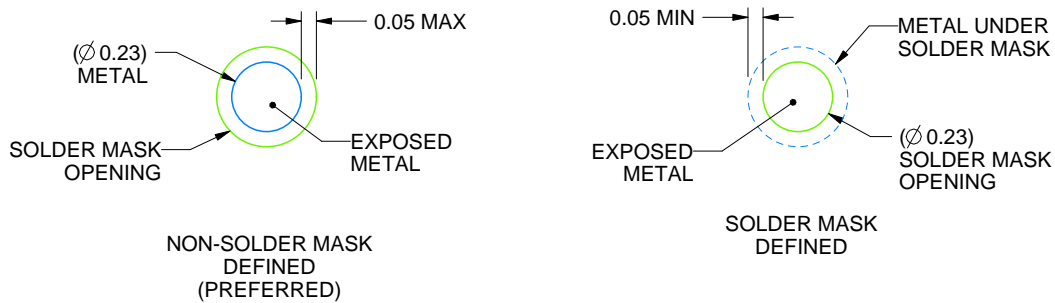
YFP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 50X



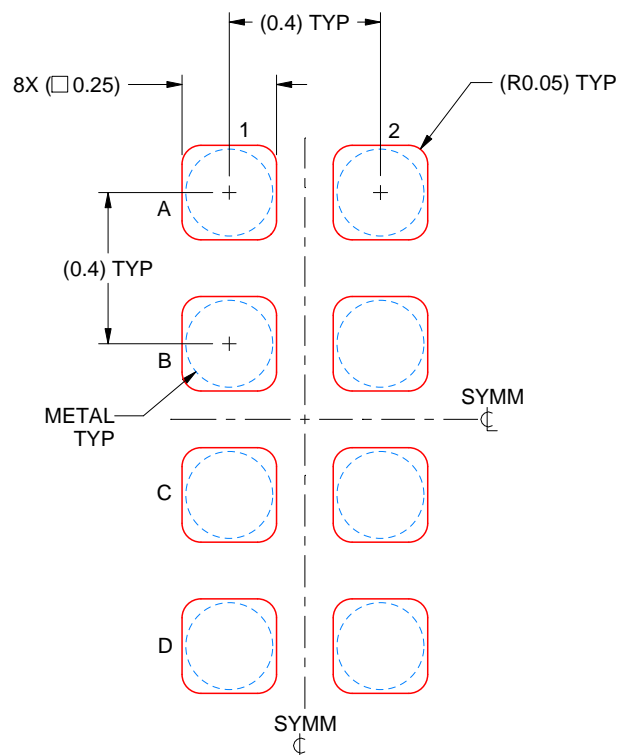
SOLDER MASK DETAILS  
NOT TO SCALE

4225242/A 08/2019

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).



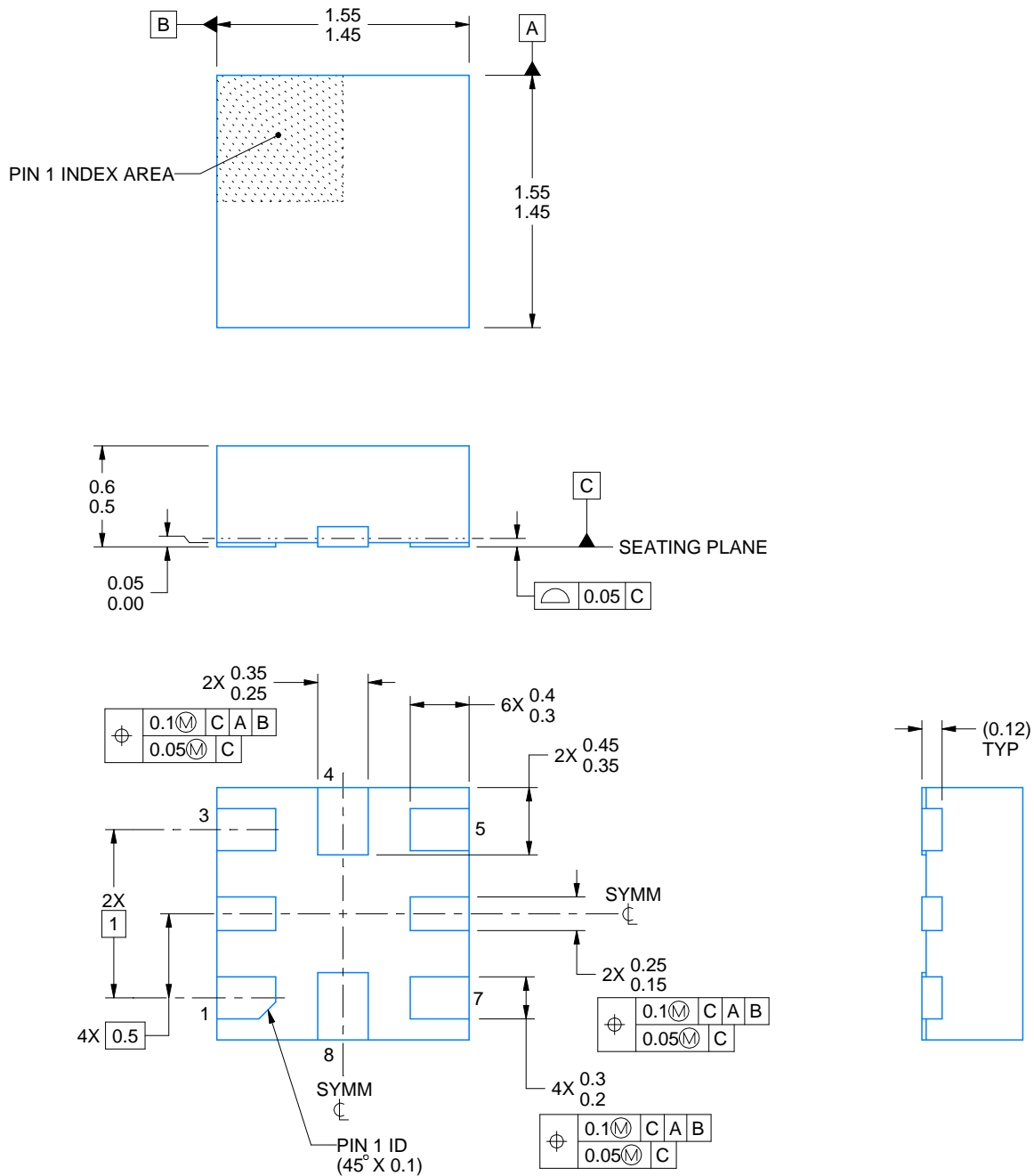
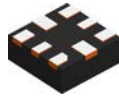


SOLDER PASTE EXAMPLE  
 BASED ON 0.1 mm THICK STENCIL  
 SCALE: 50X

4225242/A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4220323/B 03/2018

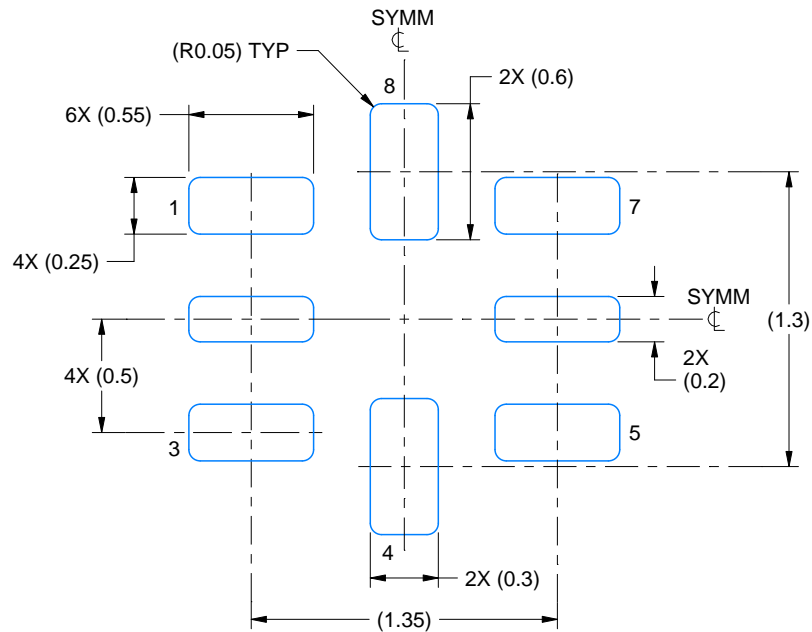
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

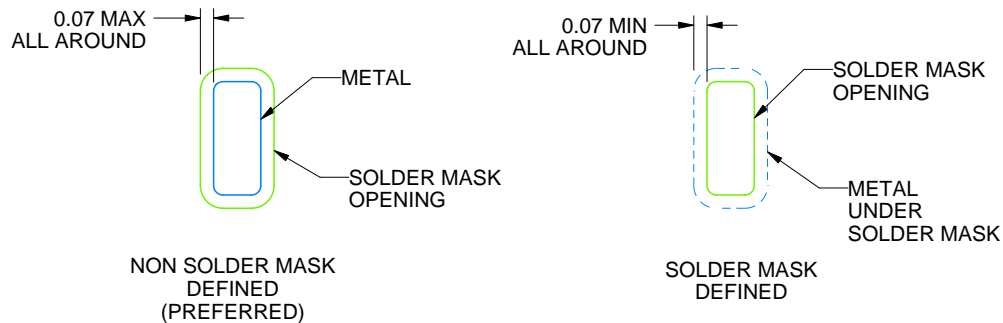
**RSE0008A**

### UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:30X



**SOLDER MASK DETAILS**  
**NOT TO SCALE**

4220323/B 03/2018

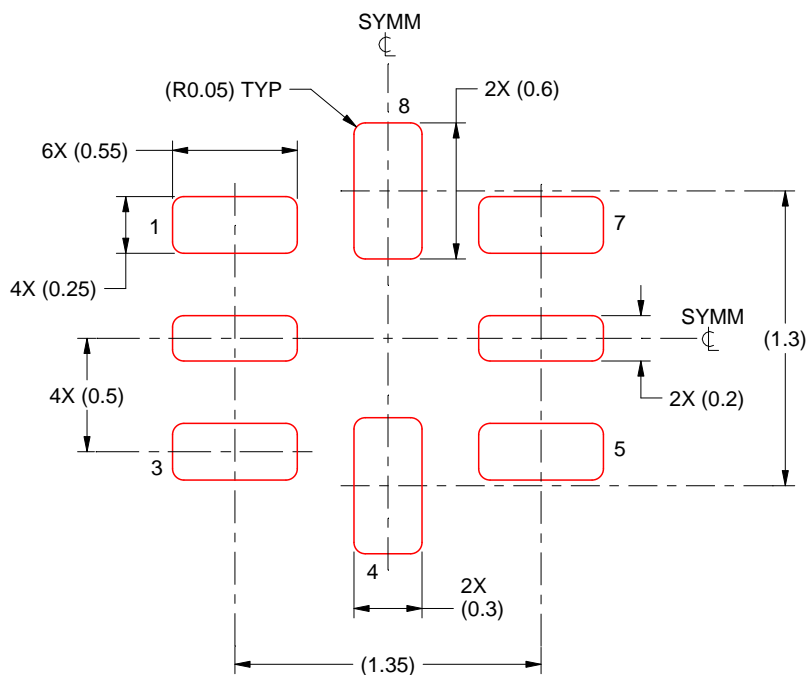
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).

**RSE0008A**

### UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
**BASED ON 0.1 mm THICKNESS**  
**SCALE: 30X**

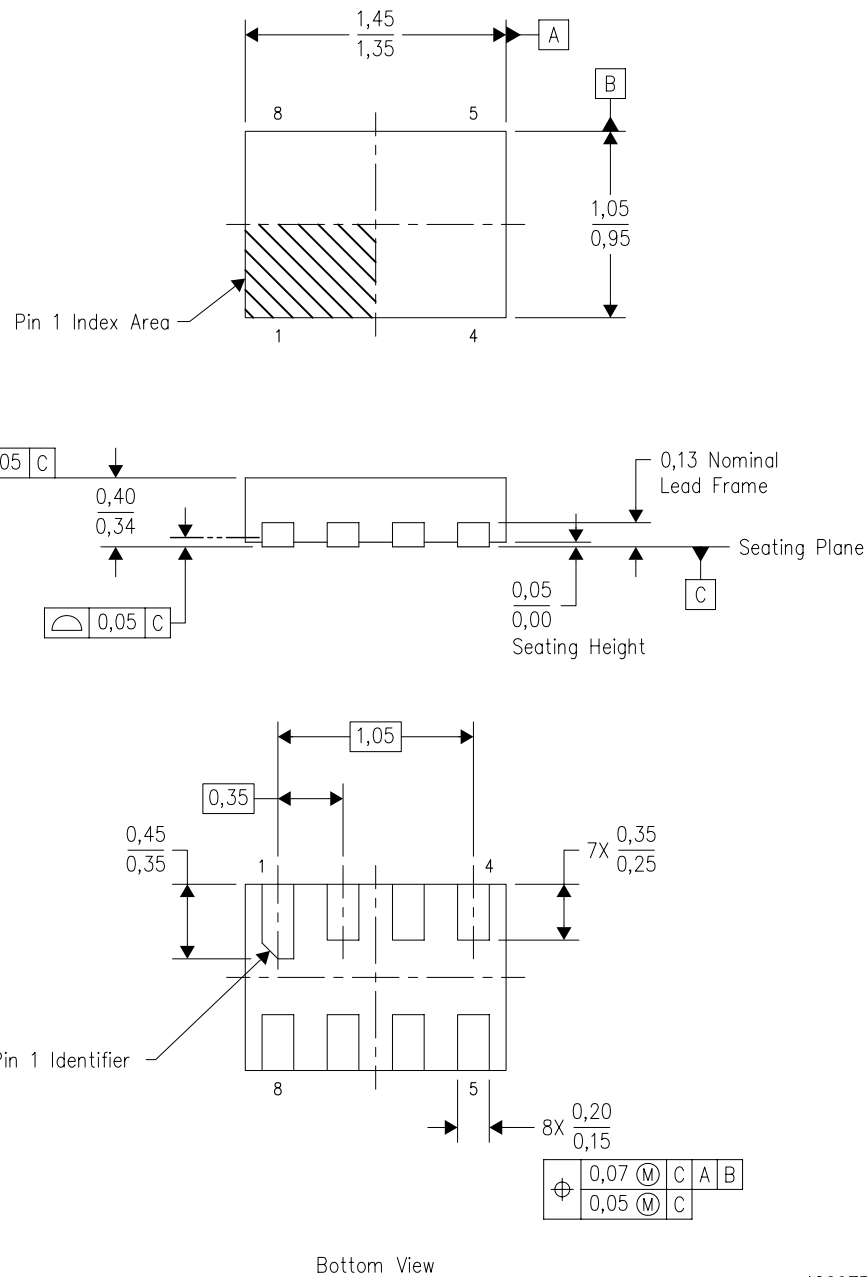
4220323/B 03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

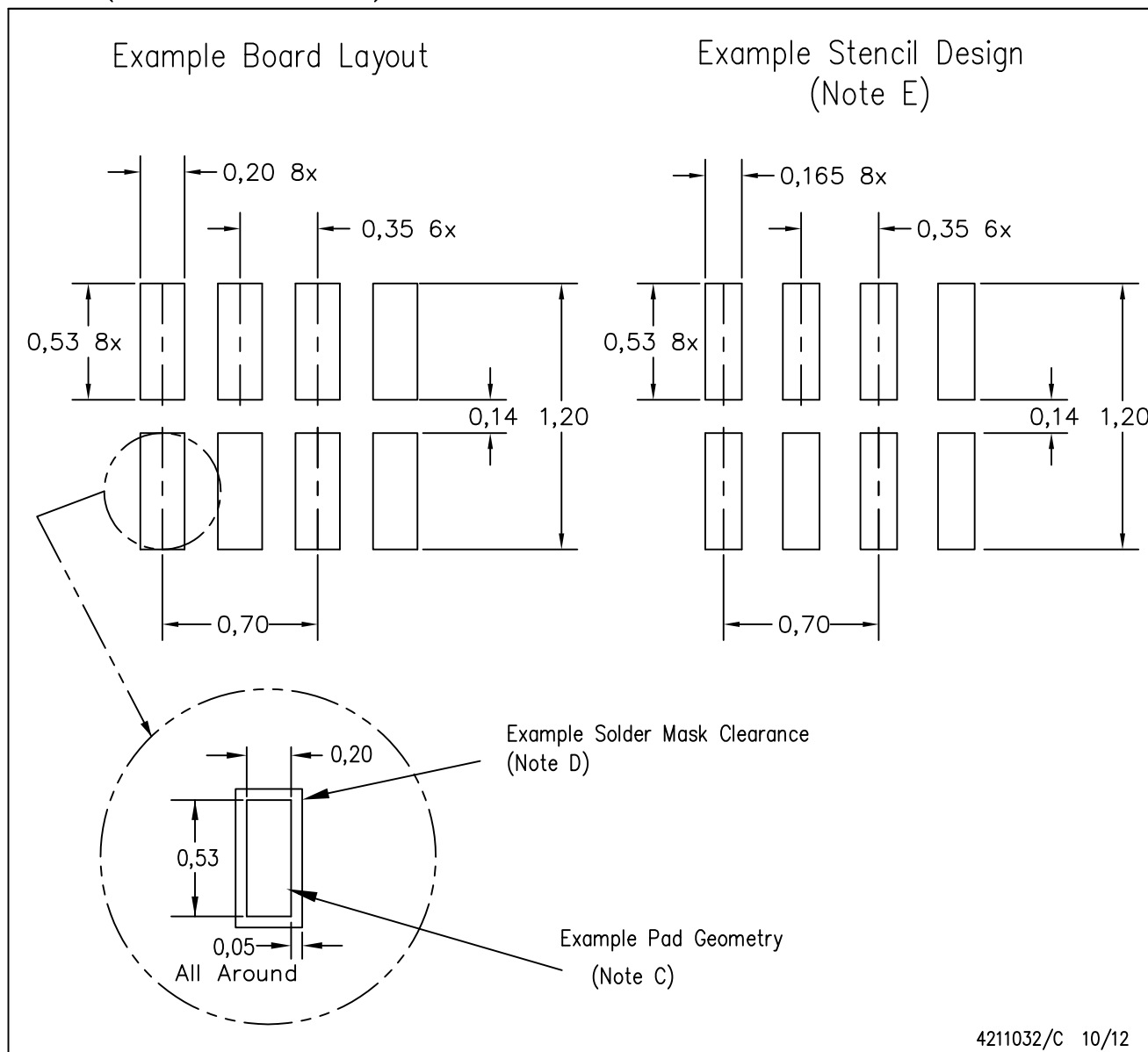


4209779/B 10/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. This package complies to JEDEC MO-287 variation X2EAF.

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.  
If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Over-printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
  - H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - I. Component placement force should be minimized to prevent excessive paste block deformation.

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