TPS62100, TPS62101, TPS62102, TPS62103
MULTIMODE LOW-POWER BUCK CONVERTER

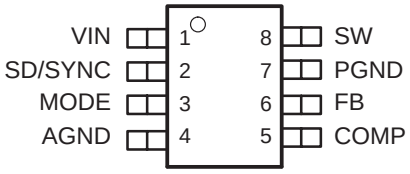
SLUS446B – MAY 2000 – REVISED DECEMBER 2000

- **2.5-V to 9-V Input Range**
- **0.8-V to 8-V Output Range**
- **Dual-Auto-Mode for High-Efficiency at Light Loads**
- **Externally Synchronizable**
- **0% to 100% Duty Cycle**
- **Low-Quiescient, Standby, and Shutdown Currents**
- **8-Pin SOIC Package**
- **Four PWM Frequency Versions (Maximum 2 MHz)**

applications

- **Cellular Telephones**
- **Satellite Telephones**
- **GPS Devices**
- **Digital Still Cameras**
- **PDAs and Handheld Cameras**

D PACKAGE
(TOP VIEW)



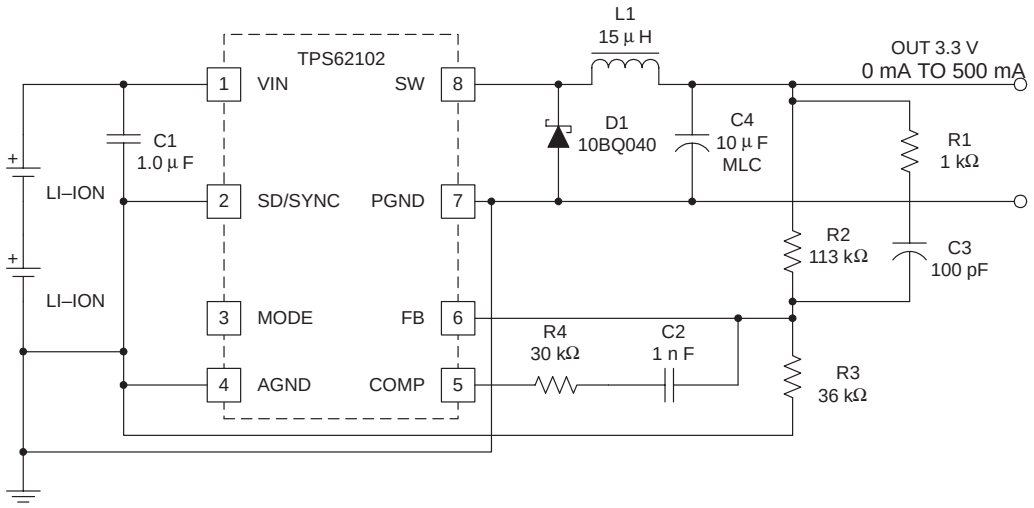
description

The TPS6210x family of low-power high-efficiency buck converters is designed to operate from 1 or 2 li-ion cell battery packs. This part, with its wide input range of 2.5 V to 9 V, has an adjustable output from 0.8 V to 8 V and is capable of 500-mA output current. The TPS6210x family of synchronizable dc-to-dc converters is available in four different operating frequencies: 300 kHz, 600 kHz, 1 MHz, and 2 MHz. The circuit can be allowed to run at a fixed frequency, or sychronized, using the dual function SD/SYNC input pin.

The TPS6210x family is highly efficient at both low and high output currents. The tri-function MODE input pin is used to select constant-frequency, auto-mode, or light-load modes of operation. The multimode operation allows the IC to select the most efficient operating mode, or if desirable, the user can determine which of three modes to operate in. In the auto-mode, the output load detector circuitry determines if the converter should be running in the constant-frequency, heavy-load mode, or pulsed-variable frequency, light-load mode.

The TPS6210x family also has a shutdown mode for optimum battery shelf life. The IC utilizes three methods of overload protection, including thermal shutdown and two levels of overcurrent protection. The TPS6210x is available in the small outline 8-pin SOIC package.

typical application (automatic mode switcher)



UDG–00059

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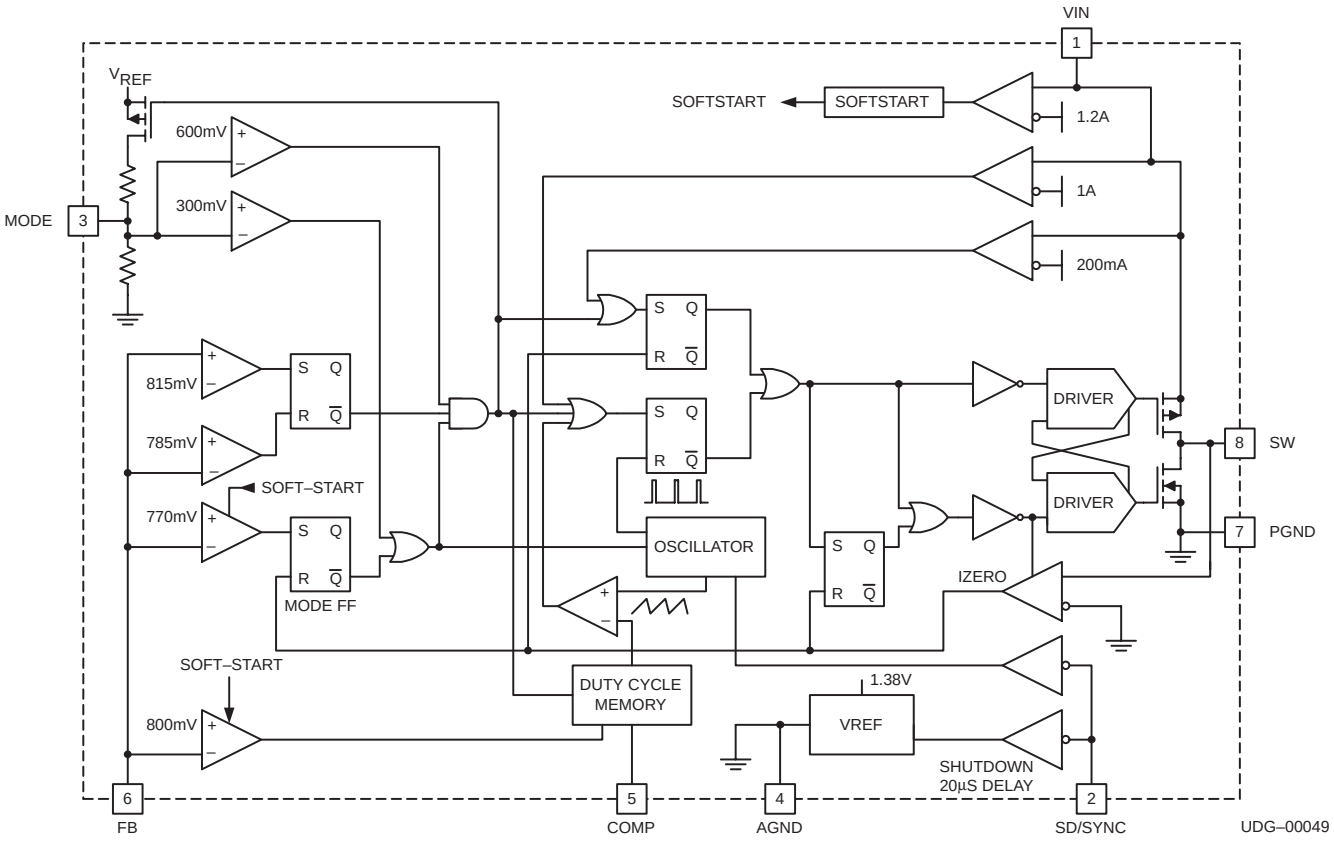
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AVAILABLE OPTIONS†

T_A	OPERATING FREQUENCY	PACKAGED DEVICES
		SOIC (D)
T_A = –40°C to 85°C	300 kHz	TPS62100D
	600 kHz	TPS62101D
	1 MHz	TPS62102D
	2 MHz	TPS62103D

† The D package is available taped and reeled. Add R suffix to device type (e.g. TPS62100DTR) to order quantities of 3000 devices per reel.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

VIN input supply voltage . . . . . –0.3 V to 10 V
SD/SYNC input voltage . . . . . –0.3 V to VIN + 0.3 V
MODE input voltage . . . . . –0.3 V to VIN + 0.3 V
COMP input voltage . . . . . –0.3 V to 10 V
SW output voltage . . . . . –0.3 V to VIN + 0.3 V
SW output current . . . . . 1.6 A
Operating junction temperature . . . . . –40°C to +150°C
Storage temperature . . . . . –65°C to +150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Unless otherwise noted, voltages are reference to ground and currents are positive into and negative out of the specified terminals. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500 µs. Consult the Packaging Section of the *Portable Products Data Book* (TI Literature No. SLUD001) for thermal limitations and considerations of the package.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, VIN, SD/SYNC, MODE		9	V
Regulated output voltage		8	V
Average output current, I_{OUT}§		500	mA
Operating junction temperature, T_J§	–40	85	°C

§ It is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
COMP	5	O	Output of the error amplifier. The loop compensation network connects between this pin and FB. When the converter enters the light-load mode, this pin goes into a high-impedance state..
FB	6	I	Feedback voltage input. In the constant-frequency mode, the output duty cycle is varied to keep this pin at 800 mV. In light-load mode, this pin is kept between 785 mV and 815 mV. If this pin falls below 770 mV while the converter is in auto mode and light-load mode, the converter re-enters the constant-frequency mode.
AGND	4		Reference point for the internal reference and all thresholds, as well as the return for the remainder of the device.
MODE	3	I	This pin allows the user to program the IC into one of three operating modes. Driving the pin high forces the converter into the constant-frequency mode. Driving the pin low forces it into the low-power mode. Letting the pin float puts the converter into the auto mode.
PGND	7		Return for all high-level currents.
SD/SYNC	2	I	This dual function pin serves as the SYNC and SHUTDOWN input. To synchronize the internal clock, this pin must be driven from 0 V to 2 V. The clock syncs on the rising edge of the input pulse. To shutdown the converter, this pin must be driven high for more than 20 µs.
SW	8	O	This is the PWM power output of the converter and is connected to an L-C (inductor-capacitor) filter and a Schottky catch diode.
VIN	1	I	Input to the converter.

electrical characteristics over recommended operating free-air temperature range, T_A = –40 C to 85 C, T_A = T_J, typical values are at T_A = 25 C, V_{IN} = 7.2 V, MODE = 1 (constant frequency), SD/SYNC = 0 V. (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Section						
VIN operating range			2.5	7.2	9	V
VIN supply current (constant frequency mode)	VIN = 3.6 V,	not switching		625	900	µA
	VIN = 7.2 V,	not switching		650	915	µA
	VIN = 9.0 V,	not switching		700	925	µA
VIN supply current (burst mode)	VIN = 3.6 V,	not switching		220	295	µA
	VIN = 7.2 V,	not switching		250	370	µA
VIN supply current (sleep mode)	VIN = 3.6 V			230	340	µA
	VIN = 7.2 V			190	275	µA
VIN shutdown current	VIN = 7.2 V,	SD/SYNC = VIN		1	15	µA
	VIN = 7.2 V,	SD/SYNC = 4 V		2	25	µA
	VIN = 3.6 V,	SD/SYNC = 3.6 V		1	15	µA
Error Amplifier Section						
FB input voltage	COMP = 0.5 V,	T_A = 25°C	790	800	810	mV
FB voltage line regulation	T_A = 25°C,	VIN = 2.8 V to 9 V			0.1	%/V
	T_A = 25°C,	VIN = 2.8 V to 2.5 V			0.5	%
FB input voltage	COMP = 0.5 V,	T_A = 0°C to 70°C	784	800	816	mV
	COMP = 0.5 V,	T_A = –40°C to 85°C	777	800	823	mV
FB input bias current	COMP = 0.5 V			100	500	nA
Open loop gain	COMP = 0.2 V to 0.5 V		50	80	130	dB
Unity gain BW	See Note 1			5		MHz
Maximum sinking current			250	500		µA
Maximum sourcing current				–500	–250	µA
COMP output high voltage	I_{COMP} = –10 µA		1.60	2.00	2.75	V
COMP output low voltage	I_{COMP} = 10 µA			250	500	mV
Soft-start time			1	5	9	ms
Light Load Detectors Section						
FB V_{OFF} threshold			778	808	838	mV
FB V_{ON} threshold			741	778	815	mV
FB V_{MODE} threshold			725	762	799	mV

NOTE 1: Ensured by design. Not production tested.

electrical characteristics over recommended operating free-air temperature range, T_A = –40 C to 85 C, T_A = T_J, typical values are at T_A = 25 C, V_{IN} = 7.2 V, MODE = 1 (constant frequency), SD/SYNC = 0 V. (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Width Modulator Section					
SW switching frequency	TPS62100, 300 kHz version, VIN = 5 V	225	300	375	kHz
	TPS62101, 600 kHz version, VIN = 5 V	450	600	750	kHz
	TPS62102, 1 MHz version, VIN = 5 V	0.75	1	1.25	MHz
	TPS62103, 2 MHz version, VIN = 5 V	1.5	2	2.5	MHz
Maximum sync. frequency	TPS62100, 300 kHz version, VIN = 5 V, See Notes 1 and 2			490	kHz
	TPS62101, 600 kHz version, VIN = 5 V, See Notes 1 and 2			966	kHz
	TPS62102, 1 MHz version, VIN = 5 V, See Notes 1 and 2			1.61	MHz
	TPS62103, 2 MHz version, VIN = 5 V, See Notes 1 and 2			2.5	MHz
Maximum duty cycle	COMP = 2.5 V			100%	
Minimum duty cycle	COMP = 0 V	0%			
Output Switch Section					
SW NFET $R_{DS(on)}$	I_{SW} = 500 mA VIN = 7.2 V		0.3	0.6	Ω
SW PFET $R_{DS(on)}$	I_{SW} = –500 mA VIN = 7.2 V		0.5	1	Ω
SW NFET $R_{DS(on)}$	I_{SW} = 500 mA VIN = 3.6 V		0.6	1.2	Ω
SW PFET $R_{DS(on)}$	I_{SW} = –500 mA VIN = 3.6 V		0.8	1.6	Ω
SW output leakage	SW = 4.5V VIN = 9 V	–10	0	10	µA
SW charge switch current limit 1	Terminates pulse	0.65	0.95	1.25	A
SW charge switch current limit 2	Initiates soft-start, See Note 1	0.75	1.15	1.55	A
SW current, light-load mode	Peak inductor current	112	160	208	mA
Shutdown and Synchronization Section					
SD/SYNC threshold		0.5	1	2.3	V
SD/SYNC input current	SD/SYNC = 0 V	–100	0	100	nA
SD/SYNC input current	SD/SYNC = 7.2 V	–1	0	1	µA
Maximum synchronization pulse width			25	37	µs
Minimum synchronization pulse width		50			ns
Three–State Mode Control Input Section					
Light-load MODE threshold		225	300	410	mV
Constant frequency MODE threshold		475	600	750	mV
Open circuit MODE voltage		375	450	510	mV
MODE input-low current	Mode = 0 V	–20	–12	–5	µA
MODE input-high current	Mode = 1.4 V	10	22	33	µA

NOTES: 1. Ensured by design. Not production tested.
2. Minimum synchronization frequency must be less than the natural running frequency.

APPLICATION INFORMATION

general information

The TPS6210x family of devices are low-power, synchronous buck controllers with integrated FETS. The thrust of these devices is to facilitate the construction of low-cost, small, high-frequency and fast-response dc-to-dc converters that operate from either one or two li-ion cells. Synchronous rectification allows for higher operating efficiency than relying on a Schottky diode alone. Shifting from a fixed-frequency PWM mode of operation to a fixed-current variable frequency mode during light loads preserves efficiency and increases battery life in this situation.

modes of operation

The TPS6210x family has four distinct modes of operation: automatic-constant frequency (or high-power mode), automatic-variable frequency (or low-power mode), forced-constant frequency, and forced-variable frequency. The mode that the chip is in is controlled by the MODE pin. Allowing this pin to float lets the chip automatically transition between the high-power mode and the low-power mode. The chip selects which mode to operate in depending upon load current and voltage. If the mode pin is forced high, the chip operates in the forced-constant frequency PWM mode. If the pin is driven low, the chip operates in the forced variable frequency mode. Detailed descriptions of the modes follow.

forced constant frequency (MODE = high)

In this mode, the chip behaves like a standard buck regulator with a synchronous rectifier added. The synchronous rectifier turns on shortly after the buck switch turns off, and the buck switch turns on shortly after the synchronous rectifier turns off. During the small time interval when neither the buck switch nor the synchronous rectifier is turned on, an optional small external schottky diode carries the inductor freewheel current.

In this mode, the error amplifier is used in a normal feedback arrangement, forcing the divided output voltage to be equal to the 0.8-V reference. Also, note that the overall converter should be designed so that it always operates in the continuous conduction region, (i.e. the inductor current should never be allowed to decay to zero). If the inductor current decays to zero, the control loop characteristics change dramatically. Consequently, the loop must be designed for the worst case load condition and is not optimal in the general sense for a continuous mode converter.

APPLICATION INFORMATION

forced variable frequency (MODE = low)

In this mode, the chip behaves like a 100-mA current source that is turned on and off as the output voltage falls below or rises above predetermined thresholds. These thresholds are located approximately 1.9% above and below the nominal output voltage. For instance, if the nominal output is 3.3 V, then the on and off thresholds are approximately 3.237 V and 3.363 V, respectively. The operational sequence is as follows:

1. As the output voltage falls below the turn-on threshold, the chip enters a burst period, and the buck switch is turned on.
2. When the current in the buck switch rises to 200 mA, the switch is turned off and the synchronous rectifier is turned on to pass the freewheel current.
3. As the current in the synchronous rectifier decays to zero, it is turned off and the buck switch is again turned on, continuing at step 2.
4. When the output voltage rises above the turn-off threshold, the buck switch is immediately turned off and the synchronous rectifier is turned on to handle the last cycle of free wheel current. The chip is also taken out of its burst period and remains dormant until the output voltage falls below the turn-on threshold, at which point operation continues at step 1.

The reason for limiting the current to 200 mA is to place a limit on the amount of overshoot that can occur from charging the inductor up with a large current and having a relatively small output capacitance available to absorb the energy stored.

In this mode, the error amplifier is not used and is essentially turned off, and its output is disconnected from the COMP pin. The FB pin is connected to two comparators, which generate the internal signals that put the chip into and out of a burst interval. The threshold levels, referenced to the FB pin, are 0.815 V and 0.785 V (off and on). Also, the largest load current that can be supplied by the converter operating in this mode is 100 mA. Sustained load currents greater than 100 mA deplete the energy in the output storage capacitor and cause the output voltage to fall.

APPLICATION INFORMATION

the automatic modes, or the high power and low power modes (MODE = floating)

Leaving the MODE pin unconnected or floating lets the chip automatically select one of two operating modes. In these two modes, operation is the same as for the forced modes with the exception that the chip is free to switch between the constant- and variable-frequency modes based upon the operating conditions of the converter. When the chip is initially powered, it is in the constant frequency (high-power) mode, and stays in this mode until it senses that the converter is on the verge of breaking into discontinuous operation. When this condition is sensed, the converter enters the variable-frequency mode of operation. The chip remains in the variable-frequency mode of operation until the voltage at the FB pin falls to approximately 0.770 V or 3.75% below nominal. When this happens, the chip enters the constant-frequency mode of operation and remains in that mode until it senses the converter is about to go discontinuous.

This has some design implications. In order for the transition to occur smoothly, the discontinuous current level of the converter must be less than 100 mA. This in turn implies a minimum inductor size for a given set of operating conditions. The minimum inductor size for smooth transitions is approximately:

$$L = \frac{V_O \left(1 - \frac{V_O}{V_I}\right)}{0.16 \times F} \quad (1)$$

Where:

- V_O is the output voltage
- V_I is the input voltage and
- F is the frequency of operation
- 0.16 is the minimum peak-inductor-current in low-power mode

It is recommended that something more than the minimum inductance be used to give a little hysteresis to the mode transition. A 10% increase in inductance over the minimum value should be sufficient.

Note that in **all modes**, on initial power-up, after a shutdown, and when there is a second stage overcurrent, the chip transitions into a constant frequency mode of operation and goes through a soft-start cycle. The chip remains in the constant frequency mode until the voltage presented to the FB pin exceeds 0.770 V. At this point the chip may go into a variable frequency mode if MODE is held low, or the load is insufficient to cause continuous inductor current and the MODE pin is left floating.

soft start

The TPS6210x family has a built in soft-start time of approximately 5 ms. The soft start is a *closed-loop* soft start, meaning that the reference input to the error amplifier is ramped up over the soft start interval and the converter control loop is allowed to track the ramping reference signal. This method generally allows for faster soft-start times with minimal output voltage overshoot at startup.

APPLICATION INFORMATION

shutdown and synchronization

The TPS6210x family incorporates a dual function shutdown and synchronization pin. Pulsing the SD/SYNC pin higher than 1 V forces the internal oscillator to reset, allowing synchronization to an external signal source. It is recommended that the part not be synchronized higher than two times its nominal operating frequency. The reason for this is that synchronizing to a higher frequency causes the internal saw-tooth voltage to have less amplitude. Since this is the signal that is compared to the error-amplifier output to determine the duty cycle, the reduction in amplitude causes a corresponding increase in PWM gain as well as increased susceptibility to noise. Doubling the operating frequency through synchronization effectively cuts the saw-tooth amplitude in half, doubling the PWM gain.

Bringing the SD/SYNC pin high and holding it for more than 20 μs forces the chip to enter a shutdown state. This causes almost all sections of the chip to enter a dormant state to conserve power. Bringing this pin low again allows the chip to resume operation, starting with a full soft-start cycle.

This pin **must not** be allowed to float, since there are no internal pulldown resistors. Floating this pin could cause the device to operate erratically.

error amplifier

The internal error amplifier has a unity gain frequency of 3 MHz (typ). When designing a compensation network for this chip, the response of the error amplifier may be a limiting consideration. This is especially true with the 1-MHz and 2-MHz switching frequencies. The phase and gain characteristics of the error amplifier are shown in Figure 1.

Due to the method of sensing voltage thresholds in the variable-frequency mode, it is recommended that the compensation loop use integral compensation (no dc path from the COMP pin to the FB pin) if the chip is allowed to automatically switch between constant- and variable-frequency modes of operation. The reason for this is to avoid dc offsets creeping into the sense point and changing the nominal output voltage in the variable-frequency mode.

APPLICATION INFORMATION

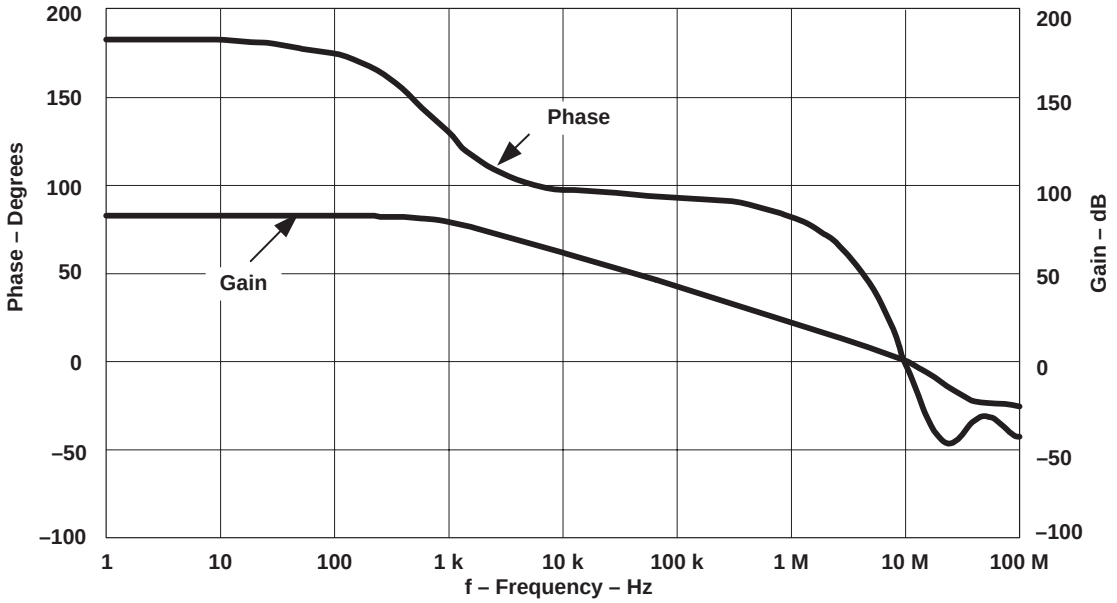


Figure 1. Error Amplifier Gain Phase Response

loop compensation and the TPS6210X series of converters

Feedback-loop compensation in the data sheet examples assumes that the output-filter capacitor is a mulit-layer ceramic (MLC) type. With this type of output capacitor, the ESR zero will be too high in frequency to use as part of the compensation network. This can complicate the loop compensation, especially in the higher-switching frequency versions where error-amplifier bandwidth must be taken into consideration. A typical PWM- and output-filter response plot is shown in Figure 2. Note the lightly-loaded circuit has a pair of complex poles that cause the gain peaking and rapid-phase shift near the L-C resonant frequency.

The strategy that has been the best to date for designing a compensator for this circuit has been to use:

- an origin pole (no dc path from COMP to FB),
- a zero placed below the L-C resonance,
- a zero placed above the L-C resonance,
- and the remaining pole placed above the last zero.

APPLICATION INFORMATION

loop compensation and the TPS6210X series of converters (continued)

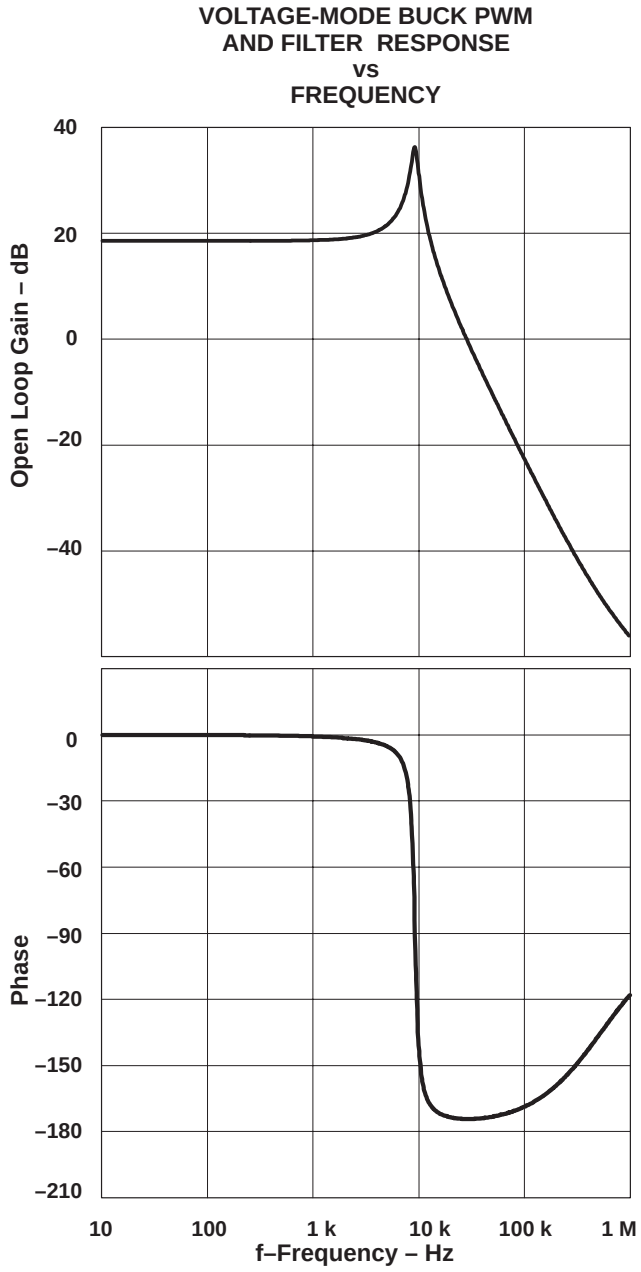


Figure 2

APPLICATION INFORMATION

loop compensation and the TPS6210X series of converters (continued)

The circuit shown in Figure 3, implements an origin pole, two zeros and a high frequency pole. A second high frequency pole will be added by the response of the error amplifier. If desired, this additional pole can be controlled by adding a capacitor across the series R–C from COMP to FB.

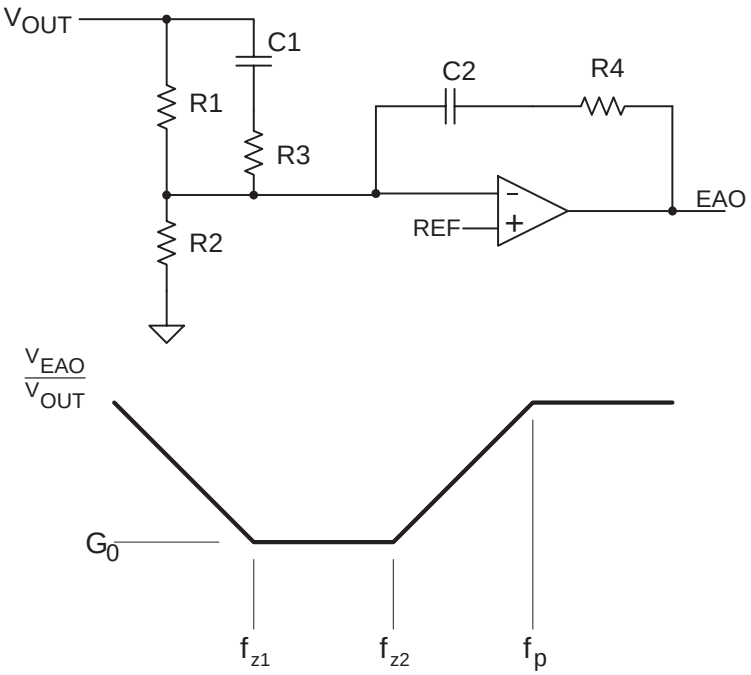


Figure 3. Compensation Network and Gain Response

In this schematic and line approximation of response, the components are calculated as follows:

$$R_1 = R_2 \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}} \right) \quad (2)$$

$$R_4 = R_1 \| R_2 \times G_0 \quad (3)$$

$$C_2 = \left(2 \times \pi \times f_{z1} \times R_4 \right)^{-1} \quad (4)$$

$$C_1 = \left(2 \times \pi \times f_{z2} \times R_1 \| R_2 \right)^{-1} \quad (5)$$

$$R_3 = \left(2 \times \pi \times f_p \times C_1 \right)^{-1} \quad (6)$$

APPLICATION INFORMATION

loop compensation and the TPS6210X series of converters (continued)

Note that f_{z1} is a lower frequency than f_{z2}. It is suggested that a spice or other simulator be used to verify feedback loop characteristics. When doing this modeling, be sure to use an amplifier that has a band limited response. Setting the amplifier up for an 80 dB gain with a single dominant pole at 200 Hz (2 MHz GBWP) will lead to a good loop design. The gain/phase plots for the example circuits were all done using a 2 MHz GBWP amplifier. Look at the example schematics and note where the poles and zeros are for an indication of where to start compensating a new design.

current limiting

The TPS6210x family has built-in over-current protection and thermal shutdown. The over-current protection is done in two stages. The first stage trips at approximately 1 A and simply causes an immediate pulse termination. If a hard short is present at the output of the LC filter, propagation delays from the first-level over current could allow the current to ratchet up in the inductor. To prevent this from happening, a second level of over-current protection trips at approximately 1.2 A. When this level is tripped, the chip is forced to do a soft start. If the chip is in an abnormally high ambient temperature, or has an inadequate heatsink for the power levels demanded, the thermal shutdown circuitry causes the chip to shut down if the die temperature ever reaches 170°C. After the die cools, normal operation resumes with a full soft start.

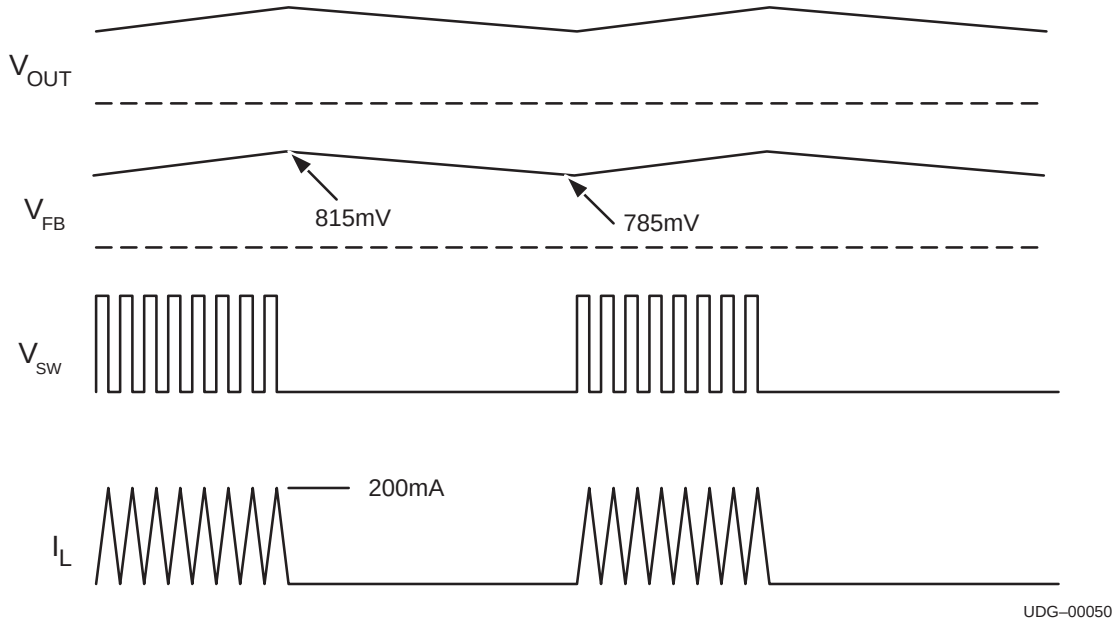


Figure 4. Typical Pulsed-Variable-Frequency Mode (PFM) Circuit Waveform

APPLICATION INFORMATION

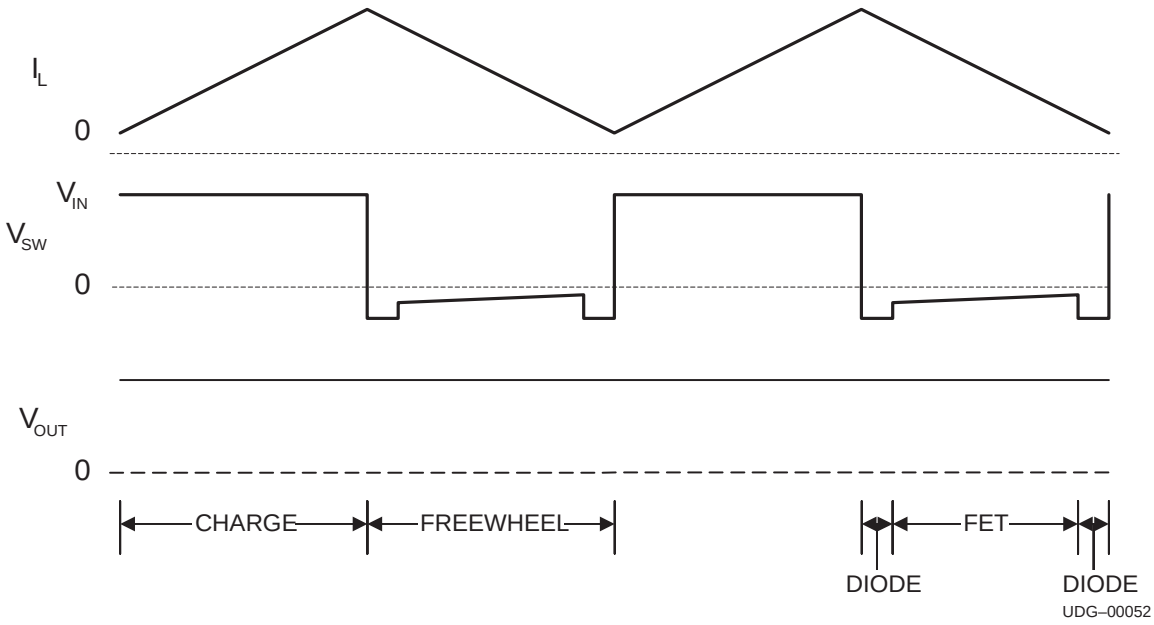


Figure 5. Typical Constant-Frequency Mode Circuit Waveforms

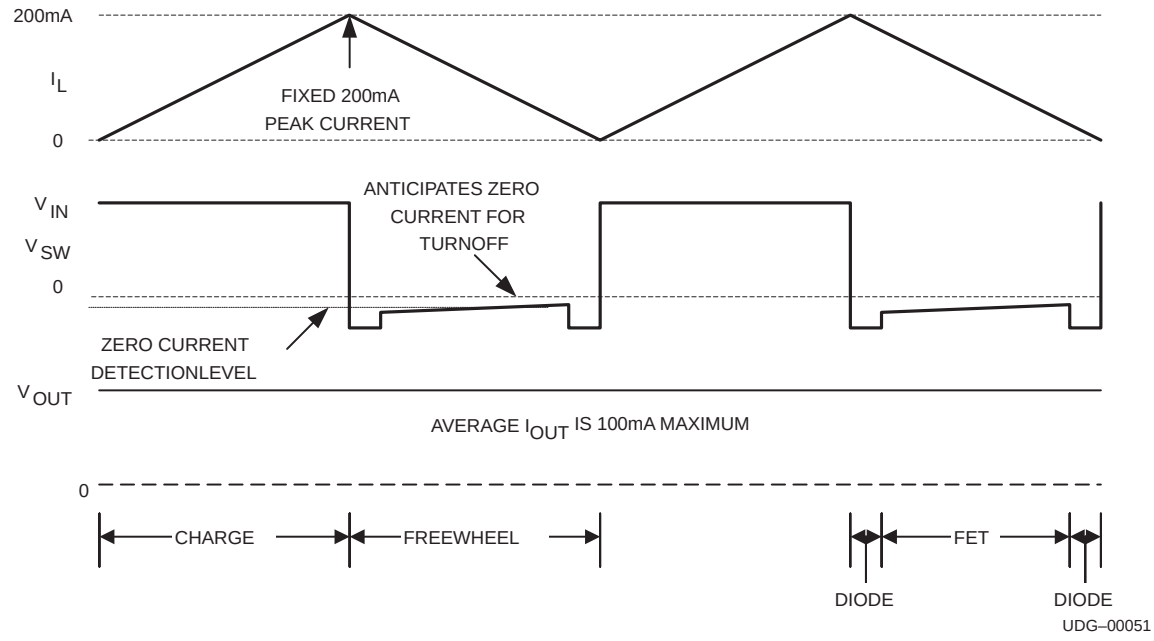
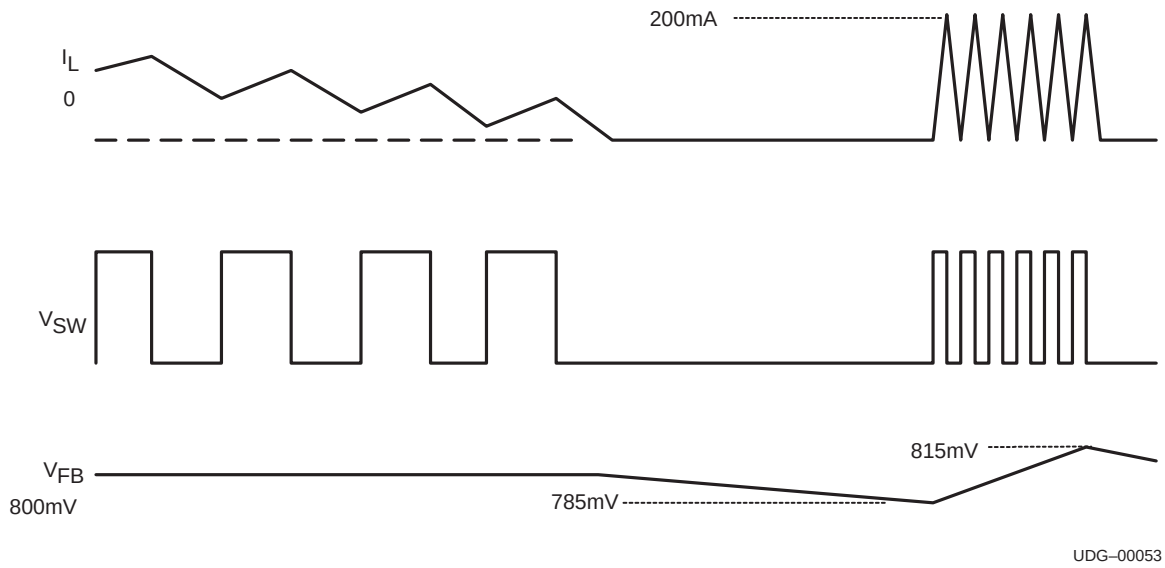


Figure 6. PFM Circuit Waveforms (Expanded View)

APPLICATION INFORMATION



NOTE A: Time scale not constant for CF and PFM modes.

Figure 7. Constant Frequency To PFM Transition

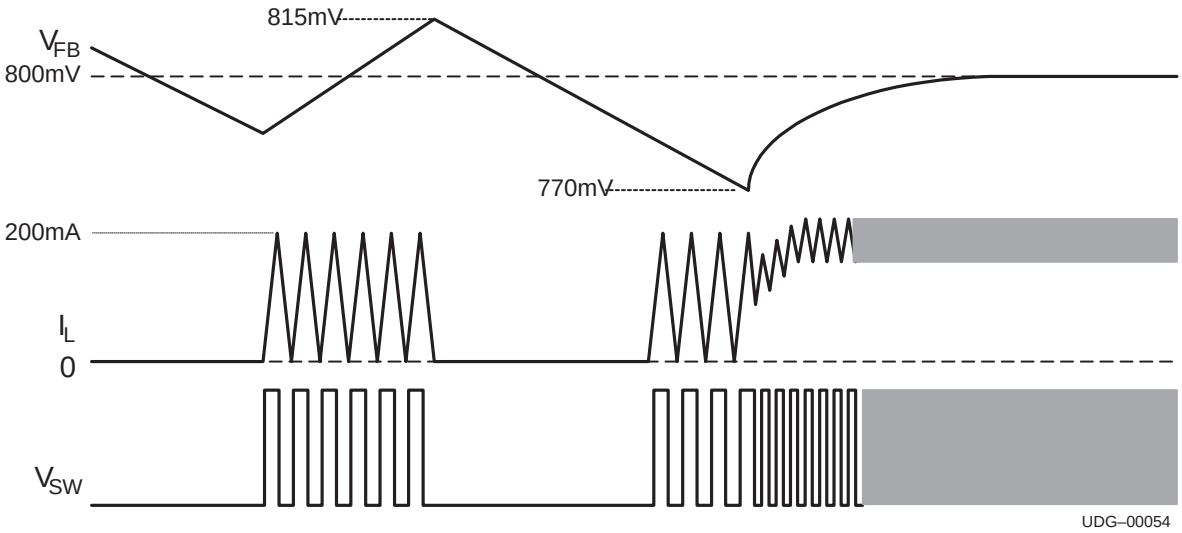


Figure 8. PFM to Constant Frequency Transition

APPLICATION INFORMATION

design example: automatic-mode switching converter, two li-ion cell input, 3.0-V output

Figure 9 shows the schematic of an automatic-mode switching converter based upon the TPS62102. The output current for this design can range from 0 mA to 500 mA.

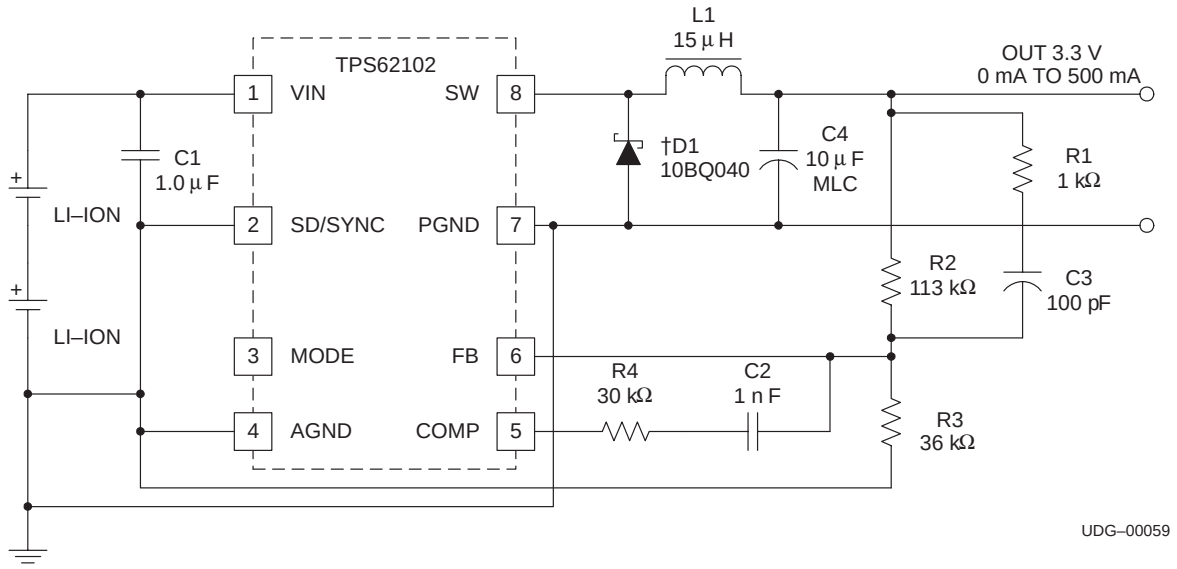


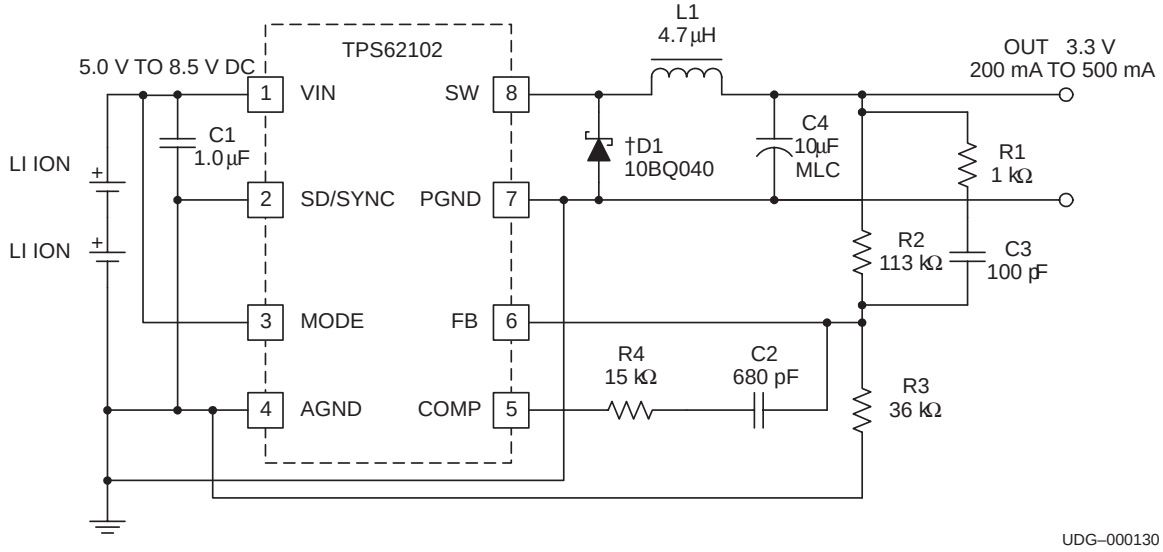
Figure 9. Automatic-Mode Switching Converter Application Circuit

† Optional

APPLICATION INFORMATION

design example: forced constant-frequency mode switching converter, two li-ion cell input, 3.0-V output

Figure 10 shows the schematic of a forced constant-frequency mode switching converter based upon the TPS62102. The output current for this design can range from 200 mA to 500 mA.



† Optional

Figure 10. Forced Constant-Frequency Mode Application Circuit

**AUTOMATIC MODE SWITCHING CONVERTER
OPEN LOOP GAIN AND PHASE RESPONSE
vs
FREQUENCY**

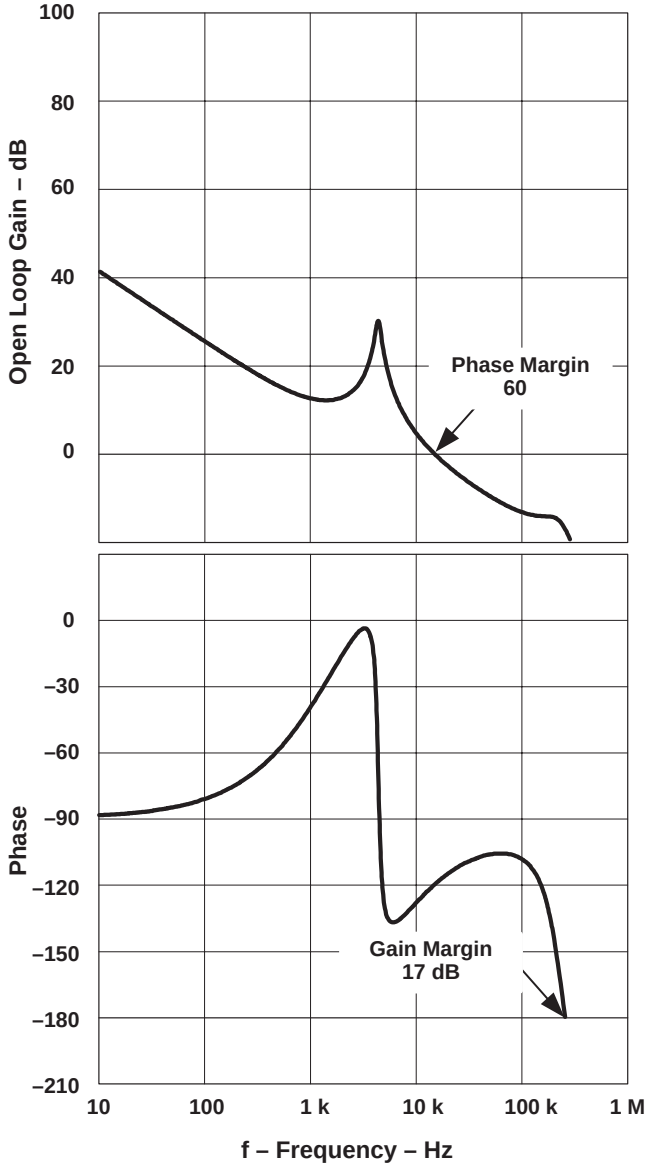


Figure 11

**FORCED CONSTANT FREQUENCY CONVERTER
OPEN LOOP GAIN AND PHASE RESPONSE
vs
FREQUENCY**

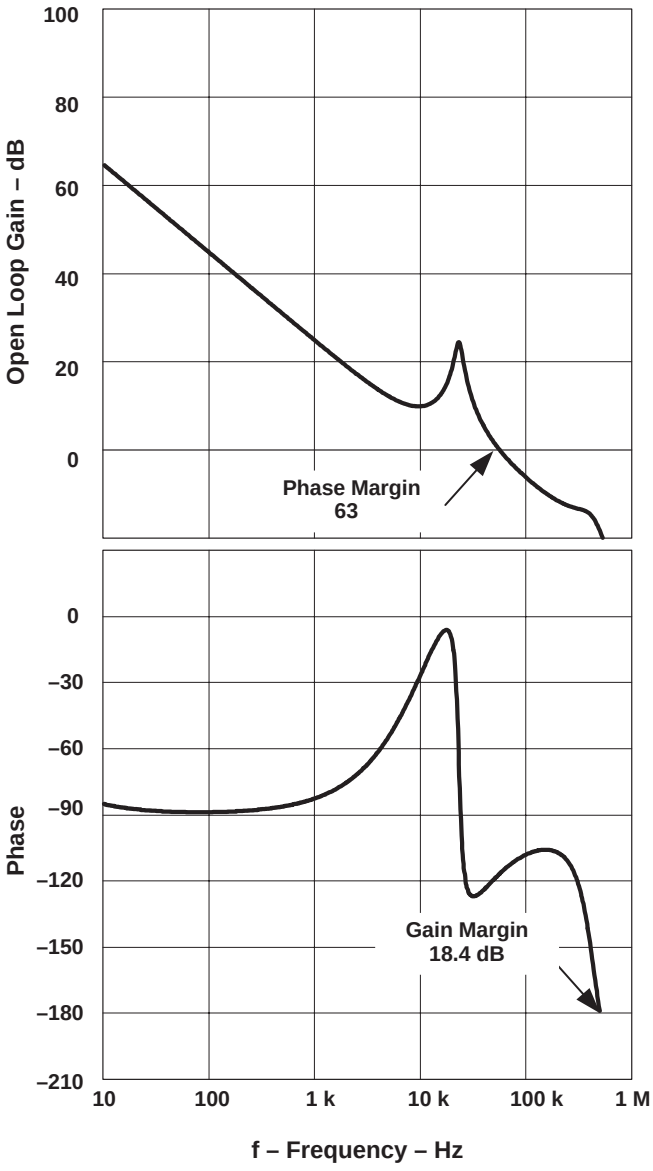
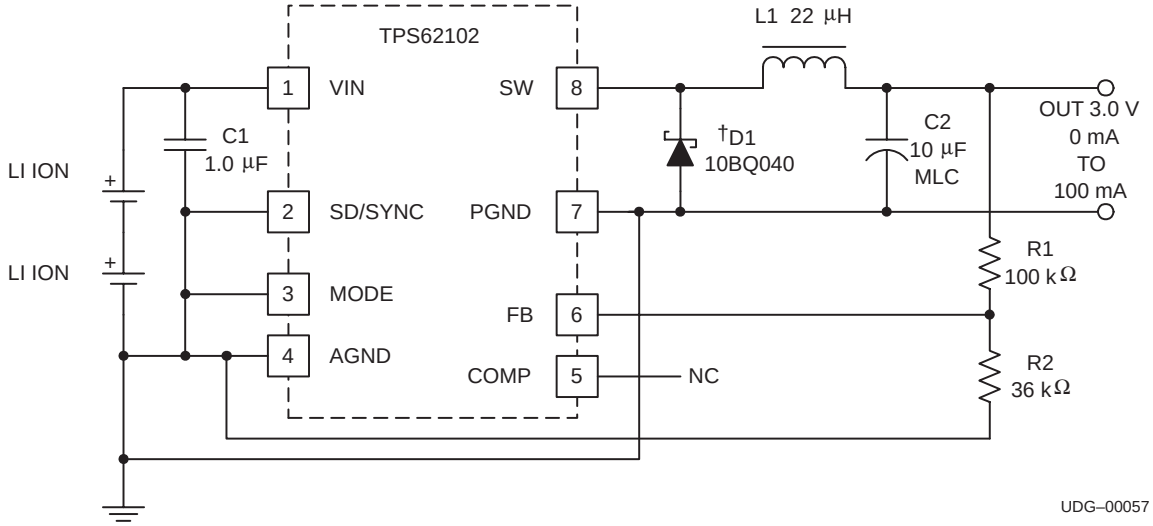


Figure 12

design example: forced variable-frequency mode switching converter, two li-ion cell input, 3.0-V output

Figure 13 shows the schematic of a forced variable-frequency mode switching converter based upon the TPS62102. The output current for this design can range from 0 mA to 100 mA.

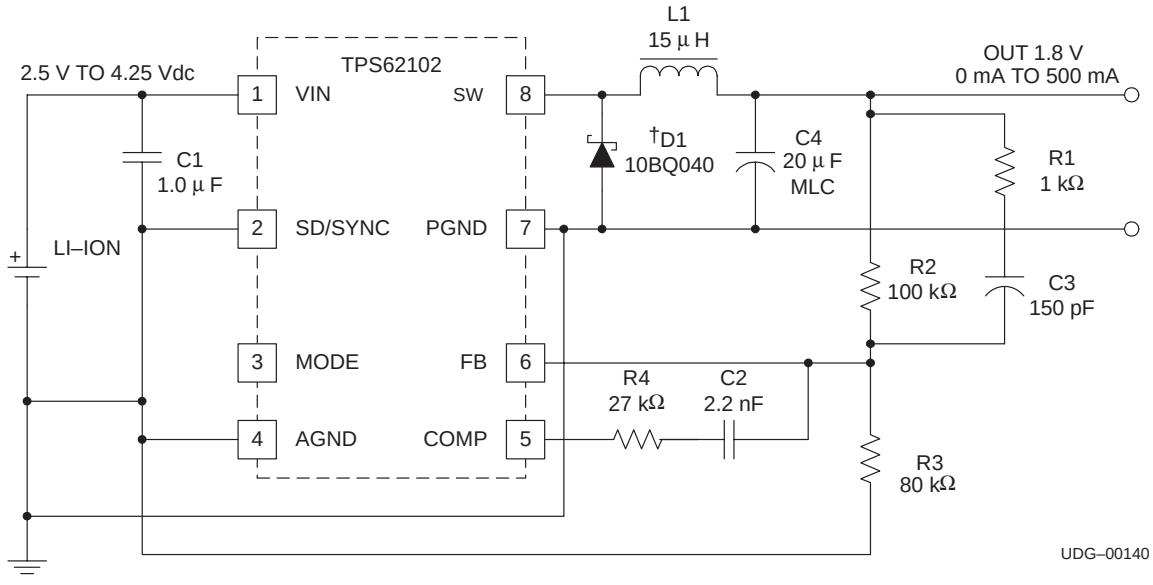


† Optional

Figure 13. Forced Variable-Frequency Mode Application Circuit

design example: automatic mode switching converter, single li-ion cell input, 1.8-V output

Figure 14 shows the schematic of an automatic-mode switching converter based upon the TPS62102. The output current for this design can range from 0 mA to 500 mA.



† Optional

Figure 14. 1.8-V Output Automatic-Mode Switching Converter Application Circuit

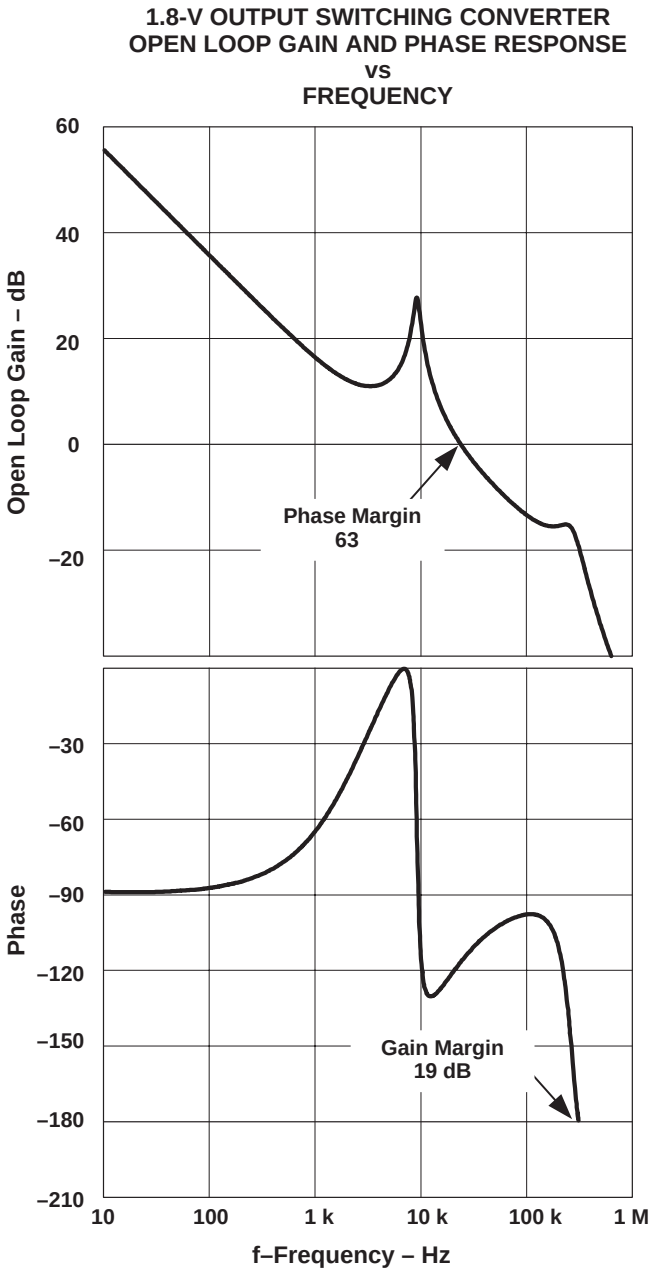

1.8-V OUTPUT SWITCHING CONVERTER
OPEN LOOP GAIN AND PHASE RESPONSE
vs
FREQUENCY
Open Loop Gain – dB
60
40
20
0
–20
Phase Margin
63
Phase
–30
–60
–90
–120
–150
–180
–210
Gain Margin
19 dB
10
100
1 k
10 k
100 k
1 M
f–Frequency – Hz

Figure 15

PARAMETER MEASUREMENT INFORMATION

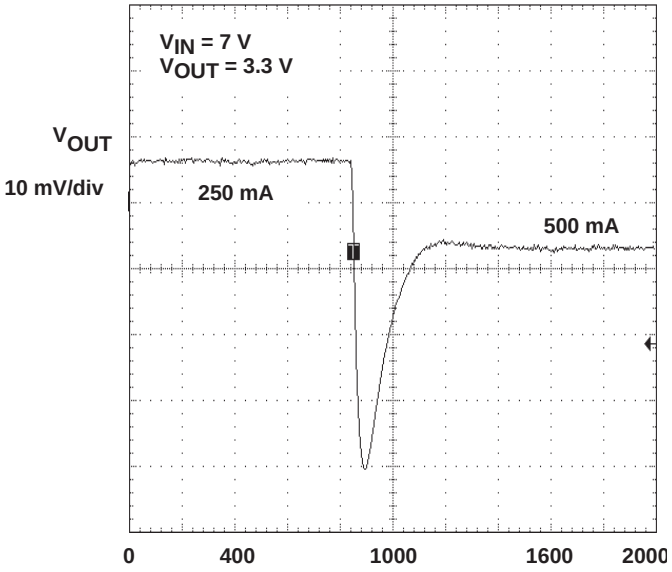


Figure 16. Load Step 250 mA Transition to 500 mA (Circuit Shown in Figure 9.)

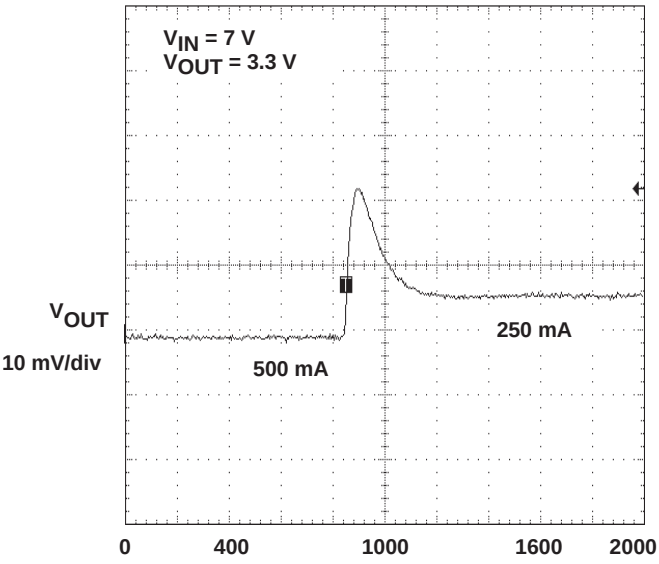


Figure 17. Load Step 500 mA Transition to 250 mA (Circuit Shown in Figure 9.)

TYPICAL CHARACTERISTICS

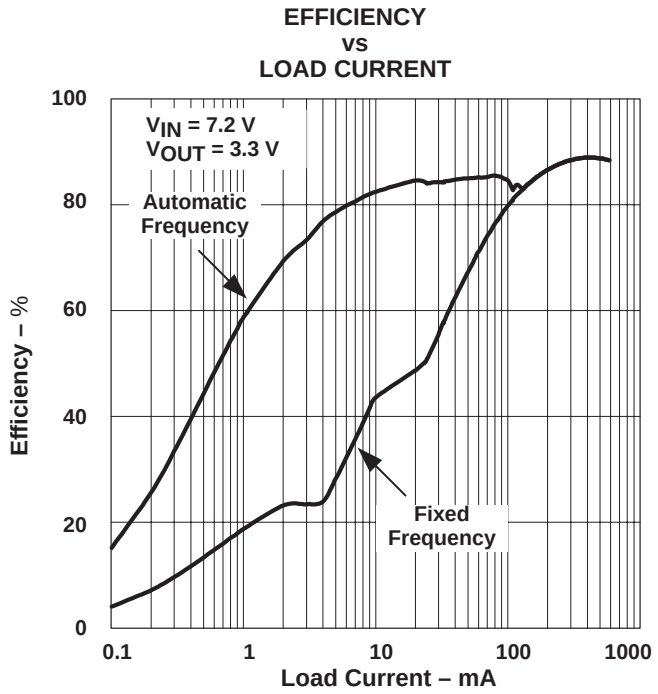


Figure 18

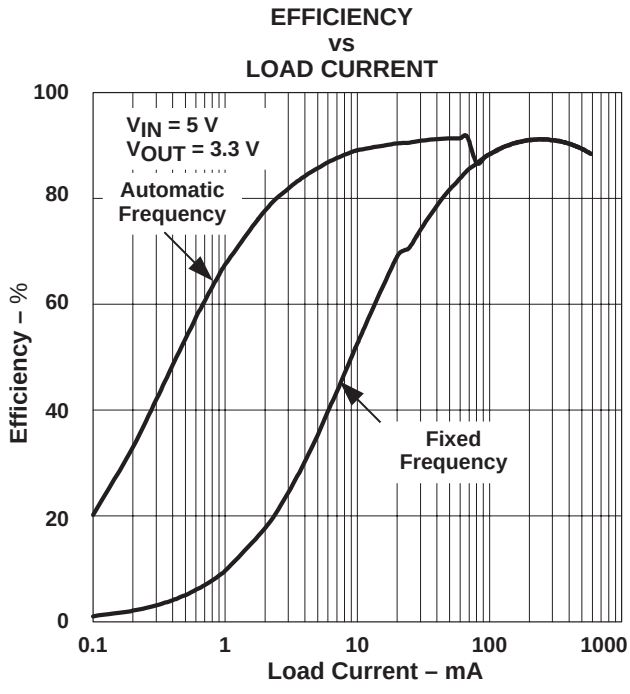


Figure 19

TYPICAL CHARACTERISTICS

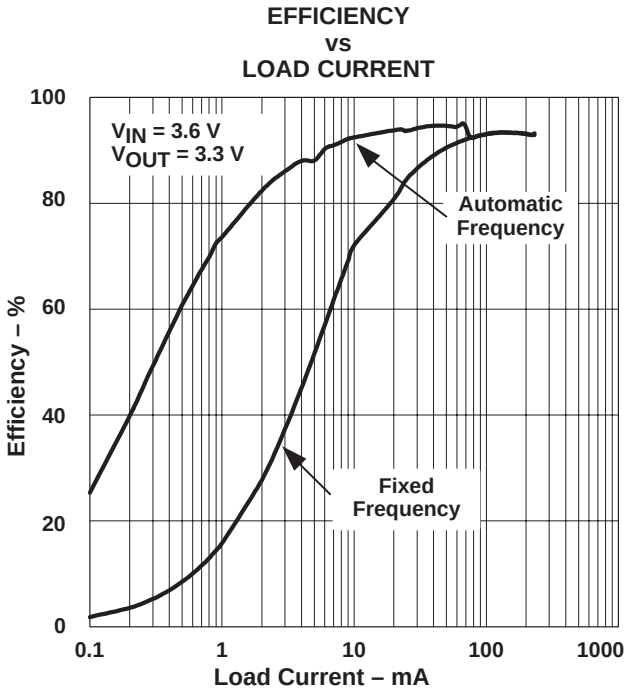


Figure 20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62100D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	62100	Samples
TPS62101D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	62101	Samples
TPS62101DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	62101	Samples
TPS62102D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	62102	Samples
TPS62103D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	62103	Samples
TPS62103DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	62103	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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