TPS65012 Power and Battery Management IC for Li-Ion Powered Systems

1 Features

- Linear Charger Management for Single Li-Ion or Li-Polymer Cells
- Dual Input Ports for Charging From USB or From Wall Plug, Handles 100-mA and 500-mA USB Requirements
- Charge Current Programmable via External Resistor
- 1-A, 95% Efficient Step-Down Converter for I/O and Peripheral Components (VMAIN)
- 400-mA, 90% Efficient Step-Down Converter for Processor Core (VCORE)
- 2x 200-mA LDOs for I/O and Peripheral Components, LDO Enable via Bus
- Serial Interface Compatible With I^2C, Supports 100-kHz, 400-kHz Operation
- LOW_PWR Pin to Lower or Disable Processor Core Supply Voltage in Deep Sleep Mode
- 70-µA Quiescent Current
- 1% Reference Voltage
- Thermal Shutdown Protection

2 Applications

- All Single Li-Ion Cell-Operated Products Requiring Multiple Supplies Including:
  - PDA
  - Cellular and Smart Phone
  - Internet Audio Player
  - Digital Still Camera
- Digital Radio Player
- Split Supply DSP and µP Solutions

3 Description

The TPS65012 device is an integrated power and battery management IC for applications powered by one Li-Ion or Li-Polymer cell and which require multiple power rails. The TPS65012 device provides two highly efficient, 1.25–MHz step down converters targeted at providing the core voltage and peripheral, I/O rails in a processor-based system. Both step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents. The TPS65012 device also integrates two 200-mA LDO voltage regulators, which are enabled via the serial interface. Each LDO operates with an input voltage range between 1.8 V and 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the battery.

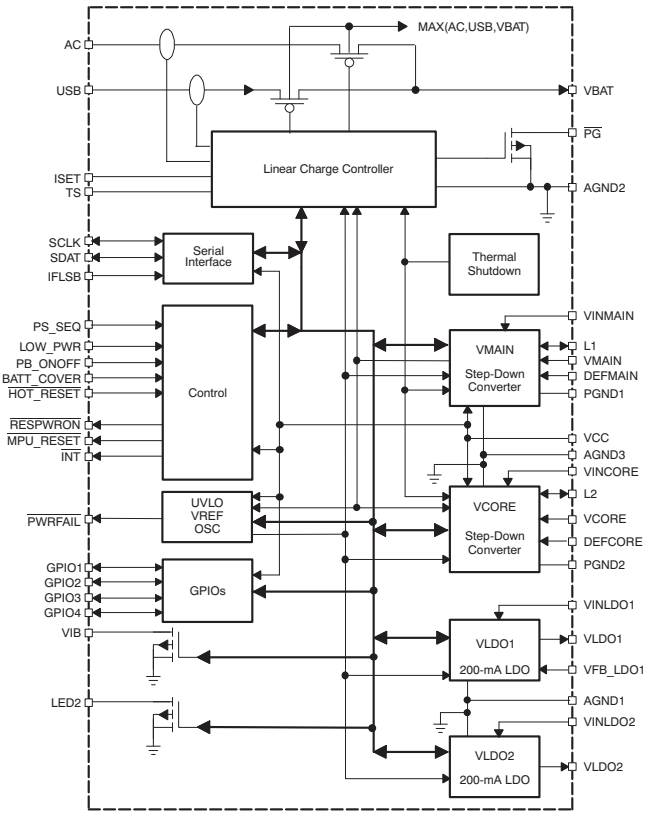
The TPS65012 device has a highly integrated and flexible Li-Ion linear charger and system power management. It offers integrated USB-port and AC-adapter supply management with autonomous power-source selection, power FET and current sensor, high accuracy current and voltage regulation, charge status, and charge termination.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65012	VQFN (48)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Block Diagram



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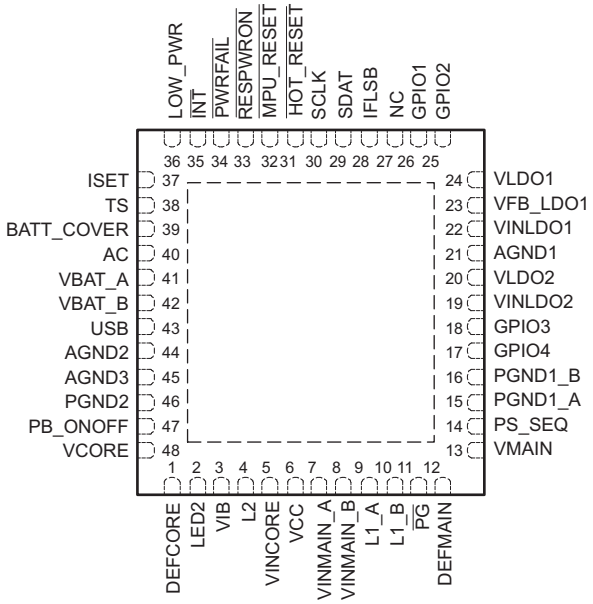
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2005) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



NC - No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CHARGER SECTION			
AC	40	I	Charger input voltage from AC adapter. The AC pin can be left open or can be connected to ground if the charger is not used.
AGND2	44		Analog ground connection. All analog ground pins are connected internally on the chip.
ISET	37	I	External charge current setting resistor connection for use with AC adapter
NC	27		Connect this pin to GND.
$\overline{PG}$	11	O	Indicates when a valid power supply is present for the charger (open drain)
Thernal Pad	-		Connect the thermal pad to GND
TS	38	I	Battery temperature sense input
USB	43	I	Charger input voltage from USB port. The USB pin can be left open or can be connected to ground if the charger is not used.
VBAT_A	41	I	Sense input for the battery voltage. Connect directly with the battery.
VBAT_B	42	O	Power output of the battery charger. Connect directly with the battery.
SWITCHING REGULATOR SECTION			
AGND3	45		Analog ground connection. All analog ground pins are connected internally on the chip.
L1_A, L1_B	9,10		Switch pin of VMAIN converter. The VMAIN inductor is connected here.
L2	4		Switch pin of VCORE converter. The VCORE inductor is connected here.
PGND1_A, PGND1_B	15,16		Power ground for VMAIN converter
PGND2	46		Power ground for VCORE converter
VCC	6	I	Power supply for digital and analog circuitry of MAIN and CORE DC-DC converters. This must be connected to the same voltage supply as VINCORE and VINMAIN. Also supplies serial interface block
VCORE	48	I	VCORE feedback voltage sense input, connect directly to VCORE

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VINCORE	5	I	Input voltage for VCORE step-down converter. This must be connected to the same voltage supply as VINMAIN and VCC.
VINMAIN_A, VINMAIN_B	7,8	I	Input voltage for VMAIN step-down converter. This must be connected to the same voltage supply as VINCORE and VCC.
VMAIN	13	I	VMAIN feedback voltage sense input, connect directly to VMAIN
LDO REGULATOR SECTION			
AGND1	21		Analog ground connection. All analog ground pins are connected internally on the chip.
VFB_LDO1	23	I	Feedback input from external resistive divider for LDO1
VINLDO1	22	I	Input voltage for LDO1
VINLDO2	19	I	Input voltage for LDO2
VLDO1	24	O	Output voltage for LDO1
VLDO2	20	O	Output and feedback voltage for LDO2
DRIVER SECTION			
LED2	2	O	LED driver, with blink rate programmable via serial interface
VIB	3	O	Vibrator driver, enabled via serial interface
CONTROL AND I2C SECTION			
BATT_COVER	39	I	Indicates if battery cover is in place
DEFCORE	1	I	Input signal indicating default VCORE voltage, 0 = 1.5 V, 1 = 1.6 V
DEFMAIN	12	I	Input signal indicating default VMAIN voltage, 0 = 3.0 V, 1 = 3.3 V
GPIO1	26	I/O	General-purpose open-drain input/output
GPIO2	25	I/O	General-purpose open-drain input/output
GPIO3	18	I/O	General-purpose open-drain input/output
GPIO4	17	I/O	General-purpose open-drain input/output
$\overline{\text{HOT\_RESET}}$	31	I	Push-button reset input used to reboot or wakeup processor via TPS65012
IFLSB	28	I	LSB of serial interface address used to distinguish two devices with the same address
$\overline{\text{INT}}$	35	O	Indicates a charge fault or termination, or if any of the regulator outputs are below the lower tolerance level, active low (open drain)
LOW_PWR	36	I	Input signal indicating deep sleep mode, VCORE is lowered to predefined value or disabled
$\overline{\text{MPU\_RESET}}$	32	O	Open-drain reset output generated by user activated $\overline{\text{HOT\_RESET}}$
PB_ONOFF	47	I	Push-button enable pin, also used to wakeup processor from *low-power* mode
PS_SEQ	14	I	Sets power-up/down sequence of step-down converters
$\overline{\text{PWRFAIL}}$	34	O	Open-drain output. Active low when UVLO comparator indicates low VBAT condition or when shutdown is about to occur due to an overtemperature condition or when the battery cover is removed (BATT_COVER has gone low).
$\overline{\text{RESPWRON}}$	33	O	Open-drain system reset output, generated according to the state of the LDO1 output voltage.
SCLK	30	I	Serial interface clock line
SDAT	29	I/O	Serial interface data/address

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Input voltage on VAC pin with respect to AGND		20	V
Input voltage range on all other pins except AGND/PGND pins with respect to AGND	–0.3	7	V
HBM and CBM capabilities at pins VIB, $\overline{PG}$, and LED2		1	kV
Current at AC, VBAT, VINMAIN, L1, PGND1		1800	mA
Peak current at all other pins		1000	mA
Continuous power dissipation	See *Dissipation Ratings*		
Operating free-air temperature, T_A	–40	85	°C
Maximum junction temperature, T_J		125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature range ,T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±1000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{(AC)}$	Supply voltage from AC adapter	4.5		5.5	V
$V_{(USB)}$	Supply voltage from USB	4.4		5.25	V
$V_{I(MAIN)}$,$V_{I(CORE)}$,V_{CC}	Input voltage range step-down converters	2.5		6.0	V
$V_{O(MAIN)}$	Output voltage range for main step-down convertor	2.5		3.3	V
$V_{I(LDO1)}$, $V_{I(LDO2)}$	Input voltage range for LDOs	1.8		6.5	V
T_A	Operating ambient temperature range	-40		85	°C
T_J	Operating junction temperature range	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS65012 RGZ (VQFN) 48 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)} = 3.6$ V, T_A = -40°C to 85°C, typical values are at T_A = 25°C battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL SIGNALS: LOW_PWR, SCLK, SDAT (INPUT)						
V_{IH}	High level input voltage	I_{IH} = 20 µA (1)	2		V_{CC}	V
V_{IL}	Low level input voltage	I_{IL} = 10 µA	0		0.8	V
I_{IB}	Input bias current			0.01	1.0	µA
CONTROL SIGNALS: PB_ONOFF, $\overline{\text{HOT\_RESET}}$, BATT_COVER						
V_{IH}	High level input voltage	I_{IH} = 20 µA(1)	0.8 V_{CC}		6	V
V_{IL}	Low level input voltage	I_{IL} = 10 µA	0		0.4	V
$R_{(pb\_onoff)}$	Pulldown resistor at PB_ONOFF			1000		kΩ
$R_{(hot\_reset)}$	Pullup resistor at $\overline{\text{HOT\_RESET}}$, connected to VCC			1000		kΩ
$R_{(batt\_cover)}$	Pulldown resistor at BATT_COVER			2000		kΩ
$t_{(glitch)}$	De-glitch time at all 3 pins		38	56	77	ms
$t_{(batt\_cover)}$	Delay after $t_{(glitch)}$ ($\overline{\text{PWRFAIL}}$ goes low) before supplies are disabled when BATT_COVER goes low.		1.68	2.4	3.2	ms
CONTROL SIGNALS: $\overline{\text{MPU\_RESET}}$, $\overline{\text{PWRFAIL}}$, $\overline{\text{RESPWRON}}$, $\overline{\text{INT}}$, SDAT (OUTPUT)						
V_{OH}	High level output voltage				6	V
V_{OL}	Low level output voltage	I_{IL} = 10 mA	0		0.3	V
$t_{d(mpu\_nreset)}$	Duration of low pulse at $\overline{\text{MPU\_RESET}}$		100			µs
$t_{d(nrespwron)}$	Duration of low pulse at $\overline{\text{RESPWRON}}$ after VLDO1 is in regulation	CHGCONFIG<7> = 0 (Default)	800	1000	1200	ms
		CHGCONFIG<7> = 1	49	69	89	
$t_{d(uvlo)}$	Time between UVLO going active ($\overline{\text{PWRFAIL}}$ going low) and supplies being disabled		1.68	2.4	3.2	ms
$t_{d(overtemp)}$	Time between chip over-temperature condition being recognized ($\overline{\text{PWRFAIL}}$ going low) and supplies being disabled		1.68	2.4	3.2	ms
SUPPLY PIN: VCC						
$I_{(Q)}$	Operating quiescent current	V_I = 3.6 V, current into Main + Core + V_{CC}			58	µA
$I_{O(SD)}$	Shutdown supply current	V_I = 3.6 V, BATT_COVER = GND, Current into Main + Core + V_{CC}		15	25	µA
VMAIN STEP-DOWN CONVERTER						
V_I	Input voltage range		2.5		6.0	V
I_O	Maximum output current		1000			mA
$I_{O(SD)}$	Shutdown supply current	BATT_COVER = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance	$V_{I(MAIN)} = V_{GS}$ = 3.6 V		110	210	mΩ
$I_{lkg(p)}$	P-channel leakage current	$V_{(DS)}$ = 6.0 V			1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance	$V_{I(MAIN)} = V_{GS}$ = 3.6 V		110	200	mΩ
$I_{lkg(N)}$	N-channel leakage current	$V_{(DS)}$ = 6.0 V			1	µA
I_L	P-channel current limit	2.5 V< $V_{I(MAIN)}$ < 6.0 V	1.4	1.75	2.1	A
f_S	Oscillator frequency		1	1.25	1.5	MHz

(1) If the input voltage is higher than V_{CC}, an additional input current, limited by an internal 10-kΩ resister, flows.

Electrical Characteristics (continued)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)} = 3.6$ V, T_A = -40°C to 85°C, typical values are at T_A = 25°C battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(MAIN)}$	Fixed output voltage	2.5 V	$V_{I(MAIN)}$ = 2.7 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 2.7 V to 6.0 V; 0 mA ≤ I_O ≤ 1000 mA	3%		3%	
		2.75 V	$V_{I(MAIN)}$ = 2.95 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 2.95 V to 6.0 V; 0 mA ≤ I_O ≤ 1000 mA	3%		3%	
		3.0 V	$V_{I(MAIN)}$ = 3.2 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 3.2 V to 6.0 V; 0 mA ≤ I_O ≤ 1000 mA	3%		3%	
		3.3 V	$V_{I(MAIN)}$ = 3.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 3.5 V to 6.0 V; 0 mA ≤ I_O ≤ 1000 mA	3%		3%	
	Line regulation		$V_{I(MAIN)}$ = $V_{O(MAIN)}$ + 0.5 V (min. 2.5 V) to 6.0 V, I_O = 10 mA		0.5		%/V
	Load regulation		I_O = 10 mA to 1000 mA		0.12		%/A
$R_{(VMAIN)}$	VMAIN discharge resistance				400		Ω
VCORE STEP-DOWN CONVERTER							
V_I	Input voltage range			2.5		6.0	V
I_O	Maximum output current			400			mA
$I_{O(SD)}$	Shutdown supply current		BATT_COVER = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		$V_{I(CORE)}$ = V_{GS} = 3.6 V		275	530	mΩ
$I_{lkg(p)}$	P-channel leakage current		V_{DS} = 6.0 V		0.1	1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		$V_{I(CORE)}$ = V_{GS} = 3.6 V		275	500	mΩ
$I_{lkg(N)}$	N-channel leakage current		V_{DS} = 6.0 V		0.1	1	µA
I_L	P-channel current limit		2.5 V< $V_{I(CORE)}$ < 6.0 V	600	700	900	mA
f_S	Oscillator frequency			1	1.25	1.5	MHz
$V_{O(CORE)}$	Fixed output voltage	0.85 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA, C_O = 22 µF	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA, C_O = 22 µF	3%		3%	
		1.0 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA, C_O = 22 µF	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA, C_O = 22 µF	3%		3%	
		1.1 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA, C_O = 22 µF	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA, C_O = 22 µF	3%		3%	
		1.2 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O≤ 400 mA	3%		3%	
		1.3 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA	3%		3%	
		1.4 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA	3%		3%	
		1.5 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA	3%		3%	
		1.6 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA	3%		3%	
	Line regulation		$V_{I(CORE)}$ = $V_{O(MAIN)}$ + 0.5 V (min. 2.5 V) to 6.00 V, I_O = 10 mA		1		%/V

Electrical Characteristics (continued)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)} = 3.6$ V, T_A = -40°C to 85°C, typical values are at T_A = 25°C battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Load regulation	I_O = 10 mA to 400 mA		0.002		%/mA
$R_{(VCORE)}$	VCORE discharge resistance			400		Ω
VLDO1 AND VLDO2 LOW-DROPOUT REGULATORS						
V_I	Input voltage range		1.8		6.5	V
V_O	LDO1 output voltage range		0.9		VINLDO1	V
V_{ref}	Reference voltage		485	500	515	mV
V_O	LDO2 output voltage range		1.8		3.0	V
I_O	Maximum output current	Full-power mode	200			mA
		Low-power mode	30			
$I_{(SC)}$	LDO1 and LDO2 short-circuit current limit	VLDO1 = GND, VLDO2 = GND			600	mA
	Dropout voltage	I_O = 200 mA, VINLDO1,2 = 1.8 V			300	mV
	Total accuracy				±3%	
	Line regulation	VINLDO1,2 = VLDO1,2 + 0.5 V (min. 2.5 V) to 6.5 V, I_O = 10 mA		0.75		%/V
	Load regulation	I_O = 10 mA to 200 mA		0.011		%/mA
	Regulation time	Load change from 10% to 90%			0.1	ms
		Low-power mode		0.1		ms
$I_{(QFP)}$	LDO quiescent current (each LDO)	Full-power mode		16	30	µA
$I_{(QLPM)}$	LDO quiescent current (each LDO)	Low-power mode		12	18	µA
$I_{O(SD)}$	LDO shutdown current (each LDO)			0.1	1	µA
$I_{lkg(FB)}$	Leakage current feedback			0.01	0.1	µA

6.6 Battery Charger Electrical Characteristics

$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)} = V_{(AC)}$ or $V_{(USB)}$, $I_{(TERM)} < I_O \le 1$ A, 0°C < T_A < 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(AC)}$	Input voltage range		4.5		5.5	V
$V_{(USB)}$	Input voltage range		4.35		5.25	V
$I_{CC(VCHG)}$	Supply current	$V_{(CHG)} > V_{(CHG)}$ min		1.2	2	mA
$I_{CC(SLP)}$	Sleep current	Sum of currents into VBAT pin, $V_{(CHG)} < V_{(SLP-ENTRY)}$, 0°C≤ T_J ≤ 85°C		2	5	µA
$I_{CC(STBY)}$	Standby current	Current into USB pin			45	µA
		Current into AC pin		200	400	
VOLTAGE REGULATOR						
V_O	Output voltage	$V_{(CHG)}$ min ≥ 4.5 V	4.15	4.20	4.25	V
V_{DO}	Dropout voltage ($V_{(AC)}$ - VBAT)	$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)}$, $I_{O(OUT)}$ = 1 A		500	800	mV
	Dropout voltage ($V_{(USB)}$ - VBAT)	$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)}$, $I_{O(OUT)}$ = 0.5 A		300	500	mV
	Dropout voltage ($V_{(USB)}$ - VBAT)	$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)}$, $I_{O(OUT)}$ = 0.1 A		100	150	mV
CURRENT REGULATION						
$I_{O(AC)}$	Output current range for AC operation(1)	$V_{CHG} \ge 4.5$ V, $V_{I(OUT)} > V_{(LOWV)}$, $V_{(AC)} - V_{I(BAT)} > V_{(DO-MAX)}$	100		1000	mA

(1) $$I_{O(AC)} = \frac{KSET \times V_{(SET)}}{R_{(ISET)}}$$

Battery Charger Electrical Characteristics (continued)

$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)} = V_{(AC)}$ or $V_{(USB)}$, $I_{(TERM)} < I_O \le 1$ A, 0°C < T_A < 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SET)}$	Output current set voltage for AC operation at ISET pin. 100% output current I^2C register CHGCONFIG<4:3> = 11	$V_{min} \ge 4.5$ V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{(AC)} - V_{I(BAT)} > V_{(DO-MAX)}$	2.45	2.50	2.55	V
	75% output current I^2C register CHGCONFIG<4:3> = 10		1.83	1.91	1.99	V
	50% output current I^2C register CHGCONFIG<4:3> = 01		1.23	1.31	1.39	V
	32% output current I^2C register CHGCONFIG<4:3> = 00		0.76	0.81	0.86	V
KSET	Output current set factor for AC operation	100 mA < I_O < 1000 mA	310	330	350	
		10 mA < I_O < 100 mA	300	340	380	
$I_{O(USB)}$	Output current range for USB operation	$V_{(CHG)}$ min ≥ 4.35 V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{(USB)} - V_{I(BAT)} > V_{(DO-MAX)}$, I^2C register CHGCONFIG<2> = 0	80		100	mA
		$V_{(CHG)}$ min ≥ 4.5 V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{USB} - V_{I(BAT)} > V_{(DO-MAX)}$, I^2C register CHGCONFIG<2> = 1	400		500	mA
$R_{(ISET)}$	Resistor range at ISET pin		825		8250	Ω
PRECHARGE CURRENT REGULATION, SHORT-CIRCUIT CURRENT, AND BATTERY DETECTION CURRENT						
$V_{(LOWV)}$	Precharge to fast-charge transition threshold, voltage on VBAT pin.	$V_{(CHG)}$ min ≥ 4.5 V	2.8	3.0	3.2	V
	De-glitch time	$V_{(CHG)}$ min ≥ 4.5 V, $V_{I(OUT)}$ decreasing below threshold; 100-ns fall time, 10-mV overdrive	250	375	500	ms
$I_{(PRECHG)}$	Precharge current (2)	$0 \le V_{I(OUT)} < V_{(LOWV)}$, $t < t_{(PRECHG)}$	10		100	mA
$I_{(DETECT)}$	Battery detection current			200		µA
$V_{(SET-PRECHG)}$	Voltage at ISET pin	$0 \le V_{I(OUT)} < V_{(LOWV)}$, $t < t_{(PRECHG)}$	240	255	270	mV
CHARGE TAPER AND TERMINATION DETECTION						
$I_{(TAPER)}$	Taper current detect range (3)	$V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TAPER)}$	10		100	mA
$V_{(SET\_TAPER)}$	Voltage at ISET pin for charge TAPER detection	$V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TAPER)}$	235	250	265	mV
$V_{(SET\_TERM)}$	Voltage at ISET pin for charger termination detection(4)	$V_{I(OUT)} > V_{(RCH)}$	11	18	25	mV
	De-glitch time for $I_{(TAPER)}$	$V_{(CHG)}$ min ≥ 4.5 V, charging current increasing or decreasing above and below; 100-ns fall time, 10-mV overdrive	250	375	500	ms
	De-glitch time for $I_{(TERM)}$	$V_{(CHG)}$ min ≥ 4.5 V, charging current decreasing below;100-ns fall time, 10-mV overdrive	250	375	500	ms
TEMPERATURE COMPARATOR						
$V_{(LTF)}$	Low (cold) temperature threshold		2.475	2.50	2.525	V
$V_{(HTF)}$	High (hot) temperature threshold		0.485	0.5	0.515	V
$I_{(TS)}$	TS current source		95	102	110	µA
	De-glitch time for temperature fault		250	375	500	ms
BATTERY RECHARGE THRESHOLD						
$V_{(RCH)}$	Recharge threshold	$V_{(CHG)}$ min ≥ 4.5 V	$V_{O(REG)}$ - 0.115	$V_{O(REG)}$ - 0.1	$V_{O(REG)}$ - 0.085	V

$$I_{(PRECHG)} = \frac{KSET \times V_{(SET\_PRECHG)}}{R_{(ISET)}} \quad (2)$$

$$I_{(TAPER)} = \frac{KSET \times V_{(SET\_TAPER)}}{R_{(ISET)}} \quad (3)$$

$$I_{(TERM)} = \frac{KSET \times V_{(SET\_TERM)}}{R_{(ISET)}} \quad (4)$$

Battery Charger Electrical Characteristics (continued)

$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)} = V_{(AC)}$ or $V_{(USB)}$, $I_{(TERM)} < I_O \le 1$ A, 0°C < T_A < 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	De-glitch time		$V_{(CHG)}$ min ≥ 4.5 V, $V_{I(OUT)}$ decreasing below threshold; 100-ns fall time, 10-mV overdrive	250	375	500	ms
TIMERS							
$t_{(PRECHG)}$	Precharge timer		$V_{(CHG)}$ min ≥ 4.5 V	1500	1800	2160	s
$t_{(TAPER)}$	Taper timer		$V_{(CHG)}$ min≥ 4.5 V	1500	1800	2160	s
$t_{(CHG)}$	Charge timer		$V_{(CHG)}$ min≥ 4.5 V	15000	18000	21600	s
SLEEP AND STANDBY							
$V_{(SLP-ENTRY)}$	Sleep-mode entry threshold, $\overline{PG}$ output = high		2.3 V≤ $V_{I(OUT)}$ ≤ $V_{O(REG)}$			$V_{(CHG)}$≤ $V_{I(OUT)}$ +150 mV	V
$V_{(SLP\_EXIT)}$	Sleep-mode exit threshold,$\overline{PG}$ output = low		2.3 V≤ $V_{I(OUT)}$ ≤ $V_{O(REG)}$	$V_{(CHG)}$≥ $V_{I(OUT)}$+19 0 mV			V
	De-glitch time for sleep mode entry and exit		AC or USB decreasing below threshold; 100-ns fall time, 10-mV overdrive	200	375	500	ms
$t_{(USB\_DEL)}$	Delay between valid USB voltage being applied and start of charging process from USB				375		ms
CHARGER POWER-ON-RESET, UVLO, AND $V_{(IN)}$ RAMP RATE							
$V_{(CHGUVLO)}$	Charger under-voltage lockout		$V_{(CHG)}$ decreasing	2.27	2.5	2.75	V
	Hysteresis				27		mV
$V_{(CHGOVLO)}$	Charger over-voltage lockout		$V_{(AC)}$ increasing		6.6		V
	Hysteresis					0.5	V
CHARGER OVER TEMPERATURE SUSPEND							
$T_{(suspend)}$	Temperature at which charger suspends operation				145		°C
$T_{(hyst)}$	Hysteresis of suspend threshold				20		°C
LOGIC SIGNALS DEFMAIN, DEFCORE, PS_SEQ, IFLSB							
V_{IH}	High level input voltage		I_{IH} = 20 µA	V_{CC}-0.5		V_{CC}	V
V_{IL}	Low level input voltage		I_{IL} = 10 µA	0		0.4	V
I_{IB}	Input bias current				0.01	1.0	µA
LOGIC SIGNALS GPIO1-4							
V_{OL}	Low level output voltage		I_{OL} = 1 mA, configured as an open-drain output			0.3	V
V_{OH}	High level output voltage		Configured as an open-drain output			6	V
V_{IL}	Low level input voltage			0		0.8	V
V_{IH}	High level input voltage			2		V_{CC} (5)	V
I_I	Input leakage current					1	µA
$r_{DS(on)}$	Internal NMOS		V_{OL} = 0.3 V		150		Ω
LOGIC SIGNALS $\overline{PG}$, LED2							
V_{OL}	Low level output voltage		I_{OL} = 20 mA			0.5	V
V_{OH}	High level output voltage					6	V
VIBRATOR DRIVER VIB							
V_{OL}	Low level output voltage		I_{OL} = 100 mA		0.3	0.5	V
V_{OH}	High level output voltage					6	V
THERMAL SHUTDOWN							
$T_{(SD)}$	Thermal shutdown		Increasing junction temperature		160		°C
UNDERVOLTAGE LOCKOUT							
$V_{(UVLO)}$	Undervoltage lockout threshold	$V_{(UVLO)}$ 2.5 V	Filter resistor = 10R in series with V_{CC}, V_{CC} decreasing	-3%		3%	
		$V_{(UVLO)}$ 2.75 V		-3%		3%	
		$V_{(UVLO)}$ 3.0 V		-3%		3%	
	Default value	$V_{(UVLO)}$ 3.25 V		-3%		3%	

(5) If the input voltage is higher than V_{CC} an additional current, limited by an internal 10-k resistor, flows.

Battery Charger Electrical Characteristics (continued)

$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)} = V_{(AC)}$ or $V_{(USB)}$, $I_{(TERM)} < I_O \le 1$ A, 0°C < T_A < 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(UVLO\_HYST)}$	UVLO comparator hysteresis	V_{CC} rising	150		200	mV
POWER GOOD						
		VMAIN, VCORE, VLDO1, VLDO2 decreasing	-12%	-10%	-8%	
		VMAIN, VCORE, VLDO1, VLDO2 increasing	-7%	-5%	-3%	

6.7 Serial Interface Timing Requirements

		MIN	MAX	UNIT
f_{MAX}	Clock frequency		400	kHz
$t_{wH(HIGH)}$	Clock high time	600		ns
$t_{wL(LOW)}$	Clock low time	1300		ns
t_R	DATA and CLK rise time		300	ns
t_F	DATA and CLK fall time		300	ns
$t_{h(STA)}$	Hold time (repeated) START condition (after this period the first clock pulse is generated)	600		ns
$t_{h(DATA)}$	Setup time for repeated START condition	600		ns
$t_{h(DATA)}$	Data input hold time	0		ns
$t_{su(DATA)}$	Data input setup time	100		ns
$t_{su(STO)}$	STOP condition setup time	600		ns
$t_{(BUF)}$	Bus free time	1300		ns

6.8 Dissipation Ratings

See (1)

THERMAL RESISTANCE(2) $R_{\Theta JA}$	DERATING FACTOR ABOVE T_A = 55°C	AMBIENT TEMPERATURE	MAX POWER DISSIPATION FOR T_j = 125°C
33°C/W	3 mW/°C	25°C	3 W
		55°C	2.1 W

(1) The TPS65012 is housed in a 48-pin QFN PowerPAD™ package with exposed leadframe on the underside.
(2) Thermal resistance when mounted on a JEDEC high-K board. Consideration needs to be given to the maximum charge current when the assembled application board exhibits a thermal impedance which differs significantly from the JEDEC high-K board.

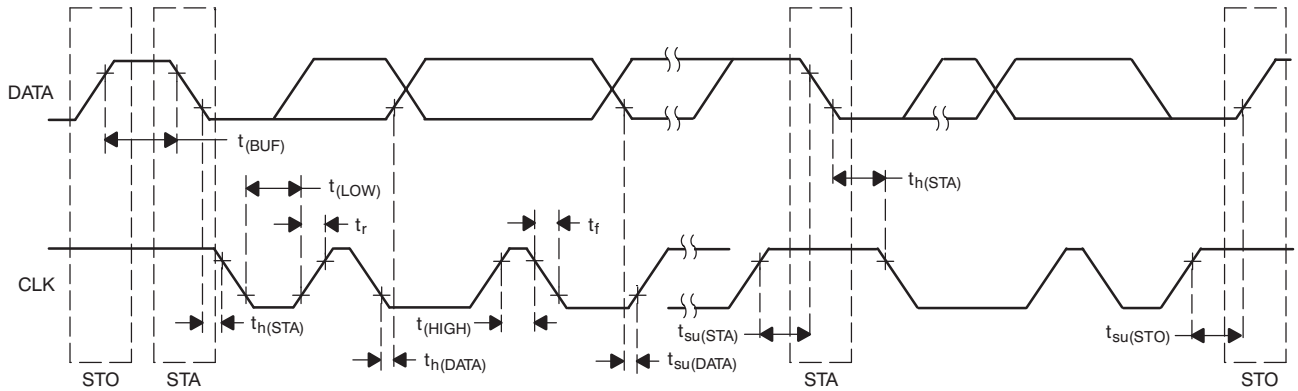


Figure 1. Serial Interface Timing Diagram

6.9 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Efficiency	vs Output current	Figure 2, Figure 3, Figure 4, Figure 5
Quiescent current	vs Input voltage	Figure 6
Switching frequency	vs Temperature	Figure 7
Output voltage	vs Output current	Figure 8, Figure 9
LDO1 Output voltage	vs Output current	Figure 10
LDO2 Output voltage	vs Output current	Figure 11
Line transient response (main)		Figure 12
Line transient response (core)		Figure 13
Line transient response (LDO1)		Figure 14
Line transient response (LDO2)		Figure 15
Load transient response (main)		Figure 16
Load transient response (core)		Figure 17
Load transient response (LDO1)		Figure 18
Load transient response (LDO2)		Figure 19
Output Voltage Ripple (PFM)		Figure 20
Output Voltage Ripple (PWM)		Figure 21
Start-up timing		Figure 22
Dropout voltage	vs Output current	Figure 23, Figure 24
PSRR (LDO1 and LDO2)	vs Frequency	Figure 25

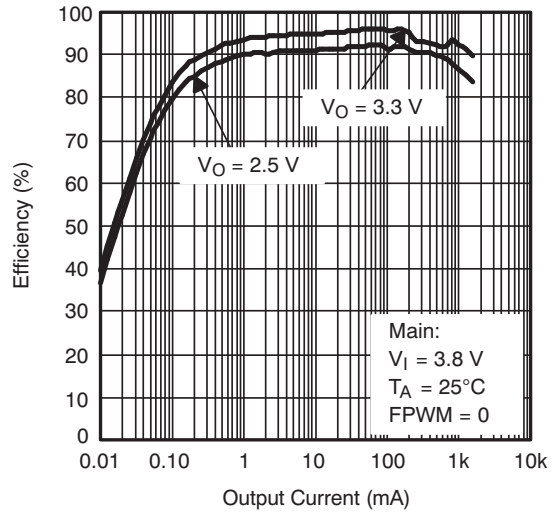


Figure 2. Efficiency vs Output Current

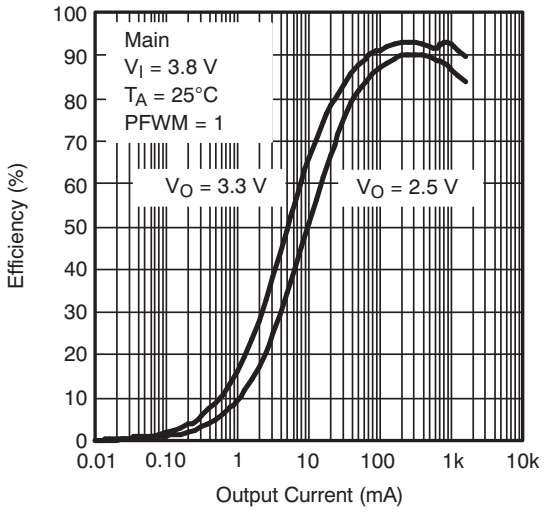


Figure 3. Efficiency vs Output Current

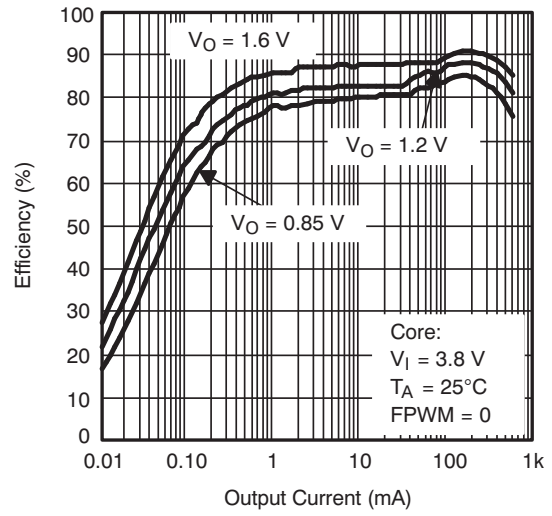


Figure 4. Efficiency vs Output Current

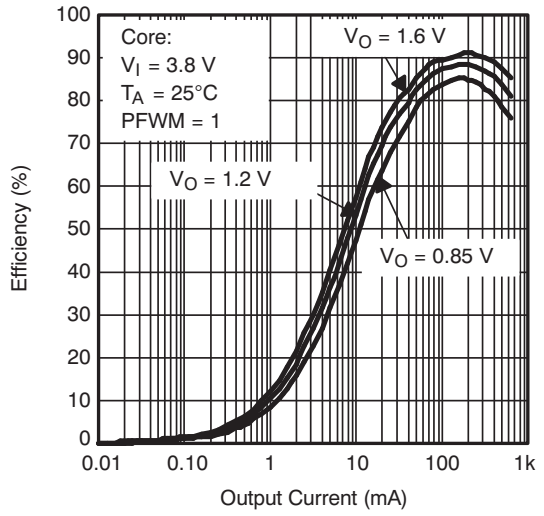


Figure 5. Efficiency vs Output Current

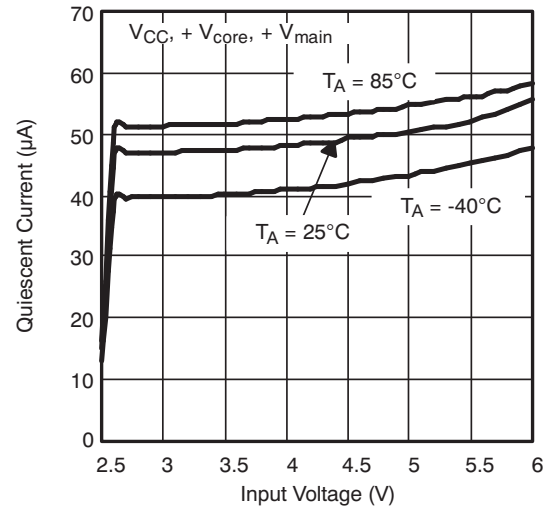


Figure 6. Quiescent Current vs Input Voltage

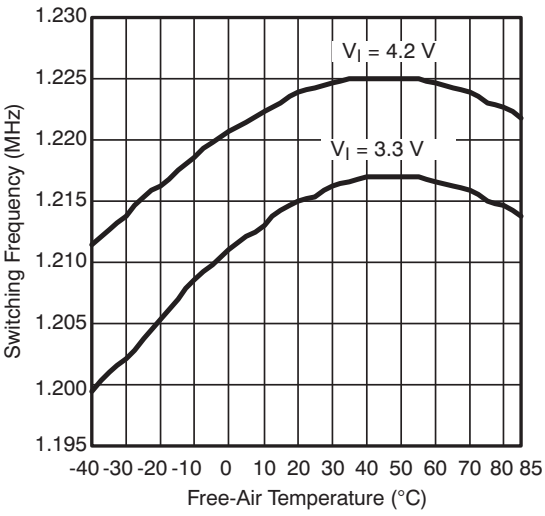


Figure 7. Switching Frequency vs Temperature

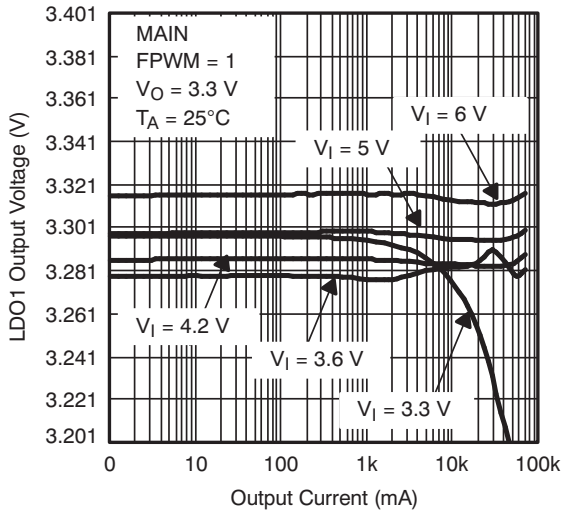


Figure 8. LDO1 Output Voltage vs Output Current

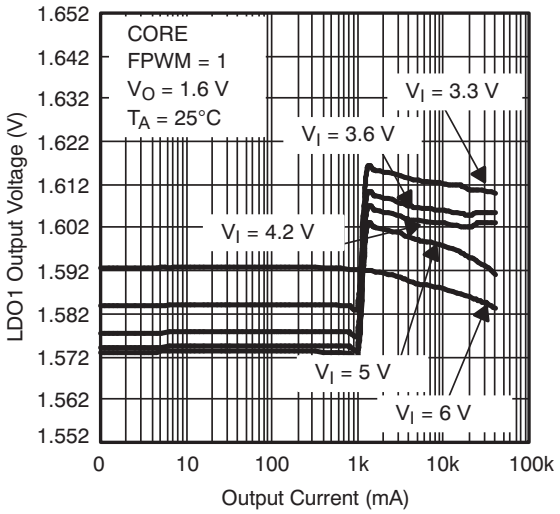


Figure 9. LDO1 Output Voltage vs Output Current

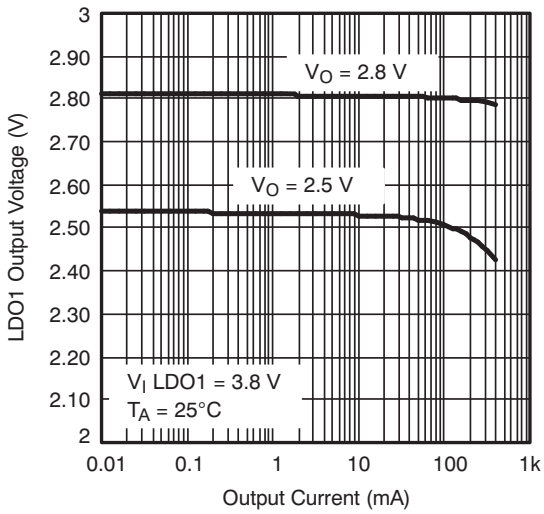


Figure 10. LDO1 Output Voltage vs Output Current

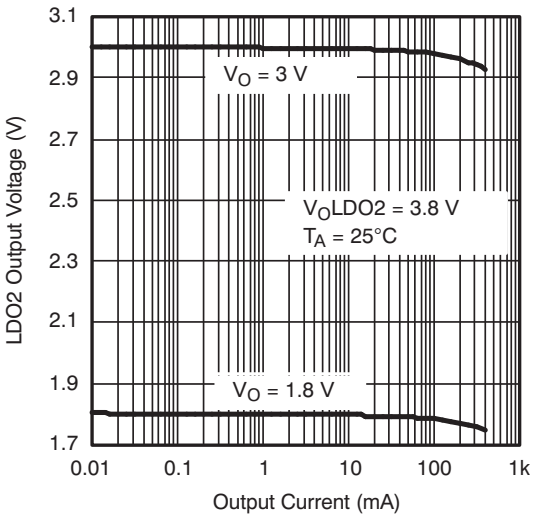


Figure 11. LDO2 Output Voltage vs Output Current

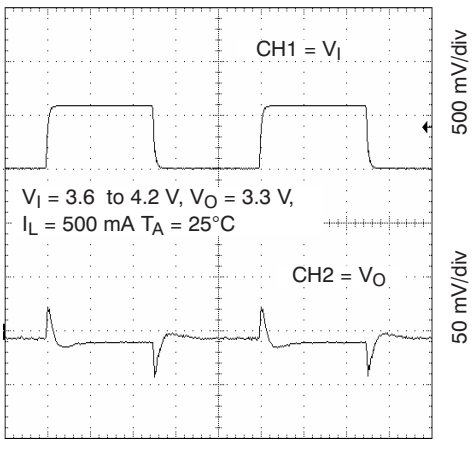


Figure 12. Line Transient Response (MAIN)

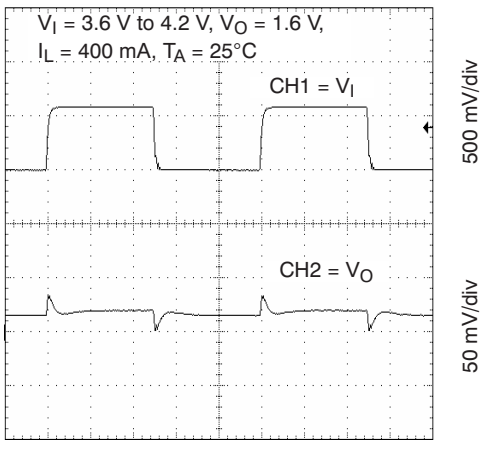


Figure 13. Line Transient Response (CORE)

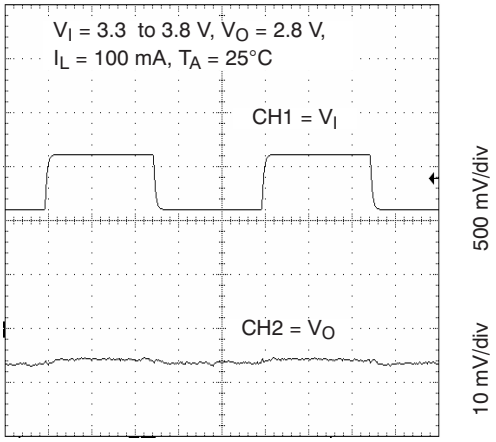


Figure 14. Line Transient Response (LDO1)

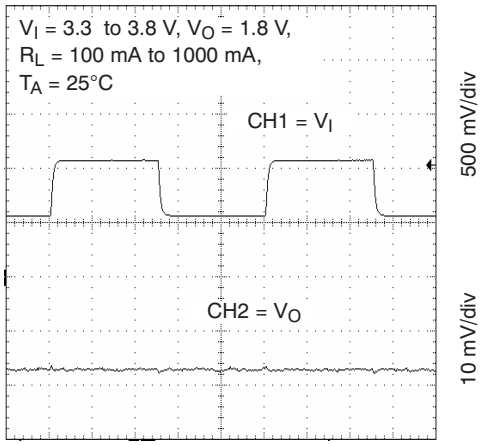


Figure 15. Line Transient Response (LDO2)

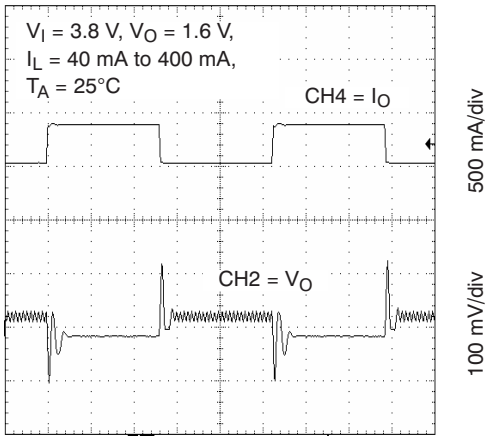


Figure 16. Line Transient Response (CORE)

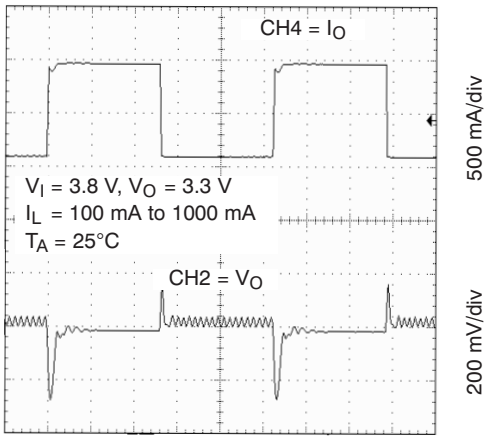


Figure 17. Line Transient Response (MAIN)

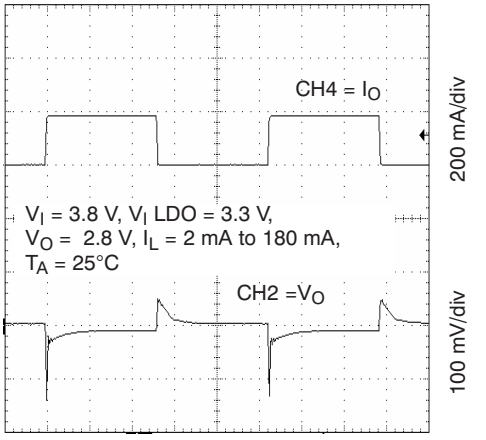


Figure 18. Line Transient Response (LDO1)

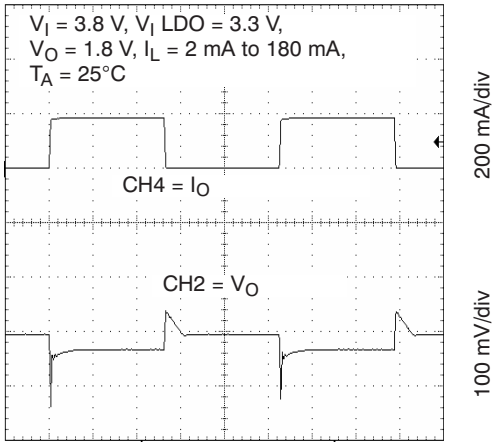
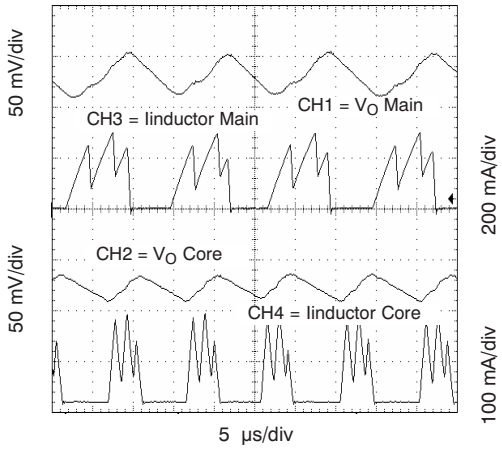
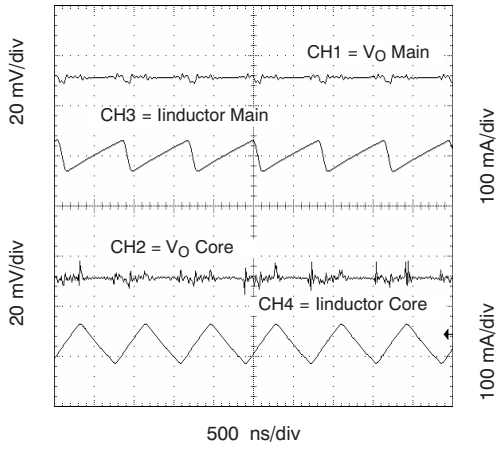


Figure 19. Line Transient Response (LDO2)



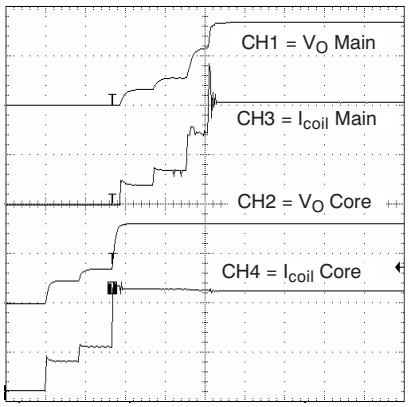
V_I = 3.8 V, T_A = 25°C
V_O Main = 3.3 V I_L Main = 100 mA,
V_O Core = 1.6 V, I_L Core = 40 mA

Figure 20. Output Ripple (PFM)



V_I = 3.8 V, T_A = 25°C
V_O Main = 3.3 V R_L Main = 500 mA,
V_O Core = 1.6 V, R_L Core = 400 mA

Figure 21. Output Ripple (PWM)



V_I = 3.8 V, V_O Main = 3.3 V,
R_L Main = 1 A, V_O Core = 1.6 V,
R_L Core = 400 mA, T_A = 25°C

Figure 22. Start-Up Timing

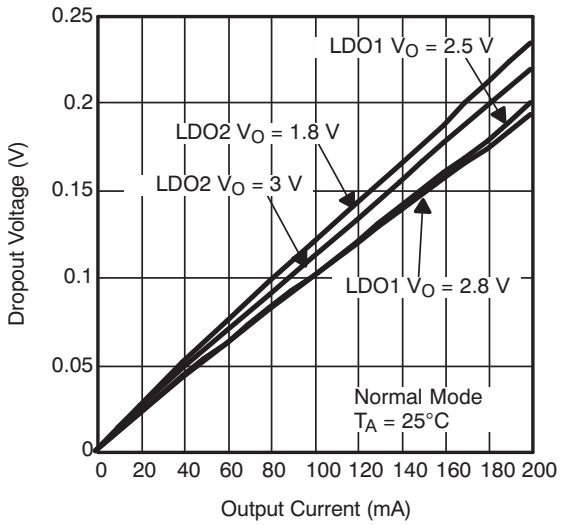


Figure 23. Dropout Voltage vs Output Current

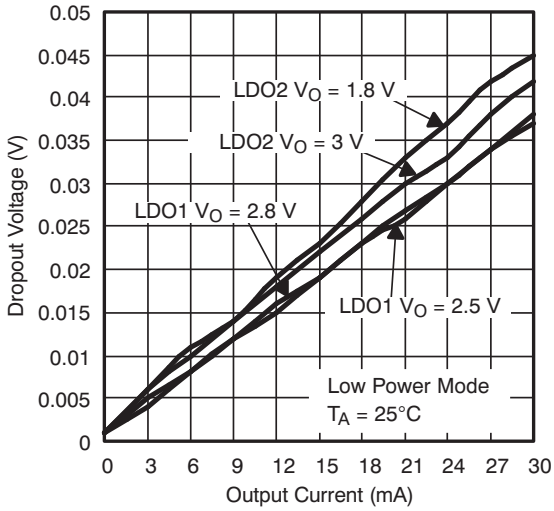


Figure 24. Dropout Voltage vs Output Current

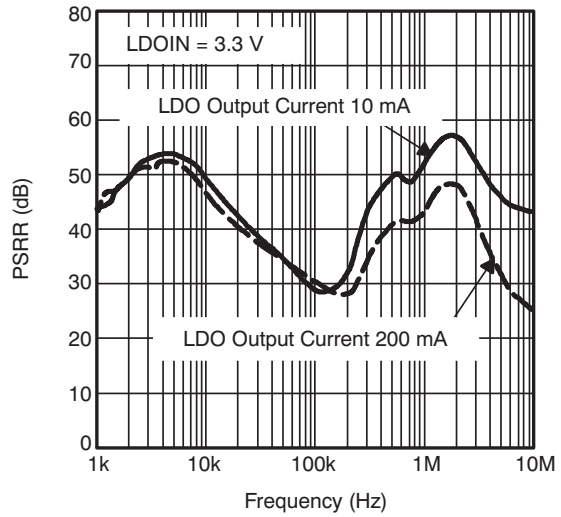


Figure 25. PSRR (LDO1, LDO2) vs Frequency

7 Detailed Description

7.1 Overview

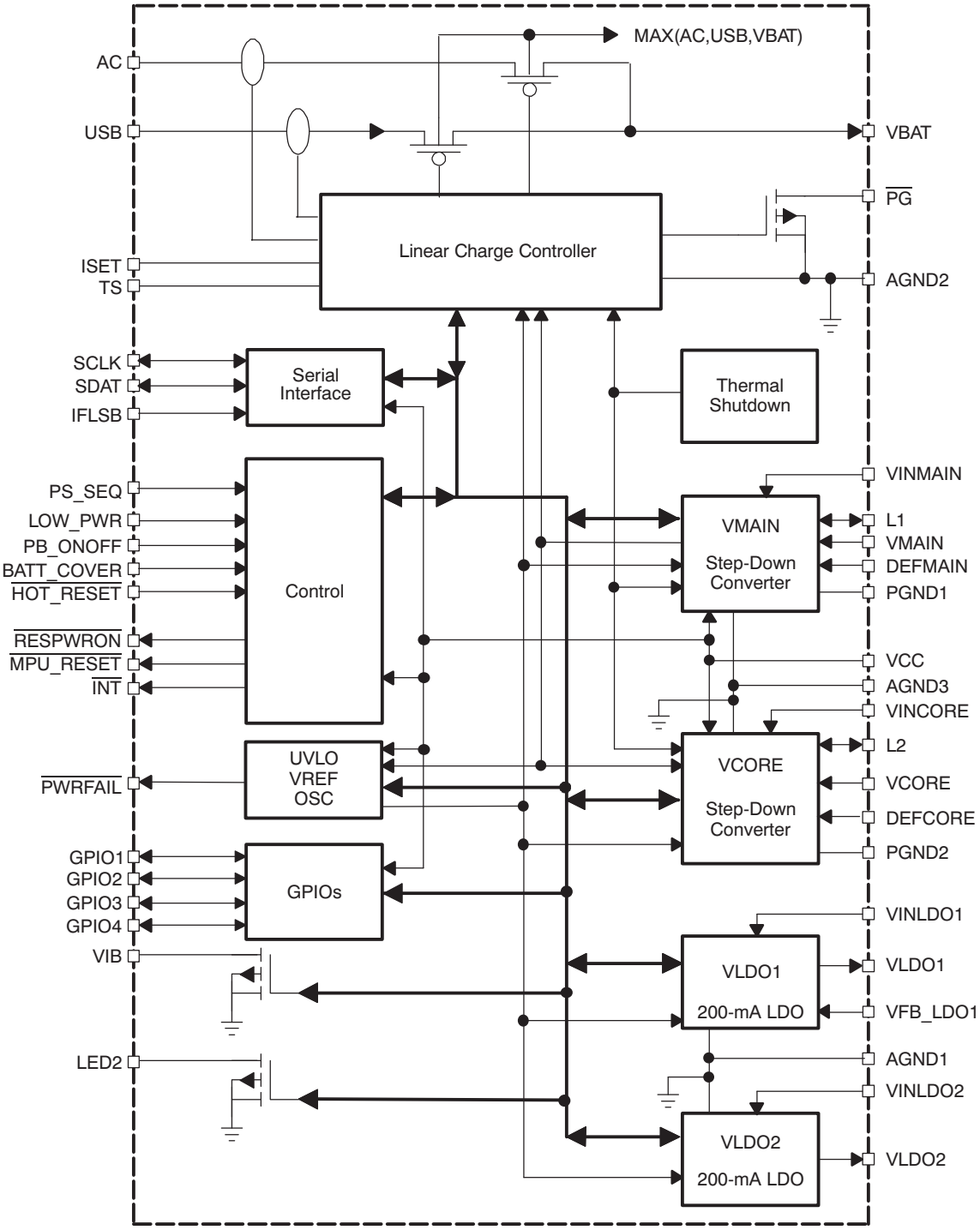
The TPS65012 charger automatically selects the USB port or the AC adapter as the power source for the system. In the USB configuration, the host can increase the charge current from the default value of maximum 100 mA to 500 mA via the interface. In the AC-adapter configuration, an external resistor sets the maximum value of charge current.

The battery is charged in three phases: conditioning, constant current, and constant voltage. Charge is normally terminated based on minimum current. An internal charge timer provides a safety backup for charge termination. The TPS65012 device automatically restarts the charge if the battery voltage falls below an internal threshold. The charger automatically enters sleep mode when both supplies are removed.

The serial interface can be used for dynamic voltage scaling, for collecting information on and controlling the battery charger status, for optionally controlling 2 LED driver outputs, a vibrator driver, masking interrupts, or for disabling/enabling and setting the LDO output voltages. The interface is compatible with the fast/standard mode specification allowing transfers at up to 400 kHz.

Battery Charger, Step-Down Converters, LDOs, UVLO protection, Rail Sequencing, Vibrator Driver, and various logic level controls. The LOW_PWR pin allows the core converter to lower its output voltage when the application processor goes into deep sleep.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Battery Charger

The TPS65012 supports a precision Li-Ion or Li-Polymer charging system suitable for single cells with either coke or graphite anodes. Charging the battery is possible even without the application processor being powered up. The TPS65012 starts charging when an input voltage on either AC or USB input is present, which is greater than the charger UVLO threshold. See Figure 26 for a typical charge profile.

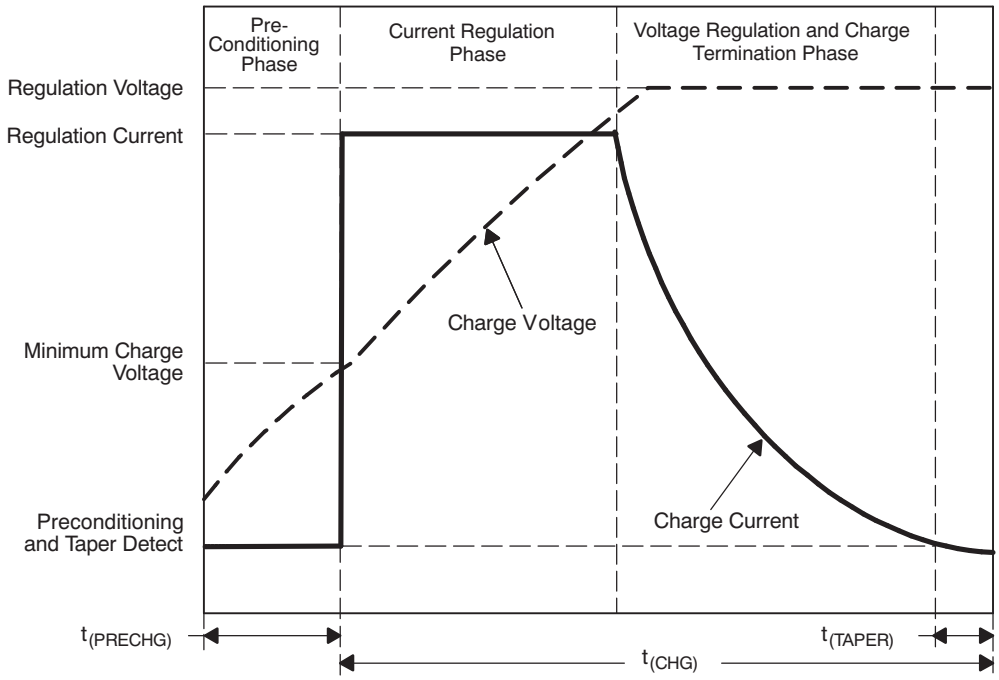


Figure 26. Typical Charging Profile

7.3.1.1 Autonomous Power Source Selection

Per default the TPS65012 attempts to charge from the AC input. If AC input is not present, the USB is selected. If both inputs are available, the AC input has priority. The charge current is initially limited to 100 mA when charging from the USB input. This can be increased to 500 mA via the serial interface. The charger can be completely disabled via the interface, and it is also possible just to disable charging from the USB port. The start of the charging process from the USB port is delayed in order to allow the application processor time to disable USB charging, for example, if a USB OTG port is recognized. The recommended input voltage for charging from the AC input is 4.5 V < VAC < 5.5 V. However, the TPS65012 is capable of withstanding (but not charging from) up to 20 V. Charging is disabled if VAC is greater than typically 6.6 V.

7.3.1.2 Temperature Qualification

The TPS65012 continuously monitors battery temperature by measuring the voltage between the TS and AGND pins. An internal current source provides the bias for most common 10K negative-temperature coefficient thermistors (NTC) (see Figure 27). The IC compares the voltage on the TS pin against the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected, the IC immediately suspends the charge. The IC suspends charge by turning off the power FET and holding the timer value (i.e., timers are *not* reset). Charge is resumed when the temperature returns to the normal range.

The allowed temperature range for 103-A T-type thermistor is 0°C to 45°C. However, the user may modify these thresholds by adding two external resistors. See Figure 28.

Feature Description (continued)

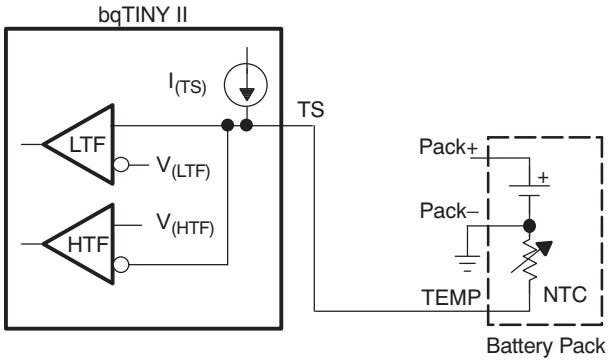


Figure 27. TS Pin Configuration

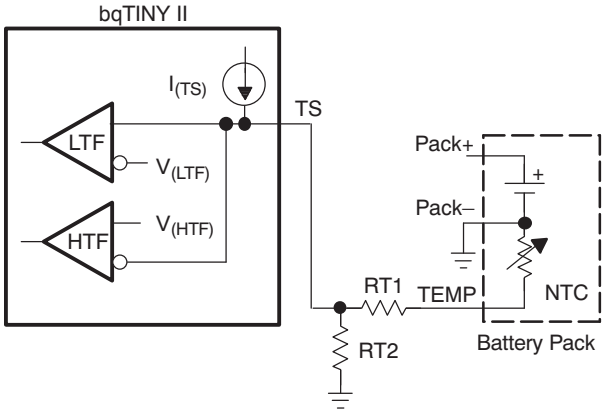


Figure 28. TS Pin Threshold

7.3.1.3 Battery Preconditioning

On power up, if the battery voltage is below the $V_{(LOWV)}$ threshold, the TPS65012 applies a precharge current, $I_{(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The charge current during this phase is one tenth of the value in current regulation phase which is set with $I_{O(out)}$ = KSET × $V_{(SET)}/R_{(SET)}$. The load current in preconditioning phase must be lower than $I_{(PRECHG)}$ and must allow the battery voltage to rise above $V_{(LOWV)}$ within $t_{(Prechg)}$. VBAT_A is the sense pin to the voltage comparator for the battery voltage. This allows a power-on sense measurement if the VBAT_A and VBAT_B pins are connected together at the battery.

The TPS65012 activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the TPS65012 turns off the charger and indicates the fault condition in the CHGSTATUS register. In the case of a fault condition, the TPS65012 reduces the current to $I_{(DETECT)}$. $I_{(DETECT)}$is used to detect a battery replacement condition. Fault condition is cleared by power-on-reset (POR) or battery replacement or via the serial interface.

7.3.1.4 Battery Charge Current

TPS65012 offers on-chip current regulation. When charging from an AC adapter, a resistor connected between the ISET1 and AGND pins determines the charge rate. A maximum of 1-A charger current from the AC adapter is allowed. When charging from a USB port either a 100-mA or 500-mA charge rate can be selected via the serial interface; default is 100 mA maximum. Two bits are available in the CHGCONFIG register in the serial interface to reduce the charge current in 25% steps. These only influence charging from the AC input and may be of use if charging is often suspended due to excessive junction temperature in the TPS65012 (e.g., at high AC input voltages) and low battery voltages.

Feature Description (continued)

7.3.1.5 Battery Voltage Regulation

The voltage regulation feedback is through the VBAT pin. This pin is tied directly to the positive side of the battery pack. The TPS65012 monitors the battery-pack voltage between the VBAT and AGND pins. The TPS65012 is offered in a fixed-voltage version of 4.2 V.

As a safety backup, the TPS65012 also monitors the charge time in the fast-charge mode. If taper current is not detected within this time period, $t_{(CHG)}$, the TPS65012 turns off the charger and indicates FAULT in the CHGSTATUS register. In the case of a FAULT condition, the TPS65012 reduces the current to $I_{(DETECT)}$. $I_{(DETECT)}$ is used to detect a battery replacement condition. Fault condition is cleared by POR via the serial interface. Note that the safety timer is reset if the TPS65012 is forced out of the voltage regulation mode. The fast-charge timer is disabled by default to allow charging during normal operation of the end equipment. It is enabled via the CHGCONFIG register.

7.3.1.6 Charge Termination and Recharge

The TPS65012 monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected, the TPS65012 initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The TPS65012 resets the taper timer in the event that the charge current returns above the taper threshold, $I_{(TAPER)}$. After a charge termination, the TPS65012 restarts the charge once the voltage on the VBAT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times. The fast charge timer and the taper timer must be enabled by programming CHGCONFIG(5)=1. A thermal suspend will suspend the fast-charge and taper timers.

In addition to the taper current detection, the TPS65012 terminates charge in the event that the charge current falls below the $I_{(TERM)}$ threshold. This feature allows for quick recognition of a battery removal condition. When a full battery is replaced with an empty battery, the TPS65012 detects that the VBAT voltage is below the recharge threshold and starts charging the new battery. The taper and termination bits are cleared in the CHGSTATUS register and if the $\overline{INT}$ pin is still active due to these two interrupt sources, then it is de-asserted. Depending on the transient seen at the VCC pin, all registers may be set to their default values and require reprogramming with any nondefault values required, such as enabling the fast-charge timer and taper termination; this should only happen if VCC drops below approximately 2 V.

7.3.1.7 Sleep Mode

The TPS65012 charger enters the low-power sleep mode if both input sources are removed from the circuit. This feature prevents draining the battery during the absence of input power.

7.3.1.8 $\overline{PG}$ Output

The open-drain power-good ($\overline{PG}$) output indicates when a valid power supply is present for the charger. This can be either from the AC adapter input or from the USB. The output turns ON when a valid voltage is detected. A valid voltage is detected whenever the voltage on either pin AC or pin USB rises above the voltage on VBAT plus 100 mV. This output is turned off in the sleep mode. The $\overline{PG}$ pin can be used to drive an LED or communicate to the host processor. A voltage greater than the $V_{(CHGOVLO)}$ threshold (typ 6.6 V) at the AC input is not valid and does not activate the $\overline{PG}$ output. The $\overline{PG}$ output is held in high impedance state if the charger is in reset by programming CHGCONFIG(6)=1.

The $\overline{PG}$ output can also be programmed via the LED1_ON and LED1_PER registers in the serial interface. It can then be programmed to be permanently on, off, or to blink with defined on- and period-times. $\overline{PG}$ is controlled per default via the charger.

7.3.1.9 Thermal Considerations for Setting Charge Current

The TPS65012 is housed in a 48-pin QFN package with exposed leadframe on the underside. This 7 mm × 7 mm package exhibits a thermal impedance (junction-to-ambient) of 33 K/W when mounted on a JEDEC high-K board with zero air flow.

Feature Description (continued)

Table 2. Thermal Considerations for Setting Charge Current

AMBIENT TEMPERATURE	MAX POWER DISSIPATION FOR T_j= 125°C	DERATING FACTOR ABOVE T_A= 55°C
25°C	3 W	30 mW/°C
55°C	2.1 W	

Consideration needs to be given to the maximum charge current when the assembled application board exhibits a thermal impedance, which differs significantly from the JEDEC high-K board. The charger has a thermal shutdown feature, which suspends charging if the TPS65012 junction temperature rises above a threshold of 145°C. This threshold is set 15°C below the threshold used to power down the TPS65012 completely.

7.3.2 Step-Down Converters, VMAIN and VCORE

The TPS65012 incorporates two synchronous step-down converters operating typically at 1.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter power-save mode and operate with pulse frequency modulation (PFM). The main converter is capable of delivering 1-A output current, and the core converter is capable of delivering 400 mA.

The converter output voltages are programmed via the VDCDC1 and VDCDC2 registers in the serial interface. The main converter defaults to 3-V or 3.3-V output voltage depending on the DEFMAIN configuration pin, if DEFMAIN is tied to ground, the default is 3 V; if it is tied to V_{CC} the default is 3.3 V. The core converter defaults to either 1.5 V or 1.6 V depending on whether the DEFCORE configuration pin is tied to GND or to V_{CC}, respectively. Both the main and core output voltages can subsequently be reprogrammed after start-up via the serial interface. In addition, the LOW_PWR pin can be used either to lower the core voltage to a value defined in the VDCDC2 register when the application processor is in deep sleep mode or to disable the core converter. An active signal at LOW_PWR is ignored if the ENABLE_LP bit is not set in the VDCDC1 register.

The step-down converter outputs (when enabled) are monitored by power-good comparators, the outputs of which are available via the serial interface. The outputs of the DC-DC converters can be optionally discharged when the DC-DC converters are disabled.

During PWM operation, the converters use a unique fast-response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. After the dead time preventing current shoot through, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal, again turning off the N-channel rectifier and turning on the P-channel switch.

The error amplifier, together with the input voltage, determines the rise time of the saw-tooth generator, and therefore, any change in input voltage or output voltage directly controls the duty cycle of the converter giving a good line and load transient regulation.

The two DC-DC converters operate synchronized to each other, with the MAIN converter as the master. A 270° phase shift between the MAIN switch turn on and the CORE switch turn on decreases the input RMS current, and smaller input capacitors can be used. This is optimized for a typical application where the MAIN converter regulates a Li-Ion battery voltage of 3.7 V to 3.3 V and the CORE from 3.7 V to 1.5 V.

7.3.2.1 Power-Save Mode Operation

As the load current decreases, the converter enters the power-save mode operation. During power save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

In order to optimize the converter efficiency at light load, the average current is monitored; if in PWM mode, the inductor current remains below a certain threshold, then power-save mode is entered. The typical threshold can be calculated as:

$$I_{(skipmain)} = \frac{V_{I(MAIN)}}{17\ \Omega} \qquad I_{(skipcore)} = \frac{V_{I(CORE)}}{42\ \Omega} \tag{1}$$

During the power-save mode, the output voltage is monitored with the comparator by the thresholds comp low and comp high. As the output voltage falls below the comp-low threshold, set to typically 0.8% above the nominal V_{out}, the P-channel switch turns on. The converter then runs at 50% of the nominal switching frequency. If the load is below the delivered current, then the output voltage rises until the comp-high threshold is reached, typically 1.6% above the nominal V_{out}. At this point, all switching activity ceases, hence reducing the quiescent current to a minimum until the output voltage has dropped below comp low again. If the load current is greater than the delivered current, then the output voltage falls until it crosses the nominal output voltage threshold (comp-low 2 threshold), whereupon power-save mode is exited, and the converter returns to PWM mode.

These control methods reduce the quiescent current typically to 12-µA per converter and the switching frequency to a minimum achieving the highest converter efficiency. Setting the comparator thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic voltage positioning achieving lower absolute voltage drops during heavy load transient changes. This allows the converters to operate with a small output capacitor of just 10 µF for the core and 22 µF for the main output and still have a low absolute voltage drop during heavy load transient changes. See Figure 29 for detailed operation of the power-save mode. The power-save mode can be disabled through the I^2C interface to force the converters to stay in fixed frequency PWM mode.

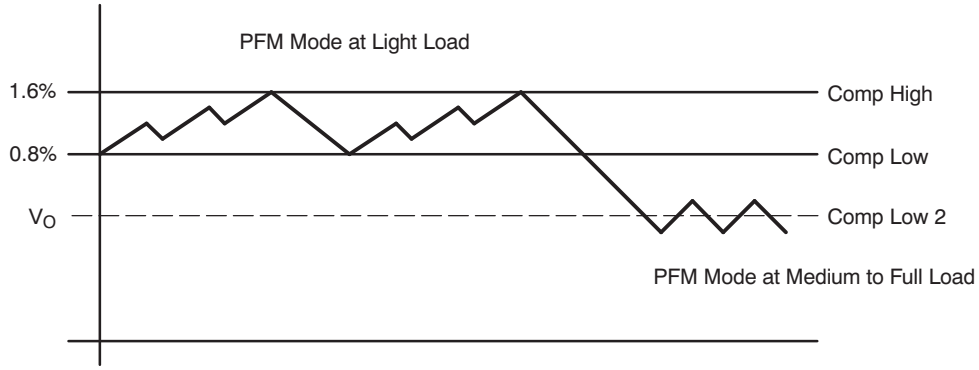


Figure 29. Power-Save Mode Thresholds and Dynamic Voltage Positioning

7.3.2.2 Forced PWM

The core and main converters are forced into PWM mode by setting bit 7 in the VDCDC1 register. This feature minimizes ripple on the output voltages.

7.3.2.3 Dynamic Voltage Positioning

As described in the power-save mode operation sections and as detailed in Figure 13, the output voltage is typically 1.2% above the nominal output voltage at light load currents as the device is in power-save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. During a load transient from full load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel rectifier switch.

7.3.2.4 Soft Start

Both converters have an internal soft start circuit that limits the inrush current during start-up. The soft start is implemented as a digital circuit increasing the switch current in 4 steps up to the typical maximum switch current limit of 700 mA (core) and 1.75 A (main). Therefore, the start-up time mainly depends on the output capacitor and load current.

7.3.2.5 100% Duty Cycle Low-Dropout Operation

The TPS65012 converters offer a low input to output voltage difference while maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage and is calculated as:

$$V_{I(min)} = V_{O(max)} + I_{O(max)} \times \left(r_{DS(on)max} + R_L\right)$$

where

- $I_{O(max)}$ = maximum output current plus inductor ripple current
- $r_{DS(on)max}$= maximum P-channel switch $r_{DS(on)}$.
- R_L = DC resistance of the inductor
- $V_{O(max)}$= nominal output voltage plus maximum output voltage tolerance (2)

7.3.2.6 Active Discharge When Disabled

When the CORE and MAIN converters are disabled, due to an UVLO, BATT_COVER or OVERTEMP condition, it is possible to actively pull down the outputs. This feature is disabled per default and is individually enabled via the VDCDC1 and VDCDC2 registers in the serial interface. When this feature is enabled, the core and main outputs are discharged by a 400-Ω (typical) load.

7.3.2.7 Power-Good Monitoring

Both the MAIN and CORE converters have power-good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value, with 5% hysteresis. The outputs of these comparators are available in the REGSTATUS register via the serial interface. A maskable interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the converters are disabled.

7.3.2.8 Overtemperature Shutdown

The MAIN and CORE converters are automatically shut down if the temperature exceeds the trip point (see the electrical characteristics). This detection is only active if the converters are in PWM mode, either by setting FPWM = 1, or if the output current is high enough that the device runs in PWM mode automatically.

7.3.3 Low-Dropout Voltage Regulators

The low-dropout voltage regulators are designed to operate with low value ceramic input and output capacitors. They operate with input voltages down to 1.8 V. The LDOs offer a maximum dropout voltage of 300 mV at rated output current. Each LDO has a current limit feature. Both LDOs are enabled per default; both LDOs can be disabled or programmed via the serial interface using the VREGS1 register. The LDO outputs (when enabled) are monitored by power-good comparators, the outputs of which are available via the serial interface. The LDOs also have reverse conduction prevention when disabled. This allows the possibility to connect external regulators in parallel in systems with a backup battery.

7.3.3.1 Power-Good Monitoring

Both the LDO1 and LDO2 linear regulators have power-good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value, with 5% hysteresis. The outputs of these comparators are available in the REGSTATUS register via the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The LDO2 comparator is disabled when LDO2 is disabled. The LDO1 power good comparator is always active since it generates the system reset signal, $\overline{\text{RESPWRON}}$, see the System Reset and Control Signal Section below. This also allows the possibility to monitor VLDO1, even if it is provided by an external regulator.

7.3.3.2 Enable and Sequencing

Enabling and sequencing of the DC-DC converters and LDOs are described in the power-up sequencing section. The OMAP1510 processor from Texas Instruments requires that the core power supply is enabled before the I/O power supply, which means that the CORE converter should power up before the MAIN converter. This is achieved by connecting PS_SEQ to GND.

7.3.4 Undervoltage Lockout

The undervoltage lockout circuit for the four regulators on TPS65012 prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. Basically, it prevents the converter from turning on the power switch or rectifier FET under undefined conditions. The undervoltage threshold voltage is set by default to 3.25 V. After power up, the threshold voltage can be reprogrammed through the serial interface. The undervoltage lockout comparator compares the voltage on the VCC pin with the UVLO threshold. When the VCC

voltage drops below this threshold, the TPS65012 sets the $\overline{\text{PWRFAIL}}$ pin low and after a time $t_{(UVLO)}$ disables the voltage regulators in the sequence defined by PS_SEQ. The same procedure is followed when the TPS65012 detects that its junction temperature has exceeded the overtemperature threshold, typically 160°C, with a delay $t_{(overtemp)}$. The TPS65012 automatically restarts when the UVLO (or overtemperature) condition is no longer present.

The battery charger circuit has a separate UVLO circuit with a threshold of typically 2.5 V, which is compared with the voltage on AC and USB supply pins.

7.3.5 Power-Up Sequencing

The TPS65012 power-up sequencing allows the maximum flexibility without generating excessive logistical or system complexity. The relevant control pins are described in the following table:

Table 3. Control Pins

PIN NAME	INPUT OR OUTPUT	FUNCTION
PS_SEQ	I	Input signal indicating power-up and -down sequence of the switching converters. PS_SEQ = 0 forces the core regulator to ramp up first and down last. PS_SEQ = 1 forces the main regulator to ramp up first and down last.
DEFCORE	I	Defines the default voltage of the VCORE switching converter. DEFCORE = 0 defaults VCORE to 1.5 V, DEFCORE = VCC defaults VCORE to 1.6 V.
DEFMAIN	I	Defines the default voltage of the VMAIN switching converter. DEFMAIN = 0 defaults VMAIN to 3.0 V, DEFMAIN = VCC defaults VMAIN to 3.3 V.
LOW_PWR	I	The LOW_PWR pin is used to lower VCORE to the preset voltage in the VDCDC2 register when the processor is in deep sleep mode. Alternatively, VCORE can be disabled in low-power mode if the LP_COREOFF bit is set in the VDCDC2 register. LOW_PWR is ignored if the ENABLE LP bit is not set in the VDCDC1 register. The TPS65012 uses the rising edge of the internal signal formed by a logical AND of LOW_PWR and ENABLE LP to enter low-power mode. TPS65012 is forced out of low-power mode by de-asserting LOW_PWR, by resetting ENABLE LP to 0, by activating the PB_ONOFF pin or by activating the $\overline{\text{HOT\_RESET}}$ pin. There are two ways to get the device back into low-power mode: a) toggle the LOW_PWR pin, or b) toggle the low-power bit when the LOW_PWR pin is held high.
PB_ONOFF	I	PB_ONOFF can be used to exit the low-power mode and return the core voltage to the value before low-power mode was entered. If PB_ONOFF is used to exit the low-power mode, then the low-power mode can be reentered by toggling the LOW_PWR pin or by toggling the low-power bit when the LOW_PWR pin is held high. A 1-MΩ pulldown resistor is integrated in TPS65012. PB_ONOFF is internally de-bounced by the TPS65012. A maskable interrupt is generated when PB_ONOFF is activated.
$\overline{\text{HOT\_RESET}}$	I	The $\overline{\text{HOT\_RESET}}$ pin has a similar functionality to the PB_ONOFF pin. In addition, it generates a reset ($\overline{\text{MPU\_RESET}}$) for the MPU when the VCORE voltage is in regulation. $\overline{\text{HOT\_RESET}}$ does not alter any TPS65012 settings unless low-power mode was active, in which case it is exited. A 1-MΩ pullup resistor to V_{CC} is integrated in TPS65012. $\overline{\text{HOT\_RESET}}$ is internally de-bounced by the TPS65012.
BATT_COVER	I	The BATT_COVER pin is used as an early warning that the main battery is about to be removed. BATT_COVER = V_{CC} indicates that the cover is in place, BATT_COVER = 0 indicates that the cover is not in place. TPS65012 generates a maskable interrupt when the BATT_COVER pin goes low. $\overline{\text{PWRFAIL}}$ is also held low when BATT_COVER goes low. This feature may be disabled by tying BATT_COVER permanently to VCC. The TPS65012 shuts down the main and the core converter and sets the LDOs into low-power mode. A 2-MΩ pulldown resistor is integrated in the TPS65012 at the BATT_COVER pin. BATT_COVER is internally de-bounced by the TPS65012.
$\overline{\text{RESPWRON}}$	O	$\overline{\text{RESPWRON}}$ is held low while the switching converters (and any LDOs defined as default on) are starting up. It is determined by the state of LDO1's output voltage; when the voltage is higher than the power-good comparator threshold, then $\overline{\text{RESPWRON}}$ is high; when VLDO1 is low then $\overline{\text{RESPWRON}}$ is low. $\overline{\text{RESPWRON}}$ is held low for $t_{n(RESPWRON)}$ seconds after VLDO1 has settled.
$\overline{\text{MPU\_RESET}}$	O	$\overline{\text{MPU\_RESET}}$ can be used to reset the processor if the user activates the$\overline{\text{HOT_RESET}}$ button. The $\overline{\text{MPU\_RESET}}$ output is active for $t_{(MPU\_nRESET)}$ seconds. It also forces TPS65012 to leave low-power mode. $\overline{\text{MPU\_RESET}}$ is also held low as long as $\overline{\text{RESPWRON}}$ is held low.
$\overline{\text{PWRFAIL}}$	O	$\overline{\text{PWRFAIL}}$ indicates when $V_{CC} < V_{(UVLO)}$, when the TPS65012 is about to shut down due to an internal overtemperature condition or when BATT_COVER is low. $\overline{\text{PWRFAIL}}$ is also held low as long as $\overline{\text{RESPWRON}}$ is held low.

Figure 30 shows the state diagram for the TPS65012 power sequencing. The charger function is not shown in the state diagram because this function is independent of these states.

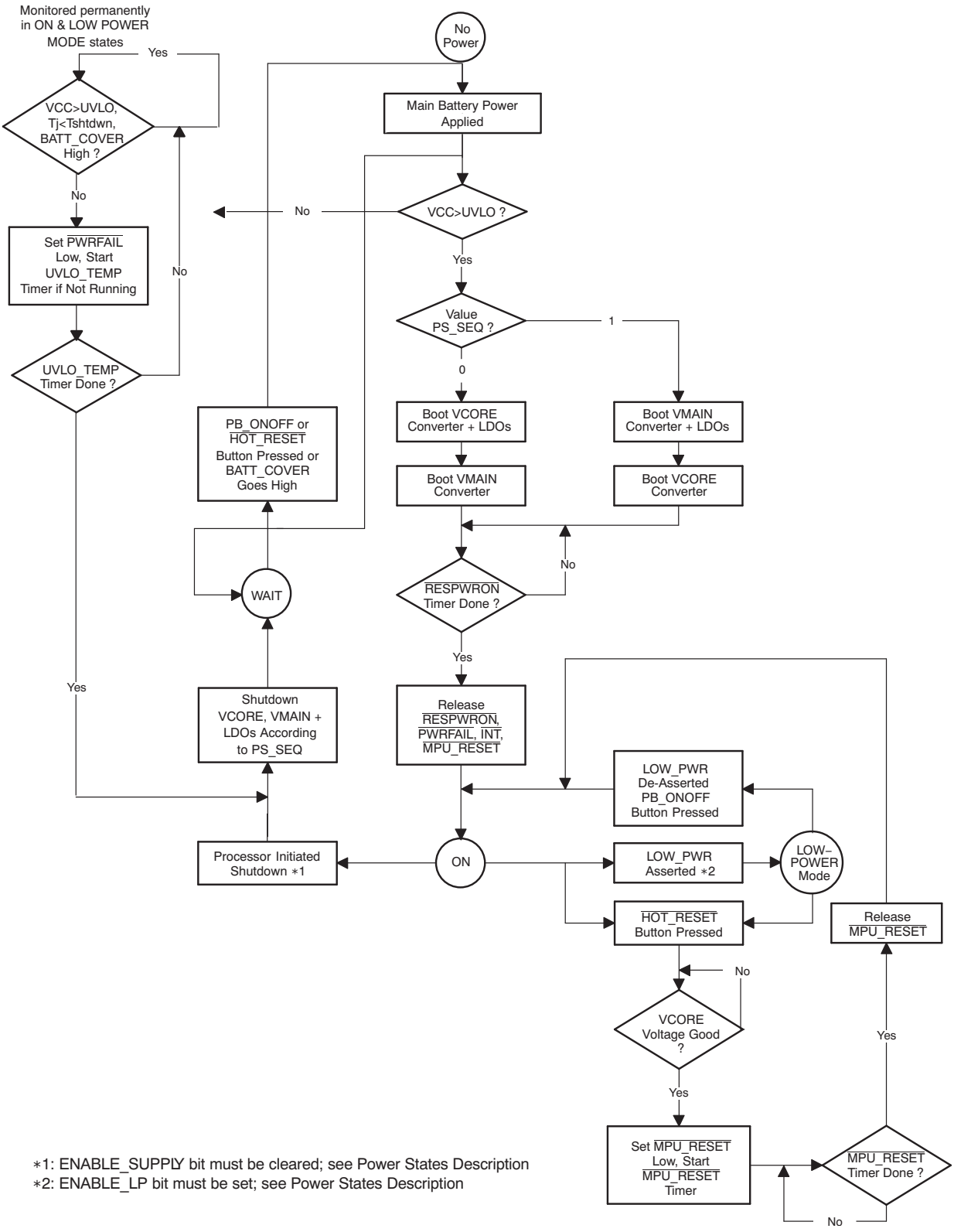


Figure 30. TPS65012 Power-On State Diagram

7.3.6 System Reset and Control Signals

The $\overline{\text{RESPWRON}}$ signal is used as a global reset for the application. It is an open-drain output. The $\overline{\text{RESPWRON}}$ signal is generated according to the power-good comparator linked to VLDO1 and remains low for $t_{n(\text{RESPWRON})}$ seconds after VLDO1 has stabilized. When $\overline{\text{RESPWRON}}$ is low, $\overline{\text{PWRFAIL}}$, $\overline{\text{MPU\_RESET}}$ and $\overline{\text{INT}}$ are also held low.

If the output voltage of LDO1 is less than 90% of its nominal value, as $\overline{\text{RESPWRON}}$ is generated, and if the output voltage of LDO1 is programmed to a higher value, which causes the output voltage to fall out of the 90% window, then a $\overline{\text{RESPWRON}}$ signal is generated.

The $\overline{\text{PWRFAIL}}$ signal indicates when VCC < UVLO or when the TPS65012 junction temperature has exceeded a reliable value or if BATT_COVER is taken low. This open-drain output can be connected at a fast interrupt pin for immediate attention by the application processor. All supplies are disabled $t_{(\text{uvlo})}$, $t_{(\text{overtemp})}$ or $t_{(\text{batt\_cover})}$ seconds after $\overline{\text{PWRFAIL}}$ has gone low, giving time for the application processor to shut down cleanly.

The BATT_COVER function detects whether the battery cover is in place or not. If the battery cover is removed, the TPS65012 generates a warning to the processor that the battery is likely to be removed and that it may be prudent to shut down the system. If not required, this feature may be disabled by connecting the BATT_COVER pin to the VCC pin. BATT_COVER is de-bounced internally. Typical de-bounce time is 56 ms. BATT_COVER has an internal 2-MΩ pulldown resistor.

The $\overline{\text{HOT\_RESET}}$ input is used to generate an $\overline{\text{MPU\_RESET}}$ signal for the application processor. The $\overline{\text{HOT\_RESET}}$ pin could be connected to a user-activated button in the application. It can also be used to exit low-power mode. In this case, the TPS65012 waits until the VCORE voltage has stabilized before generating the $\overline{\text{MPU\_RESET}}$ pulse. The $\overline{\text{MPU\_RESET}}$ pulse is active low for $t_{(\text{mpu\_nreset})}$ seconds. $\overline{\text{HOT\_RESET}}$ has an internal 1-MΩ pullup resistor to V_{CC}.

The PB_ONOFF input can be used to exit LOW-POWER MODE. It is typically driven by a user-activated push-button in the application. Both $\overline{\text{HOT\_RESET}}$ and PB_ONOFF are de-bounced internally by the TPS65012. Typical de-bounce time is 56 ms. PB_ONOFF has an internal 1-MΩ pulldown resistor.

PB_ONOFF, BATT_COVER and UVLO events also cause a normal, maskable interrupt to be generated and are noted in the REGSTATUS register.

7.3.7 Vibrator Driver

The VIB open-drain output is provided to drive a vibrator motor, controlled via the serial interface register VDCDC2. It has a maximum dropout of 0.5 V at 100-mA load. Typically, an external resistor is required to limit the motor current and a freewheel diode to limit the VIB overshoot voltage at turnoff.

7.4 Device Functional Modes

7.4.1 TPS65012 Power States Description

7.4.1.1 State 1: No Power

No batteries are connected to the TPS65012. When main power is applied, the RESPWRON, PWRFAIL, INT, and MPU_RESET signals are held low. When BATT_COVER goes high (de-bounced internally by the TPS65012), indicating that the battery cover has been put in place and if VCC > UVLO, the power supplies are ramped in the sequence defined by PS_SEQ. RESPWRON, PWRFAIL, INT, and MPU_RESET are released when the RESPWRON timer has timed out after $t_{n(RESPWRON)}$ seconds. If VCC remains valid and no OVERTEMP condition occurs, then the TPS65012 arrives in State 2: ON. The TPS65012 keeps the bandgap reference and UVLO comparator active for approximately 10 ms after BATT_COVER has been de-bounced going high. VCC must be greater than the UVLO threshold during this time, or else the TPS65012 proceeds to State 4: WAIT, where all supplies are powered down.

7.4.1.2 State 2: ON

In this state, TPS65012 is powered up and ready to go. The switching converters can have their output voltages programmed. The LDOs can be enabled, disabled, or reprogrammed. TPS65012 can exit this state due to an overtemperature condition, an undervoltage condition at VCC, by BATT_COVER going low, or by the processor programming LOW-POWER MODE, or WAIT. State 2 is left temporarily if the user activates the HOT_RESET pin.

7.4.1.3 State 3: Low-Power Mode

This state is entered via the processor setting the ENABLE LP bit in the serial interface (see the VDCDC1 register) and then raising the LOW_PWR pin. The TPS65012 actually uses the rising edge of the internal signal formed by a logical AND of the LOW_PWR and ENABLE LP signals to enter low-power mode. The VMAIN switching converter remains active, but the VCORE converter may be disabled in low-power mode via the serial interface by setting the LP_COREOFF bit in the VDCDC2 register. If left enabled, the VCORE voltage is set to the value predefined by the CORELP0/1 bits in the VDCDC2 register. The LDO1OFF/nSLP and LDO2OFF/nSLP bits in the VREGS1 register determine whether the LDOs are turned off or put in a reduced power mode (current limits are reduced and the transient speed-up circuitry disabled in order to minimize quiescent current) in low-power mode. All TPS65012 features remain addressable via the serial interface. TPS65012 can normally exit this state either by the processor deasserting the LOW_POWER pin, or by the user activating the HOT_RESET pin or the PB_ONOFF pin. If both LDOs are set to be disabled in low-power mode, then this mode must be left by activating the HOT_RESET pin or the PB_ONOFF pin. An undervoltage condition at VCC, or an OVERTEMP condition, or BATT_COVER going low forces the TPS65012 to transit to State 4: WAIT.

7.4.1.4 State 4: Shutdown

WAIT mode can be entered from any of the above states when fault conditions exist:

1. From State 1 when a discharged battery is applied.
2. From States 2 and 3 if an OVERTEMP condition exists.
3. If VCC drops below the UVLO threshold.
4. If BATT_COVER goes low indicating that the battery is about to be removed.

WAIT mode can also be initiated by the processor. This is done by setting the ENABLE SUPPLY bit (VDCDC1 register) low, the ENABLE LP bit (also VDCDC1 register) high, and then raising the low-power pin. When this occurs, the VMAIN and VCORE converters are powered down according to PS_SEQ. The LDOs can remain enabled in reduced quiescent current operation or be programmed to turn off in WAIT mode. If all supplies are disabled and both VMAIN and VCORE are discharged close to ground, then the voltage reference circuitry is disabled and the serial interface registers reset to their default values. WAIT mode is left by activating either the PB_ONOFF or HOT_RESET pins. For this to be successful, the voltage at VCC must exceed the UVLO threshold, and the BATT_COVER pin must be high.

Table 4 indicates the typical quiescent current consumption in each power state.

Device Functional Modes (continued)

Table 4. TPS65012 Typical Current Consumption

STATE	TOTAL QUIESCENT CURRENT	QUIESCENT CURRENT BREAKDOWN
1	0	
2	30 µA-70 µA	VMAIN (12 µA) + VCORE (12 µA) + LDOs (20 µA each, max 2) + UVLO + reference + PowerGood
3	30 µA-55 µA	VMAIN (12 µA) + VCORE (12 µA) + LDOs (10 µA each, max 2) + UVLO + reference + PowerGood
4	13 µA	UVLO + reference circuitry

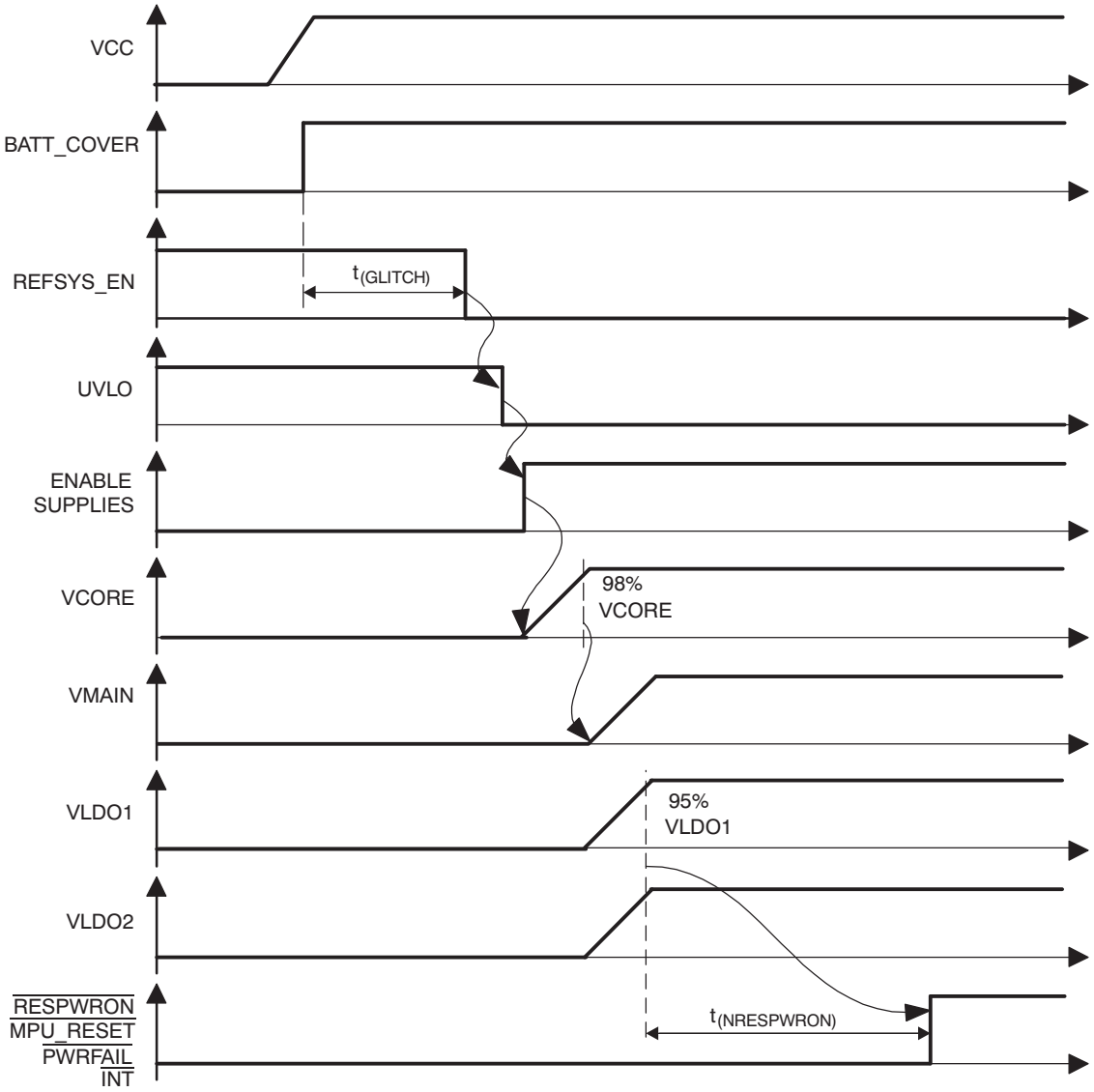


Figure 31. State 1 to State 2 Transition (PS_SEQ=0, V_{CC} > V_{UVLO} + HYST)

Valid for LDO1 supplied from VMAIN as described in *Application Information*.

If 2.4 ms after application, V_{CC} is still below the default UVLO threshold (3.425 V for V_{CC} rising), then start-up is as shown in Figure 32.

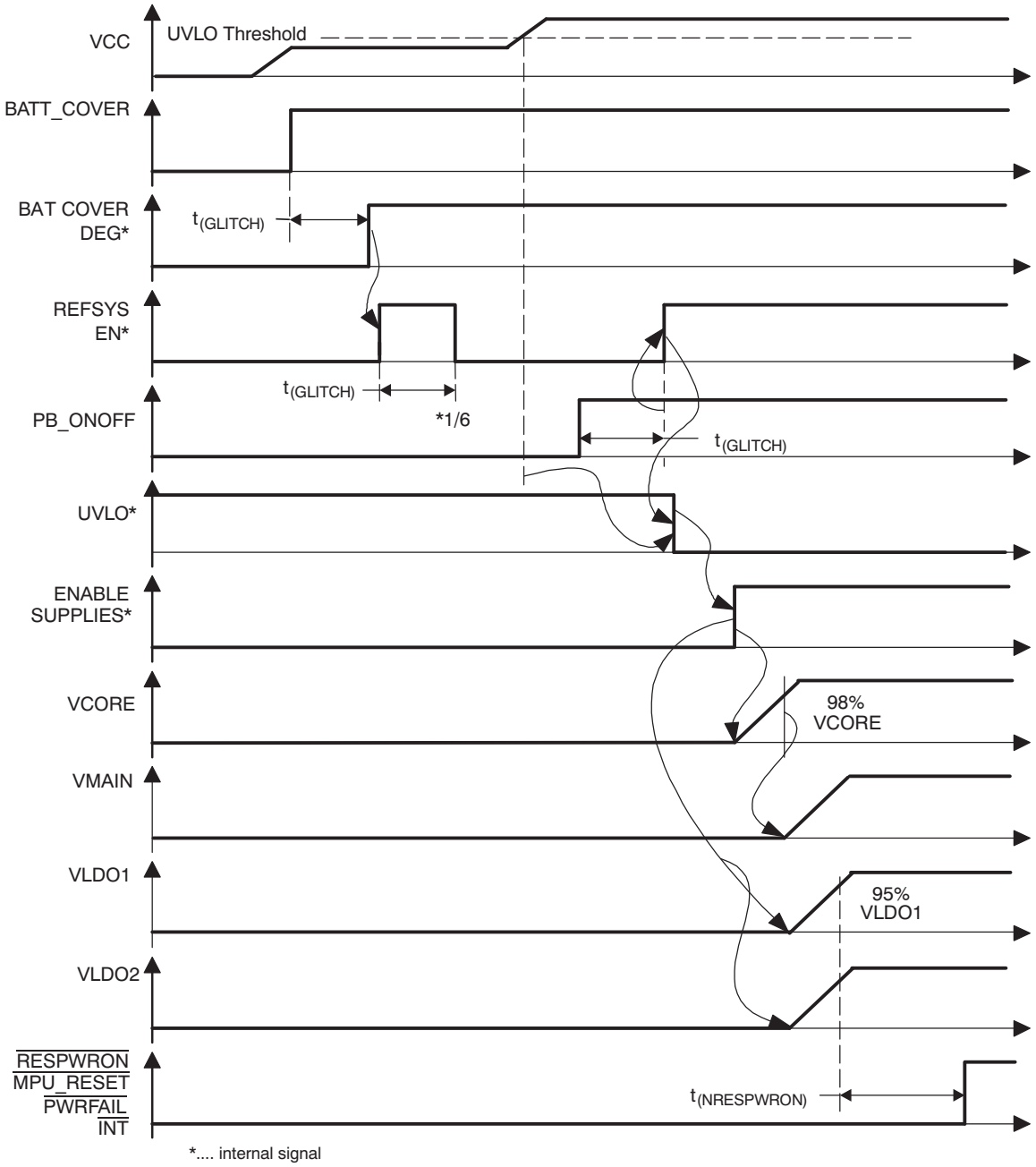


Figure 32. State 1 to State 4 to State 2 Transition (Power-Up Behavior When V_{CC} Ramp is Longer Than 2.4 ms)

Valid for LDO1 supplied from VMAIN as described in *Application Information*.

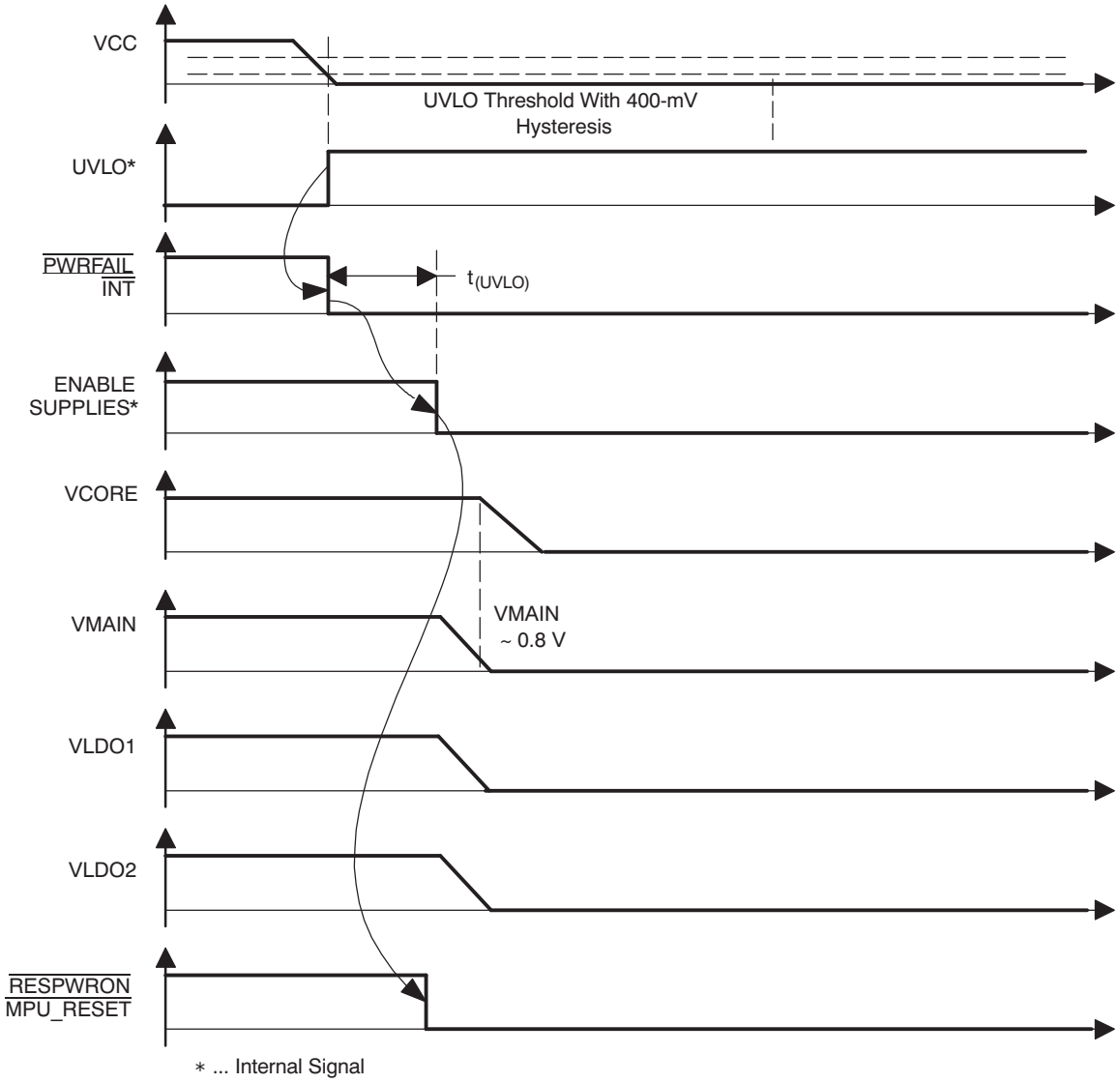


Figure 33. State 2 to State 4 Transition

Valid for LDO1 supplied from VMAIN as described in *Application Information*.

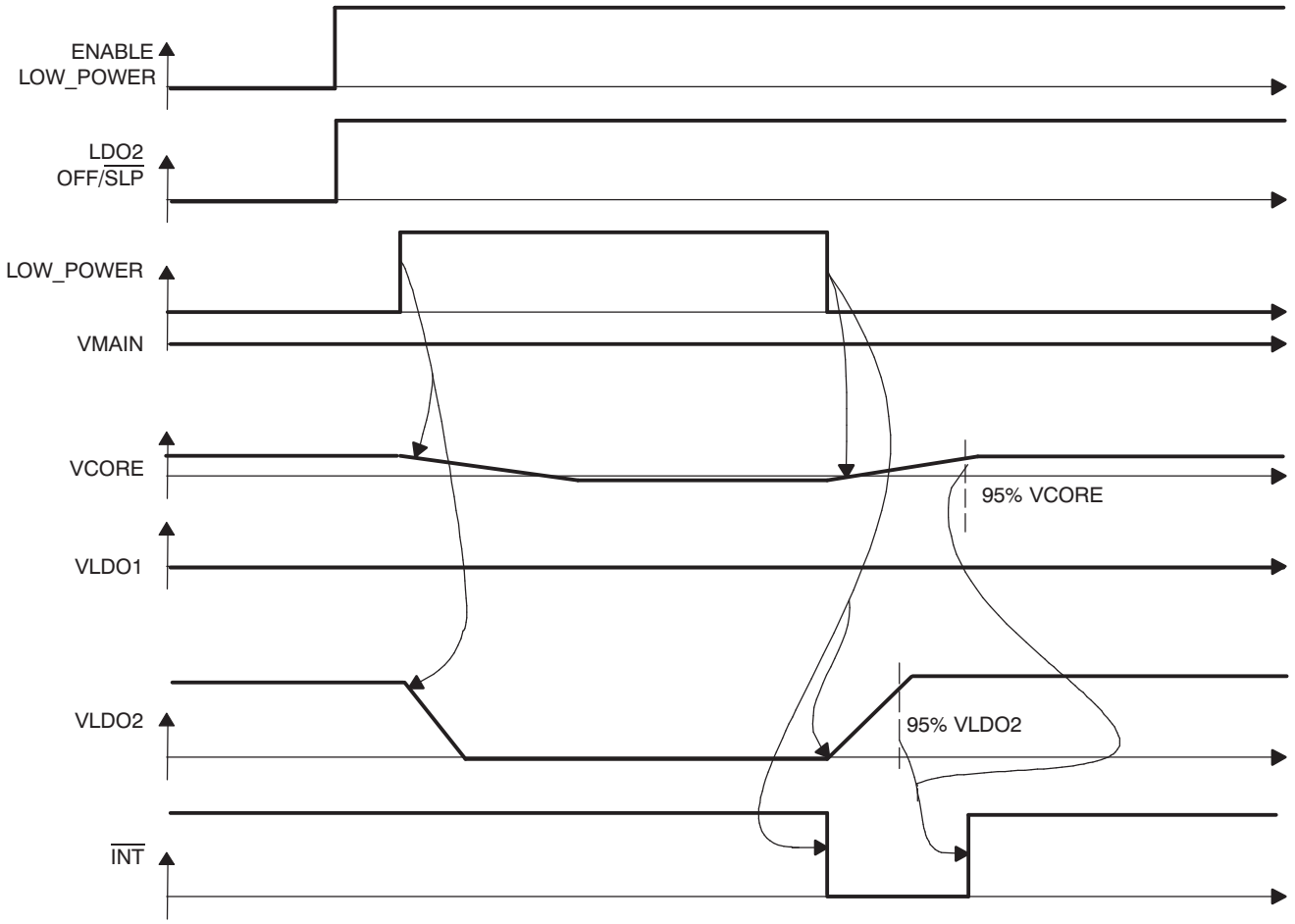


Figure 34. State 2 to State 3 Transition. VCORE Lowered, LDO2 Disabled. Subsequent State 3 to State 2 Transition When LOW-POWER Is De-Asserted.

NOTE

If both LDOs are turned off in low-power mode, the low-power mode can only be exited by activating HOT_RESET or PB_ONOFF.

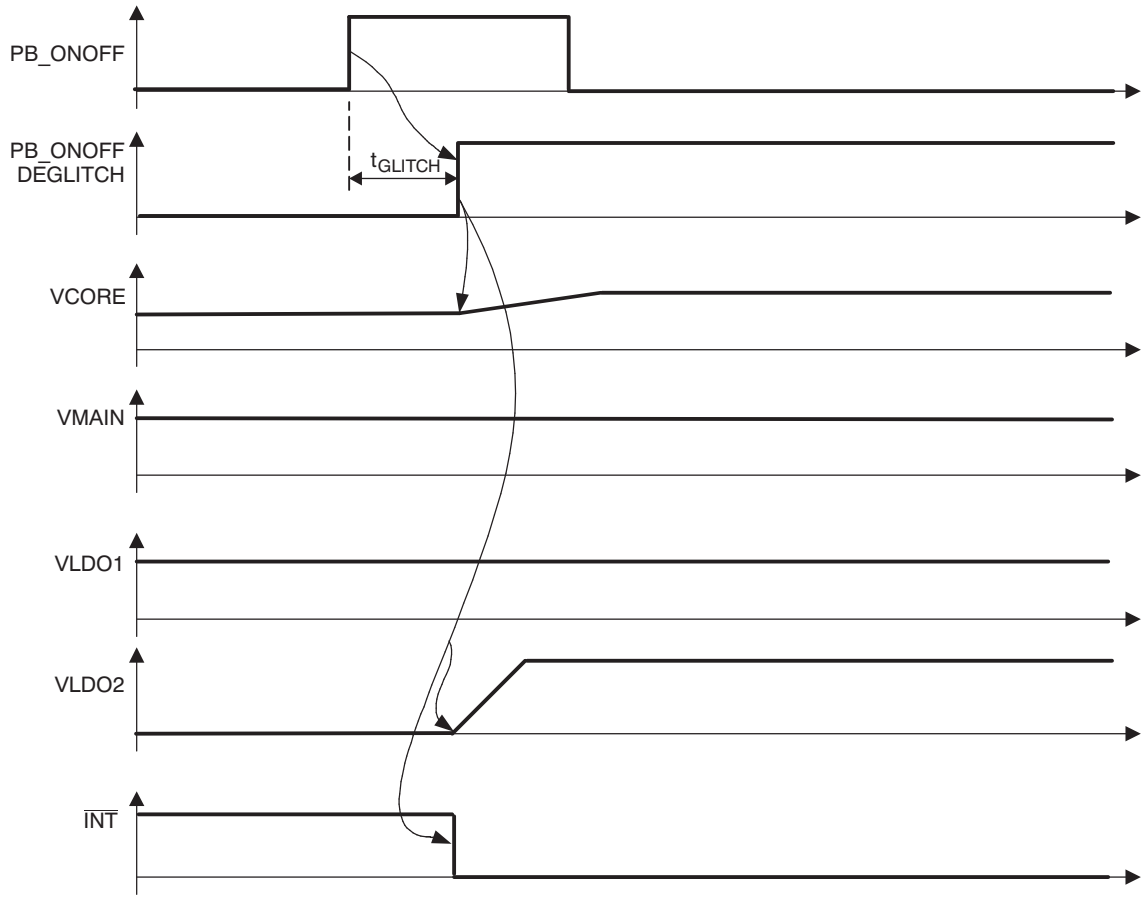


Figure 35. State 3 to State 2 Transition. PB_ONFF Activated (See *Interrupt Management* for $\overline{\text{INT}}$ Behavior)

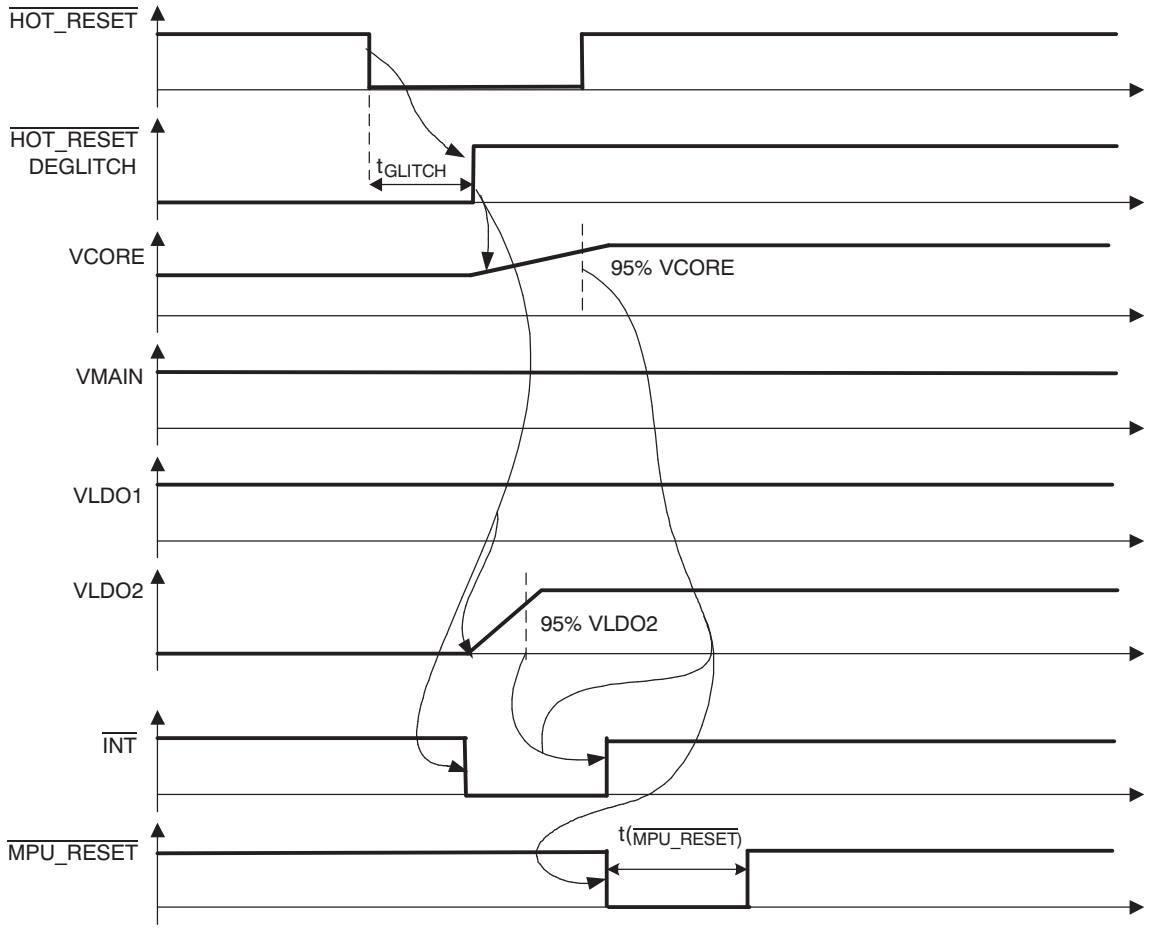


Figure 36. State 3 to State 2 Transition ($\overline{\text{HOT\_RESET}}$ Activated, See *Interrupt Management* for $\overline{\text{INT}}$ Behavior)

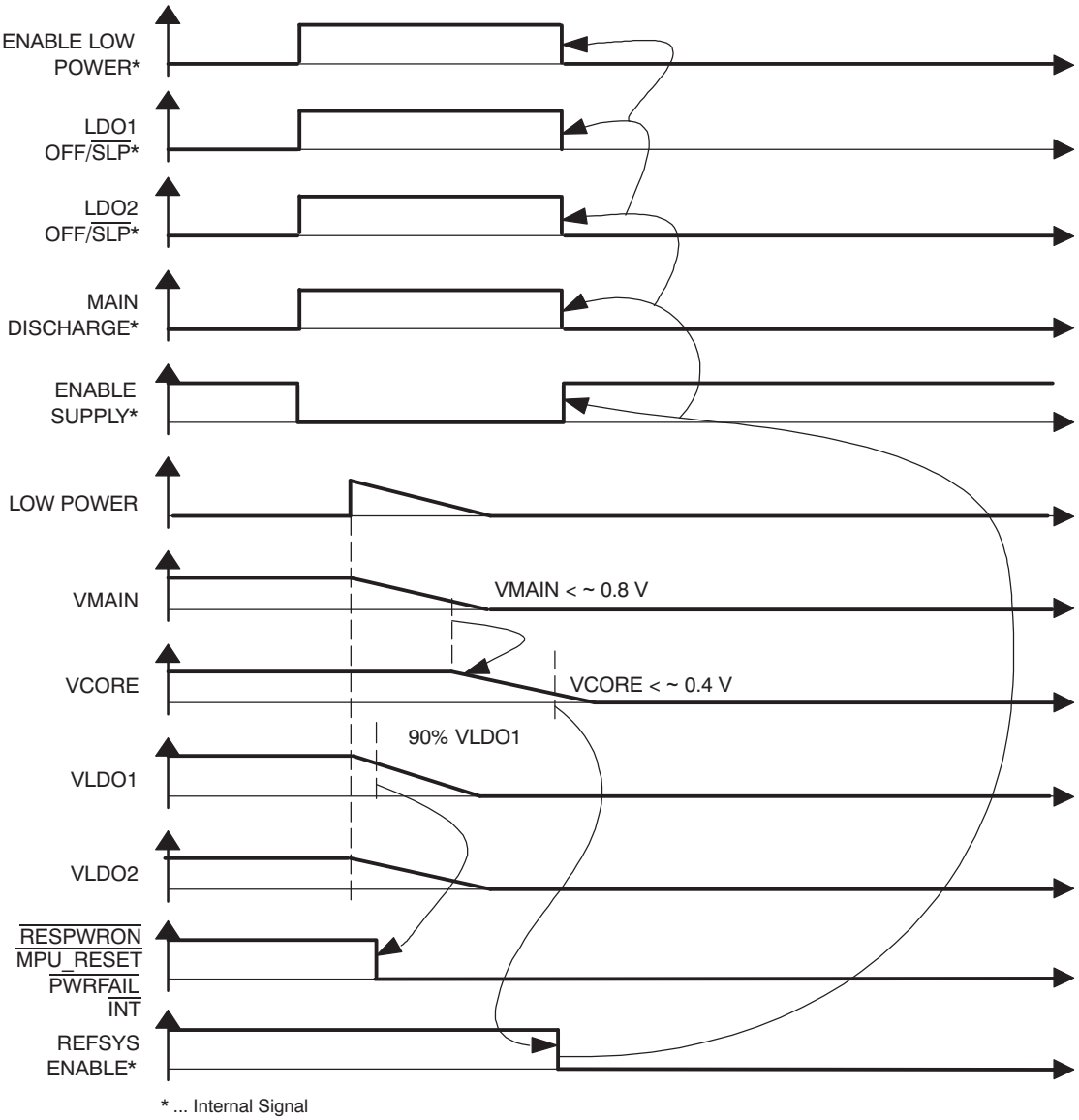


Figure 37. State 2 to State 4 Transition

7.5 Programming

7.5.1 LED2 Output

The LED2 output can be programmed in the same way as the $\overline{PG}$ output to blink or to be permanently on or off. The LED2_ON and LED2_PER registers are used to control the blink rate. For both $\overline{PG}$ and LED2, the minimum blink-on time is 10 ms. This can be increased in 127 10-ms steps to 1280 ms. For both $\overline{PG}$ and LED2, the minimum blink period is 100 ms. This can be increased in 127 100-ms steps to 12800 ms.

7.5.2 Interrupt Management

The open-drain $\overline{INT}$ pin is used to combine and report all possible conditions via a single pin. Battery and chip temperature faults, precharge timeout, charge timeout, taper timeout, and termination current are each capable of setting $\overline{INT}$ low, i.e., active. $\overline{INT}$ can also be activated if any of the regulators are below the regulation threshold. Interrupts can also be generated by any of the GPIO pins programmed to be inputs. These inputs can be programmed to generate an interrupt either at the rising or falling edge of the input signal. It is possible to mask an interrupt from any of these conditions individually by setting the appropriate bits in the MASK1, MASK2,

Programming (continued)

or MASK3 registers. By default, all interrupts are masked. Interrupts are stored in the CHGSTATUS, REGSTATUS, and DEFGPIO registers in the serial interface. CHGSTATUS and REGSTATUS interrupts are acknowledged by reading these registers. If a 1 is present in any location, then the TPS65012 automatically sets the corresponding bit in the ACKINT1 or ACKINT2 registers and releases the $\overline{INT}$ pin. The ACKINT register contents are self-clearing when the condition, which caused the interrupt, is removed. The applications processor should not normally need to access the ACKINT1 or ACKINT2 registers.

Interrupt events are always captured; thus when an interrupt source is unmasked, $\overline{INT}$ may immediately go active due to a previous interrupt condition. This can be prevented by first reading the relevant STATUS register before unmasking the interrupt source.

If an interrupt condition occurs, then the $\overline{INT}$ pin is set low. The CHGSTATUS, REGSTATUS, and DEFGPIO registers should be read. Bit positions containing a 1 (or possibly a 0 in DEFGPIO) are noted by the CPU and the corresponding situation resolved. The reading of the CHGSTATUS and REGSTATUS registers automatically acknowledges any interrupt condition in those registers and blocks the path to the $\overline{INT}$ pin from the relevant bit(s). No interrupt should be missed during the read process because this process starts by latching the contents of the register before shifting them out at SDAT. Once the contents have been latched (takes a couple of nanoseconds), the register is free to capture new interrupt conditions. Hence, the probability of missing anything is, for practical purposes, zero.

The following describes how registers 0x01 (CHGSTATUS) and 0x02 (REGSTATUS) are handled:

- CHGSTATUS(5,0) are positive edge set. Read of set CHGSTATUS(5,0) bits sets ACKINT1(5,0) bits.
- CHGSTATUS(7-6,4-1) are level set. Read of set CHGSTATUS(7-6,4-1) bits sets ACKINT1(7-6,4-1) bits.
- CHGSTATUS(5,0) clear when input signal low, and ACKINT1(5,0) bits are already set.
- CHGSTATUS(7-6,4-1) clear when input signal is low.
- ACKINT1(7-0) clear when CHGSTATUS(7-0) is clear.
- REGSTATUS(7-5) are positive edge set. Read of set REGSTATUS(7-5) bits sets ACKINT2(7-5) bits.
- REGSTATUS(3-0) are level set. Read of set REGSTATUS(3-0) bits sets ACKINT2(3-0) bits.
- REGSTATUS(7-5) clear when input signal low, and ACKINT1(7-5) bit are already set.
- REGSTATUS(3-0) clear when input signal is low.
- ACKINT2(7-0) clear when REGSTATUS(7-0) is clear.

The following describes the function of the 0x05 (ACKINT1) and 0x06 (ACKINT2) registers. These are not usually written to by the CPU since the TPS65012 internally sets/clears these registers:

- ACKINT1(7:0) - Bit is set when the corresponding CHGSTATUS set bit is read via I^2C.
- ACKINT1(7:0) - Bit is cleared when the corresponding CHGSTATUS set bit clears.
- ACKINT2(7:0) - Bit is set when the corresponding REGSTATUS set bit is read via I^2C.
- ACKINT2(7:0) - Bit is cleared when the corresponding REGSTATUS set bit clears.
- ACKINT1(7:0) - a bit set masks the corresponding CHGSTATUS bit from $\overline{INT}$.
- ACKINT2(7:0) - a bit set masks the corresponding REGSTATUS bit from $\overline{INT}$.

The following describes the function of the 0x03 (MASK1), 0x04 (MASK2) and 0x0F (MASK3) registers:

- MASK1(7:0) - a bit set in this register masks CHGSTATUS from $\overline{INT}$.
- MASK2(7:0) - a bit set in this register masks REGSTATUS from $\overline{INT}$.
- MASK3(7:4) - a bit set in this register detects a rising edge on GPIO.
- MASK3(7:4) - a bit cleared in this register detects a falling edge on GPIO.
- MASK3(3:0) - a bit set in this register clears GPIO detect signal from $\overline{INT}$.

GPIO interrupts are located by reading the 0x10 (DEFGPIO) register. The application CPU stores, or can read from DEFGPIO<7:4>, which GPIO is set to input or output. This information together with the information on which edge the interrupt was generated (the CPU either knows this or can read it from MASK3<7:4>) determines whether the CPU is looking for a 0 or a 1 in DEFGPIO<3:0>. A GPIO interrupt is blocked from the $\overline{INT}$ pin by setting the relevant MASK3<3:0> bit; this must be done by the CPU; there is no auto-acknowledge for the GPIO interrupts.

Programming (continued)

7.5.3 Serial Interface

The serial interface is compatible with the standard and fast mode I^2C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as V_{CC} remains above 2 V. The TPS65012 has a 7-bit address with the LSB set by the IFLSB pin; this allows the connection of two devices with the same address to the same bus. The 6 MSBs are 100100. Attempting to read data from register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65012 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65012 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65012 device must leave the data line high to enable the master to generate the stop condition.

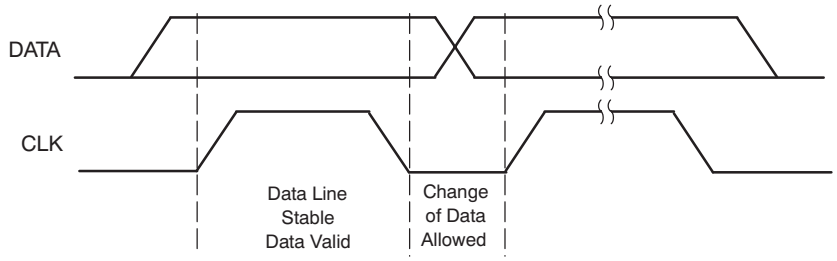


Figure 38. Bit Transfer on the Serial Interface

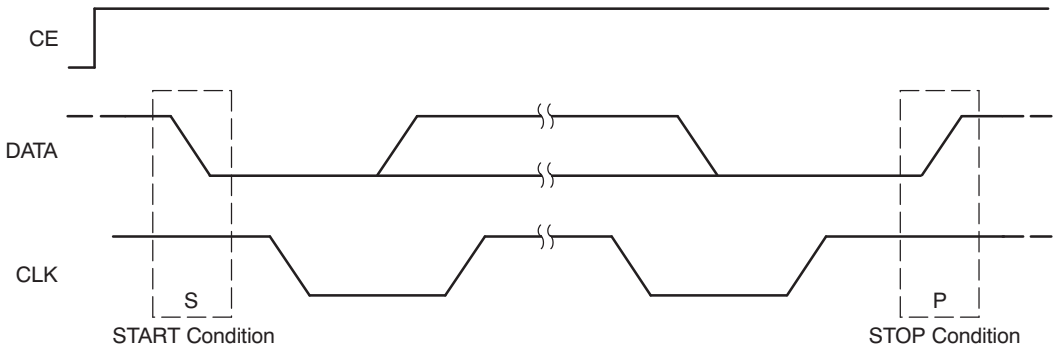


Figure 39. START and STOP Conditions

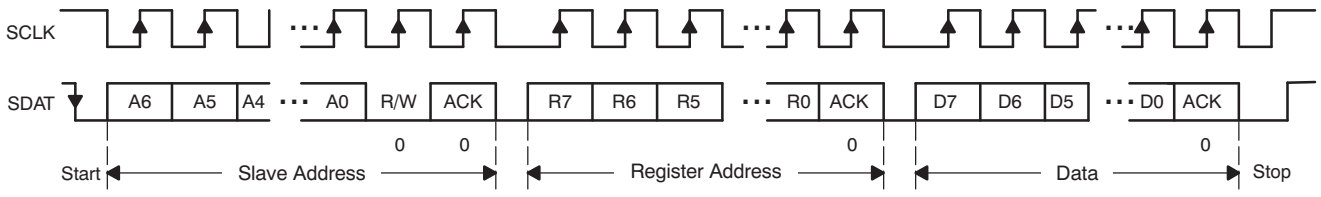


Figure 40. Serial Interface WRITE to TPS65012 Device

Programming (continued)

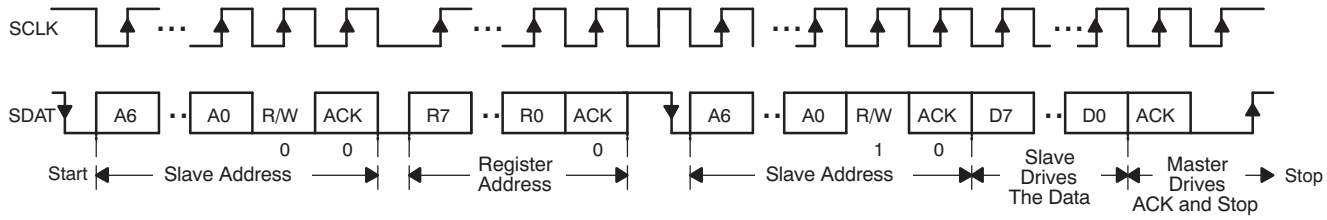


Figure 41. Serial Interface READ From TPS65012: Protocol A

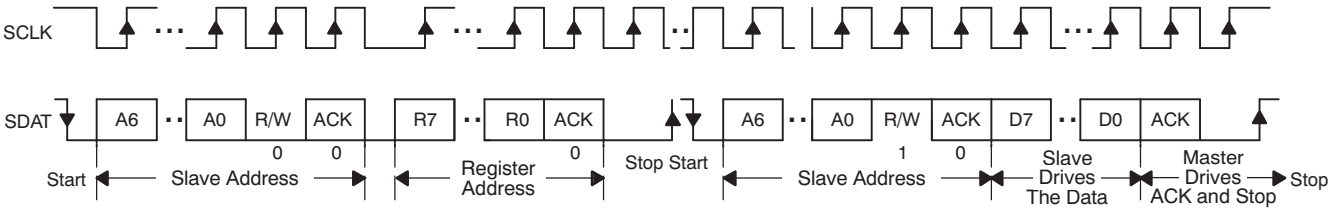


Figure 42. Serial Interface READ From TPS65012: Protocol B

7.6 Register Maps

7.6.1 CHGSTATUS Register (Address: 01h—Reset: 00h)

Table 5. CHGSTATUS Register

CHGSTATUS	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	USB charge	AC charge	Thermal Suspend	Term Current	Taper Timeout	Chg Timeout	Prechg Timeout	BattTemp error
Default	0	0	0	0	0	0	0	0
Read/write	R	R	R	R	R/W	R/W	R/W	R/W

The CHGSTATUS register contents indicate the status of charge.

Bit 7 USB charge:

0 = inactive.

1 = USB source is present and in the range valid for charging. B7 remains active as long as the charge source is present.

Bit 6 AC charge:

0 = wall plug source is not present and/or not in the range valid for charging.

1 = wall plug source is present and in the range valid for charging. B6 remains active as long as the charge source is present.

Bit 5 Thermal suspend:

0 = charging is allowed.

1 = charging is momentarily suspended due to excessive power dissipation on chip.

Bit 4 Term current:

0 = charging, charge termination current threshold has not been crossed.

1 = charge termination current threshold has been crossed and charging has been stopped. This can be due to a battery reaching full capacity or to a battery removal condition.

Bit 3-1 Prechg Timeout, Chg Timeout, Taper Timeout:

0 = charging

1 = one of the timers has timed out and charging has been terminated.

Bit 0 BattTemp error: Battery temperature error

0 = battery temperature is inside the allowed range and charging is allowed.

1 = battery temperature is outside of the allowed range and charging is suspended.

B1-4 may be reset via the serial interface in order to force a reset of the charger. Any attempt to write to B0 and B5-7 is ignored. A *1* in B<7:0> sets the $\overline{\text{INT}}$ pin active unless the corresponding bit in the MASK register is set.

7.6.2 REGSTATUS Register (Address: 02h—Reset: 00h)

Table 6. REGSTATUS Register

REGSTATUS	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	PB_ONOFF	BATT_COVER	UVLO		$\overline{\text{PGOOD}}$ LDO2	$\overline{\text{PGOOD}}$ LDO1	$\overline{\text{PGOOD}}$ MAIN	$\overline{\text{PGOOD}}$ CORE
Default	0	0	0	0	0	0	0	0
Read/write	R	R	R	R	R	R	R	R

Bit 7 PB_ONOFF:

0 = inactive

1 = user activated the PB_ONOFF switch to request that all rails are shut down

Bit 6 BATT_COVER:

0 = BATT_COVER pin is high.

1 = BATT_COVER pin is low.

Bit 5 UVLO:

0 = voltage at the VCC pin above UVLO threshold.

1 = voltage at the VCC pin has dropped below the UVLO threshold.

Bit 4 - not implemented

Bit 3 $\overline{\text{PGOOD}}$ LDO2:

0 = LDO2 output in regulation, or LDO2 is disabled with VREGS1<7> =0.

1 = LDO2 output out of regulation.

Bit 2 $\overline{\text{PGOOD}}$ LDO1:

0 = LDO1 output in regulation, or LDO1 is disabled with VREGS1<3> =0.

1 = LDO1 output out of regulation.

Bit 1 $\overline{\text{PGOOD}}$ MAIN:

0 = Main converter output in regulation.

1 = Main converter output out of regulation.

Bit 0 $\overline{\text{PGOOD}}$ CORE:

0 = Core converter output in regulation.

1 = Core converter output out of regulation register, or VDCDC2<7> =1 in low-power mode.

A rising edge in the REGSTATUS register contents causes $\overline{\text{INT}}$ to be driven low if it is not masked in the MASK2.

7.6.3 MASK1 Register (Address: 03h—Reset: FFh)

Table 7. MASK1 Register

MASK1	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	Mask USB	Mask AC	Mask Thermal Suspend	Mask Term	Mask Taper	Mask Chg	Mask Prechg	Mask BattTemp
Default	1	1	1	1	1	1	1	1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The MASK1 register is used to mask all or any of the conditions in the corresponding CHGSTATUS<7:0> positions being indicated at the INT pin. Default is to mask all.

7.6.4 MASK2 Register (Address: 04h—Reset: FFh)

Table 8. MASK2 Register

MASK2	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	Mask PB_ONOFF	Mask BATT_COVER	Mask UVLO		Mask PGOOD LDO2	Mask PGOOD LDO1	Mask PGOOD MAIN	Mask PGOOD CORE
	Default	1	1	1	1	1	1	1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The MASK2 register is used to mask all or any of the conditions in the corresponding REGSTATUS<7:0> positions being indicated at the INT pin. Default is to mask all.

7.6.5 ACKINT1 Register (Address: 05h—Reset: 00h)

Table 9. ACKINT1 Register

ACKINT1	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	Ack USB	Ack AC	Ack Thermal Shutdown	Ack Term	Ack Taper	Ack Chg	Ack Prechg	Ack BattTemp
Default	0	0	0	0	0	0	0	0
Read/write	R	R	R	R	R	R	R	R

The ACKINT1 register is internally used to acknowledge any of the interrupts in the corresponding CHGSTATUS<7:0> positions. When this is done, the acknowledged interrupt is no longer fed through to the INT pin, and so the INT pin becomes free to indicate the next pending interrupt. If none exists, then the INT pin goes high, else it remains low. A *1* at any position in ACKINT1 is automatically cleared when the corresponding interrupt condition in CHGSTATUS is removed. The application processor should not normally need to access the ACKINT1 register.

7.6.6 ACKINT2 Register (Address: 06h—Reset: 00h)

Table 10. ACKINT2 Register

ACKINT2	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	Ack PB_ONOFF	Ack BATT_ COVER	Ack UVLO		Ack PGOOD LDO2	Ack PGOOD LDO1	Ack PGOOD MAIN	Ack PGOOD CORE
Default	0	0	0	0	0	0	0	0
Read/write	R	R	R	R	R	R	R	R

The ACKINT2 register is internally used to acknowledge any of the interrupts in the corresponding REGSTATUS<7:0> positions. When this is done, the acknowledged interrupt is no longer fed through to the INT pin and so the INT pin becomes free to indicate the next pending interrupt. If none exists, then the INT pin goes high, else it remains low. A *1* at any position in ACKINT2 is automatically cleared when the corresponding interrupt condition in REGSTATUS is removed. The application processor should not normally need to access the ACKINT2 register.

7.6.7 CHGCONFIG Register Address: 07h—Reset: 1Bh

Table 11. CHGCONFIG Register

CHGCONFIG	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	POR	Charger Reset	Fast Charge Timer + Taper Timer Enabled	MSB Charge Current	LSB Charge Current	USB / 100 mA 500 mA	USB Charge Allowed	Charge Enable
Default	0	0	0	1	1	0	1	1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The CHGCONFIG register is used to configure the charger.

Bit 7 POR:

0 = $T_{n(RESPWRON)}$ duration typically 1000 ms (+/-25%)

1 = $T_{n(RESPWRON)}$ duration typically 69 ms (+/-25%)

Bit 6 Charger Reset: clears all the timers in the charger and forces a restart of the charge algorithm.

0 = Normal operation

1 = Charger is in reset.

This bit must be set, and then reset via the serial interface.

Bit 5 Fast Charge Timer + Taper Timer Enabled:

0 = fast charge and taper timers disabled (default).

1 = enables the fast charge and taper times.

Bit 4, Bit 3 MSB/LSB Charge Current:

Used to set the constant current in the current regulation phase.

Table 12. Charge Current Settings

B4:B3	CHARGE CURRENT RATE
11	Maximum current set by the external resistor at the ISET pin
10	75% of maximum
01	50% of maximum
00	32% of maximum

Bit 2 USB 100 mA / 500 mA:

0 = sets the USB charging current to max 100 mA.

1 = sets the USB charging current to max 500 mA. B2 is ignored if B1=0.

Bit 1 USB charge allowed:

0 = prevents any charging from the USB input.

1 = charging from the USB input is allowed.

Bit 0 Charge enable:

0 = charging is not allowed.

1 = charger is free to charge from either of the two input sources. If both sources are present and valid, the TPS65012 charges from the ac source.

7.6.8 LED1_ON Register (Address: 08h—Reset: 00h)

Table 13. LED1_ON Register

LED1_ON	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	$\overline{PG1}$	LED1 ON6	LED1 ON5	LED1 ON4	LED1 ON3	LED1 ON2	LED1 ON1	LED1 ON 0
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The LED1_ON and LED1_PER registers can be used to take control of the $\overline{PG}$ open-drain output normally controlled by the charger.

Bit 7 - $\overline{PG1}$: Control of the $\overline{PG}$ pin is determined by $\overline{PG1}$ and $\overline{PG2}$ according to the table under LED1_PER register

Bit 6 - BIT 0 LED1_ON<6:0> are used to program the on-time of the open-drain output transistor at the $\overline{PG}$ pin. The minimum on-time is typically 10 ms and one LSB corresponds to a 10-ms step change in the on-time.

7.6.9 LED1_PER Register (Address: 09h—Reset: 00h)

Table 14. LED1_PER Register

LED1_PER	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	$\overline{PG2}$	LED1 PER6	LED1 PER5	LED1 PER4	LED1 PER3	LED1 PER2	LED1 PER1	LED1 PER 0
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 - $\overline{PG2}$: Control of the $\overline{PG}$ pin is determined by $\overline{PG1}$ and $\overline{PG2}$ according to the following table.

Table 15. $\overline{PG}$ Open-Drain Output Settings

$\overline{PG1}$	$\overline{PG2}$	BEHAVIOR OF $\overline{PG}$ OPEN-DRAIN OUTPUT
0	**0**	**Under charger control (default) (1)**
0	1	Blink
1	0	Off
1	1	Always On

(1) $\overline{PG}$ is low if either USB or AC are in the valid range for battery charging.

Bit 6-Bit 0 LED1_PER<6:0> are used to program the time period of the open-drain output transistor at the $\overline{PG}$ pin. The minimum period is typically 100 ms and one LSB corresponds to a 100-ms step change in the period.

7.6.10 LED2_ON Register (Address: 0Ah—Reset: 00h)

Table 16. LED2_ON Register

LED2_ON	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	LED21	LED2 ON6	LED2 ON5	LED2 ON4	LED2 ON3	LED2 ON2	LED2 ON1	LED2 ON0
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The LED2_ON and LED2_PER registers are used to control the LED2 open-drain output.

Bit 7 LED22: Control is determined by LED21 and LED22 according to the table under LED2_PER register.

Bit 6-Bit 0 LED2_ON<6:0> are used to program the on-time of the open-drain output transistor at the LED2 pin. The minimum on-time is typically 10 ms and one LSB corresponds to a 10-ms step change in the on-time.

7.6.11 LED2_PER (Register Address: 0Bh—Reset: 00h)

Table 17. LED2_PER

LED2_PER	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	LED22	LED2 PER6	LED2 PER5	LED2 PER4	LED2 PER3	LED2 PER2	LED2 PER1	LED2 PER 0
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 LED22: Control is determined by LED21 and LED22 according to the table.

Bit 6-Bit 0 - LED2_PER<6:0> are used to program the on-time of the open-drain output transistor at the LED2 pin. The minimum on-time is typically 100 ms and one LSB corresponds to a 100-ms step change in the on-time.

Table 18. LED2 Open-Drain Output Setting

LED21	LED22	BEHAVIOR OF LED2 OPEN-DRAIN OUTPUT
0	0	Off
0	1	Blink
1	0	Off
1	1	Always On

7.6.12 VDCDC1 Register (Address: 0Ch—Reset: 72h/73h)

Table 19. VDCDC1 Register

VDCDC1	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	FPWM	UVLO1	UVLO0	ENABLE SUPPLY	ENABLE LP	MAIN DISCHARGE	MAIN1	MAIN0
Default	0	1	1	1	0	0	1	DEFMAIN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The VDCDC1 register is used to program the VMAIN switching converter.

Bit 7 FPWM: forced PWM mode for DC-DC converters.

0 = MAIN and the CORE DC-DC converter are allowed to switch into PFM mode.

1 = MAIN and the CORE DC-DC converter operate with forced fixed frequency PWM mode and are not allowed to switch into PFM mode at light load.

Bit 6-Bit 5 - UVLO<1:0>: The undervoltage threshold voltage is set by UVLO1 and UVLO0 according to Table 20.

Table 20. UVLO Settings

UVLO1	UVLO0	V_{UVLO}
0	0	2.5 V
0	1	2.75 V
1	0	3.0 V
1	**1**	**3.25 V** (reset)

Bit 4 ENABLE SUPPLY:

0 = Disable CORE and MAIN converters when ENABLE LP = 1 and LOW PWR pin goes high.

1 = CORE and MAIN converters remain enabled.

Bit 3 ENABLE LP:

0 = disables the low-power function of the LOW_PWR pin.

1 = enables the low-power function of the LOW_PWR pin.

Bit 2 MAIN DISCHARGE:

0 = Disable the active discharge of the VMAIN output capacitor.

1 = Enable the active discharge of the VMAIN output capacitor when the converter is disabled.

Bit 1-Bit 0 - MAIN<1:0>: The VMAIN converter output voltages are set according to Table 21, with the reset in bold set by the DEFMAIN pin. The default voltage can subsequently be overwritten via the serial interface after start-up.

Table 21. MAIN Settings

MAIN1	MAIN0	VMAIN
0	0	2.5 V
0	1	2.75 V
1	**0**	**3.0 V**
1	**1**	**3.3 V**

7.6.13 VDCDC2 Register (Address: 0Dh—Reset: 68h/78h)

Table 22. VDCDC2 Register

VDCDC2	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	LP_COREOFF	CORE2	CORE1	CORE0	CORELP1	CORELP0	VIB	CORE DISCHARGE
Default	0	1	1	DEFCORE	1	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The VDCDC2 register is used to program the VCORE switching converter output voltage. It is programmable in 8 steps between 0.85 V and 1.6 V. The reset is governed by the DEFCORE pin; DEFCORE=0 sets an output voltage of 1.5 V. DEFCORE=1 sets an output voltage of 1.6 V.

Bit 7 LP_COREOFF:

0 = VCORE converter is enabled in low-power mode.

1 = VCORE converter is disabled in low-power mode.

Bit 6-Bit 4 - CORE<2:0>: The following table shows all possible values of VCORE. The reset can subsequently be overwritten via the serial interface after start-up.

Table 23. CORE Settings

CORE2	CORE1	CORE0	VCORE
0	0	0	0.85 V
0	0	1	1.0 V
0	**1**	**0**	**1.1 V**
0	1	1	1.2 V
1	0	0	1.3 V
1	0	1	1.4 V
1	**1**	**0**	**1.5 V**
1	**1**	**1**	**1.6 V**

Bit 3-Bit 2 - CORELP<1:0>: CORELP1 and CORELP0 can be used to set the VCORE voltage in low-power mode. In low-power mode, CORE2 is effectively '0'; CORE1 and CORE0 take on the values programmed at CORELP1 and CORELP0, default '10' giving VCORE = 1.1 V as default in low-power mode. When low-power mode is exited, VCORE reverts to the value set by CORE2, CORE1, and CORE0.

Bit 1 VIB:

0 = Disables the open-drain VIB output transistor.

1 = Enables the open-drain VIB output transistor to drive the vibrator motor.

Bit 0 CORE DISCHARGE:

0 = Disable the active discharge of the VCORE output capacitor.

1 = Enable the active discharge of the VCORE output capacitor when the converter is disabled.

7.6.14 VREGS1Register (Address: 0Eh—Reset: 88h)

Table 24. VREGS1Register

VREGS1	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	LDO2 enable	LDO2 OFF / nSLP	LDO21	LDO20	LDO1 enable	LDO1 OFF / nSLP	LDO11	LDO10
Default	1	0	0	0	1	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The VREGS1 register is used to program and enable LDO1 and LDO2 and to set their behavior when low-power mode is active. The LDO output voltages can be set either on the fly, while the relevant LDO is disabled, or simultaneously when the relevant enable bit is set. Note that both LDOs are per default ON.

Bit 7-Bit 6 - The function of the LDO2 enable and LDO2 OFF/nSLP bits is shown in Table 25. See the power-on sequencing section for details of low-power mode.

Table 25. LDO2 Enable and LDO2 OFF/nSLP Functions

LDO2 ENABLE	LDO2 OFF / nSLP	LDO STATUS IN NORMAL MODE	LDO STATUS IN LOW-POWER MODE
0	X	OFF	OFF
1	0	ON, full power	ON, reduced power / performance
1	1	ON, full power	OFF

Bit 5-Bit 4 - LDO2<1:0>: LDO2 has a default output voltage of 1.8 V. If so desired, this can be changed at the same time as it is enabled via the serial interface.

Table 26. LDO2 Settings

LDO21	LDO20	VLDO2
0	**0**	**1.8 V**
0	1	2.5 V
1	0	2.75 V
1	1	3.0 V

Bit 3-Bit 2 - The function of the LDO1 enable and LDO1 OFF/nSLP bits is shown in the following table. See the power-on sequencing section for details of low-power mode. Note that programming LDO1 to a higher voltage may force a system power-on reset if the increase is in the 10% or greater range.

Table 27. LDO1 Enable and LDO1 OFF/nSLP Functions

LDO1 ENABLE	LDO1 OFF / nSLP	LDO STATUS IN NORMAL MODE	LDO STATUS IN LOW-POWER MODE
0	X	OFF	OFF
1	0	ON, full power	ON, reduced power / performance
1	1	ON, full power	OFF

Bit 1-Bit 0 - LDO1<1:0>: The LDO1 output voltage is per default set externally. If so desired, this can be changed via the serial interface. The adjustable range is 0.9 V to VINLDO1.

Table 28. LDO1 Settings

LDO11	LDO10	VLDO1
0	**0**	**ADJ**
0	1	2.5 V
1	0	2.75 V
1	1	3.0 V

7.6.15 MASK3 Register (Address: 0Fh—Reset: 00h)

Table 29. MASK3 Register

MASK3	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	Edge trigger GPIO4	Edge trigger GPIO3	Edge trigger GPIO2	Edge trigger GPIO1	Mask GPIO4	Mask GPIO3	Mask GPIO2	Mask GPIO1
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The MASK3 register must be considered when any of the GPIO pins are programmed as inputs.

Bit 7-Bit 4 edge trigger GPIO<4:1>: determine whether the respective GPIO generates an interrupt at a rising or a falling edge

0 = falling edge triggered.

1 = rising edge triggered.

Bit 3-Bit 0 - Mask GPIO<4:1>: can be used to mask the corresponding interrupt. Default is unmasked (MASK3<0:3> =0).

7.6.16 DEFGPIO Register Address: (10h—Reset: 00h)

Table 30. DEFGPIO Register

DEFGPIO	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	IO4	IO3	IO2	IO1	Value GPIO4	Value GPIO3	Value GPIO2	Value GPIO1
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DEFGPIO register is used to define the GPIO pins to be either input or output.

Bit 7-Bit 4 IO<4:1>:

0 = sets the corresponding GPIO to be an input.

1 = sets the corresponding GPIO to be an output.

Bit 3-Bit 0 Value GPIO<4:1>: If a GPIO is programmed to be an output, then the signal output is determined by the corresponding bit. The output circuit for each GPIO is an open-drain NMOS requiring an external pullup resistor.

1 = activates the relevant NMOS, hence forcing a logic low signal at the GPIO pin.

0 = turns the open-drain transistor OFF, hence the voltage at the GPIO pin is determined by the voltage to which the pullup resistor is connected

If a particular GPIO is programmed to be an input, then the contents of the relevant bit in B3-0 is defined by the logic level at the GPIO pin. A logic low forces a *0* and a logic high forces a *1*. If a GPIO is programmed to be an input, then any attempt to write to the relevant bit in B3-0 is ignored.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The VCORE and VMAIN converter are always enabled in a typical application. The VCORE output voltage can be disabled or reduced from 1.5 V to a lower, preset voltage under processor control. When the processor enters the sleep mode, a high signal on the LOW_PWR pin initiates the change.

VCORE typically supplies the digital part of the audio codec. When the processor is in sleep or low-power mode, the audio codec is powered off, so the VCORE voltage can be programmed to lower voltages without a problem. A typical audio codec (e.g., TI AIC23) consumes about 20-mA to 30-mA current from the VCORE power supply.

Supply LDO1 from VMAIN as shown in Figure 46. If this is not done, then subsequent to a UVLO, OVERTEMP, or BATT_COVER = 0 condition, the RESPWRON signal goes high before the VCORE rail has ramped and stabilized. Therefore, the processor core does not receive a power-on-reset signal.

8.2 Typical Applications

8.2.1 TPS65012 Typical Application

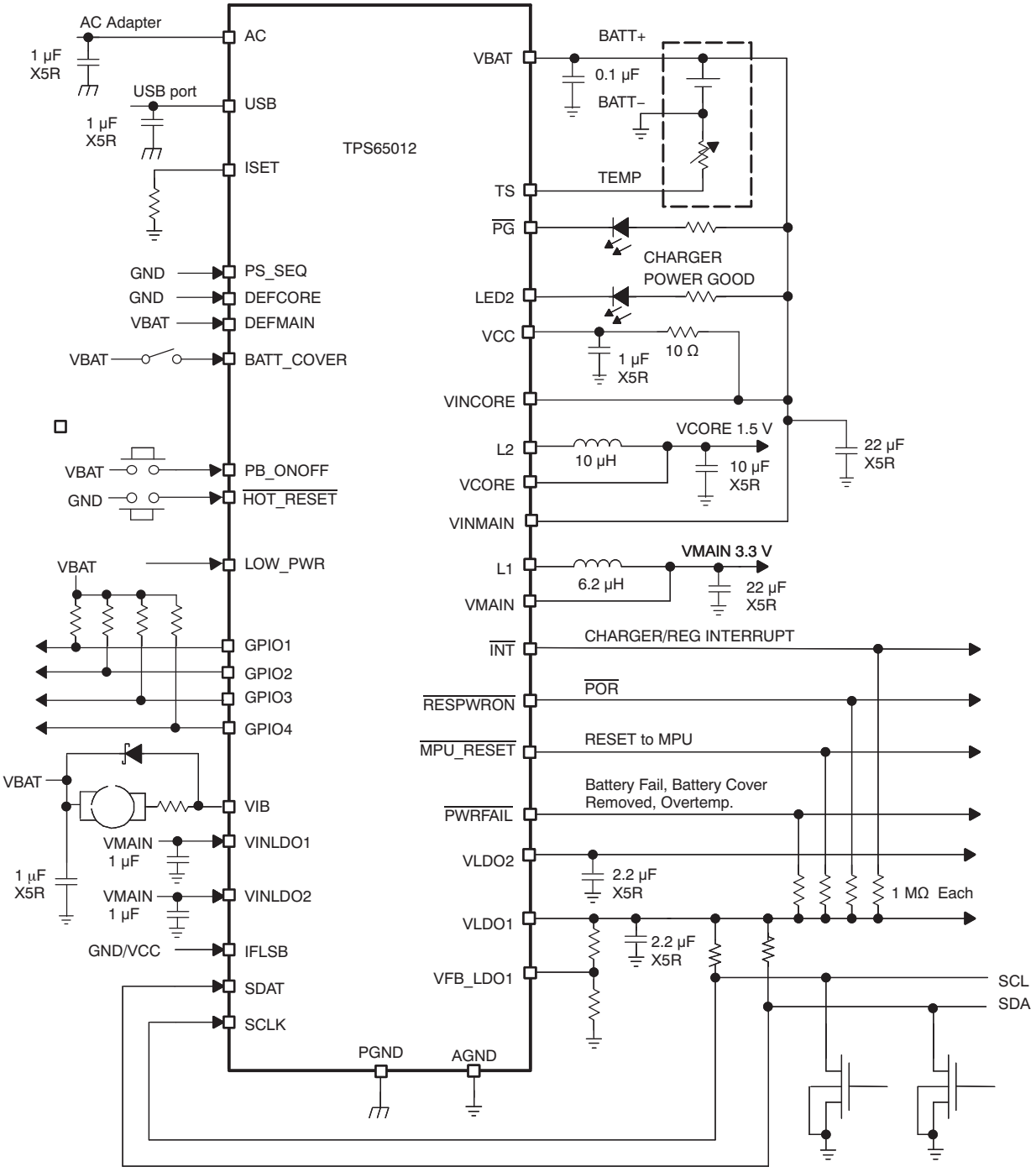


Figure 43. Typical Application Circuit

8.2.1.1 Design Requirements

Each DC/DC converter requires an external inductor and filter capacitor, capable of sustain the intended current with an acceptable voltage ripple. LDOs must have external filter capacitors, and LDO1 requires an external feedback network for regulation. Every input supply rail requires a decoupling capacitor close to the pin, and to avoid unintended states, logic inputs without internal resistors must not be left floating.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection for the Main and the Core Converter

The main and the core converters in the TPS65012 typically use a 6.2-µH and a 10-µH output inductor, respectively. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance is selected for highest efficiency.

Equation 3 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 3. This is needed because during heavy load transient, the inductor current rises above the value calculated under Equation 3.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f}$$

$$I_{L(max)} = I_{O(max)} + \frac{\Delta I_L}{2} \quad (3)$$

where

- f = Switching frequency (1.25 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current (4)

The highest inductor current occurs at maximum V_I.

Open core inductors have a soft saturation characteristic, and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS65012 (2 A for the main converter and 0.8 A for the core converter). Keep in mind that the core material from inductor to inductor differs and has an impact on the efficiency especially at high switching frequencies.

See Table 31 and the typical applications for possible inductors

Table 31. Tested Inductors

DEVICE	INDUCTOR VALUE	DIMENSIONS	COMPONENT SUPPLIER
Core converter	10 µH	6,0 mm × 6,0 mm × 2,0 mm	Sumida CDRH5D18-100
	10 µH	5,0 mm × 5,0 mm × 3,0 mm	Sumida CDRH4D28-100
Main converter	4.7 µH	5,5 mm × 6,6 mm*1,0 mm	Coilcraft LPO1704-472M
	4.7 µH	5,0 mm × 5,0 mm × 3,0 mm	Sumida CDRH4D28C-4.7
	4.7 µH	5,2 mm × 5,2 mm × 2,5 mm	Coiltronics SD25-4R7
	5.3 µH	5,7 mm × 5,7 mm × 3,0 mm	Sumida CDRH5D28-5R3
	6.2 µH	5,7 mm × 5,7 mm × 3,0 mm	Sumida CDRH5D28-6R2
	6.0 µH	7,0 mm × 7,0 mm × 3,0 mm	Sumida CDRH6D28-6R0

8.2.1.2.2 Output Capacitor Selection

The advanced fast response voltage mode control scheme of the inductive converters implemented in the TPS65012 allow the use of small ceramic capacitors with a typical value of 22 µF for the main converter and 10 µF for the core converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors with an ESR < 100 Ω resistance may be used as well.

See Table 32 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating must meet the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{RMSC(out)} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{2 \times \sqrt{3}} \right) \quad (5)$$

At nominal load current, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR \right) \quad (6)$$

Where the highest output voltage ripple occurs at the highest input voltage V_I.

At light load currents, the converters operate in power-save mode, and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the nominal output voltage. If the output voltage for the core converter is programmed to its lowest voltage of 0.85 V, the output capacitor must be increased to 22 µF for low output voltage ripple. This is because the current in the inductor decreases slowly during the off-time and further increases the output voltage even when the PMOS is off. This effect increases with low output voltages.

8.2.1.2.3 Input Capacitor Selection

A pulsating input current is the nature of the buck converter. Therefore, a low ESR input capacitor is required for best input voltage filtering. It also minimizes the interference with other circuits caused by high input voltage spikes. The main converter needs a 22-µF ceramic input capacitor and the core converter a 10-µF ceramic capacitor. The input capacitor for the main and the core converter can be combined and one 22-µF capacitor can be used instead, because the two converters operate with a phase shift of 270 degrees. The input capacitor can be increased without any limit for better input voltage filtering. The VCC pin should be separated from the input for the main and the core converter. A filter resistor of up to 100 Ω and a 1-µF capacitor is used for decoupling the VCC pin from switching noise.

Table 32. Possible Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 µF	1206	TDK C3216X5R0J226M	Ceramic
22 µF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22 µF	1210	Taiyo Yuden JMK325BJ226MM	Ceramic

8.2.1.3 Application Curves

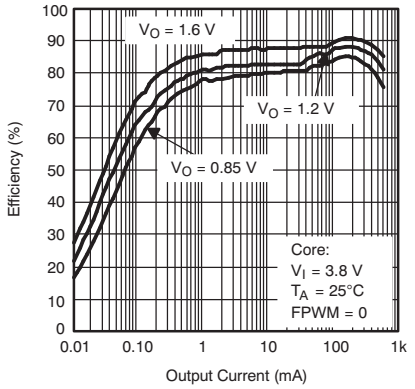


Figure 44. Efficiency vs Output Current

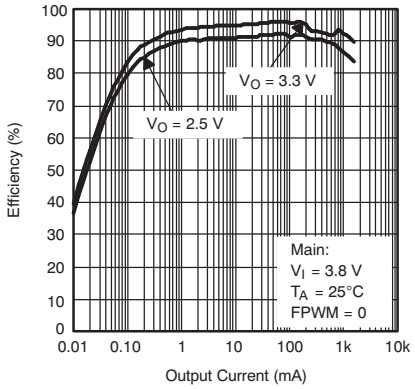


Figure 45. Efficiency vs Output Current

8.2.2 Low-Power Mode

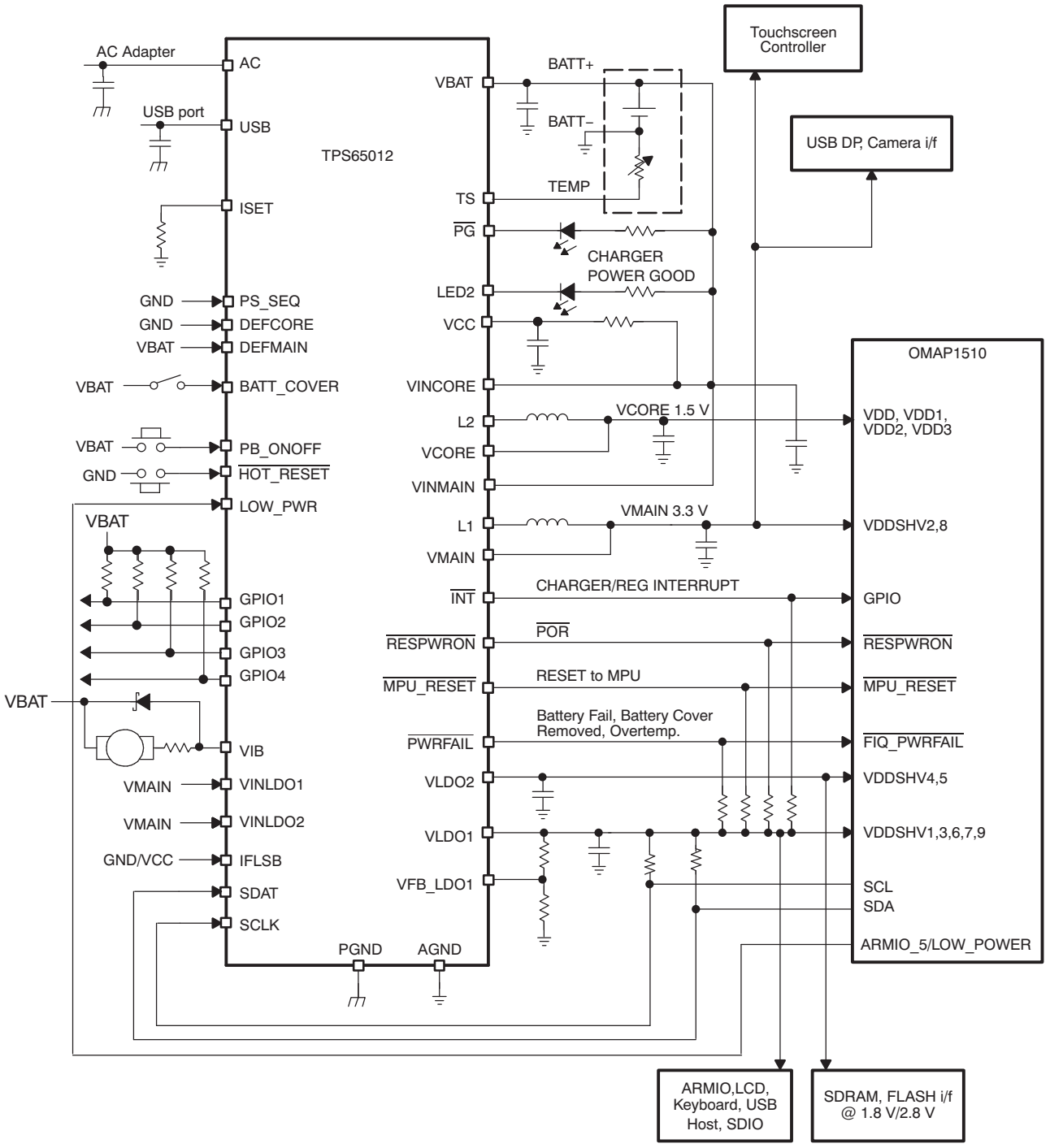


Figure 46. Typical Application Circuit in Low-Power Mode

8.2.2.1 Design Requirements

Use external logic or processor to control LOW_PWR state.

8.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

9 Power Supply Recommendations

9.1 LDO1 Output Voltage Adjustment

The output voltage of LDO1 is set with a resistor divider at the feedback pin. The sum of the two resistors must not exceed 1 MΩ to minimize voltage changes due to leakage current into the feedback pin. The output voltage for LDO1 after start-up is the voltage set by the external resistor divider. It can be reprogrammed with the I^2C interface to the three other values defined in the register VREGS1.

10 Layout

10.1 Layout Guidelines

The input capacitors for the DC-DC converters should be placed as close as possible to the VINMAIN, VINCORE, and VCC pins.

- The inductor of the output filter should be placed as close as possible to the device to provide the shortest switch node possible, reducing the noise emitted into the system and increasing the efficiency.
- Sense the feedback voltage from the output at the output capacitors to ensure the best DC accuracy. Feedback should be routed away from noisy sources such as the inductor. If possible route on the opposite side from the switch node and inductor and place a GND plane between the feedback and the noisy sources or keep out underneath them entirely.
- Place the output capacitors as close as possible to the inductor to reduce the feedback loop. This will ensure best regulation at the feedback point.
- Place the device as close as possible to the most demanding or sensitive load. The output capacitors should be placed close to the input of the load. This will ensure the best AC performance possible.
- The input and output capacitors for the LDOs should be placed close to the device for best regulation performance.
- Use vias to connect thermal pad to ground plane.
- TI recommends using the common ground plane for the layout of this device. The AGND can be separated from the PGND but, a large low parasitic PGND is required to connect the PGNDx pins to the CIN and external PGND connections. If the AGND and PGND planes are separated, have one connection point to reference the grounds together. Place this connection point close to the IC.

10.2 Layout Example

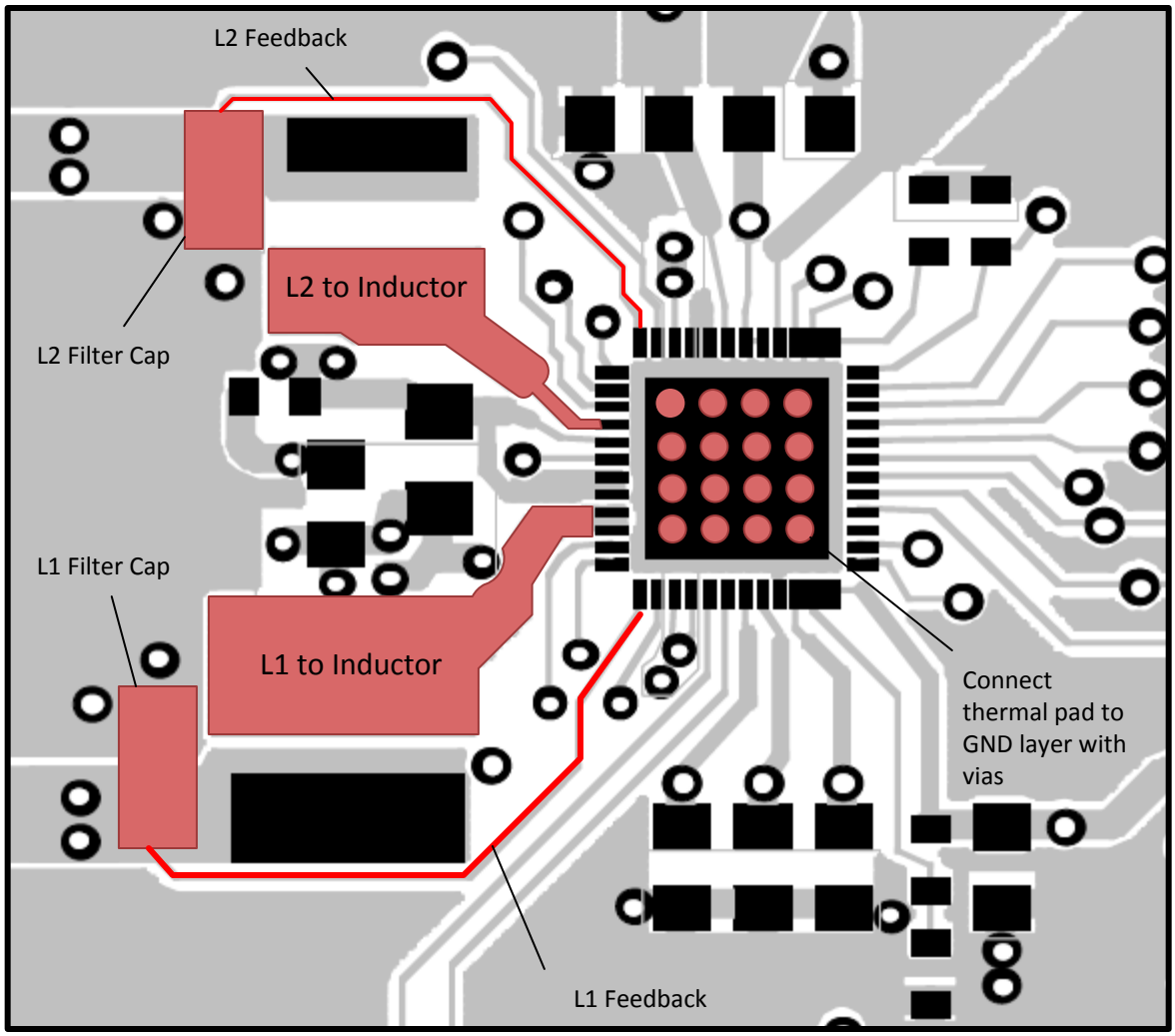


Figure 47. EVM Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65012RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65012	Samples
TPS65012RGZRG4	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65012	Samples
TPS65012RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR		TPS65012	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

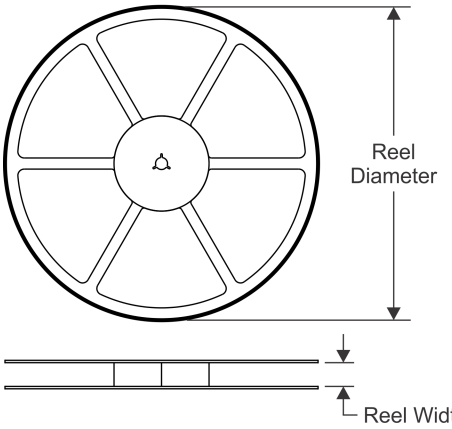
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

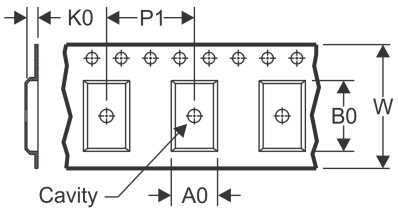
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

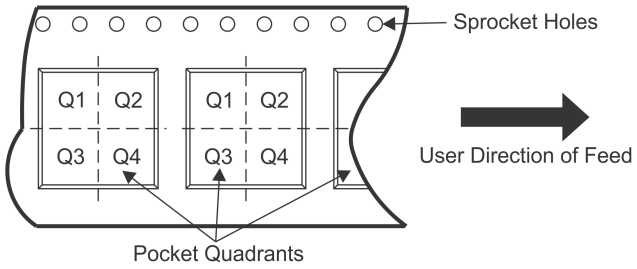


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

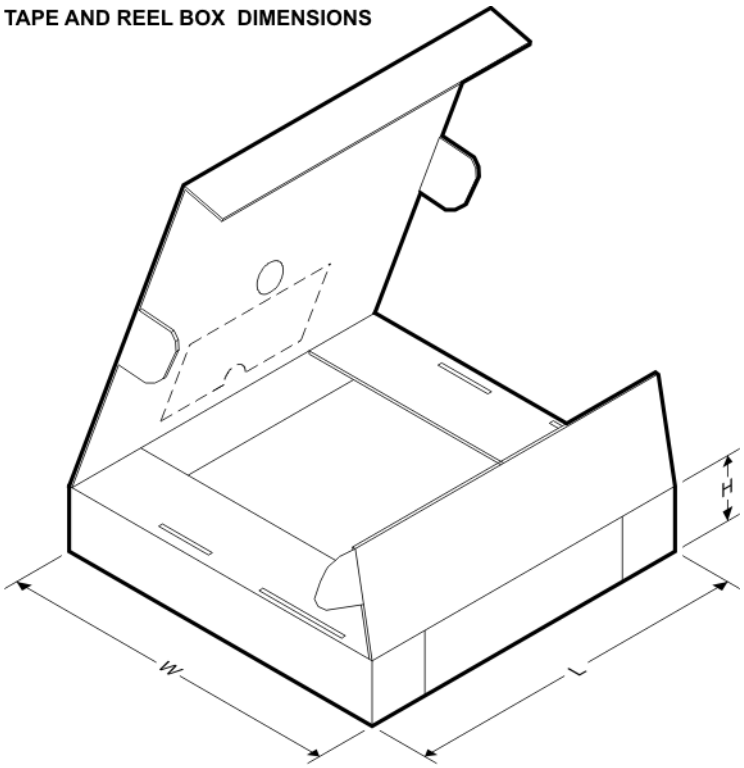
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65012RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TPS65012RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65012RGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
TPS65012RGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

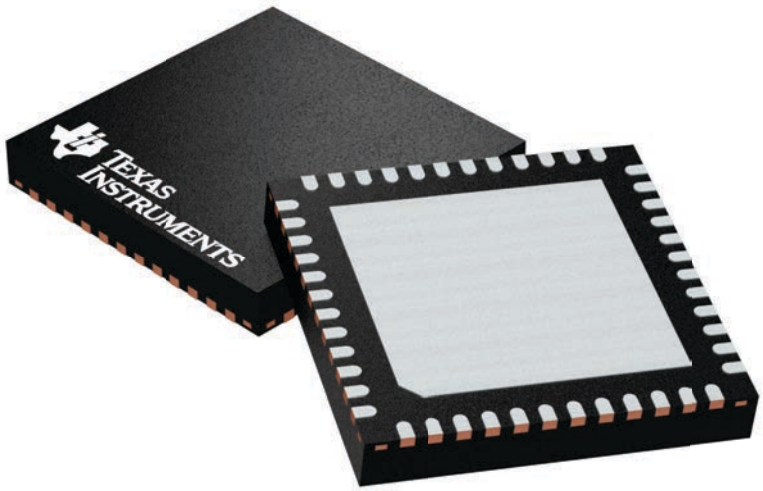
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

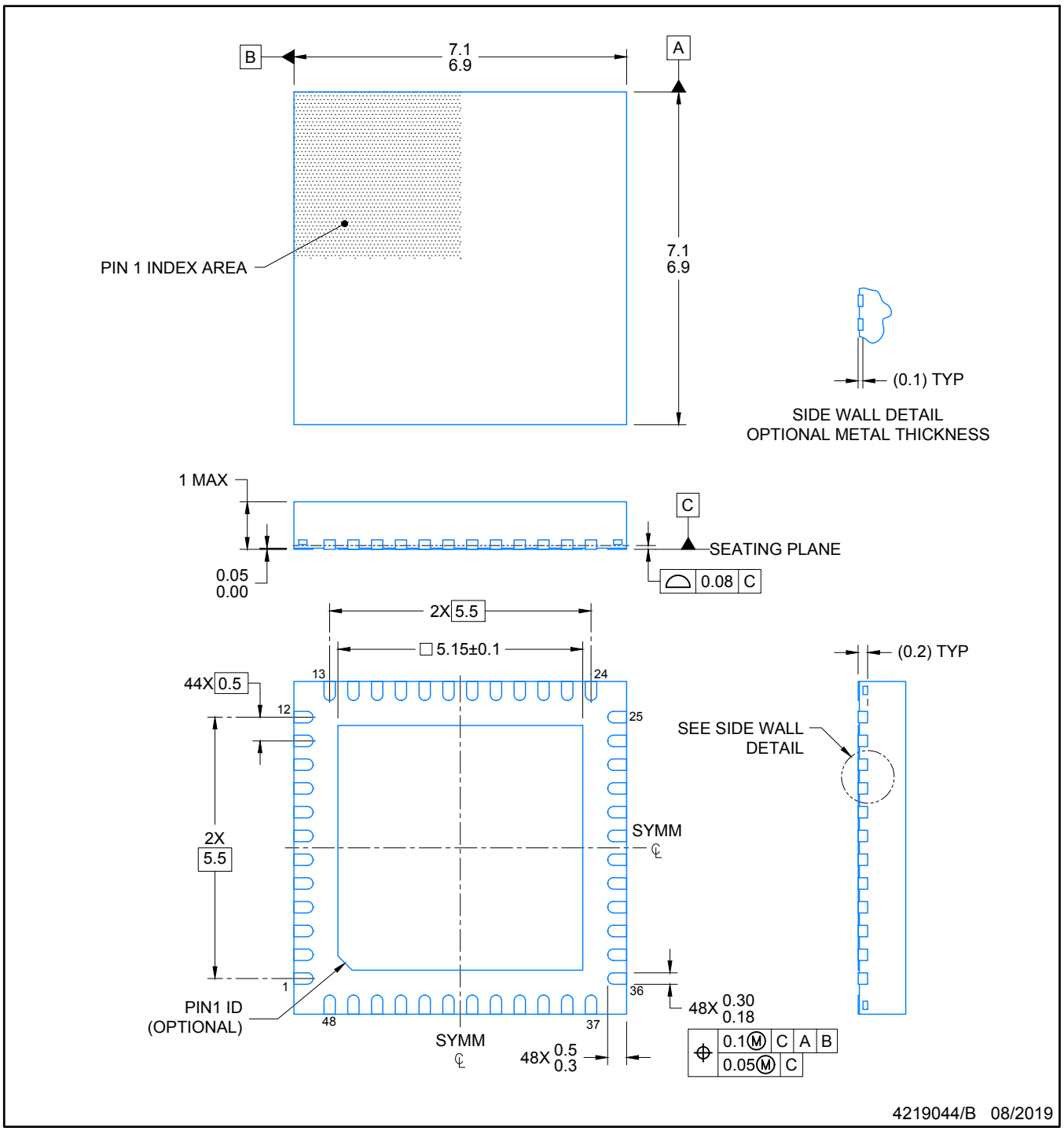
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



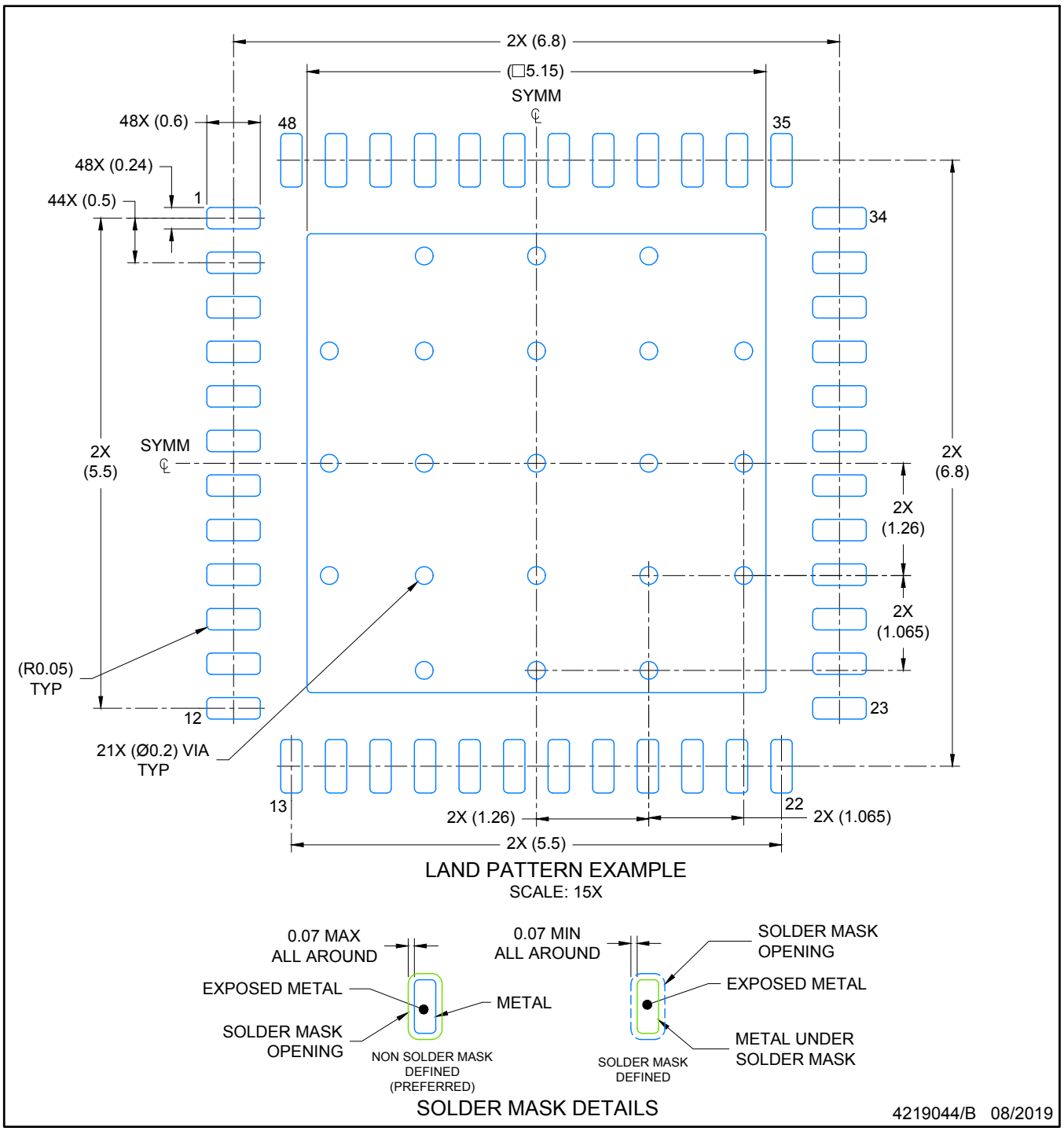
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



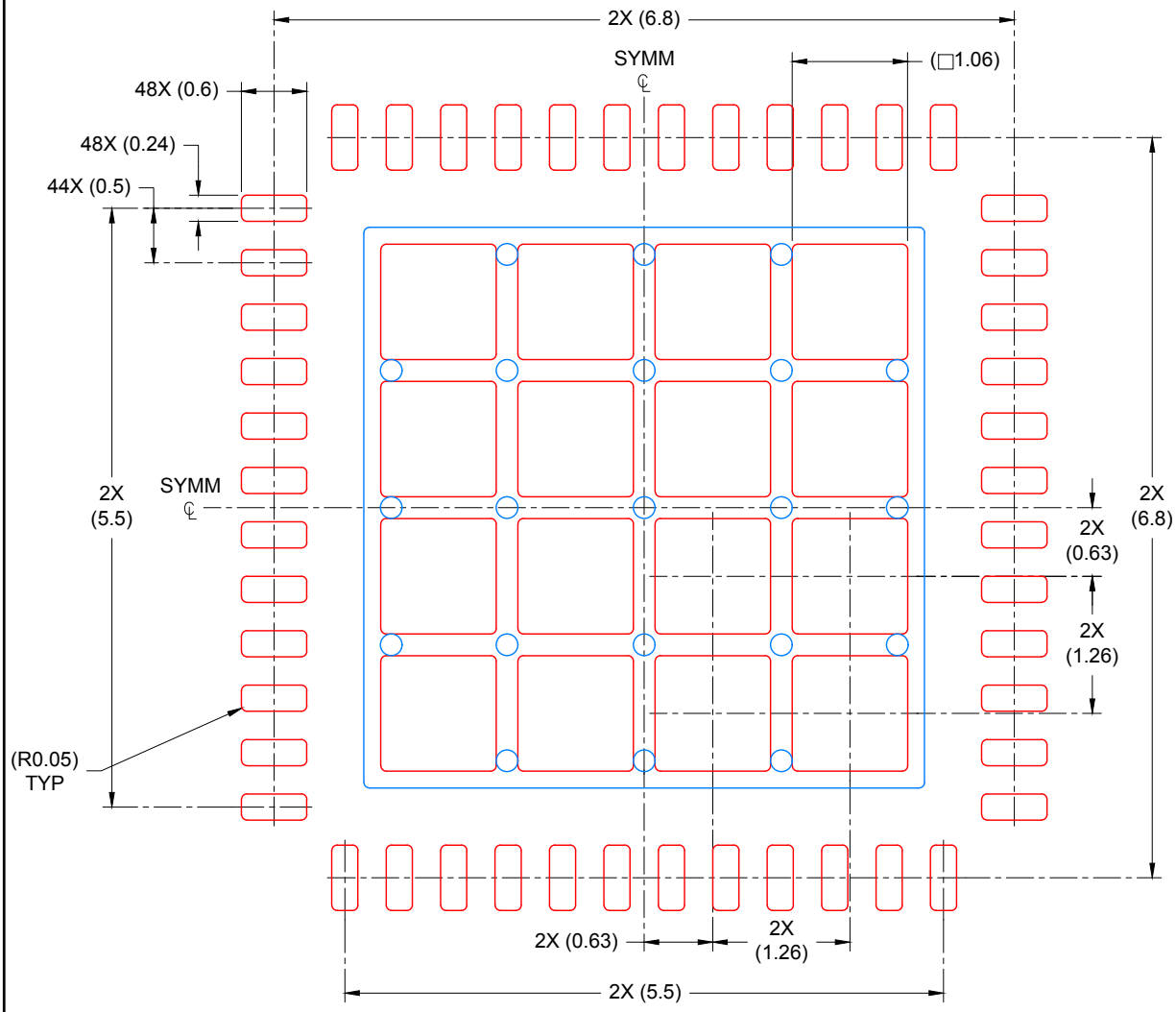
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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