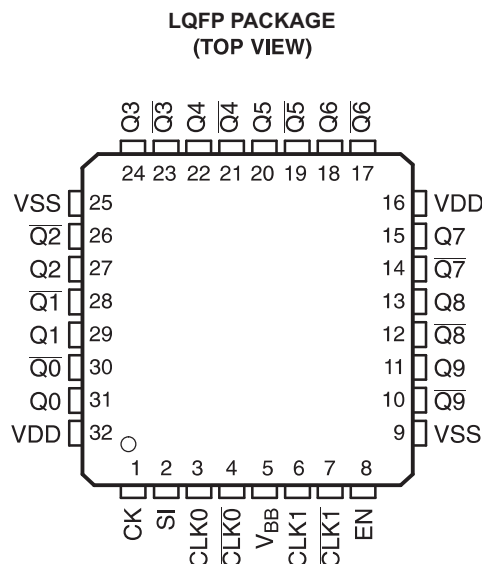


Not Recommended for New Designs PROGRAMMABLE LOW-VOLTAGE 1:10 LVDS CLOCK DRIVER

FEATURES

- Low-Output Skew <30 ps (Typical) for Clock-Distribution Applications
- Distributes One Differential Clock Input to 10 LVDS Differential Clock Outputs
- V_{CC} range 2.5 V $\pm$ 5%
- Typical Signaling Rate Capability of Up to 1.1 GHz
- Configurable Register (SI/CK) Individually Enables Disables Outputs, Selectable CLK0, CLK1 or CLK1, CLK1 Inputs
- Full Rail-to-Rail Common-Mode Input Range
- Receiver Input Threshold $\pm$ 100 mV
- Available in 32-Pin LQFP Package
- Fail-Safe I/O-Pins for $V_{DD} = 0$ V (Power Down)



DESCRIPTION

The CDCLVD110 clock driver distributes one pair of differential LVDS clock inputs (either CLK0 or CLK1) to 10 pairs of differential clock outputs (Q0, Q9) with minimum skew for clock distribution. The CDCLVD110 is specifically designed for driving 50- Ω transmission lines.

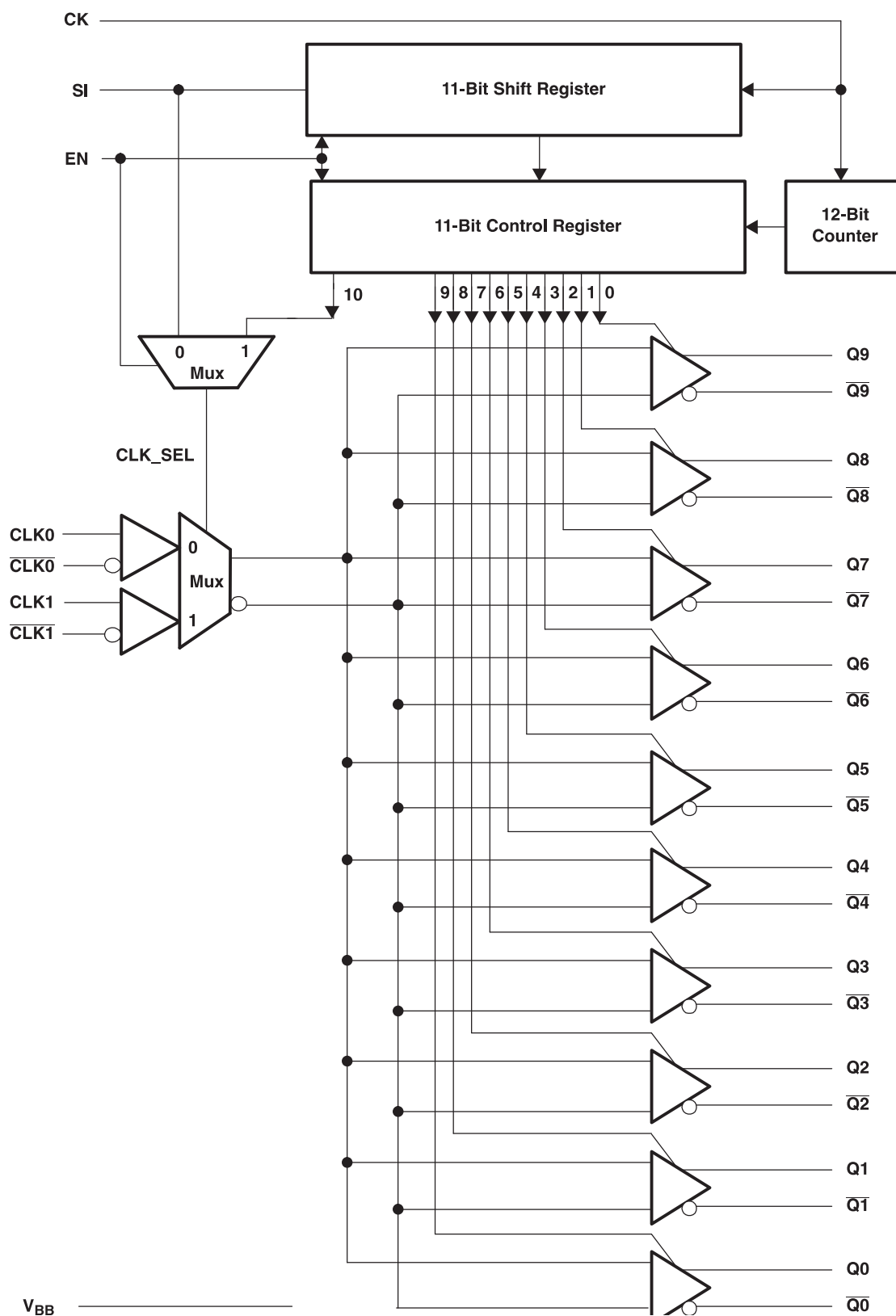
When the control enable is high ($EN = 1$), the 10 differential outputs are programmable in that each output can be individually enabled/disabled (3-stated) according to the first 10 bits loaded into the shift register. Once the shift register is loaded, the last bit selects either CLK0 or CLK1 as the clock input. However, when $EN = 0$, the outputs are not programmable and all outputs are enabled.

The CDCLVD110 is characterized for operation from -40°C to 85°C .

Not Recommended for New Designs. Use CDCLVD110A as a Replacement.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CK	1	I	Control register input clock, features a 120-k Ω pullup resistor
SI	2	I	Control register serial input/CLK Select, features a 120-k Ω pulldown resistor
CLK0	3	I	True differential input, LVDS
$\overline{\text{CLK0}}$	4	I	Complementary differential input, LVDS
V _{BB}	5	O	Reference voltage output
CLK1	6	I	True differential input, LVDS
$\overline{\text{CLK1}}$	7	I	Complementary differential input, LVDS
EN	8	I	Control enable (for programmability), features a 120-k Ω pulldown resistor, input
V _{SS}	9, 25		Device ground
V _{DD}	16, 32		Supply voltage
Q [9:0]	11, 13, 15, 18, 20, 22, 24, 27, 29, 31	O	Clock outputs, these outputs provide low-skew copies of CLKIN
$\overline{\text{Q}}[9:0]$	10, 12, 14, 17, 19, 21, 23, 26, 28, 30	O	Complementary clock outputs, these outputs provide low-skew copies of CLKIN

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

	VALUE	UNIT
V _{DD} Supply voltage	–0.3 to 2.8	V
V _I Input voltage	–0.2 to (V _{DD} + 0.2)	V
V _O VI Output voltage	–0.2 to (V _{DD} + 0.2)	V
Q _n , $\overline{\text{Q}}_n$, I _{OSD} Driver short circuit current	Continuous	
Electrostatic discharge (HBM 1.5 k Ω , 100 pF), ESD	>2000	V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V _{DD} Supply voltage	2.375	2.5	2.625	V
V _{IC} Receiver common-mode input voltage	0.5 V _{ID}		V _{DD} – 0.5 V _{ID}	V
T _A Operating free-air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
V _{OD}	Differential output voltage	R _L = 100 Ω	250	450	600	mV
ΔV_{OD}	V _{OD} magnitude change				50	mV
V _{OS}	Offset voltage	–40°C to 85°C	0.95	1.2	1.45	V
ΔV_{OS}	V _{OS} magnitude change				350	mV
I _{OS}	Output short circuit current	V _O = 0 V			–20	mA
		V _{OD} = 0 V			20	
V _{BB}	Reference output voltage	V _{DD} = 2.5 V, I _{BB} = –100 μ A	1.15	1.25	1.35	V
C _O	Output capacitance	V _O = V _{DD} or GND		3		pF

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
RECEIVER								
V _{IDH}	Input threshold high						100	mV
V _{IDL}	Input threshold low				−100			mV
V _{ID}	Input differential voltage				200			mV
I _{IH}	Input current, CLK0/ $\overline{\text{CLK0}}$, CLK1/ $\overline{\text{CLK1}}$		V _I = V _{DD}		−5		5	μA
I _{IL}			V _I = 0 V					
C _I	Input capacitance		V _I = V _{DD} or GND				3	pF
SUPPLY CURRENT								
I _{DD}	Supply current	Full loaded	All outputs enabled and loaded, R _L = 100 Ω, f = 0 Hz			130		mA
		No load	Outputs enabled, no output load, f = 0 Hz			35		
I _{DDZ}		3-State	All outputs 3-state by control logic, f = 0 Hz			35		

JITTER CHARACTERISTICScharacterized with CDCLVD110 performance EVM, V_{DD} = 3.3 V, OUTPUTS NOT UNDER TEST are terminated to 50Ω

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
j _{jitterLVDS}	Additive phase jitter from input to LVDS output Q3 and $\overline{\text{Q3}}$	12 kHz to 5 MHz, f _{out} = 30.72 MHz				650		fs rms
		12 kHz to 20 MHz, f _{out} = 125 MHz				299		

LVDS — SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, V_{DD} = 2.5 V ±5%

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay low-to-high	CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	Qn, $\overline{\text{Qn}}$		2	3	ns
t _{PHL}	Propagation delay high-to-low	CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	Qn, $\overline{\text{Qn}}$		2	3	ns
t _{duty}	Duty cycle	CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	Qn, $\overline{\text{Qn}}$	45%		55%	
t _{sk(o)}	Output skew		Any Qn, $\overline{\text{Qn}}$		30		ps
t _{sk(p)}	Pulse skew		Any Qn, $\overline{\text{Qn}}$			50	ps
t _{sk(pp)}	Part-to-part skew		Any Qn, $\overline{\text{Qn}}$			600	ps
t _r	Output rise time, 20% to 80%, R _L = 100 Ω, C _L = 5 pF		Any Qn, $\overline{\text{Qn}}$			350	ps
t _f	Output fall time, 20% to 80%, R _L = 100 Ω, C _L = 5 pF		Any Qn, $\overline{\text{Qn}}$			350	ps
f _{clk}	Max input frequency	CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	Any Qn, $\overline{\text{Qn}}$	900	1100		MHz

CONTROL REGISTER CHARACTERISTICSover recommended operating free-air temperature range, V_{DD} = 2.5 V ±5% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f _{MAX}	Maximum frequency of shift register			100	150		MHz
t _{SU}	Setup time, clock to SI					2	ns
t _H	Hold time, clock to SI					1.5	ns
t _{removal}	Removal time, enable to clock					1.5	ns
t _w	Clock pulse width, minimum			3			ns
V _{IH}	Logic input high	V _{DD} = 2.5 V		2			V
V _{IL}	Logic input low	V _{DD} = 2.5 V				0.8	V

CONTROL REGISTER CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $V_{DD} = 2.5\text{ V} \pm 5\%$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input current, CK pin	$V_I = V_{DD}$	–5		5	μA
	Input current, SI and EN pins		10		–30	
I_{IL}	Input current, CK pin	$V_I = \text{GND}$	–10		30	μA
	Input current, SI and EN pins		–5		5	

SPECIFICATION OF CONTROL REGISTER

The CDCLVD110 is provided with an 11-bit, serial-in shift register and an 11-bit control register. The control Register enables/disables each output clock and selects either CLK0 or CLK1 as the input clock. The CDCLVD110 has two modes of operation:

Programmable Mode (EN=1)

The shift register utilizes a serial input (SI) and a clock input (CK). Once the shift register is loaded with 11 clock pulses, the twelfth clock pulse loads the control register. The first bit (bit 0) on SI enables the Q9, $\overline{Q9}$ output pair, and the tenth bit (bit 9) enables the Q0, $\overline{Q0}$ pair. The eleventh bit (bit 10) on SI selects either CLK0 or CLK1 as the input clock; a bit value of 0 selects CLK0, whereas a bit value of 1 selects CLK1. To restart the control register configuration, a reset of the state machine must be done with a clock pulse on CK (shift register clock input) and EN set to low. The control register can be configured only once after each reset.

Standard Mode (EN=0)

In this mode, the CDCLVD110 is not programmable and all the clock outputs are enabled. The clock input (CLK0 or CLK1) is selected with the SI pin, as is shown in the table entitled control register.

STATE-MACHINE INPUTS			
EN	SI	CK	OUTPUT
L	L	X	All outputs enabled, CLK0 selected, control register disabled, default state
L	H	X	All outputs enabled, CLK1 selected, control register disabled
H	L	↑	First stage stores L, other stage stores data of previous stage
H	H		First stage stores H, other stage stores data of previous stage
L	X		Reset of state machine, shift and control registers

CONTROL REGISTER		
BIT 10	BITS [0-9]	$Q_N[0-9]$
L	H	CLK0
H	H	CLK1
X	L	Outputs disabled

SERIAL INPUT (SI) SEQUENCE										
BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CLK_SEL	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9

TRUTH TABLE FOR CONTROL LOGIC									
CK	EN	SI	CLK0	$\overline{\text{CLK0}}$	CLK1	$\overline{\text{CLK1}}$	Q(0-9)	$\overline{Q(0-9)}$	
L	L	L	L	H	X	X	L	H	
L	L	L	H	L	X	X	H	L	
L	L	L	Open	Open	X	X	L	H	
L	L	H	X	X	L	H	L	H	
L	L	H	X	X	H	L	H	L	
L	L	H	X	X	Open	Open	L	H	
All outputs enabled			X = Don't care						

APPLICATION INFORMATION

Fall-Safe Information

For $V_{DD} = 0$ V (power-down mode) the CDCLVD110 has fail-safe input and output pins. In power-on mode, fail-safe biasing at input pins can be accomplished with a 10-k Ω pullup resistor from CLK0/CLK1 to VDD and a 10-k Ω pulldown resistor from CLK0/CLK1 to GND.

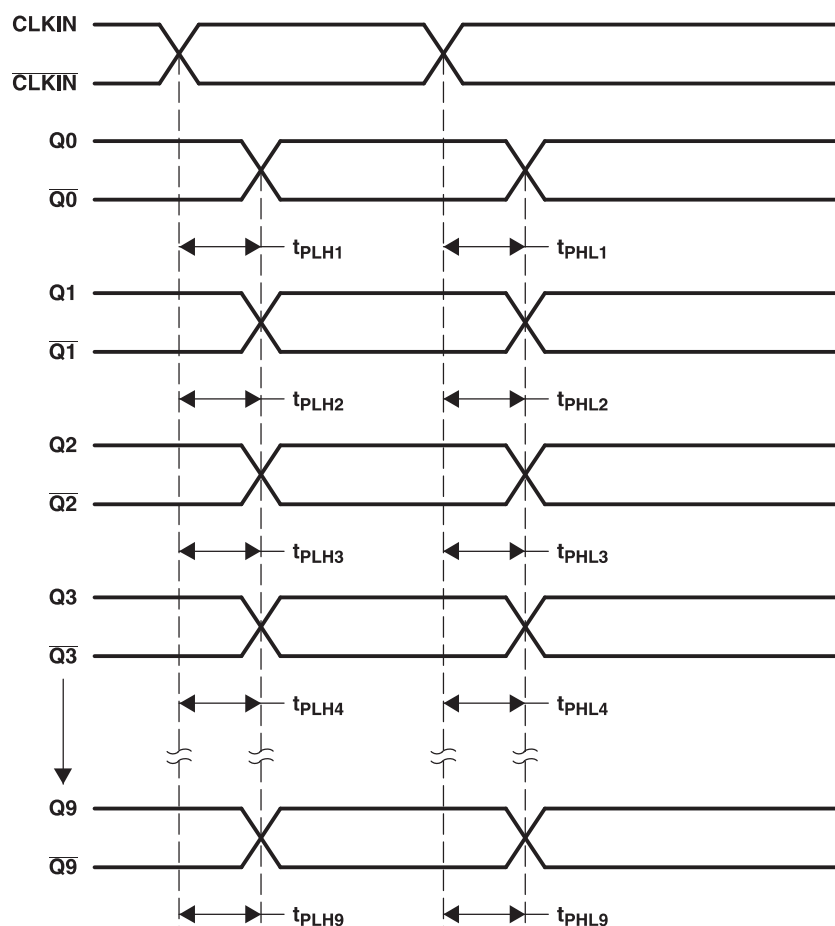
LVDS Receiver Input Termination

The LVDS receiver inputs need to have 100- Ω termination resistors placed as close as possible across the input pins.

Control Inputs Termination

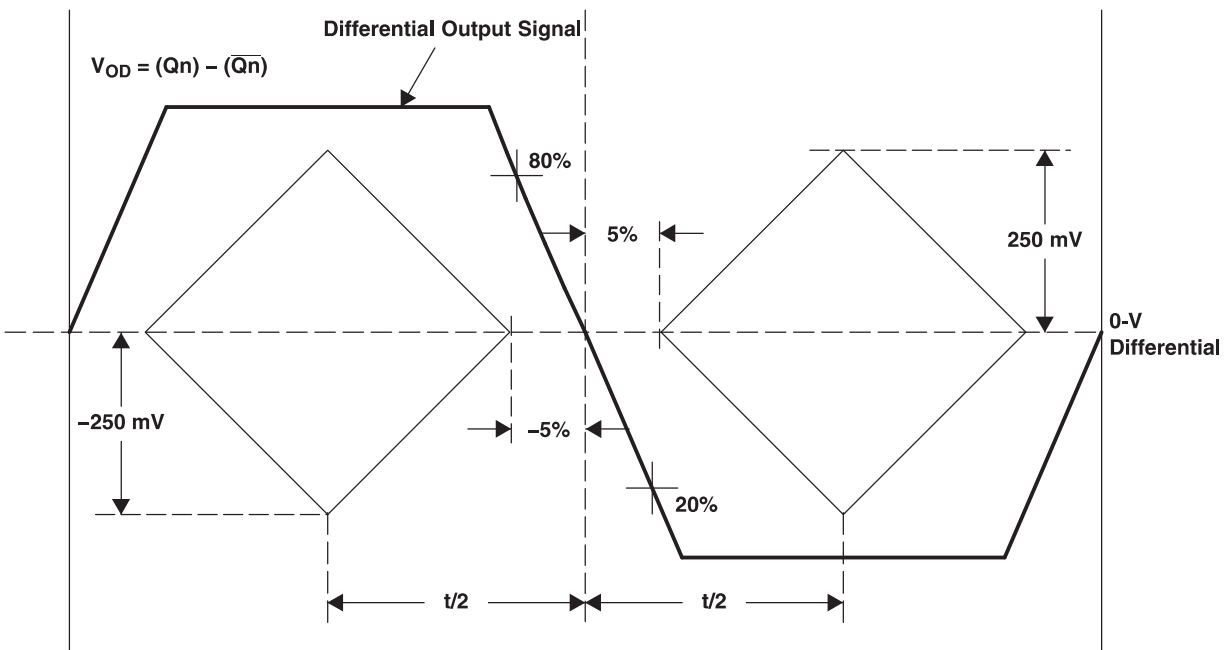
No external termination is required. The CK control input has an internal 120-k Ω pullup resistor while SI- and EN-control inputs each have an internal 120-k Ω pulldown resistor. If the control pins are left open per the default, all outputs are enabled, CLK0, CLK0 is selected, and the control register is disabled.

PARAMETER MEASUREMENT INFORMATION



- A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
 - The difference between the fastest and the slowest t_{PLHn} ($n = 1, 2, \dots, 10$)
 - The difference between the fastest and the slowest t_{PHLn} ($n = 1, 2, \dots, 10$)
- B. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
 - The difference between the fastest and the slowest t_{PLHn} ($n = 1, 2, \dots, 10$) across multiple devices
 - The difference between the fastest and the slowest t_{PHLn} ($n = 1, 2, \dots, 10$) across multiple devices
- C. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low (t_{PHL}) and the low-to-high (t_{PLH}) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)} = |t_{PHL} - t_{PLH}|$. Pulse skew is sometimes referred to as pulse width distortion or duty cycle skew.

Figure 1. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$

PARAMETER MEASUREMENT INFORMATION (continued)**Figure 2. Test Criteria for f_{clk} , Duty Cycle, t_r , t_f , V_{OD}**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCLVD110VF	NRND	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVD110	
CDCLVD110VFR	NRND	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVD110	
CDCLVD110VFRG4	NRND	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVD110	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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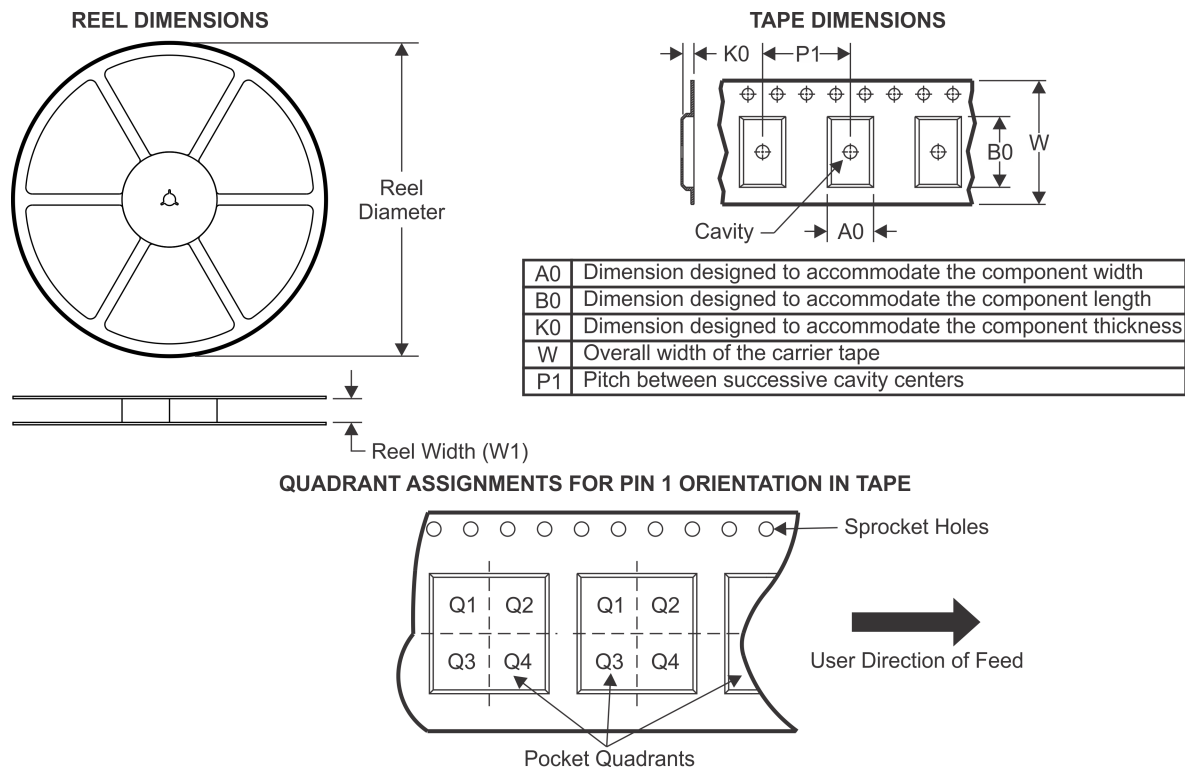


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PACKAGE OPTION ADDENDUM

6-Feb-2020

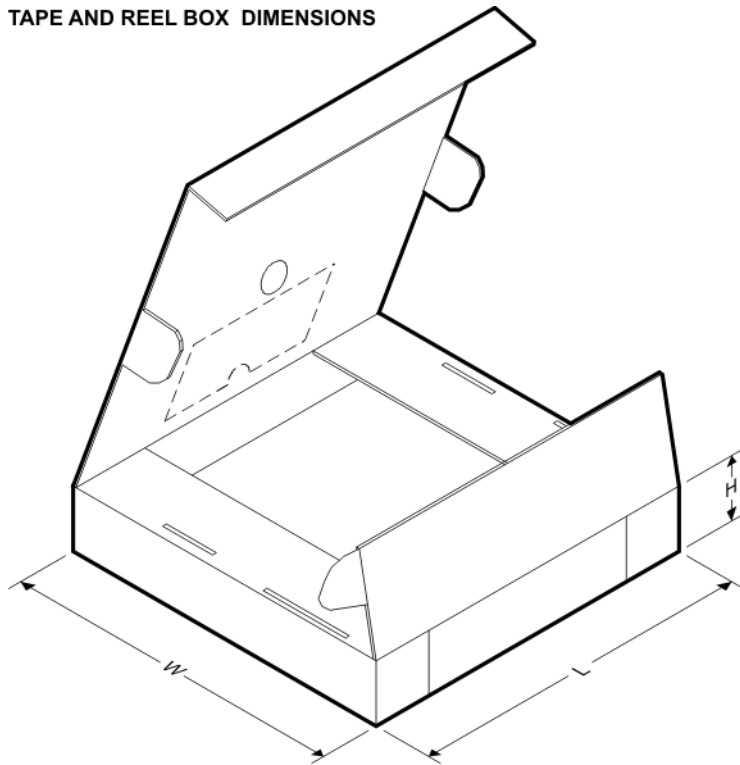
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD110VFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD110VFR	LQFP	VF	32	1000	341.0	159.0	123.5

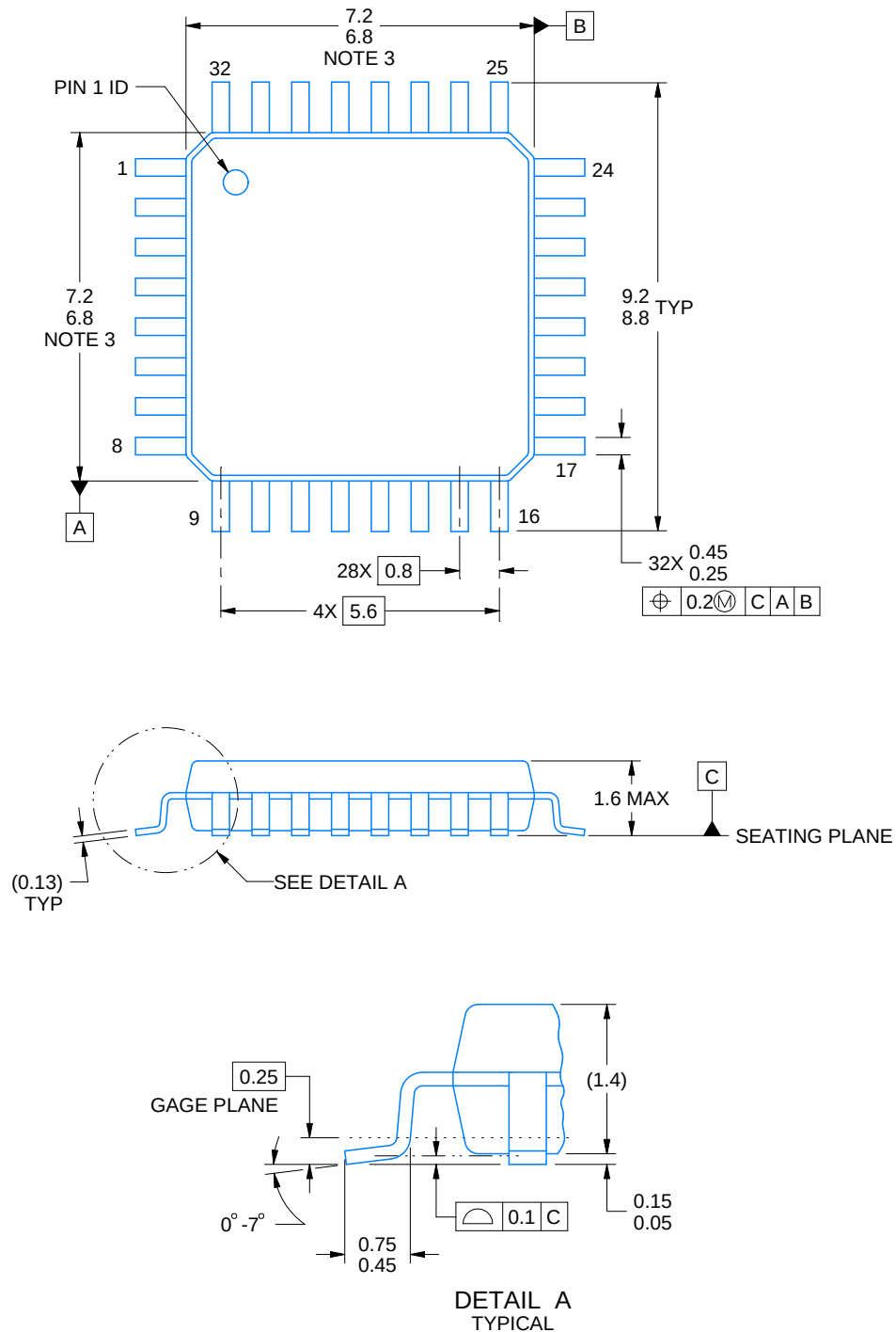
VF0032A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



4219769/A 04/2019

NOTES:

PowerPAD is a trademark of Texas Instruments.

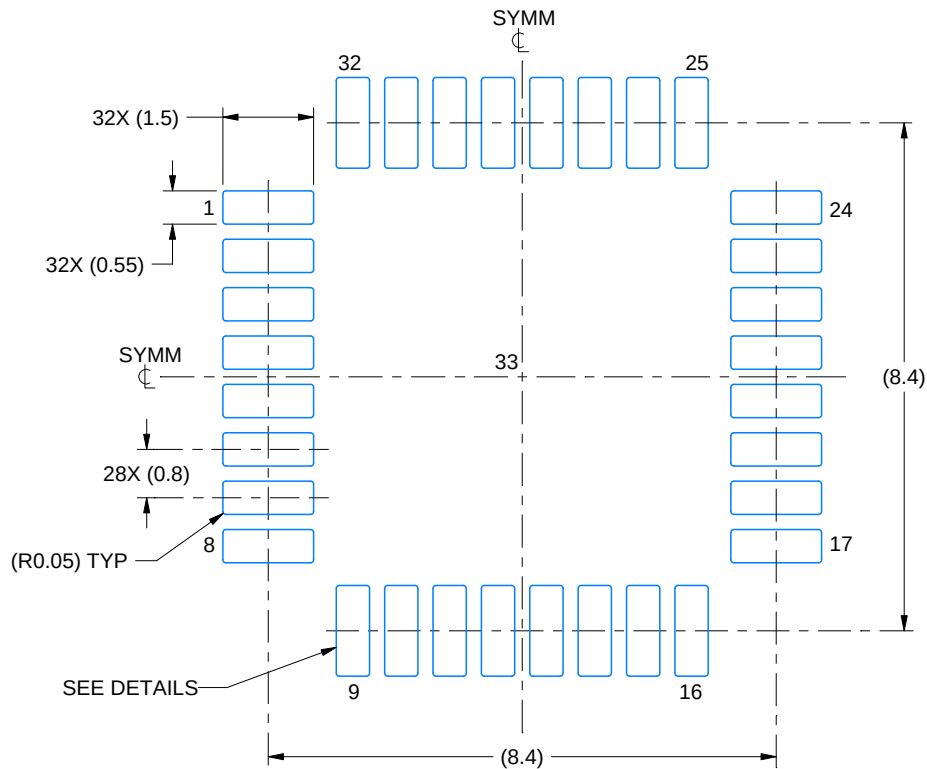
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

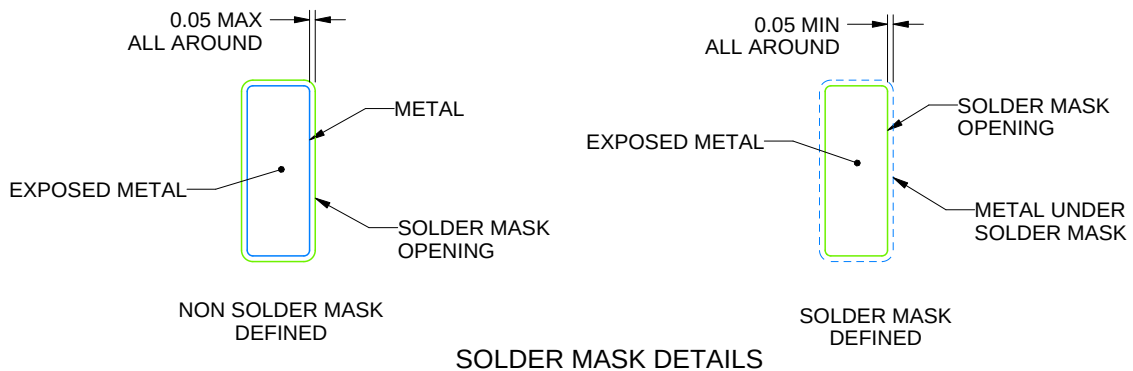
VF0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



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NOTES: (continued)

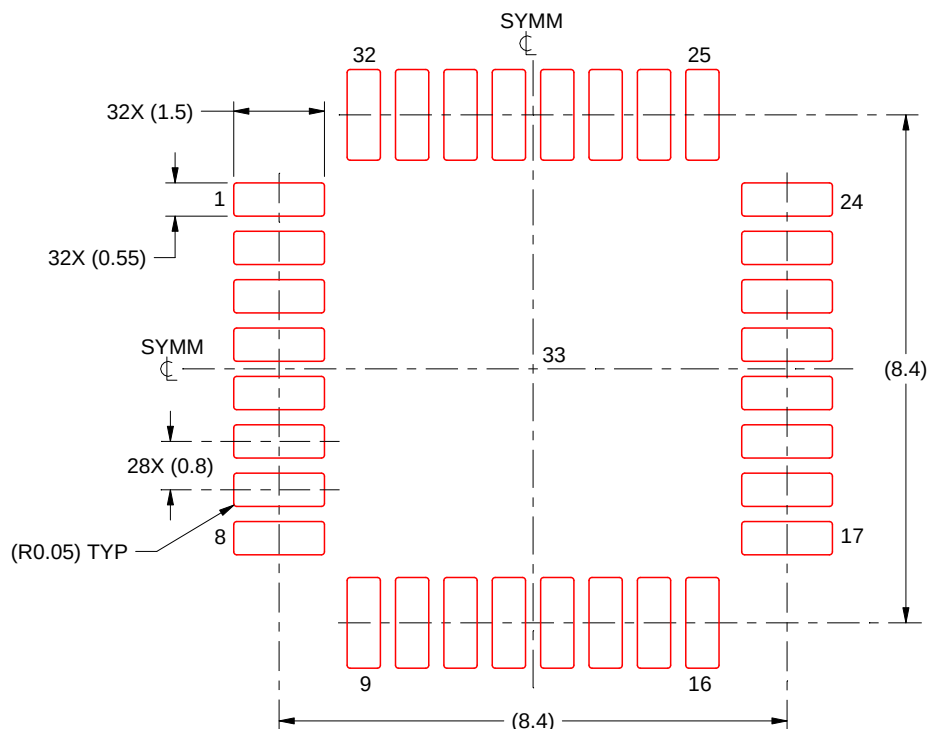
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

VF0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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