User's Guide

SLUUC12–February 2019

BQ25887 QFN boost-mode battery charger with cell balancing evaluation module

This user's guide provides detailed testing instructions for the BQ25887 evaluation module (EVM). Also included are descriptions of the necessary equipment, equipment setup, procedures, the printed-circuit board layouts, schematics, and the bill of materials (BOM).

Throughout this user's guide, the abbreviations *EVM*, BQ25887EVM, *BMS016*, and the term *evaluation module* are synonymous with the BQ25887 QFN evaluation module, unless otherwise noted.

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1 Introduction

As industry improvements continue to make portable electronics more powerful, their power requirements increase. Using two series Li-Ion polymer cells is one way to achieve this power increase. Charging these 8.4-V battery packs from a legacy 5-V USB port requires a boost charger. The BQ25887 is a highly-integrated 2-A boosting, 1.5-MHz switch-mode battery charge management device for a 2s Li-Ion and Li-polymer battery. BQ25887 integrates cell balancing solution which is essential in applications with two series connected individual discrete battery cells.

1.1 EVM Features

The BQ25887 QFN evaluation module (EVM) is a complete charger module for evaluating the I^2C-controlled, 2s battery NVDC charger in the QFN package. Key features of this EVM include:

- Easily evaluate the high-efficiency 2-A, 1.5-MHz integrated field-effect-transistor (FET), switch-mode boost charger in the QFN package
- Use of an onboard USB input adapter for connecting to a USB source and either using the PSEL pin header to set the default input current limit
- Use the EV2400 interface to program parameters for charge operation as well as monitor voltages and current with an integrated analog-to-digital converter (ADC)
- Cell balancing feature with resistor programmable current setting
- Onboard test points, sense resistors, and jumpers facilitate measurement of high-efficiency- and high-accuracy voltage and current regulation

See the device data sheet (Table 1) for detailed features and operation of the integrated circuit (IC).

Table 1. Device Data Sheets

Device	Data Sheet	EVM Label	Variant
BQ25887	SLUSDE7	BQ25887EVM-001	001

This EVM does **not** include the EV2400 interface board. To evaluate the EVM, order an EV2400 interface board separately.

1.2 I/O Descriptions

Table 2 lists the jumper connections available on this EVM.

Table 2. EVM Connections

Jack	Description
J1(2)–VBUS	Connection for positive terminal of charger power source
J1(1)–GND	Connection for negative terminal (ground terminal) of charger power source
J3(1)–PMID	PMID pin connection
J3(2)–GND	Ground
J4(1)–BAT+	Connection for battery pack positive node to BAT pin
J4(2)-TOP-/BOT+	Connection for the mid connection point of the top and bottom cell (BQ25887only. Do not use for BQ25883 or BQ25886)
J5(1)–GND	Connection to battery pack negative node = EVM ground
J5(2)–TS	Connection for the NTC thermistor
J6	I^2C 4-pin connector for EV2400
J7	Input mini-USB port

lists the EVM jumper connections.

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Table 3. EVM Jumper Connections and Shunt Installation

Jack	Description	BQ25887 Setting
JP1	STAT, $\overline{PG}$, $\overline{CE}$, $\overline{INT}$, SDA, and SCL pins 3.3-V LDO pullup source of either SYS (pin 1 to 2) or BAT (pin 2 to 3)	Shunt pins 2 and 3
JP2	ILIM pin connection to resistor to GND	Installed
JP3	DNI	NA
JP4	Connects PSEL to either REGN (pins 2 to 3) or GND (pins 1 to 2) for setting default input current limit to 500 mA or 3 A, respectively, at start-up; may be clamped lower due to resistor on ILIM pin	Shunt pins 2 and 3
JP5	TS resistor divider pullup source (REGN) connection	Installed
JP6	DNI	NA
JP7	Connects an onboard 10 kΩ from TS pin to GND	Installed
JP8	DNI	NA
JP9	Connects CD to GND	NA
JP10	Pulls up STAT through diode and resistor to pullup source	Installed
JP11	Pulls up $\overline{PG}$ through diode and resistor to pullup source	Shunt pins 2 and 3
JP12	Pull up SDA through 10-kΩ resistor; optional if I2C line has internal pullup.	Shunt pins 2 and 1
JP13	Pull up SCL through 10-kΩ resistor; optional if I2C line has internal pullup.	Installed
JP14	Pull up $\overline{INT}$ through 10-kΩ resistor	Installed
JP15	Pull up CD through 10-kΩ resistor	Open

Table 4 lists the recommended operating conditions for this EVM.

Table 4. Recommended Operating Conditions

Symbol	Description	MIN	TYP	MAX	Unit
Supply voltage, V_{VBUS}	Input voltage from AC adapter	3.9	5	6.5	V
Cell voltage, V_{CELL} in charge mode	voltage applied at BAT to TOP-/BOT+ terminal and TOP-/BOT+ to PGND terminal	0 or floating	4.2	4.6	V
I_{BAT}	Fast charging current	0	—	2.2	A
	Discharging current through internal MOSFET	6	—	—	A
Supply current, I_{IN}	Maximum input current from AC adapter input	0	—	3.3	A

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2 Test Summary

2.1 Equipment

This section includes a list of supplies required to perform tests on this EVM.

1. *Power supply (PS#1)* : The power supply must be capable of supplying up to 6.5 V at 3.3 A. While this part can handle larger voltage and current, it is not necessary for this procedure.
2. *Battery simulator (BS#1, BS#2)* : Four-quadrant supply set to constant voltage ≤ 9.2 V
   Example: Kepco Bipolar Power Supply: BOP 20–5M, DC 0 to ±20 V, 0 to ±5 A (or higher) and Keithley 2420 Sourcemeter
3. *Load #1:* Electronic or resistive load capable of sinking up to 3 A at 9.2 V
4. *Meters:* Six Fluke 75 multimeters (equivalent or better)
   - Alternatively; four equivalent voltage meters and two equivalent current meters. The current meters must be capable of measuring greater than 3 A of current. A current meter in series with the battery or battery simulator must have auto-ranging disabled and should only be used for DC measurements (no start-up, transients, and so forth).
5. *Computer:* A computer with at least one USB port and a USB cable
6. *PC communication interface:*EV2400 USB-based PC interface board
7. *Software:* Download bqStudio from Texas Instruments
   Double click the *Battery management studio* installation file and then follow the installation steps. The software supports Microsoft® Windows® 7 and Windows 10 operating systems.

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2.2 Charge Mode

2.2.1 Charge Mode Test Setup

Use the following list to set up the equipment for charge mode operation:

1. Figure 2 shows the test setup for BQ25887 when in charge (boosting) mode including jumper settings per Table 2. Ensure that the power supply and battery simulator are turned off before connecting to the EVM.

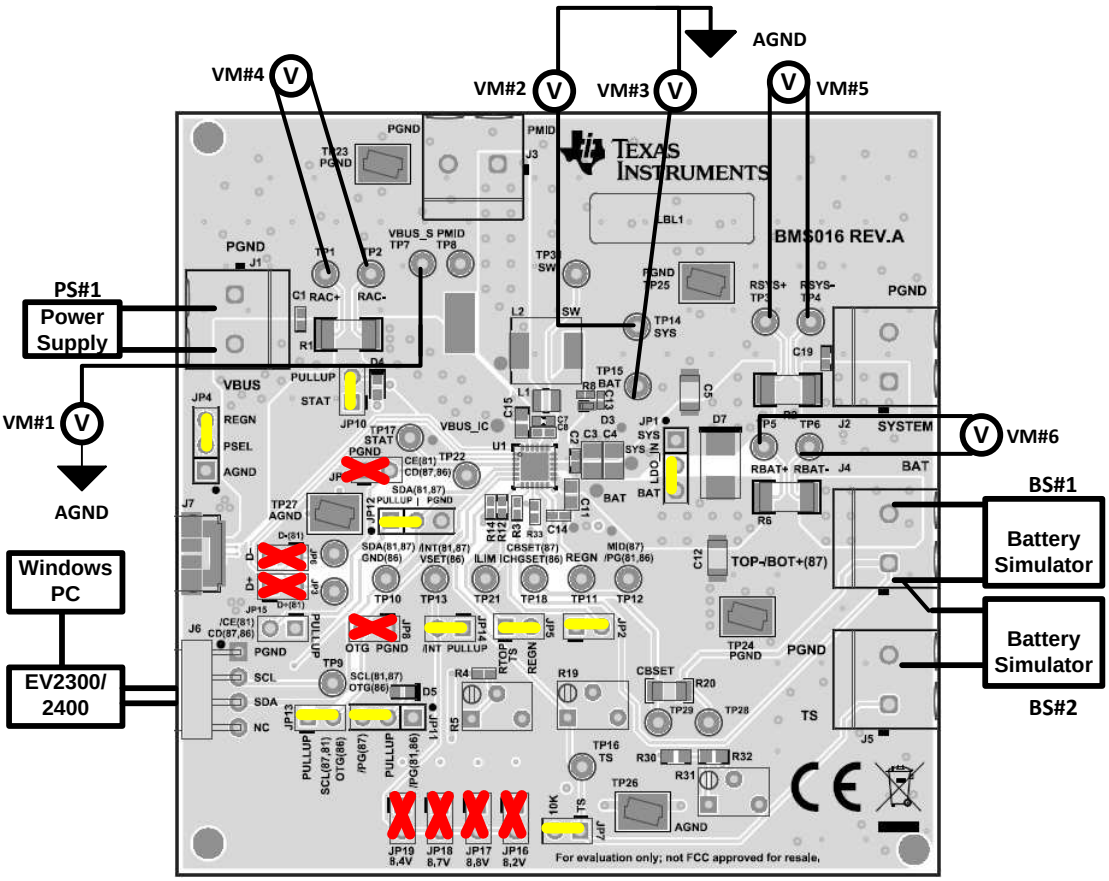


Figure 1. BQ25887 Charge Mode Test Setup

2. Voltmeters 1 through 3 (VM1, VM2, and VM3) connect to Kelvin test points for measuring VBUS, SYS, and BAT as close to the IC pins as possible. Voltmeters 4 through 6 measure the voltage across 0.01 Ω, which gives the current.
3. Before attaching to the EVM, set battery simulator 1 (BS#1) and battery simulator 2 (BS#2) no higher than 3.8V and at a 2.5-A current limit and set power supply 1 (PS#1) for 5.5 V and a 3.5-A current limit.
4. Turn off BS#1, BS#2 and PS#1 then attach BS#1 to the J4 (BAT, TOP-/BOT+) terminal and BS#2 to TOP-/BOT+ (J4) and PGND (J5) terminal of the EVM and attach PS#1 to J1 (VBUS, GND) of the EVM.
5. With the EV2400 connected to the PC and the EVM, launch *Battery Management Studio* (bqStudio). Select *Charger* and the BQ25881 or BQ25887 evaluation software.

2.2.2 Charge Mode I2C Register Setup

2.2.2.1 BQ25887EVM

1. Turn on BS#1 and BS#2 and set for 3.8 V on each of the BS.

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2. In the EVM software, specify the “I2C Address” as *D4 (6A)*.
3. Click the *Read* button.
4. In the EVM GUI software *Field View*, ensure that the following I^2C registers have the following settings:
   - Chose “Disabled” in the drop-down box for the *Watchdog Timer*
   - *Input Voltage Limit*= "4.4V" (default)
   - *Input Current Limit*= "3.3A"
   - *Charge Voltage Limit*= "4.20V" (default)
   - *Fast Charge Current Limit*= "1.00A"
   - *Pre-charge Current Limit* to "0.15A" (default)
   - Deselect *Enable Charge* to disable charge
   - Deselect *Enable ILIM pin* to disable the ILIM pin
   - Deselect *Enable HiZ*, if selected
5. Click *Read Register* to confirm that register changes were made

2.2.3 Charge Mode Test Procedure

Use the following steps for charge mode verification and testing:

1. Turn on PS#1 and click the *Read Register* button twice.
   - *Observe* → everything "Normal" at the *Fault* box
   - *Observe* → D4 (STAT) is off because charge is disabled.
   - *Observe* → D5 ($\overline{PG}$) is on indicating power is good.
   - *Measure on VM2* → V(TP14 (SYS), TP26 (AGND)) = 6.4 V ±50 mV
2. On BQ25887EVMBQ25883EVM, use the GUI to select *Enable Charge* to start charging at 1.0 A. To correct for cable resistance, adjust PS#1 until VM1 [TP7 (VBUS_S), TP26 (AGND)] measures 5.5 V ±50 mV and adjust BS1 until VM3 [TP15 (BAT), TP12 (MID)] measures 3.8 V ± 50 mV, and BS2 until VM4 [TP12 (MID), TP26 (AGND)] measures 3.8 V ± 50 mV.
   - *Measure on VM6* → V(TP5 (RBAT+), TP6 (RBAT-)) = 10 mV ±0.7 mV which corresponds to ICHG = 1.0 A ±5% through a 0.010-Ω ±1% resistor. Voltage of 0.1 mV is added to account for DMM accuracy.
   - *Measure on VM4* → V(TP1 (RAC+), TP2 (RAC-)) = 14.8 mV ±0.7 mV which corresponds to IVBUS = 1.48 A ±5% (accounting for efficiency variation across ICs and inductors) through a 0.010-Ω ±1% resistor. Voltage of 0.1 mV is added to account for DMM accuracy.
3. Adjust BS1 until VM3 [TP15 (BAT), TP12 (MID)] measures 3.9 V ± 50 mV:
   - *Measure on VM6* → V(TP5 (RBAT+), TP6 (RBAT-)) = 7.5 mV ±0.7 mV which corresponds to ICHG = 0.75 A ±5% through a 0.010-Ω ±1% resistor. Voltage of 0.1 mV is added to account for DMM accuracy.
   - Move VM5 to TP29, TP28. *Measure on VM5* → V(TP29 (CBSET), TP28 (MID)) = 3.15V ± 7 mV which corresponds to ICHG = 0.242 A ±5% through a 13-Ω ±5% resistor. Voltage of 0.1 mV is added to account for DMM accuracy.
4. Optionally, in the GUI, select *Enable ILIM pin*. Adjust the RLIM potentiometer (R5) until:
   - *Measure on VM4* → V(TP1 (RAC+), TP2 (RAC-)) = 10 mV ±0.7 mV which corresponds to IVBUS = 1.0 A ±5% through a 0.010-Ω ±1% resistor. Voltage of 0.1 mV is added to account for DMM accuracy.
   - *Obverse in bqStudio after Read Register* → IINDPM Status: In IINDPM
5. Turn off and disconnect PS#1, BS#1, BS#2 Load#1, and voltmeters.

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2.2.4 Charge Mode Evaluation Results

Figure 2 shows the *Charge Mode Startup* graph.

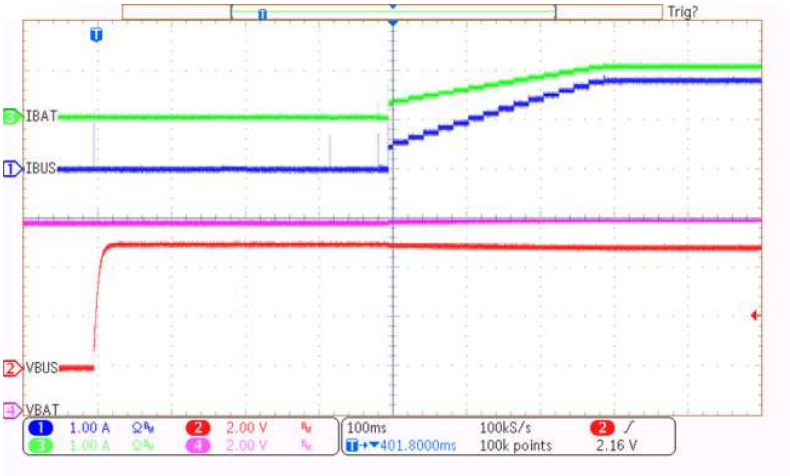


Figure 2. Charge Mode Startup

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2.3 Helpful Tips

The following list provides a few helpful tips:

- The leads and cables to the various power supplies, batteries, and loads have resistance. The current meters also have series resistance. The charger dynamically reduces charge current depending on the voltage sensed at its VBUS pin (using the VINDPM feature), BAT pin (as part of normal termination), and TS pin (through its battery temperature monitoring feature through the battery thermistor). Therefore, the designer must use voltmeters to measure the voltage as close to the IC pins (TP7, TP15, and TP16) as possible instead of relying on the digital readouts of the power supply.
- When using a source meter that can source and sink current as the battery simulator, TI highly recommends adding two large capacitors (1000uF or greater) at BAT, TOP-/BOT+, and GND connectors to prevent oscillations at the BAT pin, which are due to mismatched impedances of the charger output and source meter input within their respective regulation loop bandwidths. Configuring the source meter for four-wire sensing eliminates the requirement for a separate voltmeter to measure the voltage at the BAT pin. When using four-wire sensing, always ensure that the sensing leads are connected to prevent accidental overvoltage by the power supply.
- For precise measurements of efficiency and charge current or battery regulation (or both) near termination, a current meter in series with the battery or battery simulator must not be set to auto-range and may require removal, entirely. This EVM offers an alternate method for measuring currents by measuring the voltage across a 1%, thermally-capable (for example, 0.010 Ω in a 1210 or larger footprint) resistor in series between the power sources and power pins.

3 PCB Layout Guidelines

Minimize the switching node rise and fall times for minimum switching loss. Proper layout of the components that minimize the high-frequency current path loop is important to prevent electrical and magnetic field radiation and high-frequency resonant problems. To ensure proper layout, follow the priority list for this printed-circuit board (PCB) in the order presented:

1. Place the output capacitor as close as possible to the SYS or SNS pin and GND pin connections and use the shortest copper trace connection or GND plane.
2. Put the input capacitors near to the VBUS and PMID pins. Tie ground connections to the IC ground with a short copper trace connection or GND plane.
3. Place the inductor input terminal as close to the SW pin as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using the power pad as the single ground connection point or use a 0-Ω resistor to tie analog ground to power ground.
5. Use a single ground connection to tie the charger power ground to the charger analog ground just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place decoupling capacitors next to the IC pins and make the trace connection as short as possible.
7. One critical note regarding the layout is that the exposed power pad on the backside of the IC package must be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC connecting to the ground plane on the other layers.
8. The via size and number must be sufficient for a given current path.

See the EVM design for the recommended component placement with trace and via locations..

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4 Board Layout, Schematic, and Bill of Materials

4.1 Board Layout

Figure 3 through Figure 6 show the PCB board layouts.

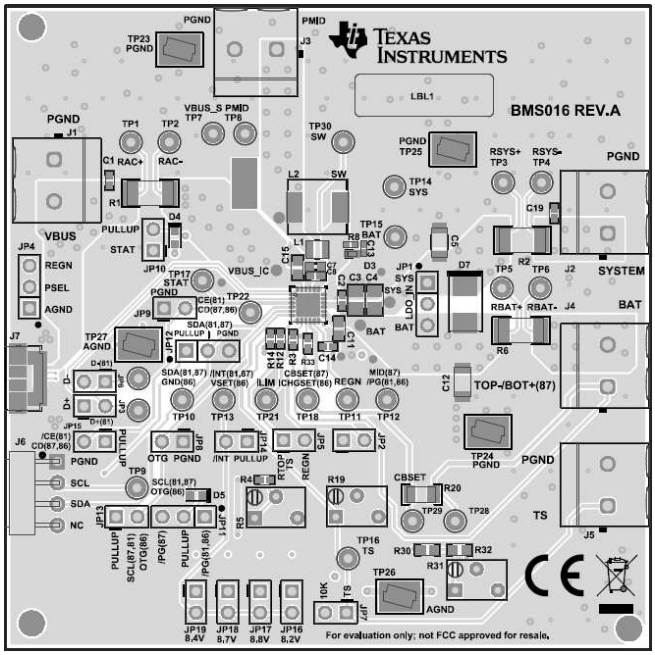


Figure 3. BQ2588xEVM Top Overlay

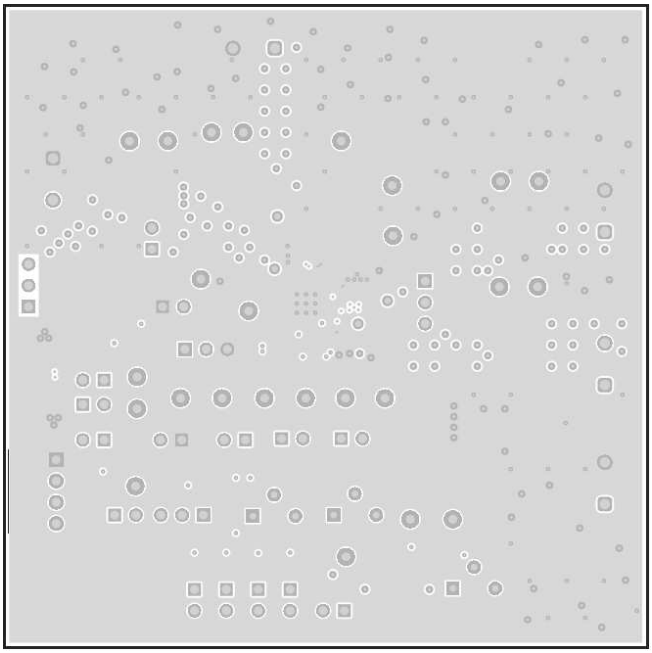


Figure 4. BQ2588xEVM Layer 2

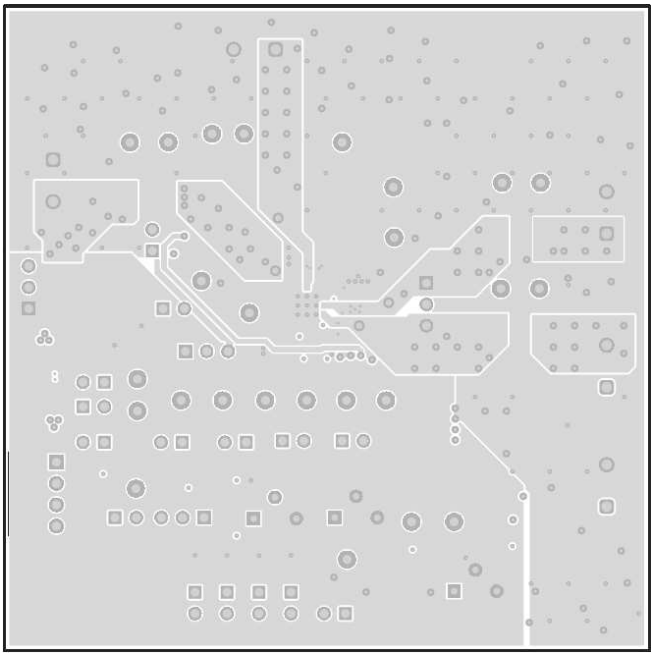


Figure 5. BQ2588xEVM Layer 3

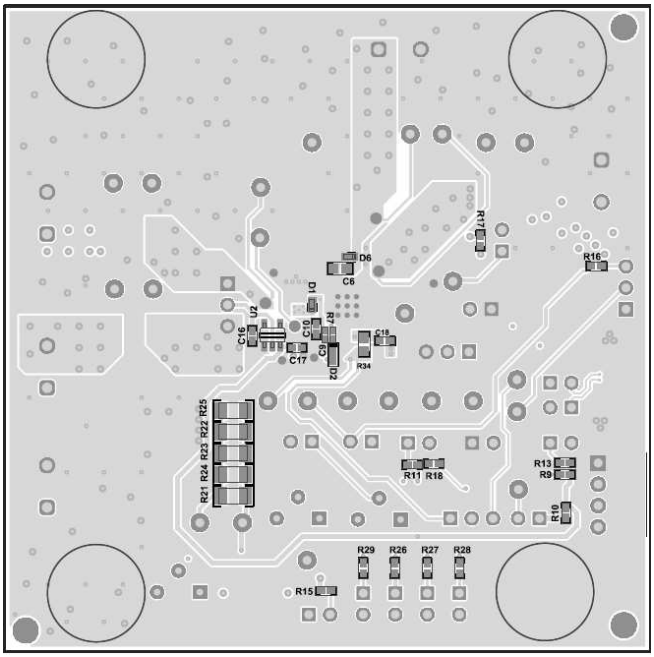


Figure 6. BQ2588xEVM Bottom Overlay

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4.2 Schematic

Figure 7 shows the schematic for the BQ2588x QFN EVM.

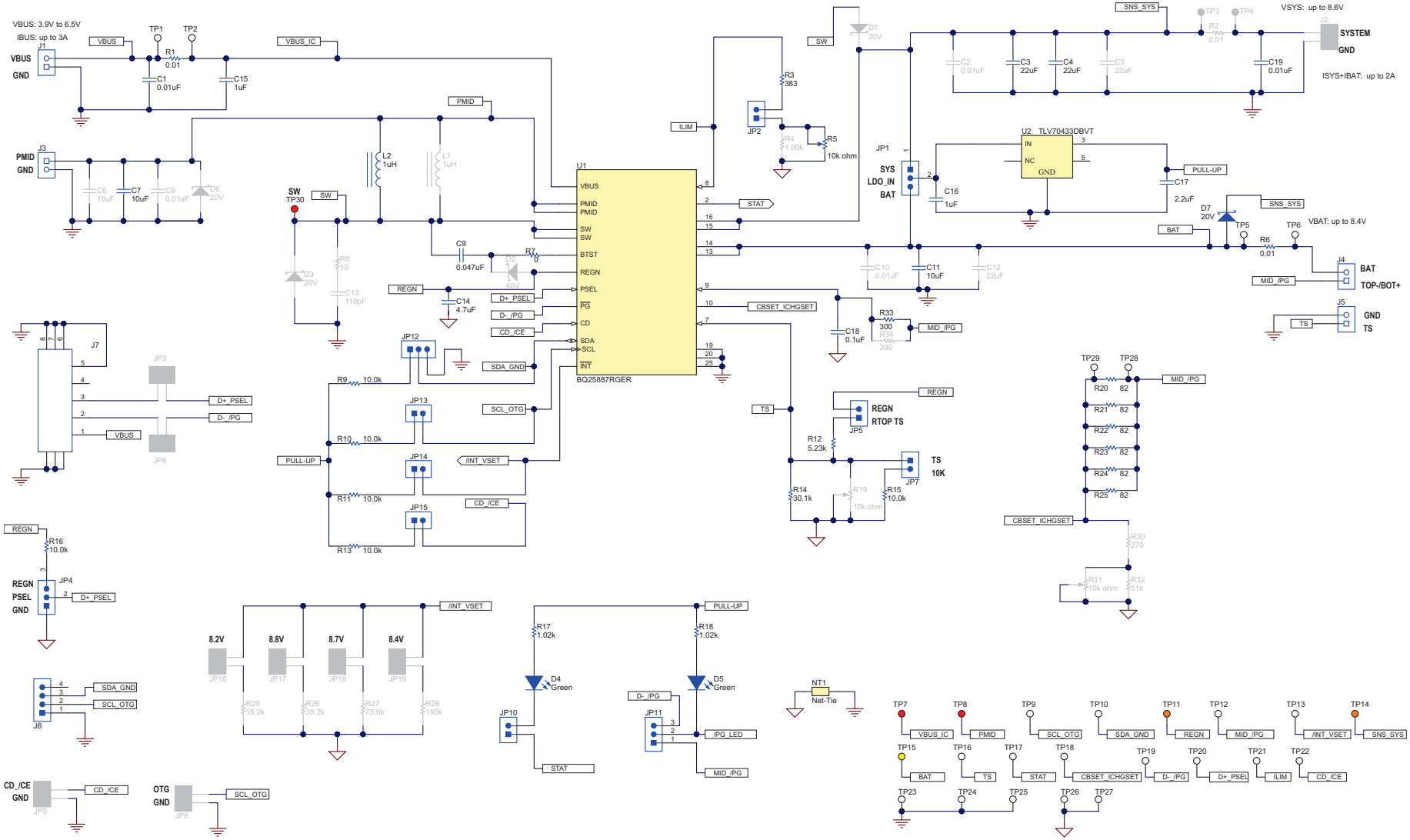


Figure 7. BQ25887EVM Schematic

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4.3 Bill of Materials

Table 5 lists the BQ25887EVM BOM.

Table 5. BQ25887EVM(1)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
!PCB	1		Printed Circuit Board		BMS016	Any	-	-
C1	1	0.01uF	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	0402	GCM155R71E103KA37D	MuRata		
C3, C4	2	22uF	CAP, CERM, 22 uF, 25 V, +/- 20%, X5R, 0805	0805	GRM21BR61E226ME44L	MuRata		
C7, C11	2	10uF	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603	0603	GRM188R61E106MA73D	MuRata		
C9	1	0.047uF	CAP, CERM, 0.047 uF, 25 V, +/- 10%, X7R, 0402	0402	GRM155R71E473KA88D	MuRata		
C14	1	4.7uF	CAP, CERM, 4.7 uF, 10 V, +/- 20%, X5R, 0402	0402	GRM155R61A475MEAAD	MuRata		
C15	1	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X5R, 0603	0603	C1608X5R1E105K080AC	TDK		
C16	1	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X5R, 0402	0402	EMK105BJ105KVHF	Taiyo Yuden		
C17	1	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 20%, X5R, 0402	0402	GRM155R61A225ME95	MuRata		
C18	1	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402	GCM155R71C104KA55D	MuRata		
C19	1	0.01uF	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	0402	GRM155R71E103KA01D	MuRata		
D4, D5	2	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On		

(1) Unless otherwise noted in the Alternate PartNumber and/or Alternate Manufacturer columns, all parts may be substituted with equivalents

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Table 5. BQ25887EVM[(1)] (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
D7	1	20V	Diode, Schottky, 20 V, 3 A, SMB	SMB	B320B-13-F	Diodes Inc.		
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
J1, J3, J4, J5	4		Terminal Block, 5mm, 2x1, R/A, TH	Terminal Block, 5mm, 2x1, R/A, TH	1792863	Phoenix Contact		
J6	1		Header (friction lock), 100mil, 4x1, R/A, TH	4x1 R/A Header	22-05-3041	Molex		
J7	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT	7.5x2.45x5mm	473460001	Molex		
JP1, JP4, JP11, JP12	4		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions		
JP2, JP5, JP7, JP10, JP13, JP14, JP15	7		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions		
L2	1	1uH	Inductor, Shielded Drum Core, Powdered Iron, 1 uH, 11 A, 0.009 ohm, SMD	IHLP-2525CZ	IHLP2525CZER1R0M01	Vishay-Dale		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		
R1, R6	2	0.01	RES, 0.01, 1%, 1 W, 2010	2010	WSL2010R0100FEA18	Vishay-Dale		
R3	1	383	RES, 383, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402383RFKED	Vishay-Dale		
R5	1	10k ohm	Trimmer, 10k ohm, 0.25W, TH	4.5x8x6.7mm	3266W-1-103LF	Bourns		
R7	1	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		
R9, R10, R11, R13, R15, R16	6	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	CRCW040210K0FKED	Vishay-Dale		
R12	1	5.23k	RES, 5.23 k, 1%, 0.063 W, 0402	0402	CRCW04025K23FKED	Vishay-Dale		

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Table 5. BQ25887EVM[(1)] (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R14	1	30.1k	RES, 30.1 k, 1%, 0.063 W, 0402	0402	CRCW040230K1FKED	Vishay-Dale		
R17, R18	2	1.02k	RES, 1.02 k, 1%, 0.063 W, 0402	0402	CRCW04021K02FKED	Vishay-Dale		
R20, R21, R22, R23, R24, R25	6	82	RES, 82, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW120682R0JNEA	Vishay-Dale		
R33	1	300	RES, 300, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402300RJNED	Vishay-Dale		
SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5, SH-JP6, SH-JP7, SH-JP8, SH-JP9, SH-JP10, SH-JP11, SH-JP12, SH-JP13, SH-JP14, SH-JP15, SH-JP16	16	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP5, TP6, TP9, TP10, TP12, TP13, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP28, TP29	17		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone		
TP7, TP8, TP30	3		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone		
TP11, TP14	2		Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone		
TP15	1		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone		
TP23, TP24, TP25, TP26, TP27	5		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U1	1		2-Cell, 2-A Boost-Mode Battery Chargers for USB Input, RGE0024H (VQFN-24)	RGE0024H	BQ25887RGER	Texas Instruments	BQ25887RGET	Texas Instruments

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Table 5. BQ25887EVM[(1)] (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
U2	1		Single Output LDO, 150 mA, Fixed 3.3 V Output, 2.5 to 24 V Input, with Ultra-Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS and no Sb/Br)	DBV0005A	TLV70433DBVT	Texas Instruments		
C2, C8, C10	0	0.01uF	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	0402	GRM155R71E103KA01D	MuRata		
C5	0	22uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X5R, 1206	1206	GRM31CR61E226KE15L	MuRata		
C6	0	10uF	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603	0603	GRM188R61E106MA73D	MuRata		
C12	0	22uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X5R, AEC-Q200 Grade 3, 1206	1206	GRT31CR61E226KE01L	MuRata		
C13	0	110pF	CAP, CERM, 110 pF, 25 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1E111JA01D	MuRata		
D1, D3, D6	0	20V	Diode, Schottky, 20 V, 1 A, 152AD	152AD	NSR10F20NXT5G	ON Semiconductor		
D2	0	40V	Diode, Schottky, 40 V, 0.38 A, SOD-523	SOD-523	ZLLS350TA	Diodes Inc.		
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J2	0		Terminal Block, 5mm, 2x1, R/A, TH	Terminal Block, 5mm, 2x1, R/A, TH	1792863	Phoenix Contact		
JP3, JP6, JP8, JP9, JP16, JP17, JP18, JP19	0		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions		
L1	0	1uH	Inductor, Shielded, Metal Composite, 1 uH, 3.3 A, 0.04 ohm, SMD	2.5x1.2x2mm	DFE252012F-1R0M=P2	MuRata Toko		

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Table 5. BQ25887EVM[(1)] (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R2	0	0.01	RES, 0.01, 1%, 1 W, 2010	2010	WSL2010R0100FEA18	Vishay-Dale		
R4	0	1.00k	RES, 1.00 k, 1%, 0.063 W, 0402	0402	CRCW04021K00FKED	Vishay-Dale		
R8	0	10	RES, 10, 5%, 0.063 W, 0402	0402	CRCW040210R0JNED	Vishay-Dale		
R19, R31	0	10k ohm	Trimmer, 10k ohm, 0.25W, TH	4.5x8x6.7mm	3266W-1-103LF	Bourns		
R26	0	39.2k	RES, 39.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040239K2FKED	Vishay-Dale		
R27	0	75.0k	RES, 75.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040275K0FKED	Vishay-Dale		
R28	0	150k	RES, 150 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF1503X	Panasonic		
R29	0	18.0k	RES, 18.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040218K0FKED	Vishay-Dale		
R30	0	270	RES, 270, 5%, 0.1 W, 0603	0603	CRCW0603270RJNEA	Vishay-Dale		
R32	0	51k	RES, 51 k, 5%, 0.1 W, 0603	0603	CRCW060351K0JNEA	Vishay-Dale		
R34	0	300	RES, 300, 1%, 0.1 W, 0603	0603	RC0603FR-07300RL	Yageo America		
TP3, TP4	0		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone		

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WARNING

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User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

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4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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