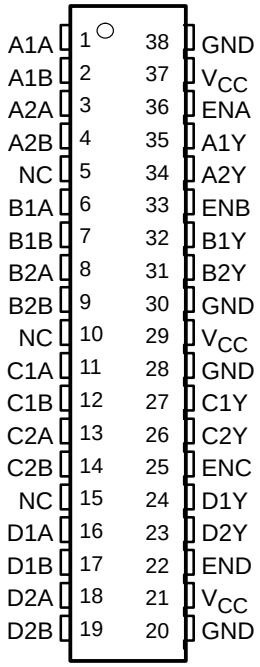
- **Eight Line Receivers Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard**
- **Integrated 110-Ω Line Termination Resistors on LVDT Products**
- **Designed for Signaling Rates† Up To 630 Mbps**
- **SN65 Version's Bus-Terminal ESD Exceeds 15 kV**
- **Operates From a Single 3.3-V Supply**
- **Propagation Delay Time of 2.6 ns (Typ)**
- **Output Skew 100 ps (Typ)**
  **Part-To-Part Skew Is Less Than 1 ns**
- **LVTTL Levels Are 5-V Tolerant**
- **Open-Circuit Fail Safe**
- **Flow-Through Pin Out**
- **Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch**

**NOT RECOMMENDED FOR NEW DESIGNS**
**For Replacement Use 'LVDx388A**

**'LVDS388, 'LVDT388**
**DBT PACKAGE**
**(TOP VIEW)**

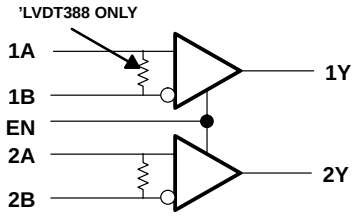



## description

The 'LVDS388 and 'LVDT388 (*T* designates integrated termination) are eight differential line receivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3-V supply rail. Any of the eight differential receivers will provide a valid logical output state with a ±100-mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes. Additionally, the high-speed switching of LVDS signals always require the use of a line impedance matching resistor at the receiving end of the cable or transmission media. The LVDT product eliminates this external resistor by integrating it with the receiver.

## logic diagram (positive logic)

**'LVDx388**




**(1/4 of 'LVDx388 shown)**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## description (continued)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with its companion, 8-channel driver, the SN65LVDS389 over 150 million data transfers per second in single-edge clocked systems are possible with very little power. Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

The SN65LVDS388 and SN65LVDT388 is characterized for operation from –40°C to 85°C. The SN75LVDS388 and SN75LVDT388 is characterized for operation from 0°C to 70°C.

**AVAILABLE OPTIONS**

| PART NUMBER | TEMPERATURE RANGE | NUMBER OF RECEIVERS | BUS-PIN ESD |
|---|---|---|---|
| SN65LVDS388DBT | –40°C to 85°C | 8 | 15 kV |
| SN65LVDT388DBT | –40°C to 85°C | 8 | 15 kV |
| SN75LVDS388DBT | 0°C to 70°C | 8 | 4 kV |
| SN75LVDT388DBT | 0°C to 70°C | 8 | 4 kV |

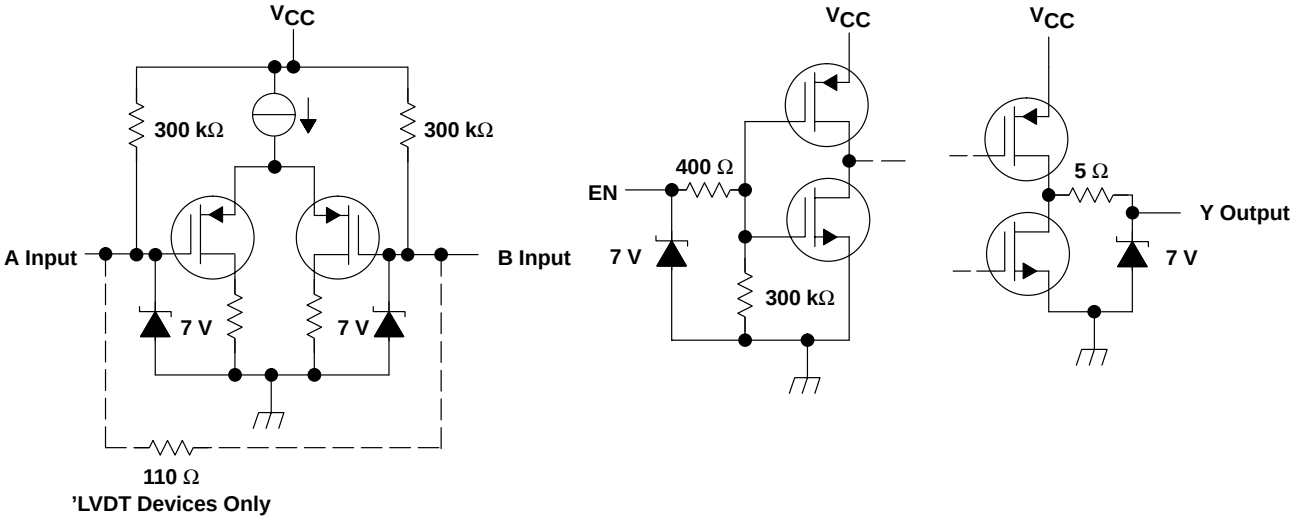
### Function Table

**SNx5LVD388 and SNx5LVDT388**

| DIFFERENTIAL INPUT | ENABLES | OUTPUT |
|---|---|---|
| A-B | EN | Y |
| $V_{ID} \geq 100$ mV | H | H |
| -100 mV < $V_{ID} \leq 100$ mV | H | ? |
| $V_{ID} \leq$ -100 mV | H | L |
| X | L | Z |
| Open | H | H |

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

## equivalent input and output schematic diagrams



### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . –0.5 V to 4 V
Voltage range: Enables or Y . . . . . –0.5 V to 6 V
A or B . . . . . –0.5 V to 4 V
Electrostatic discharge: (see Note 2)
SN65' (A, B, and GND) . . . . . Class 3, A:15 kV, B: 700 V
SN75' (A, B, and GND) . . . . . Class 2, A:4 kV, B: 400 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ | DERATING FACTOR‡ ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| DBT | 1071 mW | 8.5 mW/°C | 688 mW | 556 mW |

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 3 | 3.3 | 3.6 | V |
| High-level input voltage, $V_{IH}$ | Enables | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | Enables | | | 0.8 | V |
| Magnitude of differential input voltage, $\lvert V_{ID} \rvert$ | | 0.1 | | 0.6 | V |
| Common-mode input voltage, $V_{IC}$ (see Figure 4) | | $\frac{\lvert V_{ID} \rvert}{2}$ | | $2.4 - \frac{\lvert V_{ID} \rvert}{2}$ | V |
| | | | | $V_{CC} - 0.8$ | |
| Operating free-air temperature, $T_A$ | SN75' | 0 | | 70 | °C |
| | SN65' | –40 | | 85 | °C |

## electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going differential input voltage threshold | | See Figure 1 and Table 1 | | | 100 | mV |
| $V_{IT-}$ | Negative-going differential input voltage threshold | | See Figure 1 and Table 1 | –100 | | | mV |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –8 mA | 2.4 | 3 | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 8 mA | | 0.2 | 0.4 | V |
| $I_{CC}$ | Supply current | | Enabled, No load | | 50 | 70 | mA |
| | | | Disabled | | | 3 | mA |
| $I_I$ | Input current (A or B inputs) | 'LVDS | $V_I$ = 0 V | | –13 | –20 | µA |
| | | | $V_I$ = 2.4 V | –1.2 | –3 | | |
| | | 'LVDT | $V_I$ = 0 V, other input open | | | –40 | |
| | | | $V_I$ = 2.4 V, other input open | –2.4 | | | |
| $I_{ID}$ | Differential input current $\lvert I_{IA} - I_{IB} \rvert$ | 'LVDS | $V_{IA}$ = 0 V, $V_{IB}$ = 0.1 V, $V_{IA}$ = 2.4 V, $V_{IB}$ = 2.3 V | | | ±2 | µA |
| $I_{ID}$ | Differential input current ($I_{IA} - I_{IB}$) | 'LVDT | $V_{IA}$ = 0.2 V, $V_{IB}$ = 0 V, $V_{IA}$ = 2.4 V, $V_{IB}$ = 2.2 V | 1.5 | | 2.2 | mA |
| $I_{I(OFF)}$ | Power-off input current (A or B inputs) | 'LVDS | $V_{CC}$ = 0 V, $V_I$ = 2.4 V | | 12 | ±20 | µA |
| $I_{I(OFF)}$ | Power-off input current (A or B inputs) | 'LVDT | $V_{CC}$ = 0 V, $V_I$ = 2.4 V | | | ±40 | µA |
| $I_{IH}$ | High-level input current (enables) | | $V_{IH}$ = 2 V | | | 10 | µA |
| $I_{IL}$ | Low-level input current (enables) | | $V_{IL}$ = 0.8 V | | | 10 | µA |
| $I_{OZ}$ | High-impedance output current | | $V_O$ = 0 V | | | ±1 | µA |
| | | | $V_O$ = 3.6 V | | | 10 | |
| $C_{IN}$ | Input capacitance, A or B input to GND | | $V_{ID}$ = 0.4 sin 2.5E09 t V | | 5 | | pF |
| $Z_{(t)}$ | Termination impedance | | $V_{ID}$ = 0.4 sin 2.5E09 t V | 88 | | 132 | Ω |

† All typical values are at 25°C and with a 3.3-V supply.

## switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 2 | 1 | 2.6 | 4 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 1 | 2.5 | 4 | ns |
| $t_r$ | Output signal rise time | | 500 | 800 | 1200 | ps |
| $t_f$ | Output signal fall time | | 500 | 800 | 1200 | ps |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$) | | | 150 | 600 | ps |
| $t_{sk(o)}$ | Output skew‡ | | | 100 | 400 | ps |
| $t_{sk(pp)}$ | Part-to-part skew§ | | | | 1 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | See Figure 3 | | 7 | 15 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | | | 7 | 15 | ns |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high-impedance output | | | 7 | 15 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high-impedance output | | | 7 | 15 | ns |

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(o)}$ is the magnitude of the time difference between the $t_{PLH}$ or $t_{PHL}$ of all drivers of a single device with all of their inputs connected together.
§ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.

## PARAMETER MEASUREMENT INFORMATION

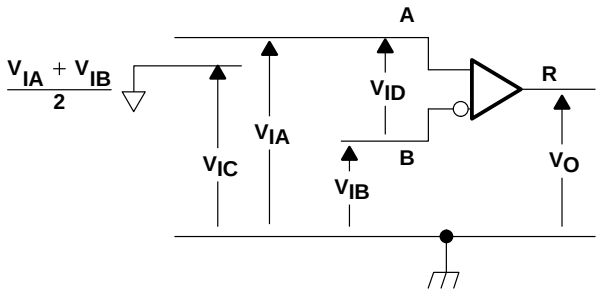
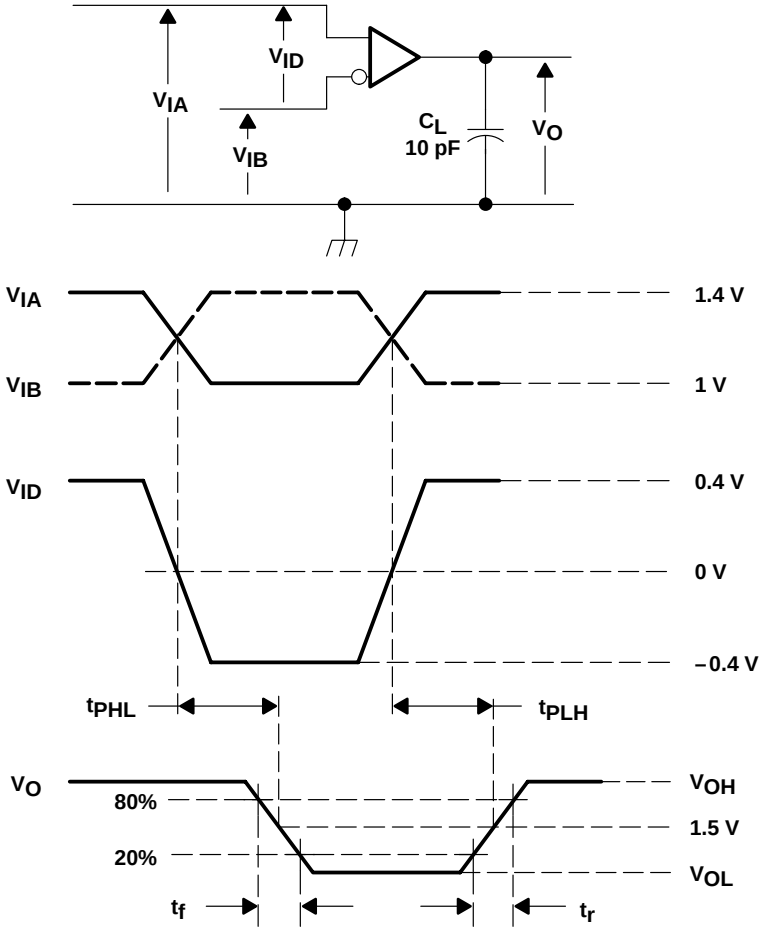



**Figure 1. Voltage Definitions**

**Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages**

| APPLIED VOLTAGES | | RESULTING DIFFERENTIAL INPUT VOLTAGE | RESULTING COMMON-MODE INPUT VOLTAGE |
|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ |
| 1.25 V | 1.15 V | 100 mV | 1.2 V |
| 1.15 V | 1.25 V | –100 mV | 1.2 V |
| 2.4 V | 2.3 V | 100 mV | 2.35 V |
| 2.3 V | 2.4 V | –100 mV | 2.35 V |
| 0.1 V | 0 V | 100 mV | 0.05 V |
| 0 V | 0.1 V | –100 mV | 0.05 V |
| 1.5 V | 0.9 V | 600 mV | 1.2 V |
| 0.9 V | 1.5 V | –600 mV | 1.2 V |
| 2.4 V | 1.8 V | 600 mV | 2.1 V |
| 1.8 V | 2.4 V | –600 mV | 2.1 V |
| 0.6 V | 0 V | 600 mV | 0.3 V |
| 0 V | 0.6 V | –600 mV | 0.3 V |

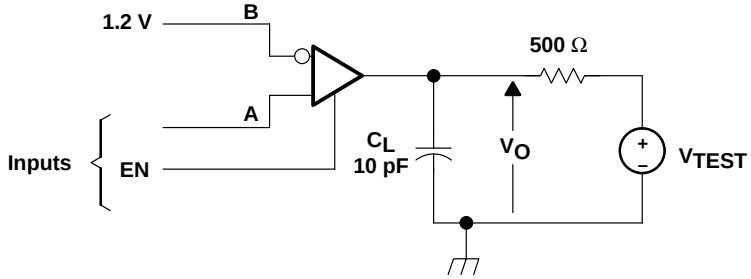
## PARAMETER MEASUREMENT INFORMATION




NOTE: All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. $C_L$ includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

**Figure 2. Timing Test Circuit and Wave Forms**

## PARAMETER MEASUREMENT INFORMATION




NOTE A: All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. $C_L$ includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

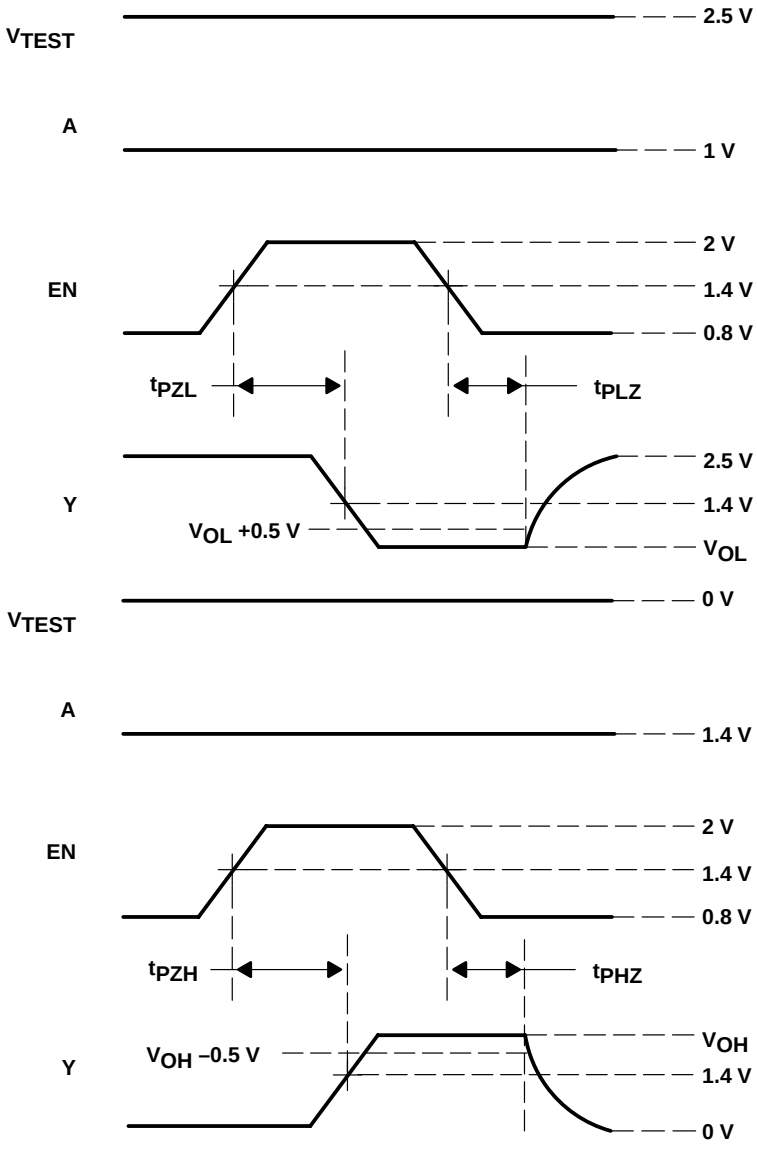



**Figure 3. Enable/Disable Time Test Circuit and Wave Forms**

## TYPICAL CHARACTERISTICS

**COMMON-MODE INPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE**

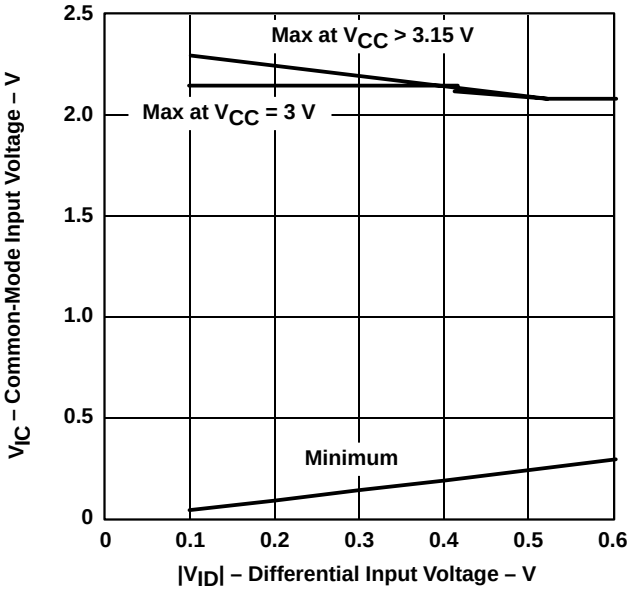



Figure 4

**LVDx388 SUPPLY CURRENT vs SWITCHING FREQUENCY**

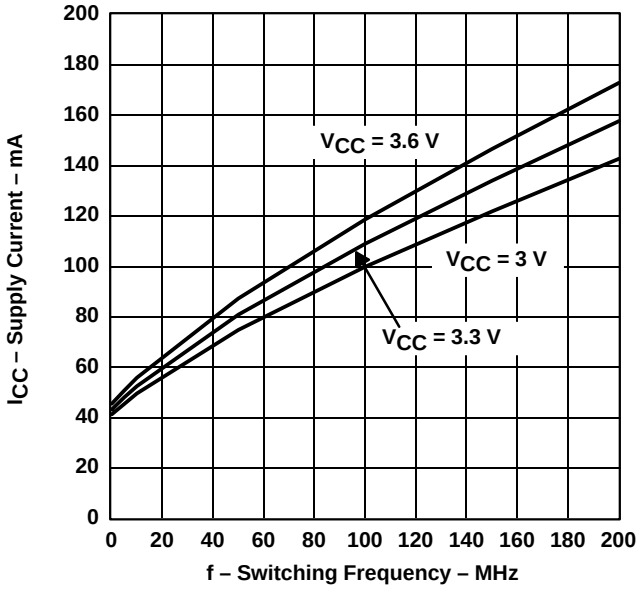



Figure 5

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

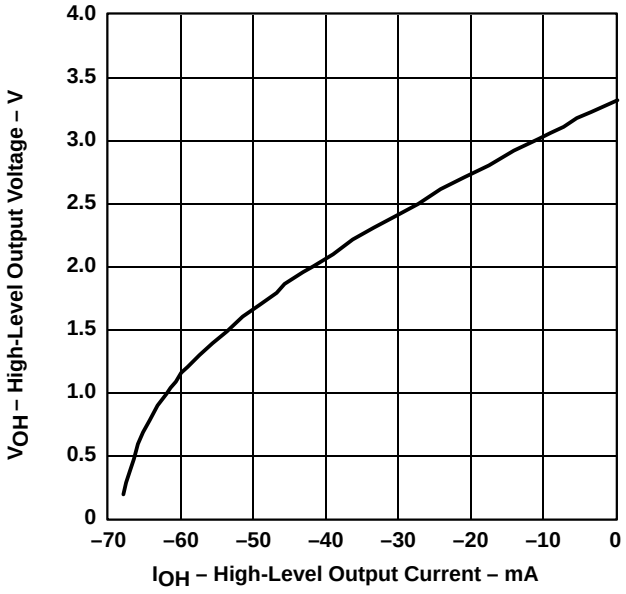



Figure 6

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

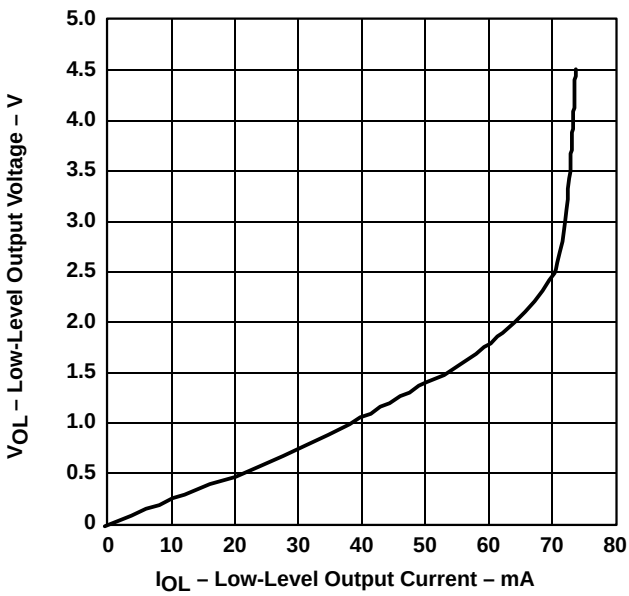



Figure 7

## TYPICAL CHARACTERISTICS

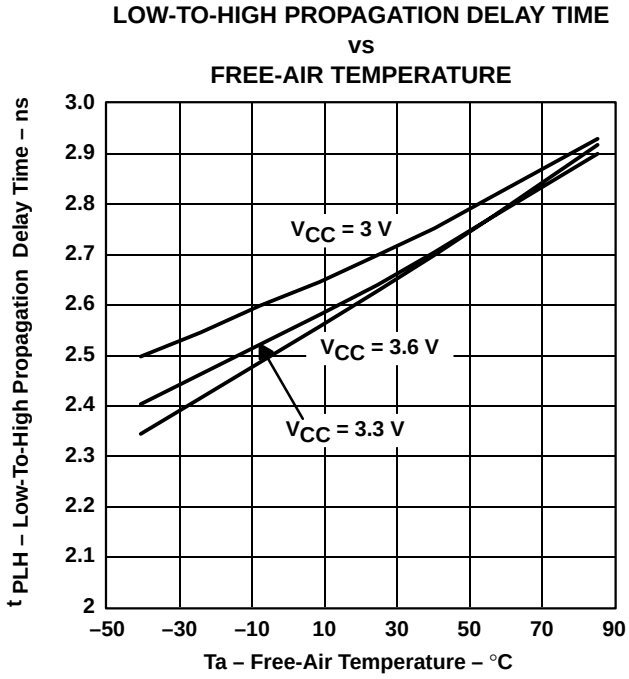



Figure 8

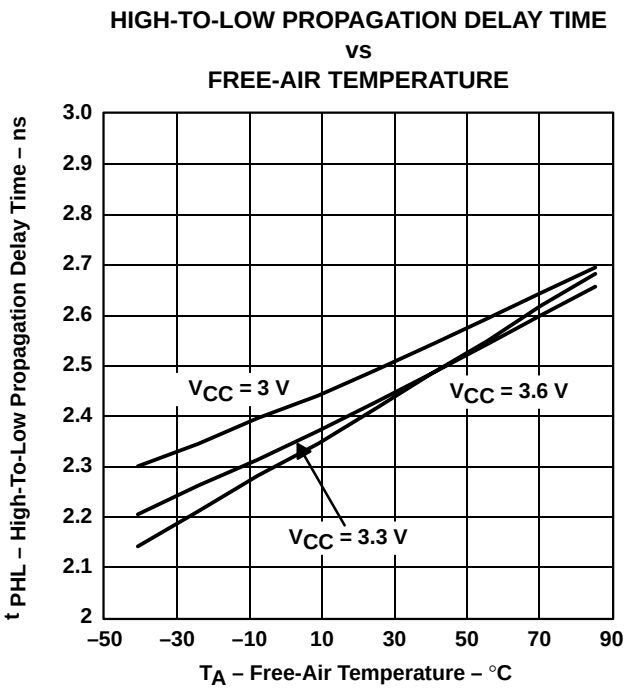



Figure 9

## APPLICATION INFORMATION

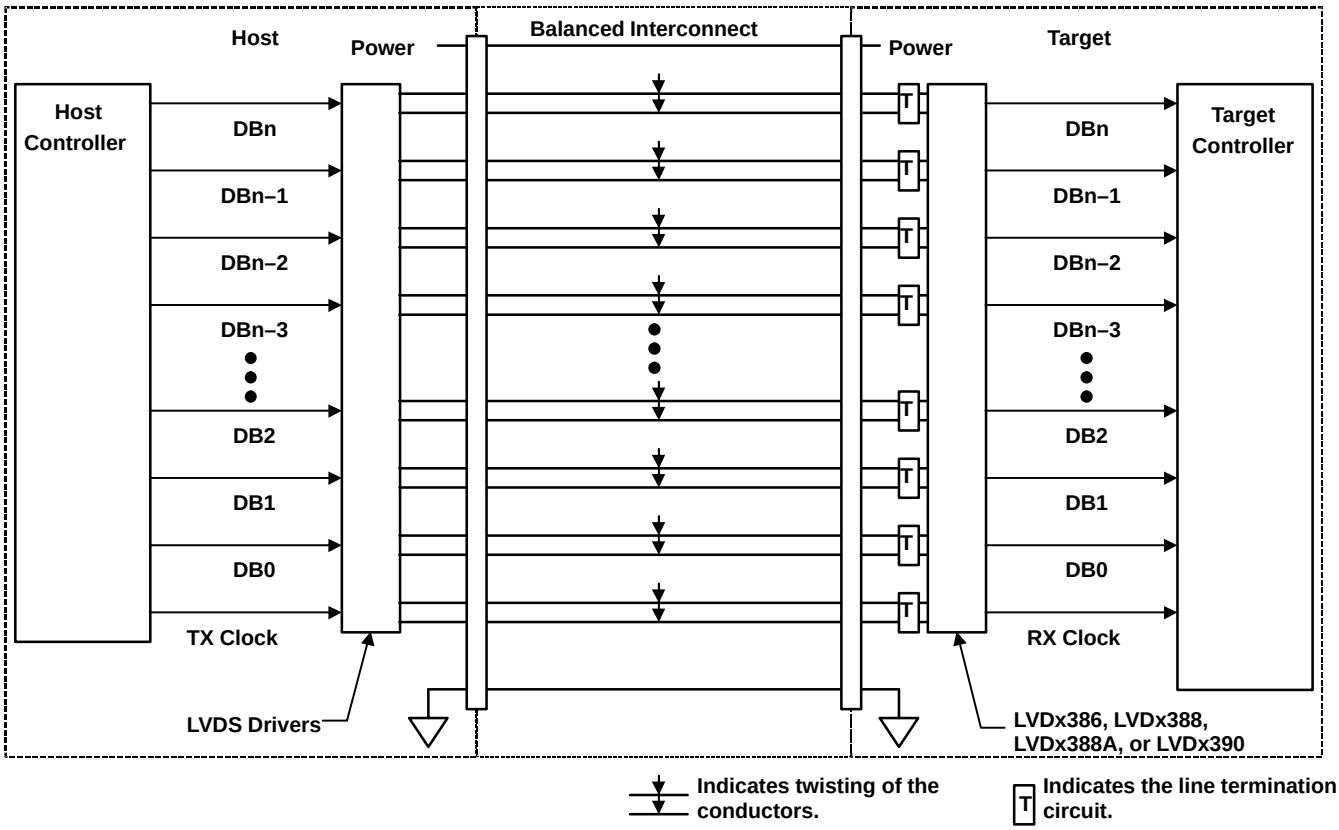



**Figure 10. Typical Application Schematic**

## APPLICATION INFORMATION

### fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near $V_{CC}$ through 300-kΩ resistors as shown in Figure 10. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

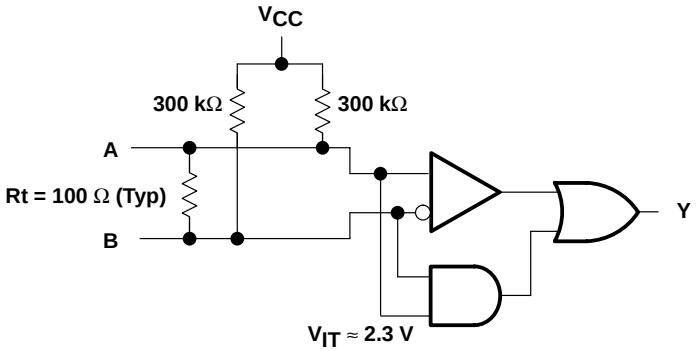



**Figure 11. Open-Circuit Fail Safe of the LVDS Receiver**

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVDT388DBT | NRND | TSSOP | DBT | 38 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVDT388 | |
| SN65LVDT388DBTR | NRND | TSSOP | DBT | 38 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVDT388 | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

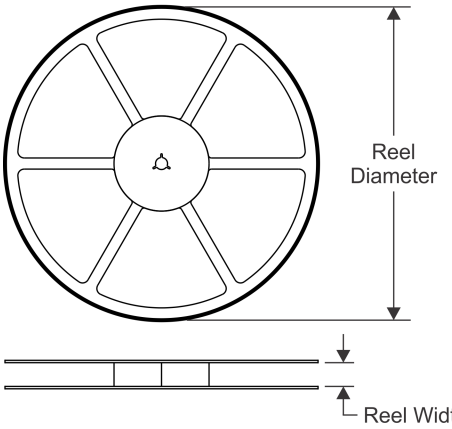
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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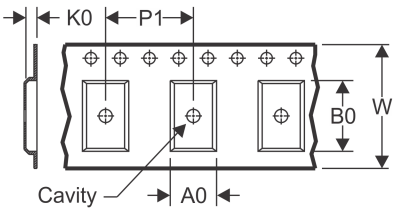
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

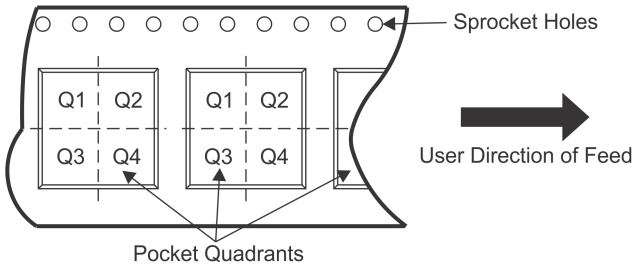



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

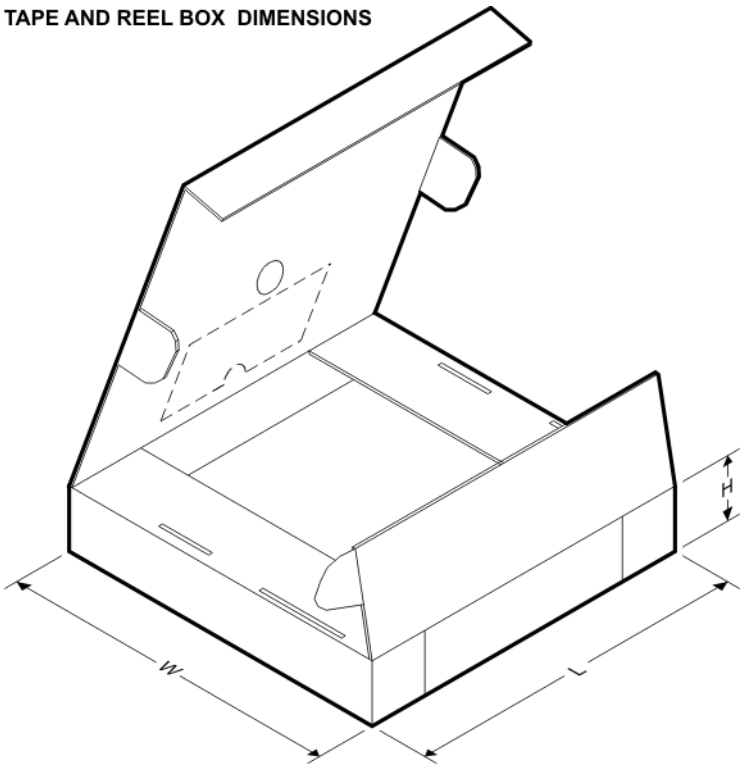
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVDT388DBTR | TSSOP | DBT | 38 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65LVDT388DBTR | TSSOP | DBT | 38 | 2000 | 350.0 | 350.0 | 43.0 |

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