TPS6131x 1.5-A Multiple LED Camera Flash and Video Light Driver With I²C Compatible Interface

1 Features

- Operational Modes:
  - Video Light and Flash Strobe
  - Voltage Regulated Converter: 3.8 V to 5.7 V With Down Mode
  - Standby: 2 µA (Typical)
- LED V_F Measurement
- Power-Save Mode for Improved Efficiency at Low Output Power, Up to 95% Efficiency
- I²C Compatible Interface up to 3.4 Mbps
- Dual Wire Camera Module Interface
- Zero Latency Tx-Masking Input
- Hardware Reset Input
- Privacy Indicator LED Output
- GPIO and Power Good Output
- Various Safe Operation and Robust Handling Features:
  - LED Temperature Monitoring
  - Open and Shorted LED Detection and Protection
  - Integrated LED Safety Timer
  - Automatic Battery Voltage Droop Monitoring and Protection
  - Smooth LED Current Ramp-Up and Ramp-Down
  - Undervoltage Lockout
- Total Solution Size of Less Than 25 mm²
- Available in a 20-Pin NanoFree™ DSBGA Package

2 Applications

- Single, Dual, or Triple White LED Flash Supply for Cell Phones and Smart-Phones
- Video Lighting for Digital Video Applications
- General Lighting Applications
- Audio Amplifier Power Supply

3 Description

The TPS6131x family is an integrated solution with a wide feature set for driving up to three LEDs for still-camera flash strobe and video-camera lighting applications. It is based on a high efficiency synchronous boost topology with combinable current sinks to drive up to three white LEDs in parallel. The 2-MHz switching frequency allows the use of small and low-profile 2.2-µH inductors. To optimize overall efficiency, the device operates with a low LED-feedback voltage and regulated output-voltage adaptation.

The device integrates a control scheme that automatically optimizes the LED current flash budget as a function of the battery voltage condition.

The TPS6131x not only operates as a regulated current source, but also as a standard voltage boost regulator. The device enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range. These operating modes can be useful to supply other high power devices in the system (for example, a hands-free audio PA).

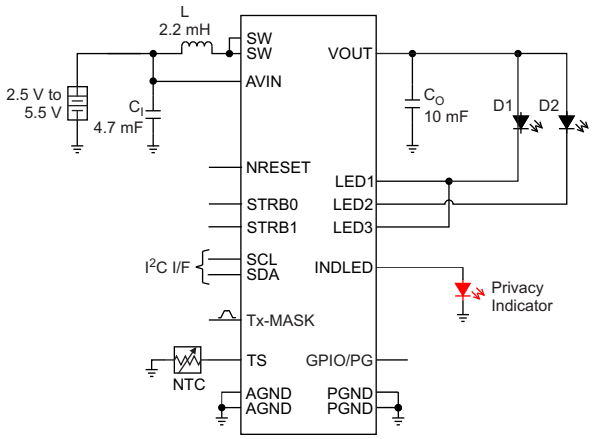
To simplify video light and flash synchronization with the camera module, the device offers a dedicated control interface (STRB0, STRB1) for zero latency LED turnon time.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61310, TPS61311	DSBGA (20)	2.20 mm × 1.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2012) to Revision D — **Page**

- Added *Device Information* table,*ESD Ratings* table,*Recommended Operating Conditions* table,*Thermal Information* table,*Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 1

Changes from Revision B (September 2011) to Revision C — **Page**

- Added revision letter C to literature number ... 1
- Added TPS61311 to ordering table ... 3
- Added Current Limit Setting for TPS61311 ... 21
- Added current limit setting for TPS61311 in register map ... 34

Changes from Revision A (October 2010) to Revision B — **Page**

- Changed V_{UVLO} to max value from 2.35 V to 2.4 V. ... 5
- Updated LED forward voltage calibration description. ... 24
- Updated SFT bit description ... 33

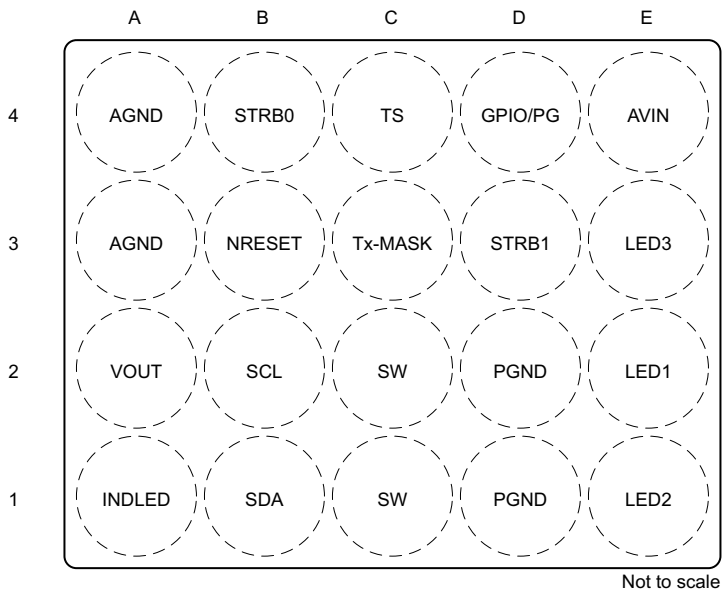
5 Device Comparison Table

PACKAGE	DEVICE SPECIFIC FEATURES(1)
TPS61310	up to 1750-mA (typical) input valley current
TPS61311	up to 2480-mA (typical) input valley current

(1) For more details, see *Detailed Description* and *Application and Implementation*.

6 Pin Configuration and Functions

YFF Package
20-Pin DSBGA
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	INDLED	O	This pin provides a constant current source to drive low V_F LEDs. Connect to LED anode.
A2	VOUT	O	This is the output voltage pin of the converter.
A3, A4	AGND	—	Analog ground.
B1	SDA	I/O	Serial interface address and data line. This pin must not be left floating and must be terminated.
B2	SCL	I	Serial interface clock line. This pin must not be left floating and must be terminated.
B3	NRESET	I	Master hardware reset input. NRESET = LOW: The device is forced in shutdown mode and the I^2C control I/F and all internal control registers are reset. NRESET = HIGH: The device is operating normally under the control of the I^2C interface.
B4	STRB0	I	LED1, LED2, and LED3 enable logic input. This pin can be used to enable or disable the high-power LEDs connected to the device. STRB0 = LOW: LED1, LED2 and LED3 current regulators are turned off. STRB0 = HIGH: LED2, LED2 and LED3 current regulators are active. The LED current level (video light or flash current) is defined according to the STRB1 logic level.
C1, C2	SW	I/O	Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor. SW is high impedance during shutdown.
C3	Tx-MASK	I	RF PA synchronization control input. Pulling this pin high turns the LED from flash to video light operation, thereby reducing almost instantaneously the peak current loading from the battery.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
C4	TS	I	NTC resistor connection. This pin can be used to monitor the LED temperature. Connect a 220-kΩ NTC resistor from the TS input to ground. In case this functionality is not desired, the TS input must be tied to AVIN or left floating.
D1, D2	PGND	—	Power ground. Connect to AGND underneath IC.
D3	STRB1	I	LED current level selection input. Pulling this input high disables the video light watchdog timer. STRB1 = LOW: flash mode is enabled. STRB1 = HIGH: video light mode is enabled.
D4	GPIO/PG	I/O	This pin can either be configured as a general purpose I/O pin (GPIO) or either as an open-drain or a push-pull output to signal when the converters output voltage is within the regulation limits (PG). Per default, the pin is configured as an open-drain Power Good output.
E1	LED2	I	
E2	LED1	I	LED return input (current sinks). This feedback pin regulates the LED current through the internal sense resistor by regulating the voltage across it. Connect to the cathode of the white LEDs.
E3	LED3	I	
E4	AVIN	I	This is the input voltage pin of the device. Connect directly to the input bypass capacitor.

7 Specifications

7.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Voltage	AVIN, VOUT, SW, LED1, LED2, LED3, SCL, SDA, STRB0, STRB1, NRESET, GPIO/PG, Tx-MASK, TS	–0.3	7	V
Current on GPIO/PG			±25	mA
Power dissipation		Internally limited		
Operating ambient temperature, T_A (2)		–40	85	°C
Maximum operating junction temperature, T_J (2)			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part in the application ($R_{\theta JA}$), as given by: $T_{A(max)} = T_{J(max)} – (R_{\theta JA} \times P_{D(max)})$

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS6131x YFF (DSBGA) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Specification applies for V_{IN} = 3.6 V over an operating junction temperature T_J = –40°C to 125°C; see Figure 24 (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage		2.5		5.5	V
I_Q	Operating quiescent current into AVIN	I_{OUT} = 0 mA, device not switching (Power Safe Mode), –40°C ≤ T_J ≤ 85°C		590	700	µA
		$I_{OUT(DC)}$ = 0 mA, PWM operation V_{OUT} = 4.95 V, voltage regulation mode		11.3		mA
I_{SD}	Shutdown current	–40°C ≤ T_J ≤ 85°C		1	5	µA
V_{UVLO}	Undervoltage lockout threshold (analog circuitry)	V_{IN} falling		2.3	2.4	V
OUTPUT						
V_{OUT}	Output voltage	Current regulation mode	V_{IN}		5.5	V
		Voltage regulation mode	3.825		5.7	
	Internal feedback voltage accuracy	2.5 V ≤ V_{IN} ≤ 4.8 V, –20°C ≤ T_J ≤ 125°C, Boost mode, PWM voltage regulation	–2%		2%	
	Power-save mode ripple voltage	I_{OUT} = 10 mA	0.015 × V_{OUT}			V_{P-P}
OVP	Output overvoltage protection	V_{OUT} rising, 0000 ≤ OV[3:0] ≤ 0100	4.5	4.65	4.8	V
		V_{OUT} rising, 0101 ≤ OV[3:0] ≤ 1111	5.8	6	6.2	
	Output overvoltage protection hysteresis	V_{OUT} falling		0.15		
POWER SWITCH						
$r_{DS(on)}$	Switch MOSFET ON-resistance	V_{OUT} = V_{GS} = 3.6 V		90		mΩ
	Rectifier MOSFET ON-resistance	V_{OUT} = V_{GS} = 3.6 V		135		mΩ
$I_{lkg(SW)}$	Leakage into SW	V_{OUT} = 0 V, SW = 3.6 V, –40°C ≤ T_J ≤ 85°C		0.3	4	µA
I_{lim}	Rectifier valley current limit (open loop)	V_{OUT} = 4.95 V, –20°C ≤ T_J ≤ 85°C, PWM operation, relative to selected ILIM	–15%		15%	
OSCILLATOR						
f_{OSC}	Oscillator frequency			1.92		MHz
f_{ACC}	Oscillator frequency		–10%		7%	
THERMAL SHUTDOWN, HOT DIE DETECTOR						
	Thermal shutdown[1]		140	160		°C
	Thermal shutdown hysteresis[1]			20		°C
	Hot die detector accuracy[1]		–8		8	°C
LED CURRENT REGULATOR						
	LED1 and LED3 current accuracy[2]	0.4 V ≤ $V_{LED[1,3]}$ ≤ 2 V, 0 mA ≤ $I_{LED[1,3]}$ ≤ 100 mA, T_J = 85°C	–10%		10%	
		0.4 V ≤ $V_{LED[1,3]}$ ≤ 2 V, 100 mA < $I_{LED[1,3]}$ ≤ 400 mA, T_J = 85°C	–7.5%		7.5%	

(1) Verified by characterization. Not tested in production.
(2) Verified by characterization. Not tested in production.

Electrical Characteristics (continued)

Specification applies for V_{IN} = 3.6 V over an operating junction temperature T_J = –40°C to 125°C; see Figure 24 (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	LED2 current accuracy(2)	0.4 V ≤ V_{LED2} ≤ 2 V, 0 mA ≤ I_{LED2} ≤ 250 mA, T_J = 85°C	–10%		10%	
		0.4 V ≤ V_{LED2} ≤ 2 V, 250 mA ≤ I_{LED2} ≤ 800 mA, T_J = 85°C	–7.5%		7.5%	
	LED1 and LED3 current matching(2)		–10%		10%	
	LED1, LED2, and LED3 current temperature coefficient			0.05		%/°C
	INDLED current accuracy	1.5 V ≤ (V_{IN} – V_{INDLED}) ≤ 2.5 V 2.6 mA ≤ I_{INDLED} ≤ 15.8 mA, T_J = 25°C	–20%		20%	
	INDLED current temperature coefficient			0.05		%/°C
	LED1, LED2, and LED3 sense voltage	$I_{LED[1,2,3]}$ = full-scale current		400		mV
V_{DO}	VOUT dropout voltage	I_{OUT} = –15.8 mA, T_J = 25°C, device not switching			250	mV
	LED1, LED2, and LED3 input leakage current	$V_{LED[1,2,3]}$ = V_{OUT} = 5 V, –40°C ≤ T_J ≤ 85°C		0.1	4	µA
	INDLED input leakage current	V_{INDLED} = 0 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
LED TEMPERATURE MONITORING						
$I_{O(TS)}$	Temperature Sense Current Source	Thermistor bias current		23.8		µA
	TS Resistance (Warning Temperature)	LEDWARN bit = 1	39	44.5	50	kΩ
	TS Resistance (Hot Temperature)	LEDHOT bit = 1	12.5	14.5	16.5	kΩ
SDA, SCL, GPIO/PG, Tx-MASK, STRB0, STRB1, NRESET						
$V_{(IH)}$	High-level input voltage		1.2			V
$V_{(IL)}$	Low-level input voltage				0.4	V
$V_{(OL)}$	Low-level output voltage (SDA)	I_{OL} = 8 mA			0.3	V
	Low-level output voltage (GPIO)	DIR = 1, I_{OL} = 5 mA			0.3	
$V_{(OH)}$	High-level output voltage (GPIO)	DIR = 1, GPIOTYPE = 0, I_{OH} = 8 mA	V_{IN} – 0.4			V
$I_{(LKG)}$	Logic input leakage current	Input connected to VIN or GND, –40°C ≤ T_J ≤ 85°C		0.01	0.1	µA
R_{PD}	STRB0, STRB1 pulldown resistance	STRB0, STRB1 ≤ 0.4 V		400		kΩ
	NRESET pulldown resistance	NRESET ≤ 0.4 V		400		
	Tx-MASK pulldown resistance	Tx-MASK ≤ 0.4 V		400		
$C_{(IN)}$	SDA Input Capacitance	SDA = V_{IN} or GND		9		pF
	SCL Input Capacitance	SCL = V_{IN} or GND		4		
	GPIO/PG Input Capacitance	DIR = 0, GPIO/PG = V_{IN} or GND		9		
	STRB0 Input Capacitance	STRB0 = V_{IN} or GND		3		
	STRB1 Input Capacitance	STRB1 = V_{IN} or GND		3		
	NRESET Input Capacitance	NRESET = V_{IN} or GND		3.5		
	Tx-MASK Input Capacitance	Tx-MASK = V_{IN} or GND		4		
TIMING						
t_{NRESET}	Reset pulse width		10			µs
	Start-up time	From shutdown into video light mode I_{LED} = 150 mA		1.2		ms
	LED current settling time(3) triggered by a rising edge on STRB0	MODE_CTRL[1:0] = 10, I_{LED2} = from 0 mA to 950 mA		500		µs
	LED current settling time(3) triggered by Tx-MASK	MODE_CTRL[1:0] = 10, I_{LED2} = from 950 mA to 150 mA		20		µs

(3) Settling time to ±15% of the target value.

7.6 I²C Interface Timing Requirements

see (1)

			MIN	MAX	UNIT
$f_{(SCL)}$	SCL Clock Frequency	Standard mode		100	kHz
		Fast mode		400	
		High-speed mode (write operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (read operation), C_B – 100 pF max		3.4	
		High-speed mode (write operation), C_B – 400 pF max		1.7	
		High-speed mode (read operation), C_B – 400 pF max		1.7	
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard mode	4.7		µs
		Fast mode	1.3		
t_{HD}, t_{STA}	Hold Time (Repeated) START Condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		
t_{LOW}	LOW Period of the SCL Clock	Standard mode	4.7		µs
		Fast mode	1.3		
		High-speed mode, C_B – 100 pF max	160		ns
		High-speed mode, C_B – 400 pF max	320		
t_{HIGH}	HIGH Period of the SCL Clock	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode, C_B – 100 pF max	60		
		High-speed mode, C_B – 400 pF max	120		
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		
t_{SU}, t_{DAT}	Data Setup Time	Standard mode	250		ns
		Fast mode	100		
		High-speed mode	10		
t_{HD}, t_{DAT}	Data Hold Time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	
		High-speed mode, C_B – 100 pF max	0	70	ns
		High-speed mode, C_B – 400 pF max	0	150	
t_{RCL}	Rise Time of SCL Signal	Standard mode	20 + 0.1 × C_B	1000	ns
		Fast mode	20 + 0.1 × C_B	300	
		High-speed mode, C_B – 100 pF max	10	40	
		High-speed mode, C_B – 400 pF max	20	80	
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode	20 + 0.1 × C_B	1000	ns
		Fast mode	20 + 0.1 × C_B	300	
		High-speed mode, C_B – 100 pF max	10	80	
		High-speed mode, C_B – 400 pF max	20	160	
t_{FCL}	Fall Time of SCL Signal	Standard mode	20 + 0.1 × C_B	300	ns
		Fast mode	20 + 0.1 × C_B	300	
		High-speed mode, C_B – 100 pF max	10	40	
		High-speed mode, C_B – 400 pF max	20	80	
t_{RDA}	Rise Time of SDA Signal	Standard mode	20 + 0.1 × C_B	1000	ns
		Fast mode	20 + 0.1 × C_B	300	
		High-speed mode, C_B – 100 pF max	10	80	
		High-speed mode, C_B – 400 pF max	20	160	

(1) Specified by design. Not tested in production.

I²C Interface Timing Requirements (continued)

see (1)

			MIN	MAX	UNIT
t_{FDA}	Fall Time of SDA Signal	Standard mode	20 + 0.1 × C_B	300	ns
		Fast mode	20 + 0.1 × C_B	300	
		High-speed mode, C_B – 100 pF max	10	80	
		High-speed mode, C_B – 400 pF max	20	160	
t_{SU}, t_{STO}	Setup Time for STOP Condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		
C_B	Capacitive Load for SDA and SCL			400	pF

7.7 Dissipation Ratings

PACKAGE	POWER RATING (T_A = 25°C)	DERATING FACTOR ABOVE T_A = 25°C(1)
YFF	1.4 W	14 mW/°C

(1) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / R_{\theta JA}$.

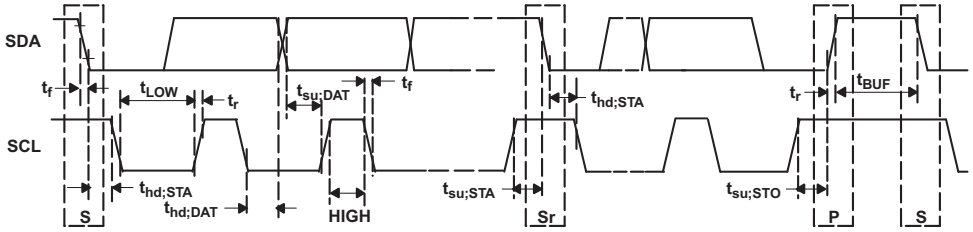
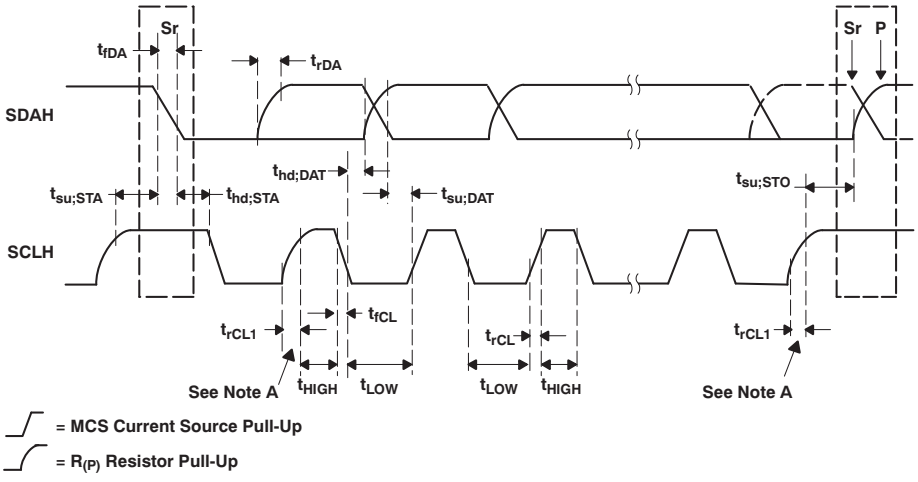


Figure 1. Serial Interface Timing For F/S-Mode



Note A: First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 2. Serial Interface Timing For H/S-Mode

7.8 Typical Characteristics

Table 1. Table of Graphs

CAPTION		FIGURE
LED Power Efficiency	Input Voltage	Figure 3, Figure 4
DC Input Current	Input Voltage	Figure 5
LED Current	LED Pin Headroom Voltage	Figure 6, Figure 7
LED Current	LED Current Digital Code	Figure 8, Figure 9, Figure 10, Figure 11
INDLED Current	INDLED Pin Headroom Voltage	Figure 12
Efficiency	Output Current	Figure 13, Figure 14
DC Output Voltage	Load Current	Figure 15, Figure 16
Maximum Output Current	Input Voltage	Figure 17
DC Precharge Current	Differential I/O Voltage	Figure 18, Figure 19
Supply Current	Input Voltage	Figure 20
Temperature Detection Threshold		Figure 21, Figure 22
Junction Temperature	Port Voltage	Figure 23

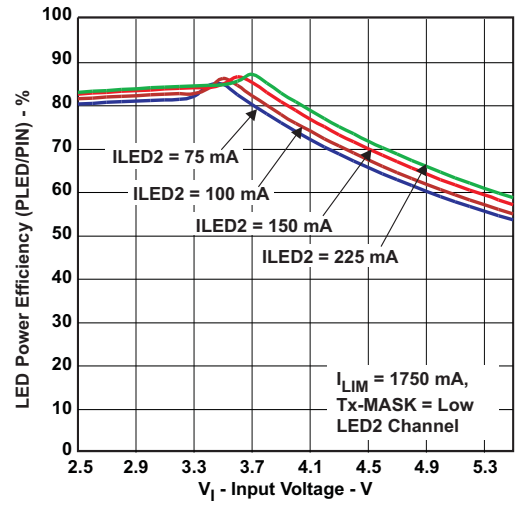


Figure 3. LED Power Efficiency vs Input Voltage

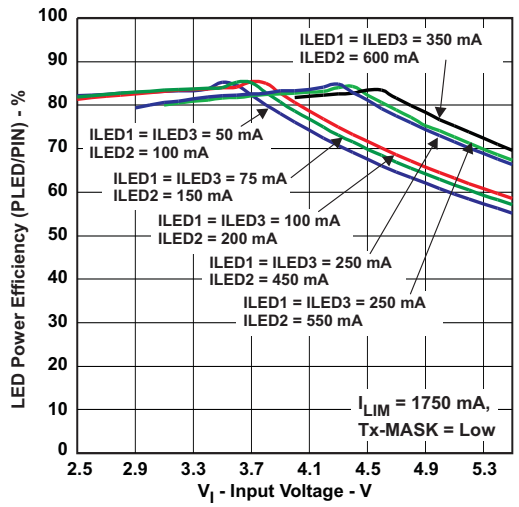


Figure 4. LED Power Efficiency vs Input Voltage

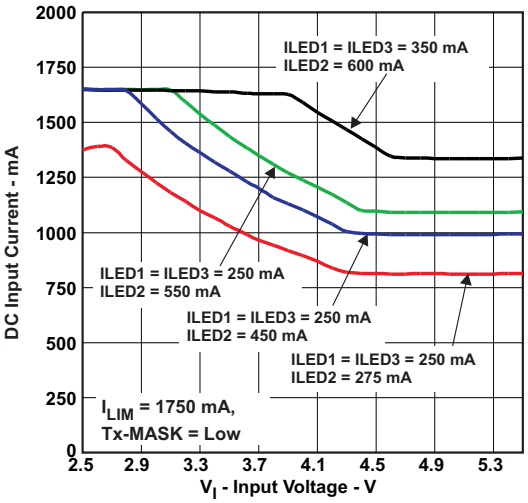


Figure 5. DC Input Current vs Input Voltage

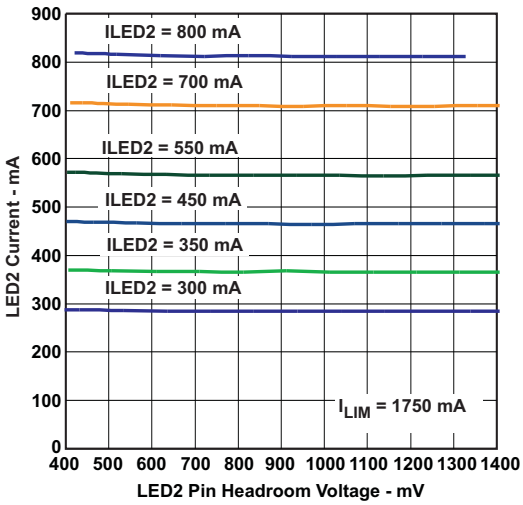


Figure 6. LED2 Current vs LED2 Pin Headroom Voltage

Typical Characteristics (continued)

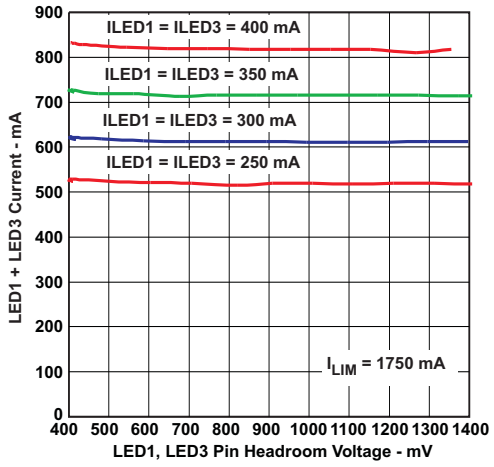


Figure 7. LED1 + LED3 Current vs LED1 + LED3 Pin Headroom Voltage

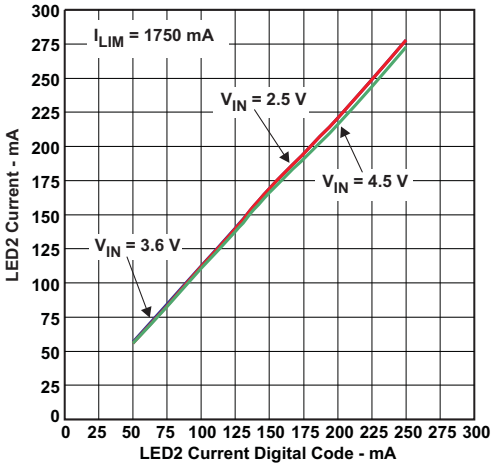


Figure 8. LED2 Current vs LED2 Current Digital Code

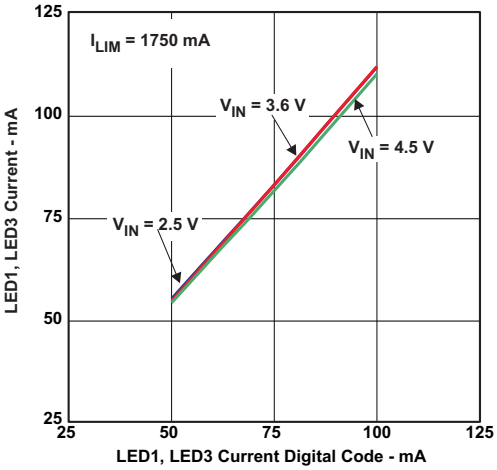


Figure 9. LED1, LED3 Current vs LED1, LED3 Current Digital Code

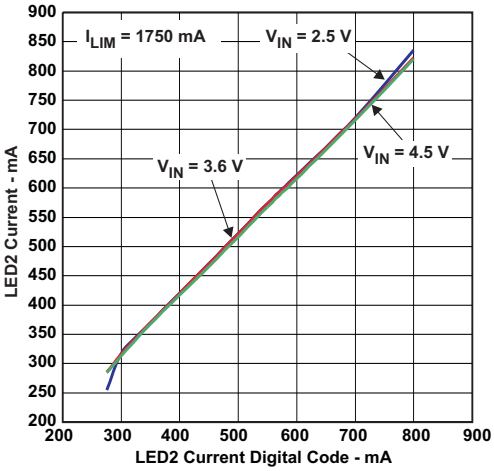


Figure 10. LED2 Current vs LED2 Current Digital Code

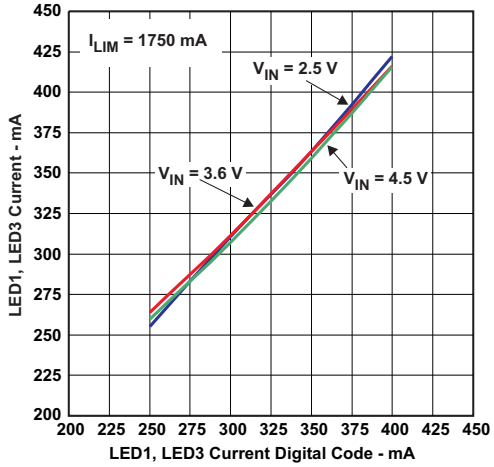


Figure 11. LED1, LED3 Current vs LED1, LED3 Current Digital Code

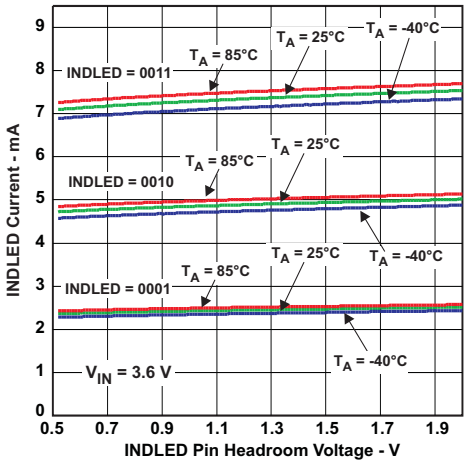


Figure 12. INDLED Current vs INDLED Pin Headroom Voltage

Typical Characteristics (continued)

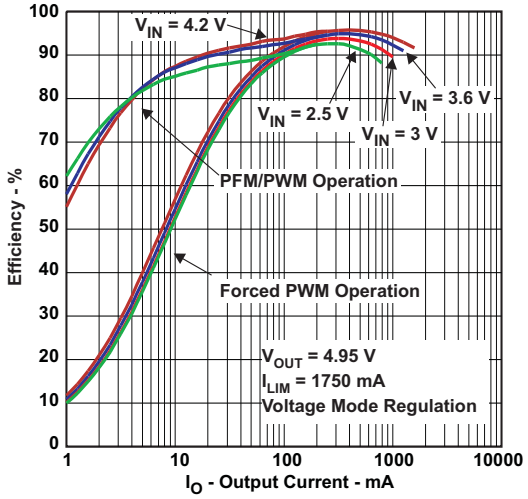


Figure 13. Efficiency vs Output Current

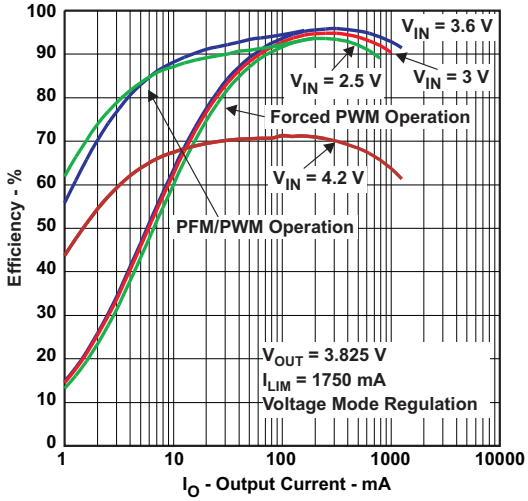


Figure 14. Efficiency vs Output Current

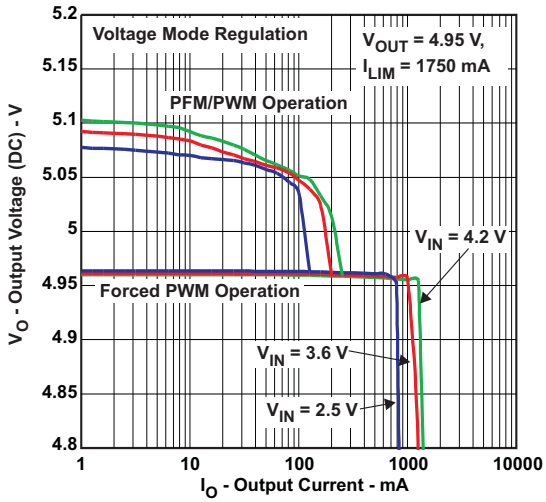


Figure 15. DC Output Voltage vs Load Current

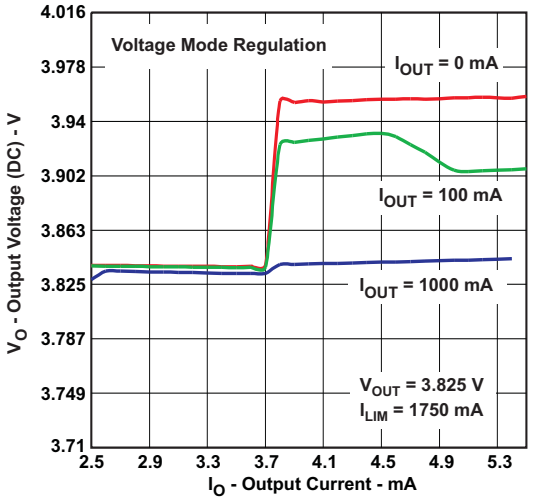


Figure 16. DC Output Voltage vs Load Current

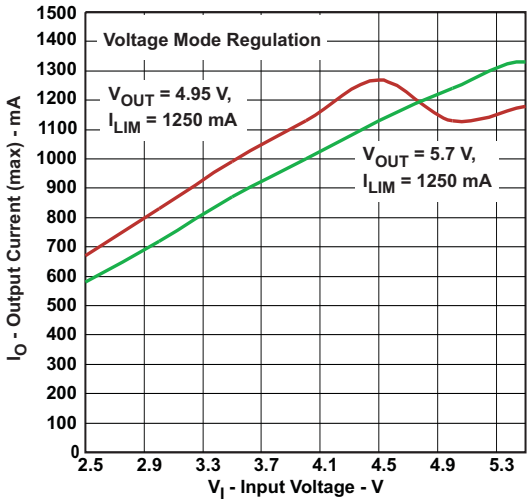


Figure 17. Maximum Output Current vs Input Voltage

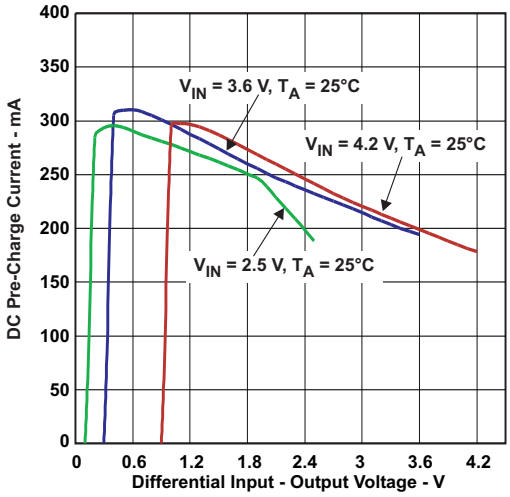


Figure 18. DC Precharge Current vs Differential I/O Voltage

Typical Characteristics (continued)

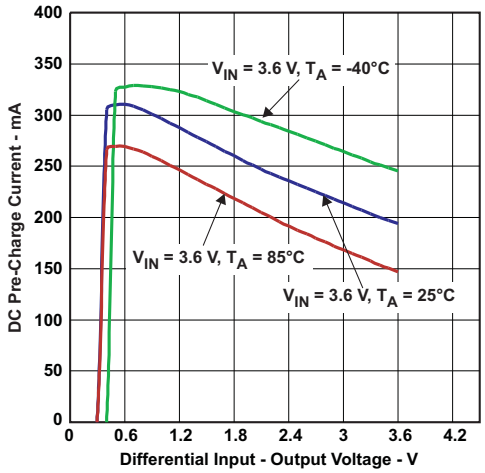


Figure 19. DC Precharge Current vs Differential I/O Voltage

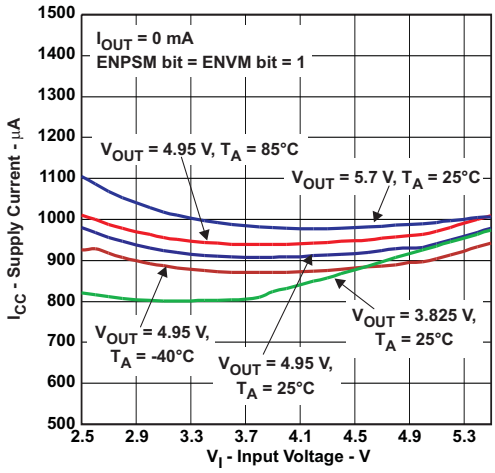


Figure 20. Supply Current vs Input Voltage

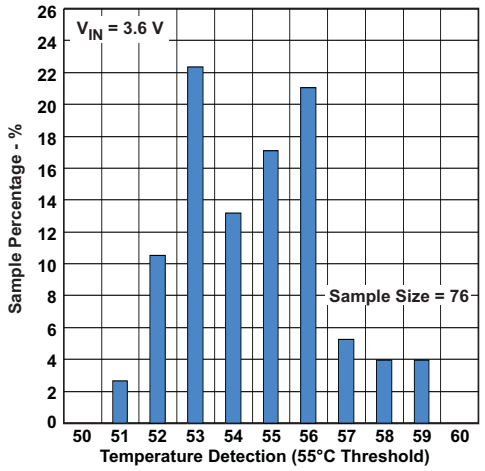


Figure 21. Temperature Detection Threshold

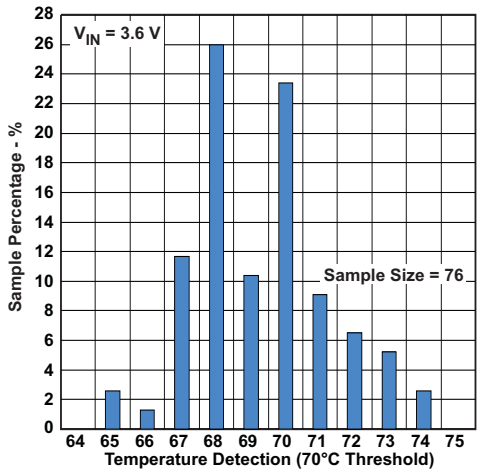


Figure 22. Temperature Detection Threshold

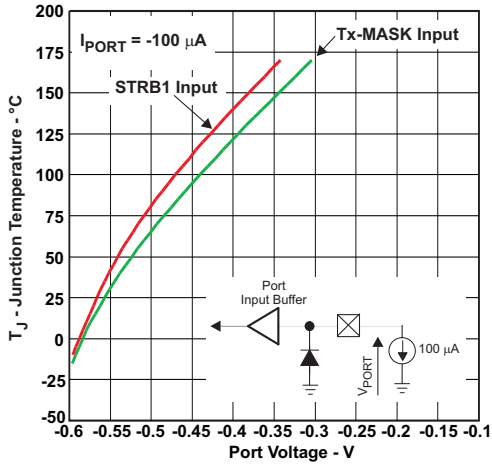
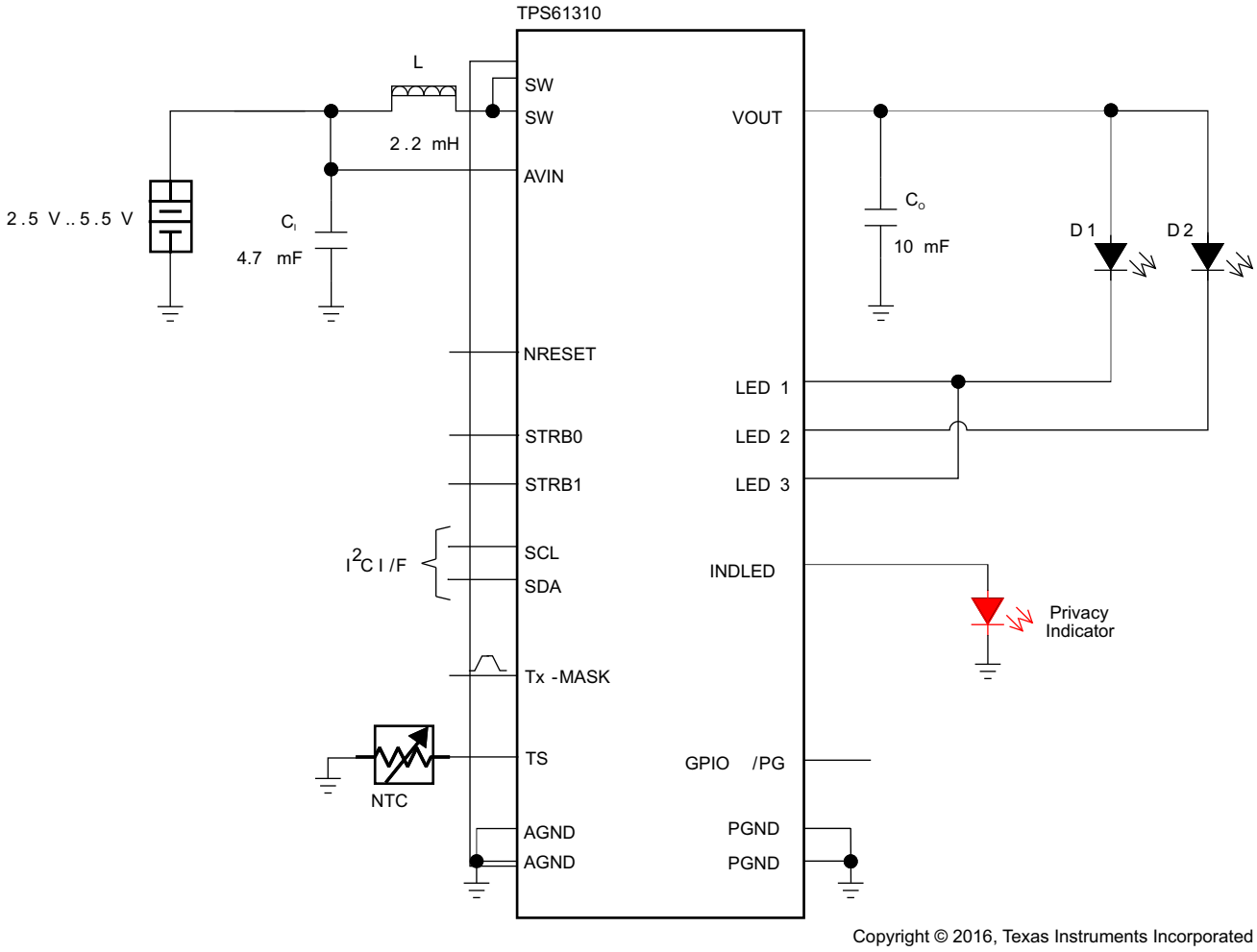


Figure 23. Junction Temperature vs Port Voltage

8 Parameter Measurement Information



L = 2.2-µH
C_I, C_O = 10-µF, 6.3-V X5R 0603
NTC = 220-kΩ

Figure 24. TPS61310 Typical Application Circuit

9 Detailed Description

9.1 Overview

The TPS6131x family is an integrated solution with a wide feature set for driving up to three LEDs for still-camera flash and video-camera lighting applications. It employs a 2-MHz fixed on-time, PWM current-mode converter to generate the output voltage required to drive up to three high-power LEDs in parallel. The device integrates an NMOS-switch power stage and a synchronous PMOS rectifier. The device also implements a set of linear low-side current regulators to control the LED current when the battery voltage is higher than the diode forward voltage.

The high-efficiency boost converter stage and LED forward voltage adoption ensure lowest device input current for a given LED output current.

A special circuit disconnects the load from the battery during shutdown of the converter. In conventional synchronous-rectifier circuits, the back-gate diode of the high-side PMOS is forward biased in shutdown, allowing current to flow from the battery to the output. The TPS6131x prevents this by disconnecting the cathode of the back-gate diode of the high-side PMOS from the source when the regulator is in shutdown.

The TPS6131x device not only operates as a regulated current source, but also as a standard voltage-boost regulator featuring a power-save mode for improved efficiency at light loads. If the input voltage is higher than the programmed output voltage, a down mode is implemented that acts similarly to an LDO.

The power stage is capable of supplying a maximum total current of roughly 1500 mA. The TPS6131x provides three constant-current sinks, capable of sinking up to 2 × 400 mA (LED1 and LED3) and 800 mA (LED2) in flash mode.

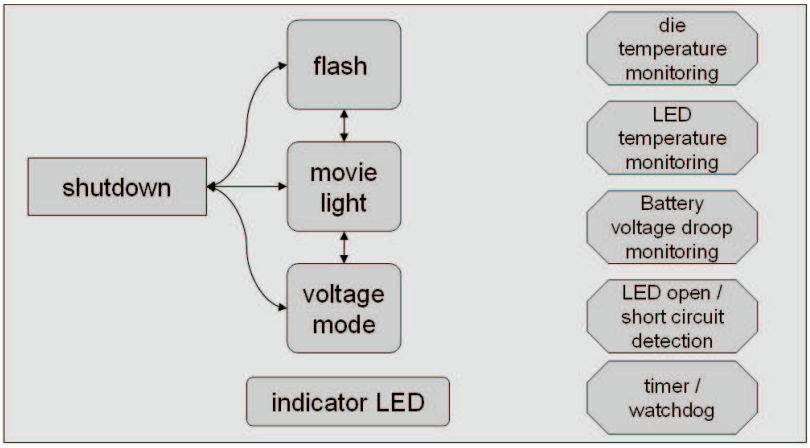


Figure 25. TPS6131x States

Special effort is taken for safe operation and robust system integration. The battery voltage can be monitored so that the flash current is not increased if the battery voltage drops by a programmable threshold. Internal timers limit the flash ON time to prevent potential camera-engine software errors, and a video light watchdog acts in a similar fashion. Multiple monitoring features (LED and die temperature, input voltage droop and so forth) keep the device and LEDs operating properly.

The TPS6131x integrates an I^2C compatible interface allowing transfers up to 3.4 Mbps for controlling the device, featuring low-speed mode, standard mode and high-speed mode compatible operation. Additionally, basic functions can be triggered by dedicated hardware input signals, such as STRB0 and STRB1 for triggering the flash or video lighting with zero latency.

9.2 Functional Block Diagram

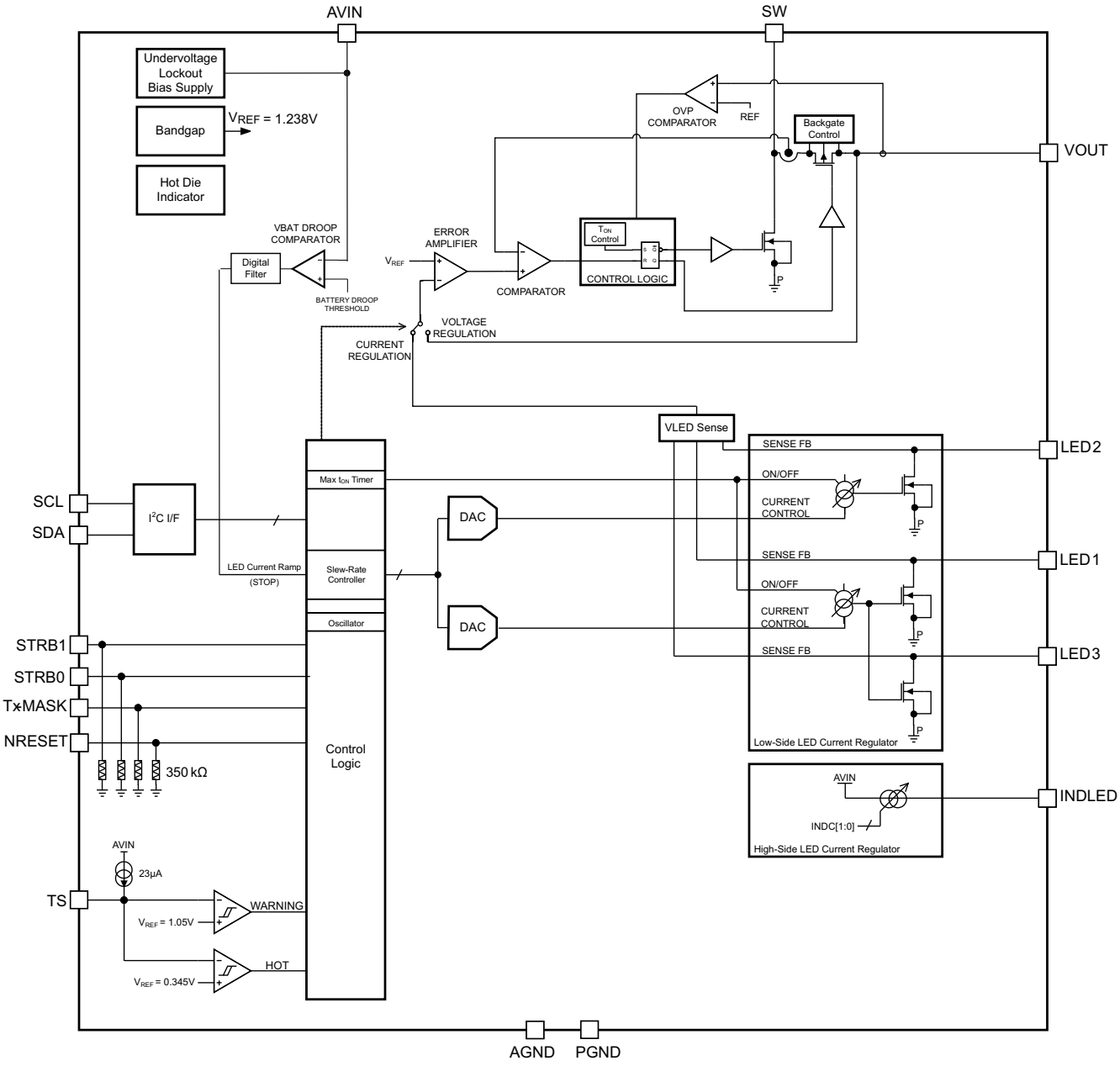


Figure 26. TPS6131x

Functional Block Diagram (continued)

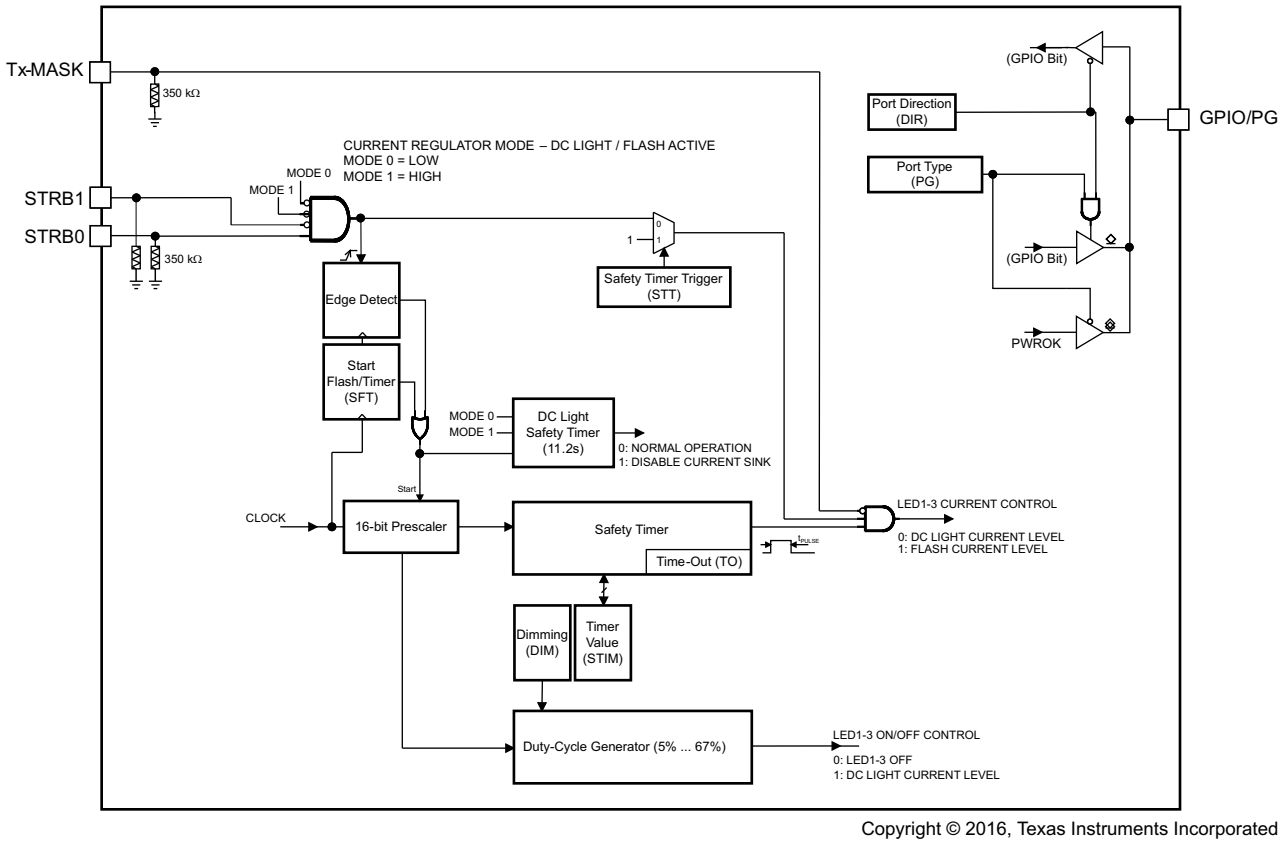


Figure 27. Timer Block

9.3 Feature Description

9.3.1 Privacy Indicator

The privacy indicator functionality can be used to indicate when a person is being photographed or filmed. The TPS6131x device offers two options of privacy indication: A dedicated pin driving an additional privacy indicator LED or using the white LEDs with pulse width modulation.

9.3.1.1 Dedicated LED Privacy Indicator

The TPS6131x device provides a high-side linear constant current source to drive low V_F LEDs. The LED current is directly regulated off the battery and can be controlled through the INDC[3:0] bits, from 2.6 mA to 15.8 mA in 7 programable current steps.

The device can drive two possible hardware configurations shown in Figure 28 and Figure 29. In Figure 28 the TPS6131x device drives a privacy indicator LED towards ground.

Feature Description (continued)

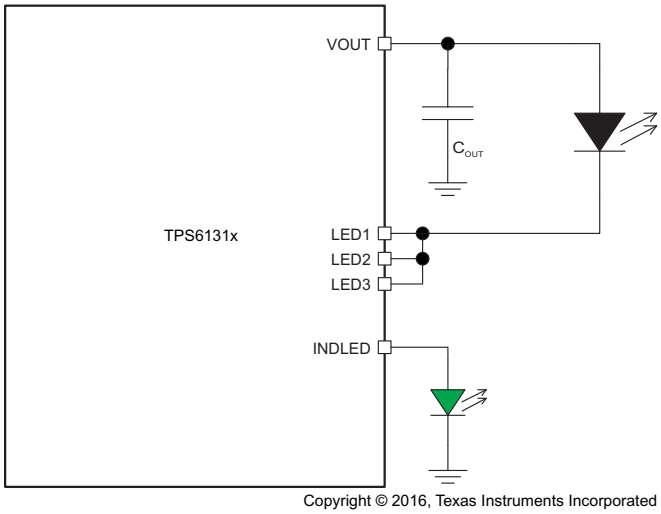


Figure 28. Configuration 1

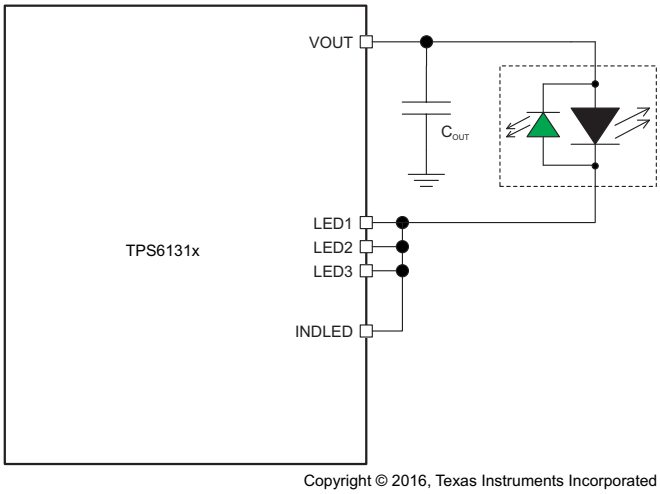


Figure 29. Configuration 2

The TPS6131x device also allows a path for driving a privacy indicator LED that is reverse biased to the white flash LED, see Figure 29. To do so, the output of the converter (VOUT) is pulled to ground thus allowing a reverse current to flow. This mode of operation is only possible when the converter's power stage is in shutdown (MODE_CTRL[1:0] = 00, ENVM = 0).

9.3.1.2 White LED Privacy Indicator

The TPS6131x device features white LED drive capability at very low light intensity. To generate a reduced LED average current, the device employs a 30-kHz fixed-frequency PWM modulation scheme. The PWM timer uses the internal oscillator as reference clock, therefore the PWM modulating frequency shows the same accuracy as the internal reference clock. Operation is shown in Figure 27.

The video light current is modulated with a duty cycle defined by the INDC[3:0] bits. The low light dimming mode can only be activated in the software-controlled video-light-only mode (MODE_CTRL[1:0] = 01, ENVM = 1), and applies to the LEDs selected through ENLED[3:1] bits. In this mode, the video light safety-timeout feature is disabled.

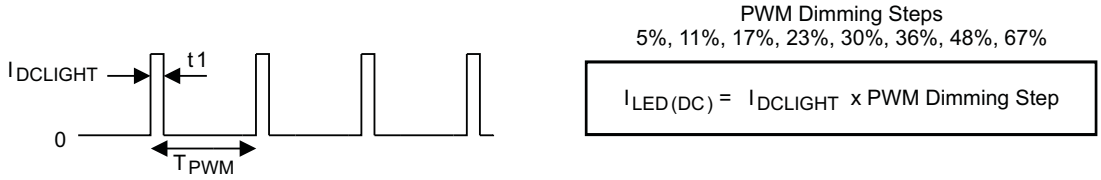


Figure 30. PWM Dimming Principle

9.3.2 Safe Operation and Protection Features

9.3.2.1 LED Temperature Monitoring (Finger-Burn Protection)

The TPS6131x device optionally monitors the LED temperature. Critical temperatures are handled in two stages reflected by two bits: LEDWARN provides an early warning to the camera engine, LEDHOT immediately suspends the flash operation.

The LED temperature is sensed by measuring the voltage drop of a negative-temperature-coefficient resistor connected between the TS and AGND pins. An internal current source provides the bias (approximately 24 µA) for the NTC, and the TS pin voltage is compared to internal thresholds (1.05 V and 0.345 V) to protect the LEDs against overheating. See *NTC Selection*.

The temperature-monitoring blocks are explicitly active in video light or flash modes. In voltage-mode operation [MODE_CTRL[1:0] = 11], the device only activates the TS input when the ENTS bit is set high.

Feature Description (continued)

The LEDWARN and LEDHOT bits reflect the LED temperature. The LEDWARN bit is set when the voltage at the TS pin is lower than 1.05 V. This threshold corresponds to an LED warning temperature value; device operation is still permitted. While regulating LED current, video light or flash modes, the LEDHOT bit is latched when the voltage at the TS pin is lower than 0.345 V. This threshold corresponds to an excessive LED temperature value; device operation is immediately suspended, (MODE_CTRL[1:0] bits are reset, and the HOTDIE[1:0] bits are set).

9.3.2.2 LED Failure Modes (Open and Short Detection) and Overvoltage Protection

The TPS6131x devices incorporate protection features to indicate if the connected LEDs are failing. These protections cover overvoltage conditions, which are caused by a failing LED showing open circuit behavior, as well as short-circuit conditions caused by a failing LED or further reasons causing a short-circuit condition. If such failure conditions occur, these are indicated by setting a failure detection flag. Furthermore, the maximum current drawn from the output is limited and can be programmed by the current-limit setting.

9.3.2.2.1 LED Open Circuit Detection and Overvoltage Protection

If the connected LED(s) fail showing an open circuit behavior or are disconnected, the VOUT output voltage must be limited to prevent the step-up converter from exceeding critical values. An overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. For this protection the TPS6131x output voltage is monitored internally. The TPS6131x device limits V_{OUT} according to the overvoltage protection settings (see Table 2). In this failure mode, V_{OUT} is either limited to 4.65 V (typical) or 6 V (typical) and the HIGH-POWER LED FAILURE (HPLF) flag is set. The OVP threshold depends on the programmed output voltage (OV).

Table 2. OVP Specification

OVP THRESHOLD	OPERATING CONDITIONS
4.65 V typical	0000 ≤ OV[3:0] ≤ 0100
6 V typical	0101 ≤ OV[3:0] ≤ 1111

9.3.2.2.2 Short-Circuit Protection

The TPS6131x devices incorporate double protection to protect the device and application circuit from short-circuit conditions occurring between VOUT and the current sinks LED1, LED2, and LED3.

If a short-circuit condition occurs while the LEDs are operated, the low side current sinks LED1, LED2, LED3 limit the maximum output current as programmed for the video-light mode or flash mode respectively. If a short-circuit condition occurs, the current sinks increase their input resistance to prevent excessive current to be drawn. Furthermore, the HIGH-POWER LED FAILURE flag (HPLF) is set to indicate the short circuit condition. (HPLF) is triggered if the LED forward voltage drops below 1.23 V typically. The second protection is the current limit, which generally limits the current drawn from VOUT. See *Current Limit*.

9.3.2.3 LED Current Ramp-Up and Ramp-Down

To achieve smooth LED current waveforms and avoid excessive battery voltage drop, the TPS6131x device actively controls the LED current ramp-up and ramp-down sequence.

Table 3. LED Current Ramp-Up and Ramp-Down Control vs Operating Mode

LED CURRENT	OPERATING MODE
Ramp-up	I_{STEP} = 25 mA
	t_{RISE} = 12 µs
	Slew rate × 2.1 mA/µs
Ramp-down	I_{STEP} = 25 mA
	t_{FALL} = 0.5 µs
	Slew rate × 50 mA/µs

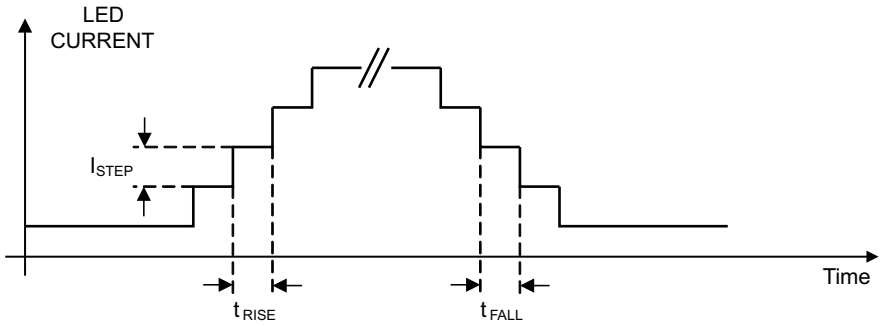


Figure 31. LED Current Slew Rate Control

9.3.2.4 Battery Voltage Droop Monitoring and Protection

During a high-power flash strobe, the battery voltage usually drops by a few hundred millivolts. To prevent the battery voltage from collapsing too much, the TPS6131x devices integrates a battery voltage droop monitoring feature to automatically limit the flash current if the battery voltage drops more than a programmable threshold.

The battery voltage droop monitoring feature can be enabled or disabled through the ENBATMON bit.

At the very beginning of the flash strobe, the device measures the battery voltage and sets a minimum battery voltage threshold based on the tolerable droop (see *REGISTER7 (address = 0x07)* for BATDROOP[2:0] bits). While the LED current is increasing to the target flash current (see *REGISTER1 (address = 0x01)* and *REGISTER2 (address = 0x02)* for FC13[4:0] and FC2[5:0] bits), a comparator monitors the actual battery voltage and stops the ramp-up sequence when the droop exceeds the limit. See *Functional Block Diagram* and Figure 32.

The battery voltage droop monitor feature is automatically disabled during a Tx-MASK event.

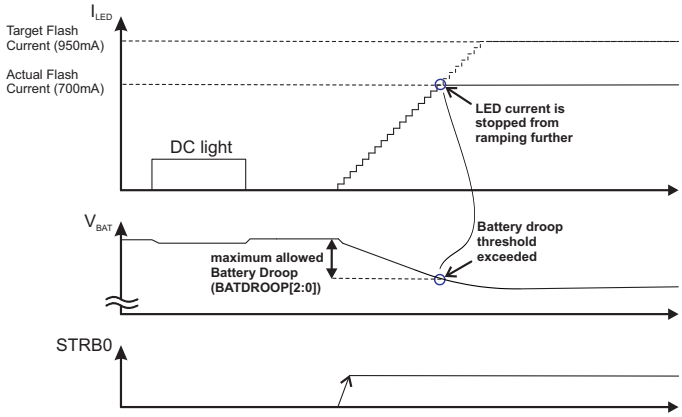


Figure 32. Battery Voltage Droop Monitoring and LED Current Control Principle (STRB1 = 0, Tx-Base = 1)

9.3.2.5 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from error conditions at low input voltages. It prevents the converter from turning on the switch MOSFET, or rectifier MOSFET for battery voltages below 2.3 V. The I^2C compatible interface is fully functional down to 2.1-V input voltage.

9.3.2.6 Hot Die Detection and Thermal Shutdown

The TPS6131x device offers two levels of die temperature monitoring and protection, which are hot die detection and thermal shutdown functionality. The hot die detector (HOTDIE[1:0] bits) reflects the instantaneous junction temperature. This functionality is always enabled except when the device is in shutdown mode.

The hot die detector monitors the junction temperature but does not shut down the device. It provides an early warning to the camera engine to avoid excessive power dissipation thus preventing from thermal shutdown during the next high-power flash strobe.

As soon as the junction temperature T_J exceeds 160°C typical, the device goes into thermal shutdown. In this mode, the power stage and the low-side current regulators are turned off, the HOTDIE[1:0] bits are set and can only be reset by a read access. In the voltage mode operation (MODE_CTRL[1:0] = 11 or ENVM = 1), the device continues its operation when the junction temperature falls below 140°C typical again. In the current regulation mode, video light or flash modes, device operation is suspended.

Table 4. Die Temperature Bits

HOTDIE[1:0]	JUNCTION TEMPERATURE
00	<55°C
01	55°C ≤ T_J ≤ 70°C
10	>70°C
11	Thermal shutdown tripped. The bit is reset after read access

9.3.2.7 Current Limit

The TPS6131x devices employ a programmable inductor current limit. This allows choosing inductors with different saturation current ratings. Furthermore, this provides protection against a shorted inductor, or if the inductance value dramatically drops. This protects the battery from excessively high current drain.

The current limit circuit employs a valley current sensing scheme. The detection threshold is user selectable through the ILIM bit. The ILIM bit can only be set before entering operation, during initial shutdown state.

Figure 33 illustrates the inductor and rectifier current waveforms during current limit operation. The output current, IOUT, is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off time is lengthened to allow the current to decrease to this threshold before the next ON time begins (so called frequency foldback mechanism).

Both the output voltage and the switching frequency are reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit operation, can be defined as:

$$I_{OUT(CL)} = (1 - D) \times \left(I_{VALLEY} + \frac{1}{2} \Delta I_L\right) \text{ with } \Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \text{ and } D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

The TPS6131x device also provides a negative current limit (≈ 300 mA) to prevent an excessive reverse inductor current when the power stage sinks current from the output in the forced continuous conduction mode.

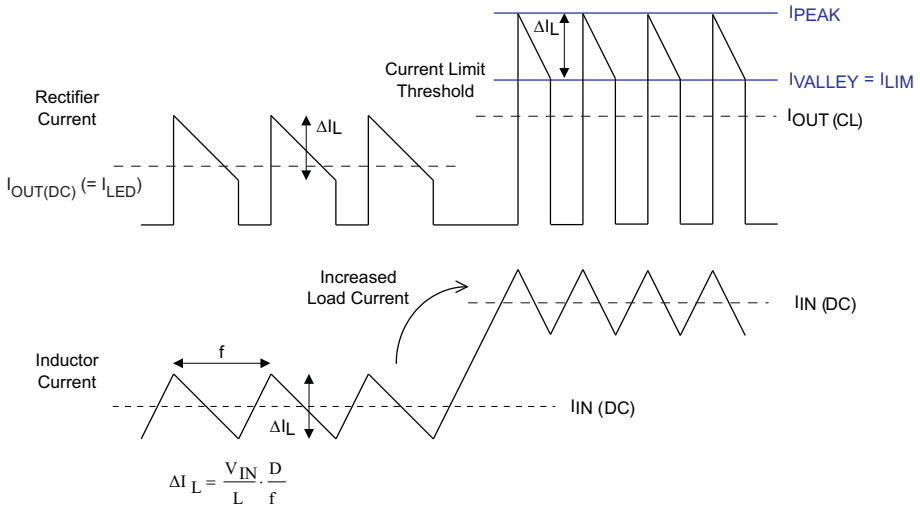


Figure 33. Inductor and Rectifier Currents in Current Limit Operation

Table 5. Inductor Current Limit Operation

CURRENT LIMIT SETTING		ILIM BIT
TPS61310	TPS61311	
1250 mA	1800 mA	Low
1750 mA	2480 mA	High

9.3.2.8 Flash Blanking (Tx-Mask) for Instantaneous Flash Current Reduction

The TPS6131x devices offer a dedicated hardware signal input (Tx-Mask) that can be used to reduce the flash current to the programmed video light level instantaneously.

This feature can be used to reduce the overall current drawn from the battery if other system components require high energy simultaneously, such as during a RF PA transmission pulse.

The Tx-MASK function has no influence on the safety timer duration.

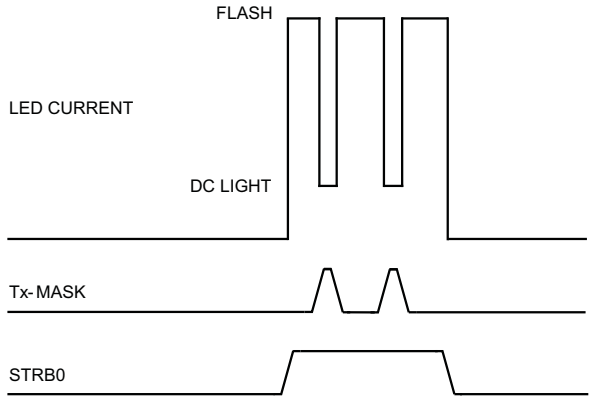


Figure 34. Synchronized Flash With Blanking Periods (STRB1 = 0)

9.3.3 Start-Up Sequence

To avoid high inrush current during start-up, control the inrush current. When the device enables, the internal start-up cycle starts with the first step, the precharge phase.

During precharge, the rectifying switch is turned on until the output capacitor is either charged to a value close to the input voltage or ≈ 3.3 V, whichever occurs first. The rectifying switch is current limited during that phase. The current limit increases with decreasing input-to-output voltage difference. This circuit also limits the output current under output short-circuit conditions.

After precharging the output capacitor, the device starts switching, and increases its current limit in three steps of typically 25 mA, 250 mA and full current limit (ILIM setting). The current limit transition from the first to the second step occurs after 1 ms of operation. Full current limit operation is set once the output voltage reaches its regulation limits. In this mode, the active balancing circuit is disabled.

9.3.4 NRESET Input: Hardware Enable or Disable

The TPS6131x family features a hardware reset pin (NRESET). This reset pin allows the device to be disabled by an external controller without requiring an I^2C write command. Under normal operation, the NRESET pin must be held high to prevent an unwanted reset. When the NRESET is driven low, the I^2C control interface and all internal control registers are reset to the default states and the part enters shutdown mode.

9.3.5 Serial Interface Description

I²C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors [1]. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives or transmits data on the bus under control of the master device.

The TPS6131x device works as a *slave* and supports these data transfer *modes*, as defined in the I²C Bus Specification: standard mode (100 kbps) and fast mode (400 kbps), and high-speed mode (3.4 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.1 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as H/S-mode. The TPS6131x device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is defined as 011 0011.

9.3.5.1 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 35. All I²C-compatible devices must recognize a start condition.

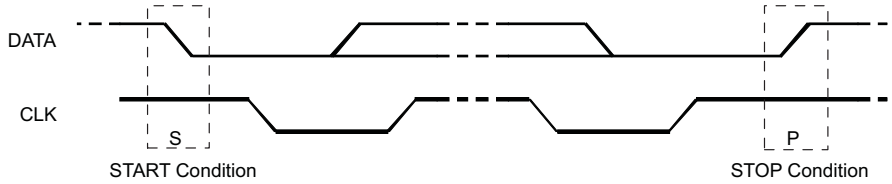


Figure 35. Start and Stop Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read or write direction bit (R/W) on the SDA line. During all transmissions, the master checks for valid data. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 36). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 37) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

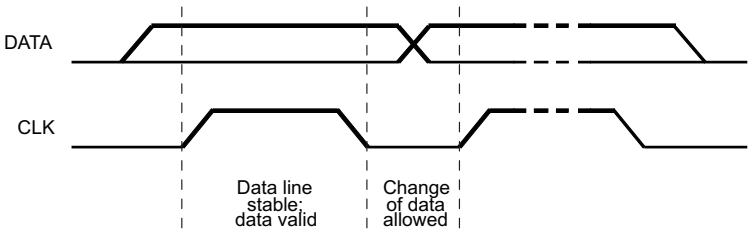


Figure 36. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver must to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 35). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

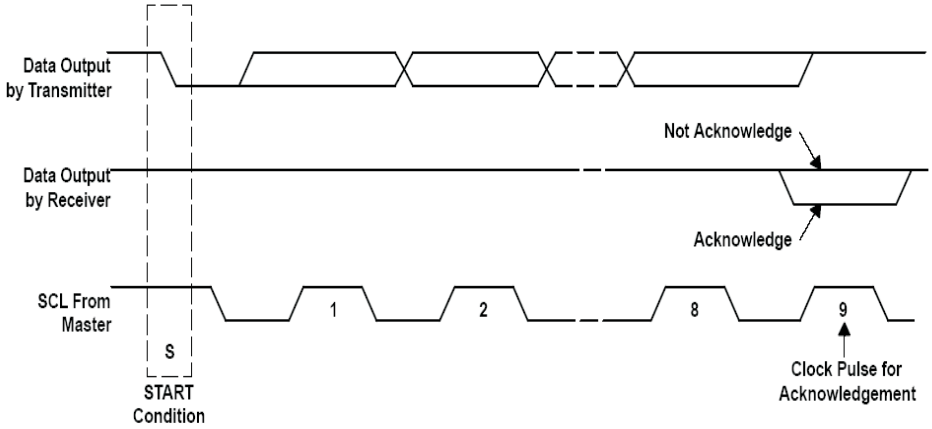


Figure 37. Acknowledge on the I^2C Bus

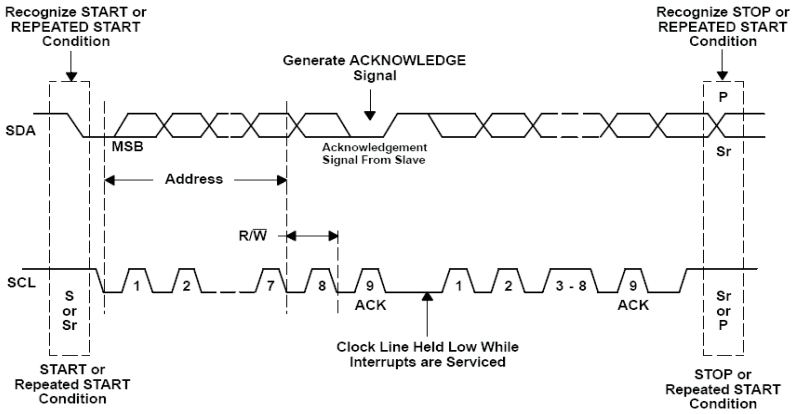


Figure 38. Bus Protocol

9.3.5.2 H/S-Mode Protocol

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the H/S-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in H/S-mode.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

9.3.5.3 TPS6131x I^2C Update Sequence

The TPS6131x requires a start condition, a valid I^2C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS6131x device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^2C address selects the TPS6131x. TPS6131x performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

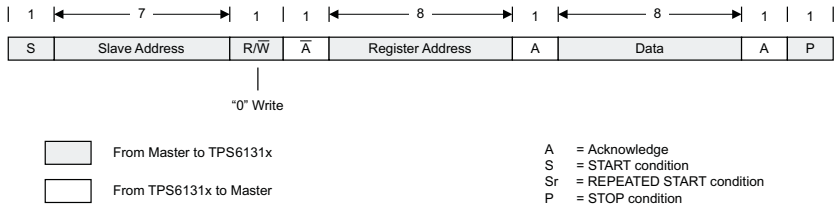


Figure 39. : *Write* Data Transfer Format in F/S-Mode

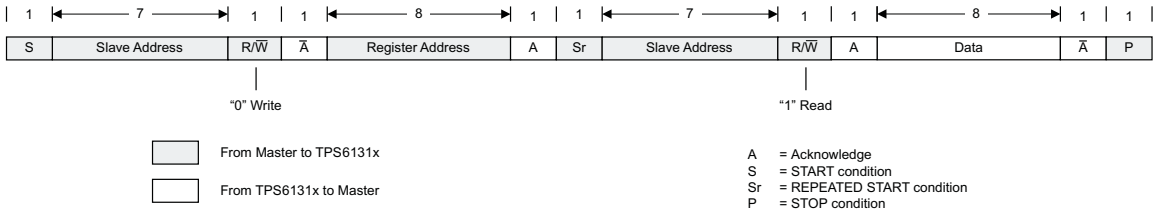


Figure 40. *Read* Data Transfer Format in F/S-Mode

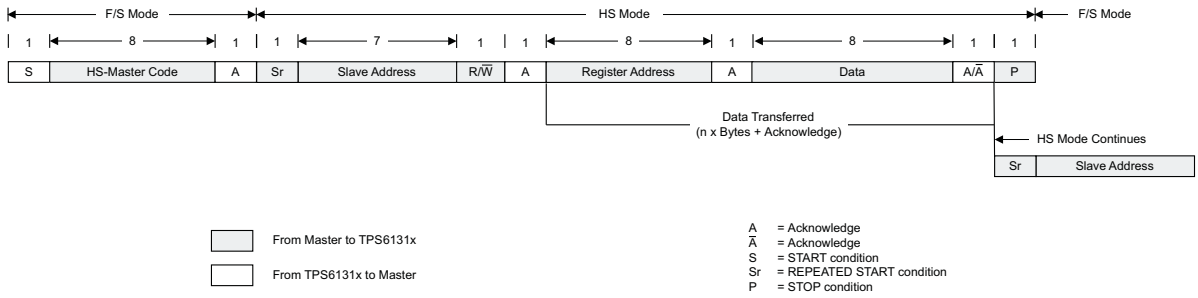


Figure 41. Data Transfer Format in H/S-Mode

9.3.5.4 Slave Address Byte

MSB							LSB
X	X	X	X	X	X	A1	A0

The slave address byte is the first byte received following the START condition from the master device.

9.3.5.5 Register Address Byte

MSB							LSB
0	0	0	0	00	D2	D1	D0

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TPS6131x, which contains the address of the register to be accessed.

9.3.6 LED Forward Voltage Calibration

High-power LEDs tend to exhibit a wide forward voltage distribution. The TPS6131x device integrates a self-calibration procedure that can be used to determine the actually LED forward voltage. The LED forward voltage *in situ* characterization can be performed at camera engine production test. This data can help to estimate more precisely the actual LED electrical power versus flash current.

This calibration procedure is meant to start at a minimum output voltage, and can be initiated by writing the SELFCAL bit (preferably with MODE_CTRL[1:0] = 00, ENVM = 0). The calibration procedure monitors the sense voltage across the low-side current regulators (according to ENLED[3:1] bits setting) and registers the worst case LED, the LED featuring the largest forward voltage. The TPS6131x device automatically sweeps through its output voltage range and performs a short duration flash strobe for each step (see *REGISTER1 (address = 0x01)* and *REGISTER2 (address = 0x02)* for FC13[4:0] and FC2[5:0] bits settings).

The sequence is stopped as soon as the device detects that each of the low-side current regulators have enough headroom voltage (400 mV typical). The device returns the according output voltage in the register OV[3:0] and sets the SELFCAL bit. This bit is only being reset at the start or restart of a calibration cycle. In other words, when SELFCAL is asserted the output voltage register (OV[3:0]) returns the result of the last calibration sequence.

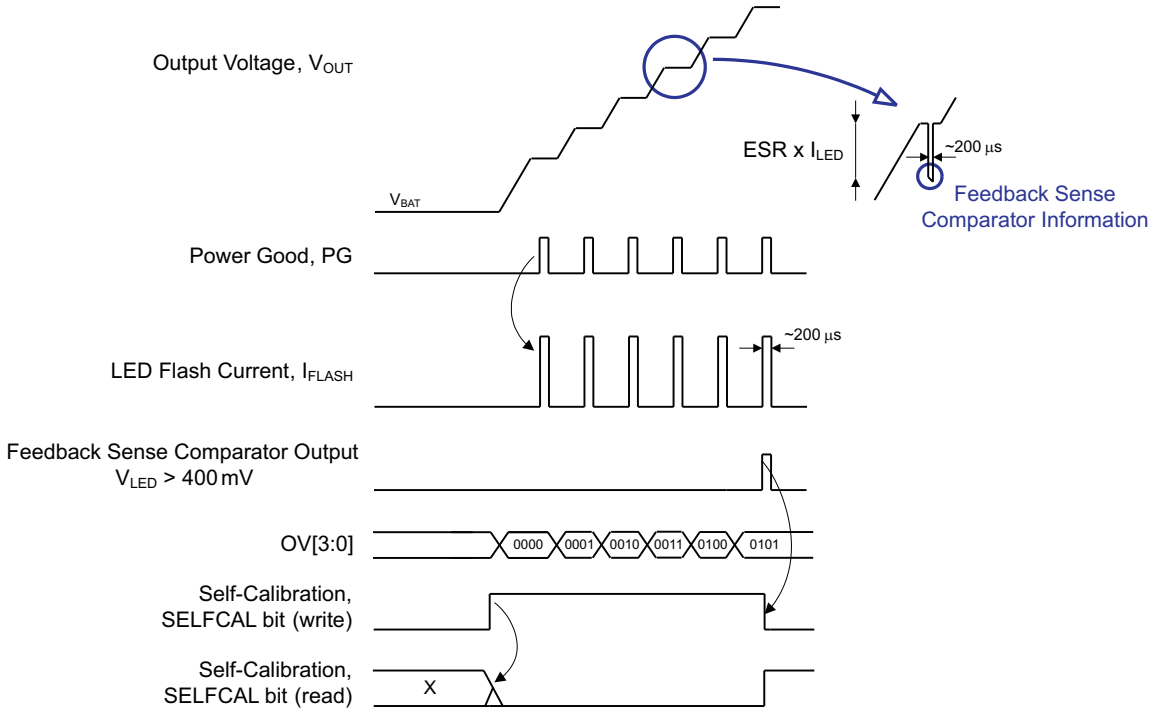


Figure 42. LED Forward Voltage Calibration Principle

9.4 Device Functional Modes

9.4.1 Video Light and Flash Strobe Operation

The TPS6131x devices drive one, two or three LEDs for video light and flash application. The video light and flash operation can either be triggered by an I^2C software command or by means of dedicated, zero latency hardware signals.

9.4.1.1 LED Hardware Setup

The TPS6131x device uses LED forward-voltage sensing circuitry on LED1, LED2, and LED3 pins to optimize the power-stage boost ratio for maximum efficiency. Due to the nature of the sensing circuitry, TI does not recommend leaving any of the LED1, LED2, and LED3 pins unused if the operation is selected through ENLED[3:1] bits. Leaving LED1, LED2, and LED3 pins unconnected, while the respective ENLEDx bits have been set, forces the control loop into high gain, and eventually trips the output overvoltage protection. Figure 43 shows the recommended LED setup for a single, dual or triple-LED application.

Device Functional Modes (continued)

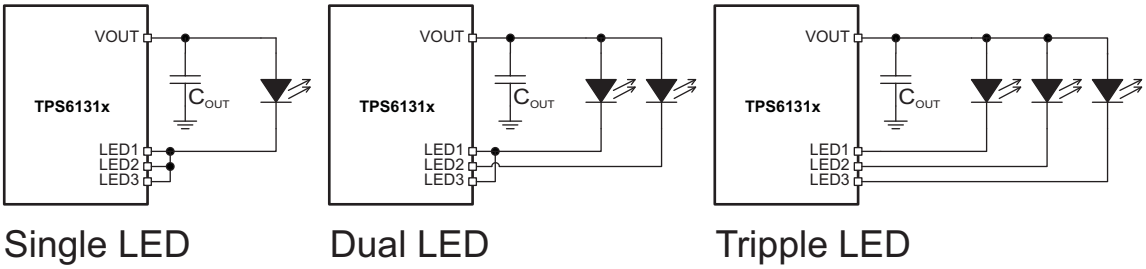


Figure 43. White LED Hardware Setup Options

The LED1, LED2, and LED3 inputs may be connected together to drive one or two LEDs at higher currents. Connecting the current sink inputs in parallel does not affect the internal operation of the TPS6131x. For best operation, TI recommends disabling the LED inputs that are not connected. (see the ENLED[3:1] bits description in *REGISTER5 (address = 0x05)*).

The video light currents are individually programmed through the video light control bits DCL13[2:0] and DCL2[2:0] , the flash currents through FC2[5:0] and FC13[4:0] bits accordingly. If, for single or dual LED application as shown in Figure 43, current sinks are connected to each other and enabled, the resulting video or flash current is the sum of the programmed currents.

9.4.1.2 Triggering Video Light and Flash

For most flexible system integration, the TPS6131x offers several options for activating the video light and flash. Depending on the settings of the MODE_CTRL[1:0] bits, the device can enter different modes of operation. It offers the option of triggering the video light and flash through hardware signals (STRB0, STRB1) or software I^2C command. The flash-signal hardware trigger can be on the leading-edge, turning on for the programmed flash on time, or level sensitive, turning on for as long as the signal is logic high.

The TPS6131x flash timer is programmed through the STIM[2:0] and SELSTIM bits. If the flash is fired by a rising-edge trigger or by an I^2C command, the timer defines the flash duration. If the flash is fired by a level-sensitive trigger, the timer defines the maximum flash ON duration, and overrides the hardware signal if the programmed on-time is exceeded.

For video lighting, a watchdog timer is implemented; this must be refreshed within 13 seconds. This function can be disabled, as described in Table 6.

Table 6. Mode Operations for Video Light and Flash

MODE_CTRL SETTING	DESCRIPTION
MODE_CTRL[1:0] = 01	The STRB0, STRB1 inputs are disabled. The device regulates the LED current in video light mode (DCLC bits) regardless of the STRB0, STRB1 inputs and the START_FLASH/TIMER (SFT) bit. To avoid device shutdown because of the video light safety timeout, MODE_CTRL[1:0] must be refreshed within less than 13 seconds (STRB1 = 0). The video light watchdog timer can be disabled by pulling the STRB1 signal high.
MODE_CTRL[1:0] = 10	The STRB0, STRB1 inputs are enabled. The flash pulse can be triggered by these synchronization signals, or by a software command (START_FLASH/TIMER (SFT) bit). The LEDs are enabled or disabled according to the STRB0, STRB1 input. The flash safety timer is activated, and the video light watchdog timer is disabled.

The dual-wire camera-module interface STRB0 and STRB1 inputs are used for selecting the video light (STRB1 = 1) or flash (STRB1 = 0) mode. The STRB0 signal then triggers the video light or flash, depending on the state of STRB1. The STT bit defines if the flash trigger is level sensitive (STT = 0), or fired on the rising edge (STT = 1).

9.4.1.3 Level-Sensitive Flash Trigger (STT = 0)

In this mode, the high-power LEDs are driven at the flash current level and the safety timer (STIM) is running. The maximum duration of the flash pulse is defined in the STIM[2:0] register.

The safety timer is triggered on rising edge and stopped by a negative logic on the synchronization source (STRB0, STRB1 = 0) or by a timeout event (TO bit).

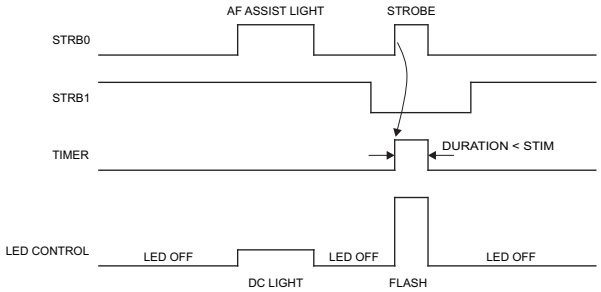


Figure 44. Hardware Synchronized Video Light and Flash Strobe

9.4.1.4 Rising-Edge Flash Trigger (STT = 1)

In this mode, the high-power LEDs are driven at the flash current level and the safety timer (STIM) is running. The duration of the flash pulse is defined in the STIM[2:0] register.

The flash strobe is started either by a rising edge on the synchronization source (STRB0 = 1, STRB1 = 0) or by a positive transition on the START-FLASH/TIMER (SFT) bit (STRB0 = 1, STRB1 = 0). Once running, the timer ignores all kind of triggering signals and only stops after a timeout (TO). START-FLASH/TIMER (SFT) bit is being reset by the timeout (TO) signal.

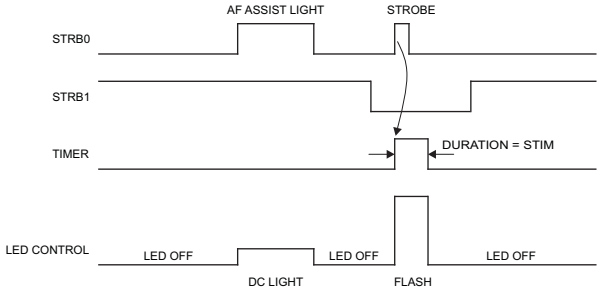


Figure 45. Edge Sensitive Timer (Single Trigger Event)

9.4.2 Voltage Mode

In this mode, the TPS6131x operates as a standard voltage-boost regulator, featuring power-save mode for improved efficiency under light loads. The voltage-mode operation is enabled by software control by setting the mode-control bit MODE_CTRL[1:0] = 11. The device regulates a constant output voltage according to the OV[3:0] bit settings (from 3.825 V to 5.7 V in 125-mV steps). In voltage mode, the LED current sinks LED1, LED2, and LED3 are turned off.

The TPS6131x integrates a software control bit (ENVM bit) that can be used to force the converter to run in voltage mode. This enables the converter to operate at a fixed programmed output voltage (according to the OV[3:0] settings) while operating the LEDs.

Table 7 provides an overview of the different voltage mode variations.

Table 7. Voltage Mode Description

INTERNAL REGISTER SETTINGS MODE_CTRL[1:0]	ENVM BIT	OPERATING MODES
11	0	LEDs are turned off and the converter operate in voltage-regulation mode (VM); the output voltage is set through register OV[3:0].
00	1	
01	1	The converter operates in voltage-regulation mode (VM); the output voltage is set through the register OV[3:0]. The LEDs are turned on for video light operation and the energy is being directly transferred from the battery to the output. The LED currents are regulated by the means of the low-side current sinks.
10	1	The converter operates in the voltage-regulation mode (VM); the output voltage is set through the register OV[3:0]. The LED currents are regulated by the low-side current sinks. The LEDs are ready for flash operation.
11	1	LEDs are turned off and the converter operates in the voltage regulation mode (VM); the output voltage is set through the register OV[3:0].

9.4.2.1 Down Mode in Voltage Mode Operation

In general, a boost converter only regulates output voltages which are higher than the input voltage. The TPS6131x can regulate 4.2 V at the output with an input voltage as high as 5.5 V. To control these applications properly, a down-conversion mode is implemented.

In voltage-regulation mode, if the input voltage reaches or exceeds the output voltage, the converter changes to down-conversion mode. In this mode, the control circuit changes the behavior of the rectifying PMOS. It sets the voltage drop across the PMOS as high as required to regulate the output voltage. This increases the power losses in the converter, and must be considered for thermal design. The down-conversion mode is automatically turned off as soon as the input voltage falls to approximately 200 mV below the output voltage.

For proper operation in down-conversion mode the output voltage must not be programmed higher than approximately 5.3 V. Take care not to violate the absolute maximum ratings at the SW pins.

9.4.2.2 Power Good Indication

The TPS6131x integrates a Power Good circuit that is activated when the device operates in voltage-regulation mode (MODE_CTRL[1:0] = 11 or ENVM = 1). In shutdown mode (MODE_CTRL[1:0] = 00, ENVM = 0), the GPIO/PG pin state is defined below, according to the GPIOTYPE bit:

Table 8. GPIO/PG State in Shutdown

GPIOTYPE	GPIO/PG SHUTDOWN STATE
0	Reset or pulled to ground
1	Open-drain

Depending on the GPIO/PG output stage type selection, push-pull or open-drain, the polarity of the Power Good output signal (PG) can be inverted or not. The Power Good software bit and hardware signal polarity is defined below:

Table 9. Power Good Signal Polarity

GPIOTYPE	PG BIT	GPIO/PG OUTPUT PORT	COMMENTS
0: push-pull output	0	0	Output is active-high
	1	1	
1: open-drain output	0	Open-drain	Output is active-low
	1	Low	

The Power Good signal is true when the output voltage is from –1.5% to 2.5% of its nominal value. Conversely, it is false when the voltage-mode operation is suspended (MODE_CTRL[1:0] ≠ 11 and ENVM = 0).

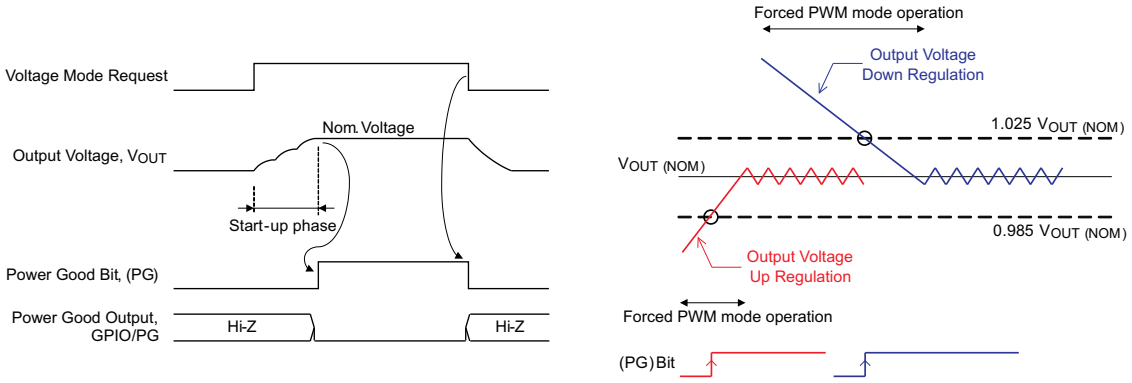


Figure 46. Power Good Operation (DIR = 1, GPIOTYPE = 1)

The TPS6131x device uses a control architecture that *recycles* excess energy that might be stored in the output capacitor. By reversing the operation of the boost power stage, the converter is capable of transferring energy from its output back into the input source. In this case, the Power Good signal is deasserted while the output voltage is decreasing towards its target value, the closest fit voltage the converter can support.

9.4.3 Power-Save Mode Operation, Efficiency

The TPS6131x integrates a power-save mode to improve efficiency under light loads. In power-save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one to several pulses and returns to power-save mode once the output voltage exceeds the set threshold voltage.

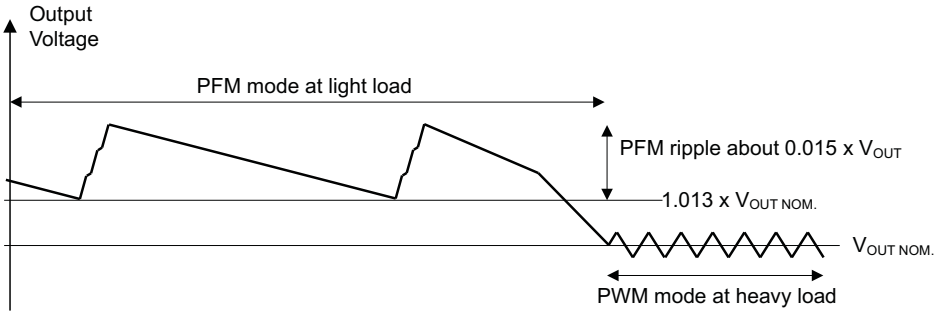


Figure 47. Operation in PFM Mode and Transfer to PWM Mode

The power-save mode can be enabled and disabled through the ENPSM bit. In down conversion mode, power-save mode is always active and the device cannot be forced into fixed frequency operation at light loads.

The LED sense voltage has a direct effect on converter efficiency. Because the voltage across the low-side current regulator does not contribute to the output power (LED brightness), the lower the sense voltage the higher the efficiency is.

The integrated current control loop automatically selects the minimum boost ratio to maintain regulation based on the LED forward voltage and current requirements. The low-side current regulators drop the voltage difference between the input voltage and the LEDs forward voltage ($V_{F(LED)} < V_{IN}$). When running in boost mode ($V_{F(LED)} > V_{IN}$), the voltage present at the LED1, LED2, and LED3 pins of the low-side current regulators is typically 400 mV, leading to high power conversion efficiency. Depending on the input voltage and the LEDs forward voltage characteristic the converter efficiency is approximately 75% to 90%.

9.4.4 Shutdown

Writing 00 to MODE_CTRL[1:0] bits forces the device into shutdown. The shutdown state can only be entered when the voltage regulation (ENVM = 0) and light modes are both turned off.

In the shutdown state:

- The regulator stops switching.
- The high-side PMOS disconnects the load from the input.
- The LEDx pins are high impedance thus eliminating any DC conduction path.
- The TPS6131x device actively discharges the output capacitor when it turns off.

9.5 Register Maps

9.5.1 REGISTER0 (address = 0x00)

Figure 48. REGISTER0 Fields

D7	D6	D5	D4	D3	D2	D1	D0
RESET	—	DCLC13[2:0]			DCLC2[2:0]		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. REGISTER0 Field Descriptions

BIT	DESCRIPTION
RESET	**Register Reset bit** 0: Normal operation. 1: Default values are set to all internal registers.
DCLC13[2:0]	**Video Light Current Control bits (LED1 and LED3)** 000: 0 mA(1)(2) 001: 25 mA 010: 50 mA 011: 75 mA 100: 100 mA 101: 125 mA 110: 150 mA 111: 175 mA
DCLC2[2:0]	**Video Light Current Control bits (LED2)** 000: 0 mA(1)(2) 001: 25 mA 010: 50 mA 011: 75 mA 100: 100 mA 101: 125 mA 110: 150 mA, 225 mA current level can be activated simultaneously with Tx-MASK = 1 111: 175 mA, 325 mA current level can be activated simultaneously with Tx-MASK = 1

(1) LEDs are off, V_{OUT} set according to OV[3:0].
(2) When DCLC2[2:0] and DCLC13[2:0] are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV[3:0].

9.5.2 REGISTER1 (address = 0x01)

Figure 49. REGISTER1 Fields

D7	D6	D5	D4	D3	D2	D1	D0
MODE_CTRL[1:0]		FC2[5:0]					
R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. REGISTER1 Field Descriptions

BIT	DESCRIPTION
MODE_CTRL[1:0]	**Mode Control bits** 00: Device in shutdown mode. 01: Device operates in video light mode. 10: Device operates in flash mode. 11: Device operates as constant voltage source. To avoid device shutdown by video light safety timeout, MODE_CTRL[1:0] bits must be refreshed within less than 13 s. Writing to REGISTER1[7:6] automatically updates REGISTER2[7:6].
FC2[5:0]	**Flash Current Control bits (LED2)** 000000: 0 mA(1)(2) 000001: 25 mA 000010: 50 mA 000011: 75 mA 000100: 100 mA 000101: 125 mA 000110: 150 mA 000111: 175 mA 001000: 200 mA 001001: 225 mA 001010: 250 mA 001011: 275 mA 001100: 300 mA 001101: 325 mA 001110: 350 mA 001111: 375 mA 010000: 400 mA 010001: 425 mA 010010: 450 mA 010011: 475 mA 010100: 500 mA 010101: 525 mA 010110: 550 mA 010111: 575 mA 011000: 600 mA 011001: 625 mA 011010: 650 mA 011011: 675 mA 011100: 700 mA 011101: 725 mA 011110: 750 mA 011111: 775 mA 100000 to 111111: 800 mA

(1) LEDs are off, V_{OUT} set according to OV[3:0].
(2) When FC13[4:0] and FC2[5:0] are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV[3:0].

9.5.3 REGISTER2 (address = 0x02)

Figure 50. REGISTER2 Fields

D7	D6	D5	D4	D3	D2	D1	D0
MODE_CTRL[1:0]		ENVM	FC13[4:0]				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. REGISTER2 Field Descriptions

BIT	DESCRIPTION
MODE_CTRL[1:0]	**Mode Control bits** 00: Device in shutdown mode. 01: Device operates in video light mode. 10: Device operates in flash mode. 11: Device operates as constant voltage source. To avoid device shutdown by video light safety timeout, MODE_CTRL[1:0] bits must be refreshed within less than 13 s. Writing to REGISTER2[6:5] automatically updates REGISTER1[6:5].
ENVM	Enable Voltage Mode bit. 0: Normal operation. 1: Forces the device into a constant voltage source. In read mode, the ENVM bit is automatically updated to reflect the logic state of the ENVM input pin.
FC13[4:0]	**Flash Current Control bits (LED1 and LED3)** 00000: 0 mA(1)(2) 00001: 25 mA 00010: 50 mA 00011: 75 mA 00100: 100 mA 00101: 125 mA 00110: 150 mA 00111: 175 mA 01000: 200 mA 01001: 225 mA 01010: 250 mA 01011: 275 mA 01100: 300 mA 01101: 325 mA 01110: 350 mA 01111: 375 mA 10000 to 11111: 400 mA

(1) LEDs are off, V_{OUT} set according to OV[3:0].
(2) When FC13[4:0] and FC2[5:0] are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV[3:0].

9.5.4 REGISTER3 (address = 0x03)

Figure 51. REGISTER3 Fields

D7	D6	D5	D4	D3	D2	D1	D0
STIM[2:0]			HPFL	SELSTIM (W) TO (R)	STT	SFT	Tx-MASK
R/W-1	R/W-1	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. REGISTER3 Field Descriptions

BIT	DESCRIPTION
STIM[2:0]	**Safety Timer bits** **STIM[2:0]** — **RANGE 0** — **RANGE 1** 000 — 68.2 ms — 5.3 ms 001 — 102.2 ms — 10.7 ms 010 — 136.3 ms — 16 ms 011 — 170.4 ms — 21.3 ms 100 — 204.5 ms — 26.6 ms 101 — 340.8 ms — 32 ms 110 — 579.3 ms — 37.3 ms 111 — 852 ms — 71.5 ms
HPFL	**High-Power LED Failure flag** 0: Proper LED operation. 1: LED failed (open or shorted). High-power LED failure flag is reset after readout
SELSTIM	**Safety Timer Selection Range (Write Only)** 0: Safety timer range 0. 1: Safety timer range 1.
TO	**Time-Out Flag (Read Only)** 0: No time-out event occurred. 1: Time-out event occurred. Time-out flag is reset at restart of the safety timer.
STT	**Safety Timer Trigger bit** 0: LED safety timer is level sensitive. 1: LED safety timer is rising edge sensitive. This bit is only valid for MODE_CTRL[1:0] = 10.
SFT	**Start/Flash Timer bit** In write mode, this bit initiates a flash strobe sequence. Notice that this bit is only active when STRB0 input is high. 0: No change in the high-power LED current. 1: High-power LED current ramps to the flash current level. In read mode, this bit indicates the high-power LED status. 0: High-power LEDs are idle. 1: Ongoing high-power LED flash strobe.
Tx-MASK	**Flash Blanking Control bit** In write mode, this bit enables and disables the flash blanking and LED current reduction function. 0: Flash blanking disabled. 1: LED current is reduced to video light level when Tx-MASK input is high. In read mode, this flag indicates whether or not the flash masking input is activated. Tx-MASK flag is reset after readout of the flag. 0: No flash blanking event occurred. 1: Tx-MASK input triggered.

9.5.5 REGISTER4 (address = 0x04)

Figure 52. REGISTER4 Fields

D7	D6	D5	D4	D3	D2	D1	D0
PG	HOTDIE[1:0]		ILIM	INDC[3:0]			
R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. REGISTER4 Field Descriptions

Bit	Description	
PG	**Power Good bit** In write mode, this bit selects the functionality of the GPIO/PG output. 0: PG signal is routed to the GPIO port. 1: GPIO PORT VALUE bit is routed to the GPIO port. In read mode, this bit indicates the output voltage conditions. 0: The converter is not operating within the voltage regulation limits. 1: The output voltage is within its nominal value.	
HOTDIE[1:0]	**Instantaneous Die Temperature bits** 00: T_J < 55°C 01: 55°C < T_J < 70°C 10: T_J > 70°C 11: Thermal shutdown tripped. Indicator flag is reset after readout.	
ILIM	**Inductor Valley Current Limit bit** The ILIM bit can only be set before the device enters operation, during initial shutdown state. **VALLEY CURRENT LIMIT SETTING** / **ILIM BIT SETTING** TPS61310: 1250 mA; TPS61311: 1800 mA; Low TPS61310: 1750 mA; TPS61311: 2480 mA; High	
INDC[3:0]	**Indicator Light Control bits**	
	INDC[3:0]: PRIVACY INDICATOR INDLED CHANNEL	**INDC[3:0]: PRIVACY INDICATOR LED1, LED2, and LED3 CHANNELS**(2)
	0000: Privacy indicator turned off 0001: INDLED current = 2.6 mA(1) 0010: INDLED current = 5.2 mA(1) 0011: INDLED current = 7.9 mA(1) 0100: Privacy indicator turned off 0101: INDLED current = 5.2 mA(1) 0110: INDLED current = 10.4 mA(1) 0111: INDLED current = 15.8 mA (1)	1000: 5% PWM dimming ratio 1001: 11% PWM dimming ratio 1010: 17% PWM dimming ratio 1011: 23% PWM dimming ratio 1100: 30% PWM dimming ratio 1101: 36% PWM dimming ratio 1110: 48% PWM dimming ratio 1111: 67% PWM dimming ratio

(1) The output node (VOUT) is internally pulled to ground.
(2) This mode of operation can only be activated for MODE_CTRL[1:0] = 01 and ENVM = 1.

9.5.6 REGISTER5 (address = 0x05)

Figure 53. REGISTER5 Fields

D7	D6	D5	D4	D3	D2	D1	D0
SELFCAL	ENPSM	DIR (W) STSTRB1 (R)	GPIO	GPIOTYPE	ENLED3	ENLED2	ENLED1
R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. REGISTER5 Field Descriptions

Bit	Description
SELFCAL	**High-Current LED Forward Voltage Self-Calibration Start bit** In write mode, this bit enables and disables the output voltage versus LED forward voltage and current self-calibration procedure. 0: Self-calibration disabled. 1: Self-calibration enabled. In read mode, this bit returns the status of the self-calibration procedure. 0: Self-calibration ongoing 1: Self-calibration done. This bit is only reset at the start or restart of a calibration cycle.
ENPSM	**Enable and Disable Power-Save Mode bit** 0: Power-save mode disabled. 1: Power-save mode enabled.
STSTRB1	**STRB1 Input Status bit (Read Only)** This bit indicates the logic state on the STRB1 state.
DIR	**GPIO Direction bit** 0: GPIO configured as input. 1: GPIO configured as output.
GPIO	**GPIO Port Value** This bit contains the GPIO port value.
GPIOTYPE	**GPIO Port Type** 0: GPIO is configured as push-pull output. 1: GPIO is configured as open-drain output.
ENLED3	**Enable and Disable High-Current LED3 bit** 0: LED3 input is disabled. 1: LED3 input is enabled.
ENLED2	**Enable and Disable High-Current LED2 bit** 0: LED2 input is disabled. 1: LED2 input is enabled.
ENLED1	**Enable and Disable High-Current LED1 bit** 0: LED1 input is disabled. 1: LED1 input is enabled.

9.5.7 REGISTER6 (address = 0x06)

Figure 54. REGISTER6 Fields

D7	D6	D5	D4	D3	D2	D1	D0
ENTS	LEDHOT	LEDWARN	LEDHDR	0V[3:0]			
R/W-0	R/W-0	R-0	R-0	R/W-1	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. REGISTER6 Field Descriptions

Bit	Description
ENTS	**Enable and Disable LED Temperature Monitoring** 0: LED temperature monitoring disabled. 1: LED temperature monitoring enabled.
LEDHOT	**LED Excessive Temperature Flag** This bit can be reset by writing a logic level zero. 0: TS input voltage > 0.345 V. 1: TS input voltage < 0.345 V.
LEDWARN	**LED Temperature Warning Flag (Read Only)** This flag is reset after readout. 0: TS input voltage > 1.05 V. 1: TS input voltage < 1.05 V.
LEDHDR	**LED High-Current Regulator Headroom Voltage Monitoring bit** This bit returns the headroom voltage status of the LED high-current regulators. This value is being updated at the end of a flash strobe, before the LED current ramp-down phase. 0: Low headroom voltage. 1: Sufficient headroom voltage.
0V[3:0]	**Output Voltage Selection bits** In read mode, these bits return the result of the high-current LED forward voltage self-calibration procedure. In write mode, these bits are used to set the target output voltage (see *Down Mode in Voltage Mode Operation* voltage regulation mode). In applications requiring dynamic voltage control, take care to set the new target code after voltage mode operation is enabled (MODE_CTRL[1:0] = 11 or ENVM bit = 1). **OV[3:0]: Target Output Voltage** 0000: 3.825 V 0001: 3.95 V 0010: 4.075 V 0011: 4.2 V 0100: 4.325 V 0101: 4.45 V 0110: 4.575 V 0111: 4.7 V 1000: 4.825 V 1001: 4.95 V 1010: 5.075 V 1011: 5.2 V 1100: 5.325 V 1101: 5.45 V 1110: 5.575 V 1111: 5.7 V

9.5.8 REGISTER7 (address = 0x07)

Figure 55. REGISTER7 Fields

D7	D6	D5	D4	D3	D2	D1	D0
ENBATMON	BATDROOP[2:0]			—	REVID[2:0]		
R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R-1	R-1	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. REGISTER7 Field Descriptions

Bit	Description
ENBATMON	**Enable and Disable Battery Voltage Droop Monitoring Bit** 0: Battery voltage droop monitoring disabled. 1: Battery voltage droop monitoring enabled.
BATDROOP[2:0]	**Battery Voltage Droop** 000: 50 mV 001: 75 mV 010: 100 mV 011: 125 mV 100: 150 mV 101: 175 mV 110: 200 mV 111: 225 mV
REVID[2:0]	**Silicon Revision ID**

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

TPS6131x family is based on a high-efficiency synchronous boost topology, which can drive up to three LEDs in parallel. The power stage is capable of supplying a maximum total current up to 1750 mA for TPS61310 and 2480 mA for TPS61311. The 2-MHz switching frequency allows the use of small and low passive components.

10.2 Typical Applications

10.2.1 2x 600-mA High Power White LED Solution Featuring Privacy Indicator

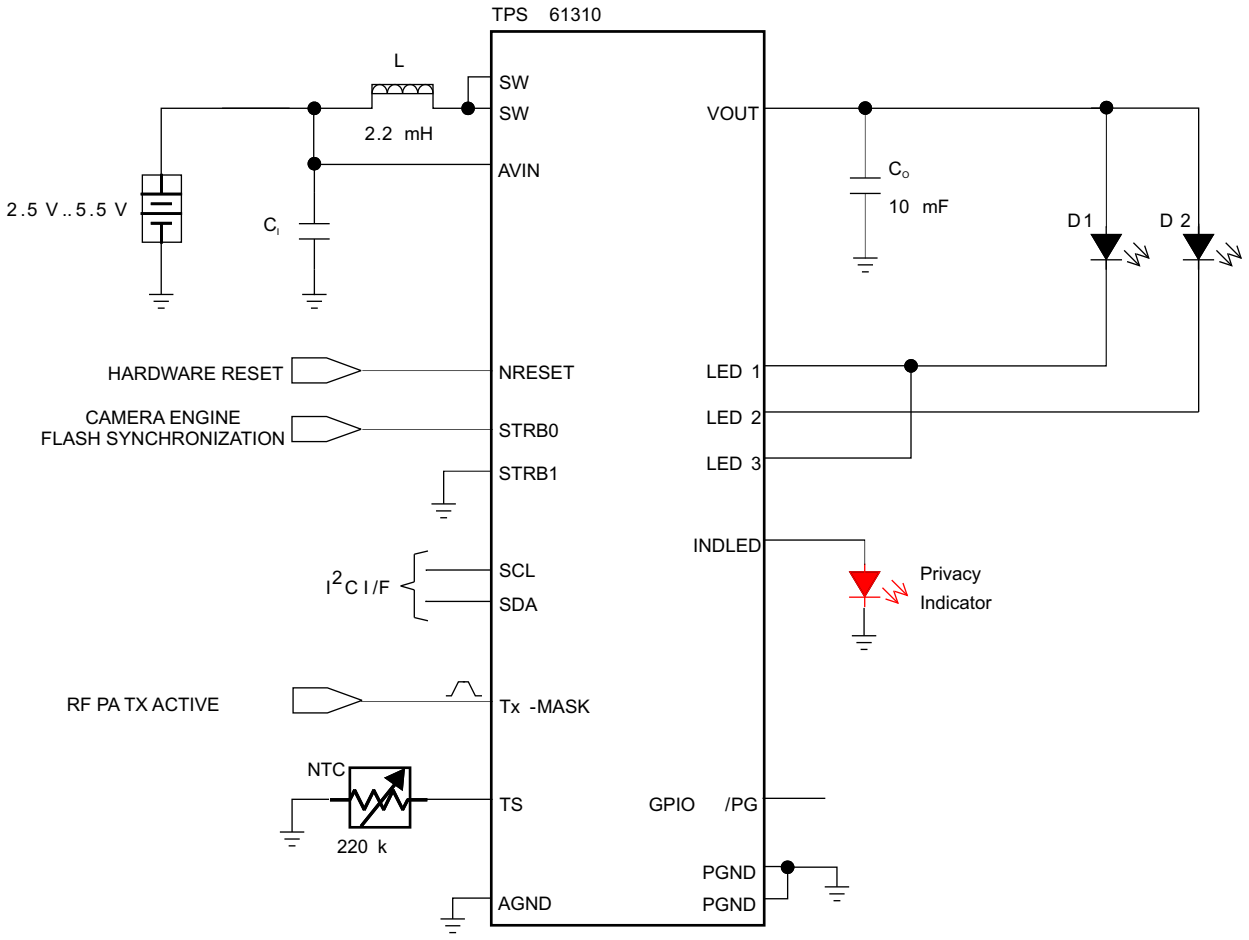


Figure 56. 2x 600-mA High Power White LED Solution Featuring Privacy Indicator

10.2.1.1 Design Requirements

In this design example, different LED current limit is set through I^2C interface, the input voltage is 2.5 V to 5.5 V, output voltage is 4.94 V, operating frequency of 2 MHz.

Typical Applications (continued)

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Inductor Selection

A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required.

The TPS6131x device integrates current-limit protection circuitry. The valley current of the PMOS rectifier is sensed to limit the maximum current flowing through the synchronous rectifier and the inductor. The valley peak current limit (1250 mA or 1750 mA) is user selectable through the I^2C interface.

To optimize solution size the TPS6131x device is designed to operate with inductance values from a minimum of 1.3 µH to a maximum of 2.9 µH. TI recommends a 2.2-µH inductance in typical high-current white LED applications.

The highest peak current through the inductor and the power switch depends on the output load, the input and output voltages. The maximum average inductor current and the maximum inductor peak current can be estimated using Equation 2 and Equation 3:

$$I_L \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}} \tag{2}$$

$$I_{L(PEAK)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1-D) \times \eta} \quad \text{with } D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

where

- f = switching frequency (2 MHz)
- L = inductance value (2.2 µH)
- η = estimated efficiency (85%)

(3)

The losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

10.2.1.2.2 Input Capacitor

For good input-voltage filtering, TI recommends low ESR ceramic capacitors. TI recommends a 10-µF input capacitor to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. The input capacitor must be placed as close as possible to the input pin of the converter.

10.2.1.2.3 Output Capacitor

The major parameter necessary to define the output capacitor is the maximum allowed output-voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance required for the defined ripple, supposing that the ESR is zero, by using Equation 4:

$$C_{min} \approx \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}}$$

where

- f is the switching frequency
- ΔV is the maximum allowed ripple

(4)

With a chosen ripple voltage of 10 mV, a minimum capacitance of 10 µF is required. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 5:

$$\Delta V_{ERR} = I_{OUT} \times R_{ESR} \tag{5}$$

The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. Additional ripple is caused by load transients. This means that the output capacitor must completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change.

Typical Applications (continued)

For the standard current white LED application, a minimum of 3-µF effective output capacitance is usually required when operating with 2.2-µH (typical) inductors. For solution size reasons, this is usually one or more X5R or X7R ceramic capacitors.

Depending on the material, size and therefore margin to the rated voltage of the used output capacitor, degradation on the effective capacitance can be observed. This loss of capacitance is related to the DC bias voltage applied. Therefore, TI recommends checking that the selected capacitors show enough effective capacitance under real operating conditions.

10.2.1.2.4 NTC Selection

The TPS6131x requires a negative thermistor (NTC) for sensing the LED temperature. Once the temperature monitoring feature is activated, a regulated bias current (approximately 24 µA) is driven out of the TS port to produce a voltage across the thermistor.

If the temperature of the NTC-thermistor rises due to the heat dissipated by the LED, the voltage on the TS input pin decreases. When this voltage goes below the *warning threshold*, the LEDWARN bit in REGISTER6 is set. This flag is cleared by reading the register.

If the voltage on the TS input decreases further and falls below *hot threshold*, the LEDHOT bit in REGISTER6 is set and the device goes automatically in shutdown mode to avoid damaging the LED. This status is latched until the LEDHOT flag gets cleared by software.

The selection of the NTC-thermistor value strongly depends on the power dissipated by the LED and all components surrounding the temperature sensor and on the cooling capabilities of each specific application. With a 220-kΩ (at 25°C) thermistor, the valid temperature window is set from 60°C to 90°C. The temperature window can be enlarged by adding external resistors to the TS pin application circuit. To obtain proper triggering of the LEDWARN and LEDHOT flags in noisy environments, the TS signal may require additional filtering capacitance.

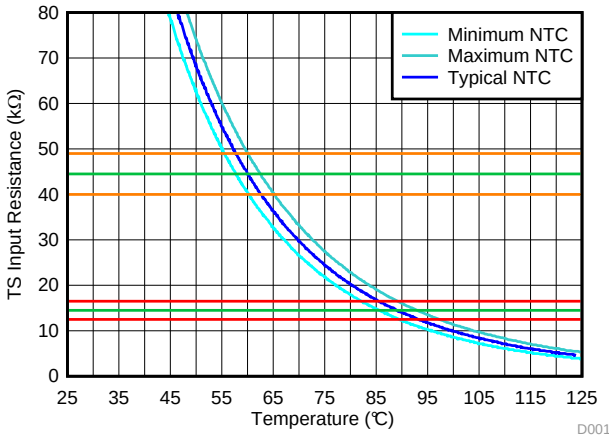


Figure 57. Temperature Monitoring Characteristic

10.2.1.2.5 Checking Loop Stability

The first step of circuit and stability evaluation is to examine these signals from a steady-state perspective:

- Switching node (SW)
- Inductor current (I_L)
- Output ripple voltage ($V_{OUT(AC)}$)

These are the basic signals that must be measured when evaluating a switching converter. If the switching waveform shows large duty-cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of improper board layout or L-C combination.

As a next step in the evaluation of the regulation loop, test the load transient response. VOUT can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. With no ringing, the loop usually has more than 45° of phase margin.

Typical Applications (continued)

Because the damping factor of the circuitry is directly related to several resistive parameters (MOSFET $r_{DS(ON)}$) that are temperature dependant, the loop stability must be analyzed over the input voltage range, output current range, and temperature range.

10.2.1.2.6 LED Flash Current Level Optimization Versus Battery Droop

In cell phone applications, the camera engine is normally specified over an operating temperature down to 0°C or –10°C. To achieve a reliable system operation, the LED flash current must be rated according to the maximum tolerable battery voltage drop, highest battery impedance and lowest ambient temperature.

To dynamically optimize the LED flash current (light output) versus battery state-of-charge and temperature, we could consider the self-adjustment procedure in Figure 58. This algorithm could be embedded into the auto-exposure, auto white-balance, or red-eye reduction pre-flash algorithms.

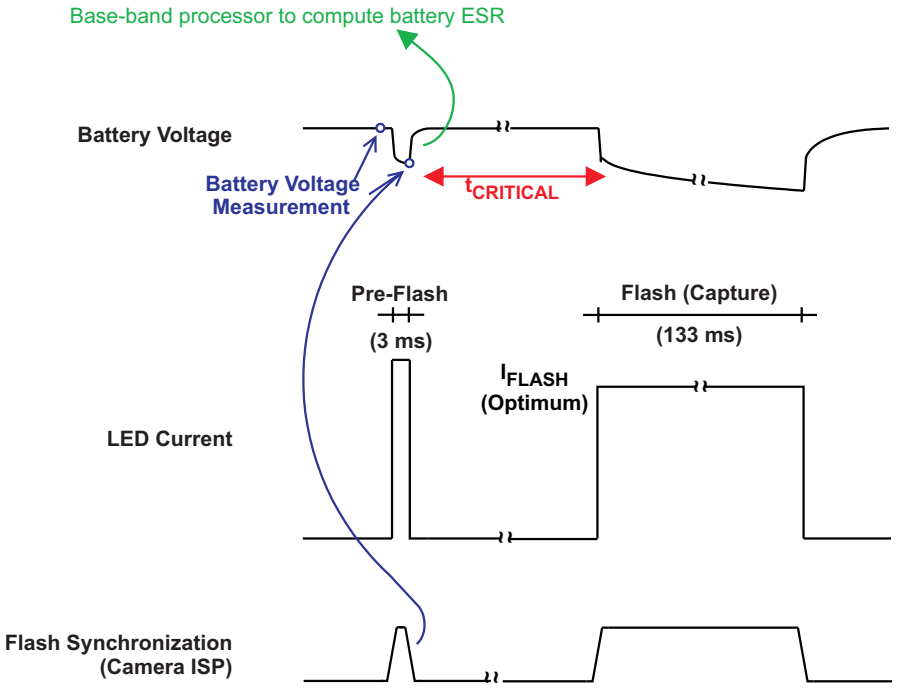


Figure 58. Image Capture Sequence

- **Phase 1: Pre-Flash, Battery Impedance Estimation**

  The battery voltage usually drops by a few hundreds of millivolts during a high-power flash strobe. For short durations, this voltage droop should not be subject to the battery intrinsic capacitance (relaxation effect) but rather to its cell impedance.

  Based on the state of the Tx-MASK input, the battery voltage drop, during pre-flash, and the LED current level, the base-band processor can compute an estimated cell-impedance value (ESR).

  Depending on the ambient temperature, the battery state-of-charge (SoC), the flash (capture) duration and the actual status of the various RF interfaces, the base-band processor can determine a safe battery voltage droop, to be tolerated during the forthcoming strobe sequence, as well as a maximum flash current rating. The maximum flash current setting can be estimated by considering nominal LEDs and approximately 85% power efficiency in the driver.

- **Phase 2: Battery Loading Monitoring Before Image Capture**

  For a reliable system operation, the base-band processor must make sure that no 'parasitic' high-current load suddenly impacts the budgeted battery voltage sag. The most critical timing is referenced as $t_{CRITICAL}$.

  The interrupt subroutine, running on the base-band processor, must be ready to detect any 'parasitic' battery load event that could occur before the image capture (see *REGISTER3 (address = 0x03)* for SFT bit description). In such a situation, the battery voltage droop budget and the maximum LED current settings would need to be revised.

Typical Applications (continued)

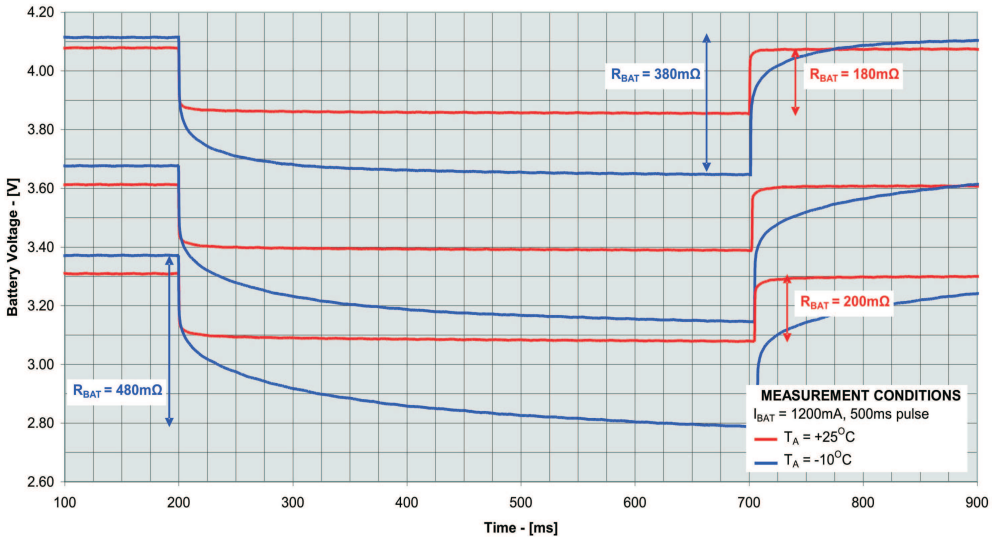
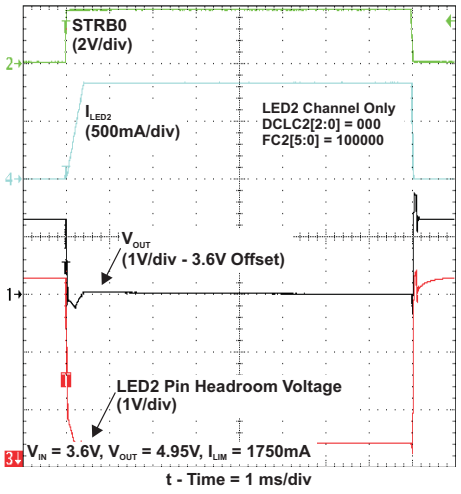


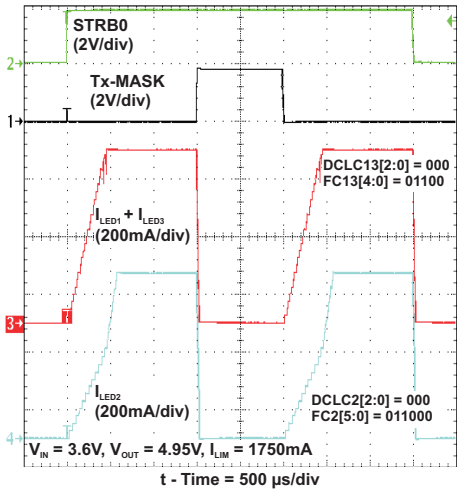
Figure 59. 900-mAh, Li-Ion Battery Transient Response vs SoC and Temperature

10.2.1.3 Application Curves



STRB1 = 0

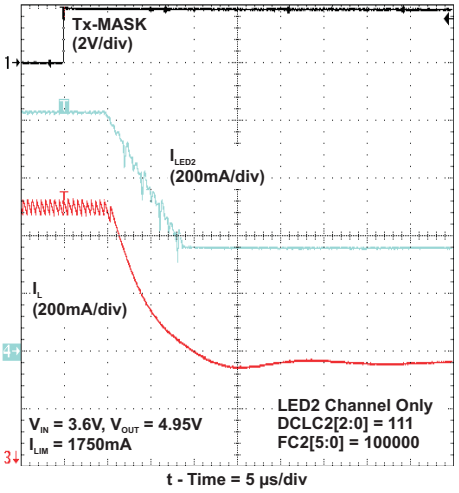
Figure 60. Flash Sequence



STRB1 = 0

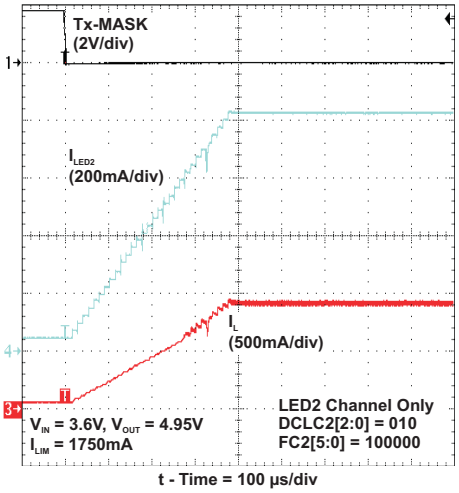
Figure 61. Tx-Masking Operation

Typical Applications (continued)



STRB1 = 0

Figure 62. Tx-Masking Operation



STRB1 = 0

Figure 63. Tx-Masking Operation

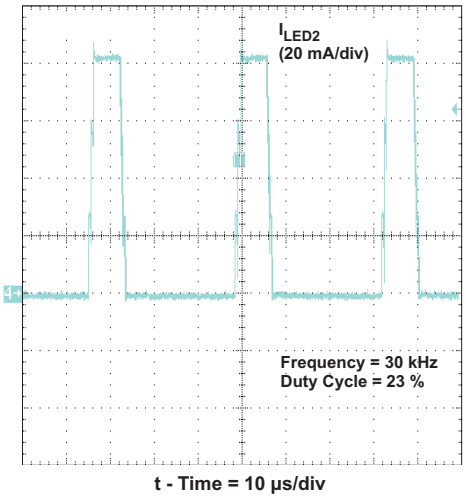


Figure 64. Low-Light Dimming Mode Operation

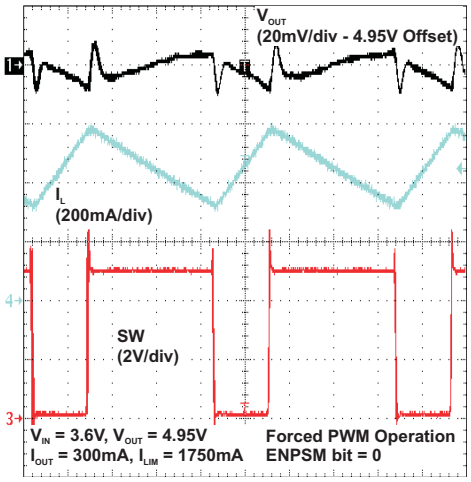


Figure 65. PWM Operation

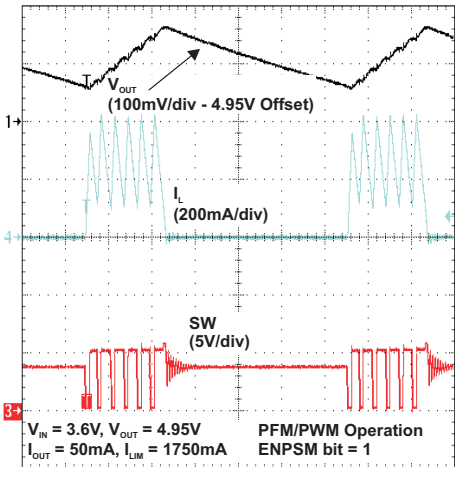


Figure 66. PFM Operation

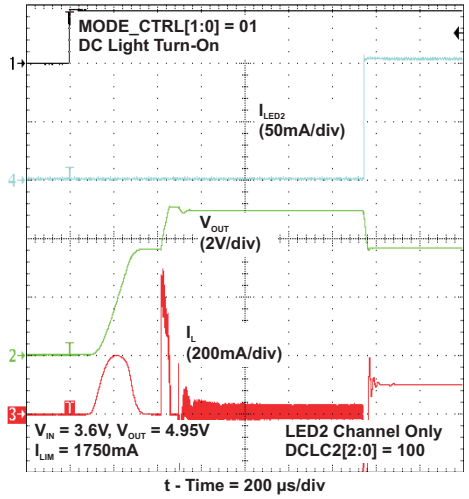


Figure 67. Start-Up Into Video Light Operation

Typical Applications (continued)

10.2.2 1200-mA High Power White LED Solution Featuring Voltage Mode

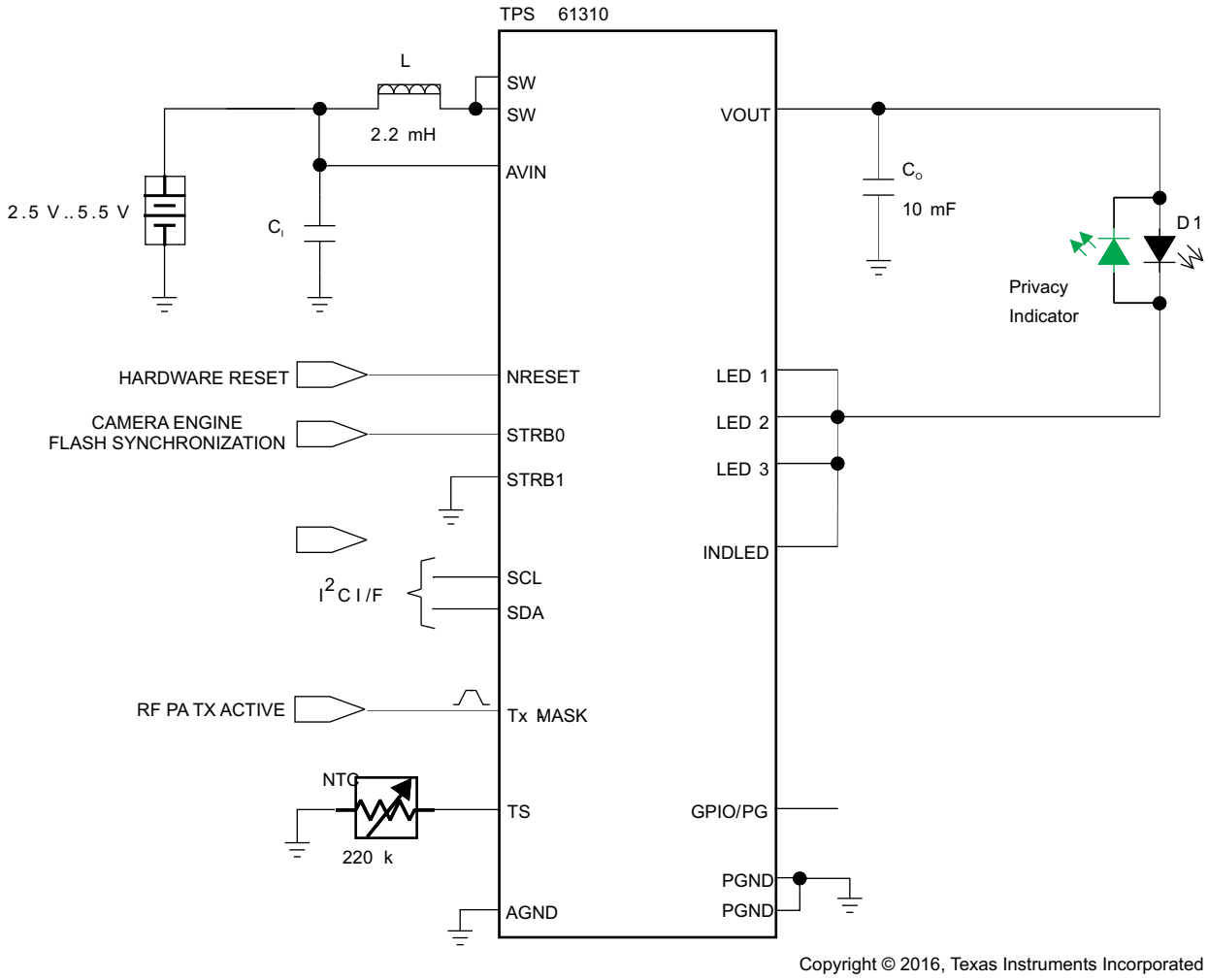


Figure 68. 1200-mA High Power White LED Solution Featuring Voltage Mode

10.2.2.1 Design Requirements

TPS6131x operates in standard voltage-boost regulator by setting mode-control bit MODE_CTRL[1:0] = 11. The LED current sink is turned off in this mode, with V_{IN} = 2.5 V to 5.5 V, V_{OUT} = 4.95 V, operating frequency 2 MHz.

Typical Applications (continued)

10.2.2.2 Application Curves

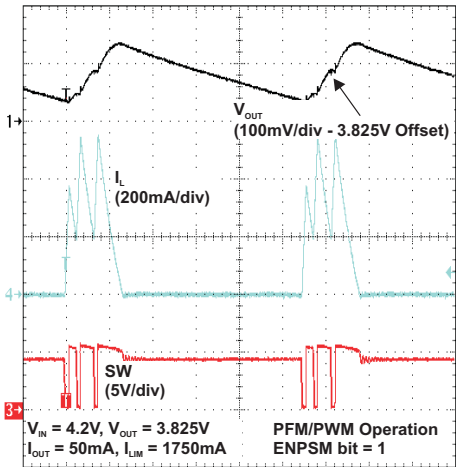


Figure 69. Down-Mode Operation (Voltage Mode)

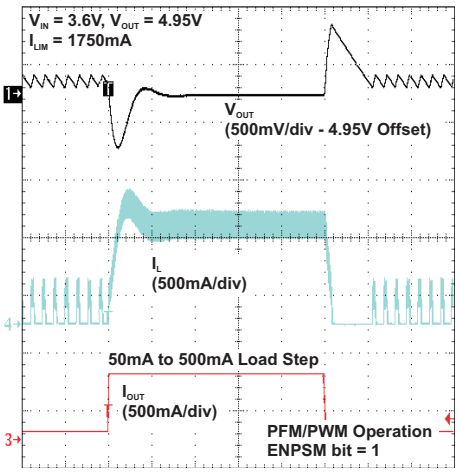


Figure 70. Voltage Mode Load Transient Response

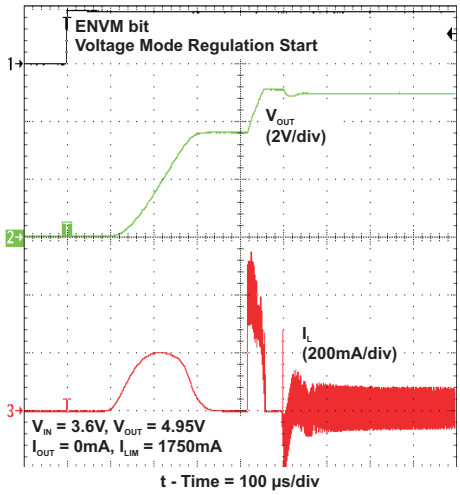


Figure 71. Start-Up Into Voltage Mode Operation

11 Power Supply Recommendations

TPS6131x is designed to operate from an input voltage supply from 2.5 V to 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is placed far from the TPS6131x, additional bulk capacitance may be required to the ceramic bypass capacitors.

12 Layout

12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks.

Layout Guidelines (continued)

The input capacitor, output capacitor, and the inductor must be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

To lay out the control ground, TI recommends using short traces which are separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

12.2 Layout Example

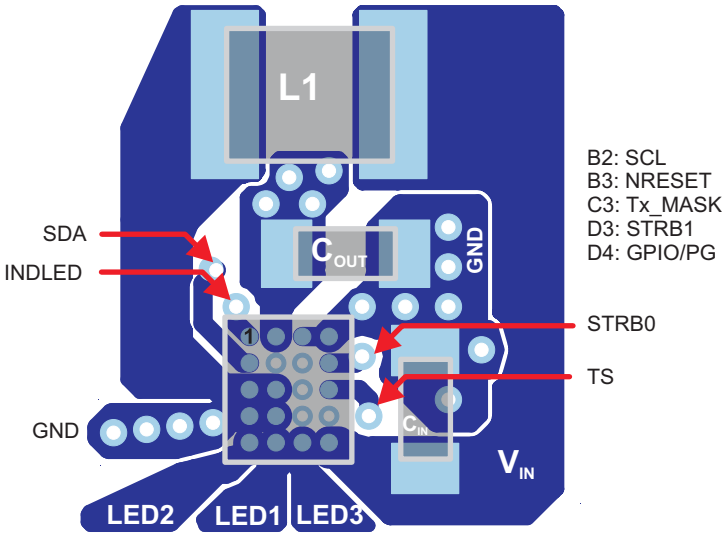


Figure 72. Suggested Layout (Top)

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat generating components affect the power-dissipation limits of a given component.

There are three basic approaches for enhancing thermal performance:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly dependent on application and board layout. In applications where high maximum power dissipation exists, thermal dissipation issues in board design must be considered. The maximum junction temperature (T_J) of the TPS6131x is 150°C.

The maximum power dissipation is especially critical when the device operates in the linear down mode at high LED current. For single-pulse power thermal analysis, such as during a flash strobe, the allowable power dissipation for the device is given by Figure 73. These values are derived using the reference design.

Thermal Considerations (continued)

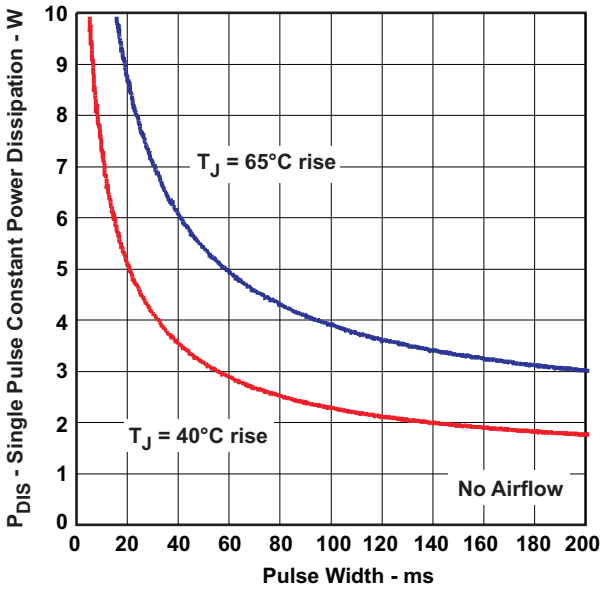


Figure 73. Single Pulse Power Capability

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

UM10204, I²C-Bus Specification and User Manual; (Rev. 6, April 2014),
http://www.nxp.com/documents/user_manual/UM10204.pdf

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 18. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61310	Click here	Click here	Click here	Click here	Click here
TPS61311	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
I²C is a trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61310YFFR	ACTIVE	DSBGA	YFF	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61310	Samples
TPS61310YFFT	ACTIVE	DSBGA	YFF	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61310	Samples
TPS61311YFFR	ACTIVE	DSBGA	YFF	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61311	Samples
TPS61311YFFT	ACTIVE	DSBGA	YFF	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61311	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

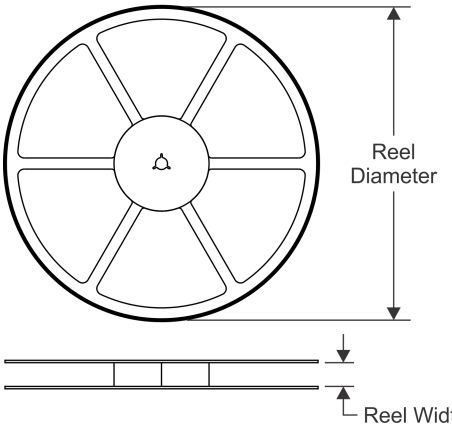
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

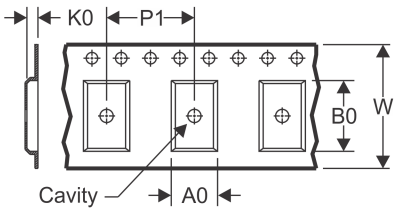
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

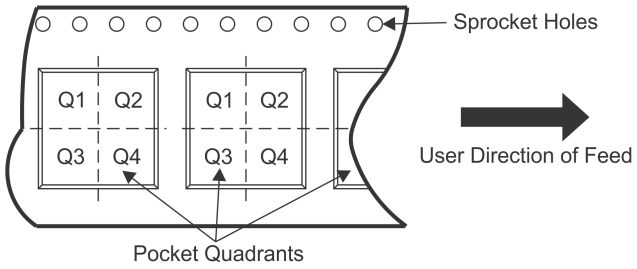


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

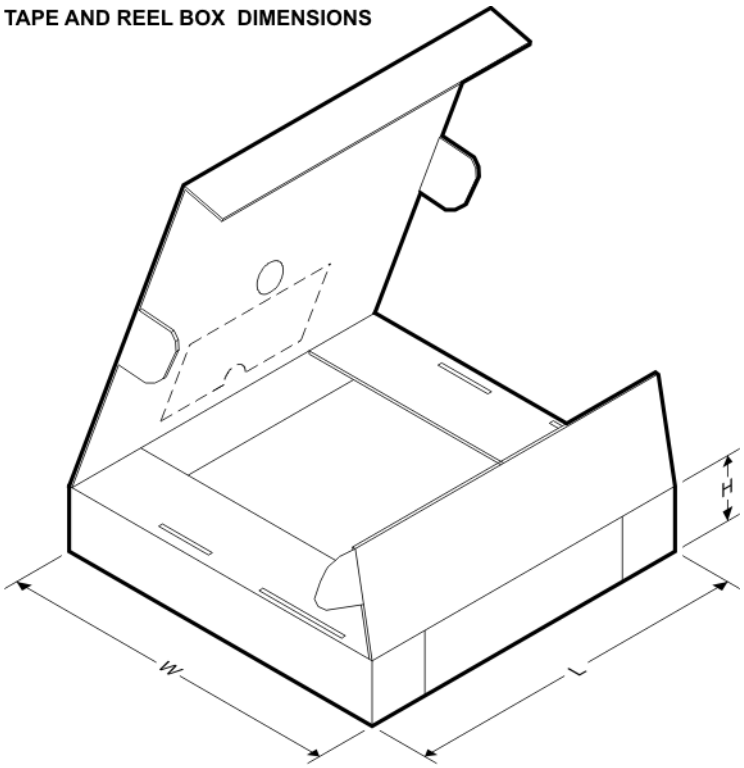
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61310YFFR	DSBGA	YFF	20	3000	180.0	8.4	2.2	2.35	0.8	4.0	8.0	Q1
TPS61310YFFR	DSBGA	YFF	20	3000	178.0	9.2	2.2	2.35	0.8	4.0	8.0	Q1
TPS61310YFFT	DSBGA	YFF	20	250	178.0	9.2	2.2	2.35	0.8	4.0	8.0	Q1
TPS61310YFFT	DSBGA	YFF	20	250	180.0	8.4	2.2	2.35	0.8	4.0	8.0	Q1
TPS61311YFFR	DSBGA	YFF	20	3000	178.0	9.2	2.2	2.35	0.8	4.0	8.0	Q1
TPS61311YFFR	DSBGA	YFF	20	3000	180.0	8.4	2.2	2.35	0.8	4.0	8.0	Q1
TPS61311YFFT	DSBGA	YFF	20	250	180.0	8.4	2.2	2.35	0.8	4.0	8.0	Q1
TPS61311YFFT	DSBGA	YFF	20	250	178.0	9.2	2.2	2.35	0.8	4.0	8.0	Q1

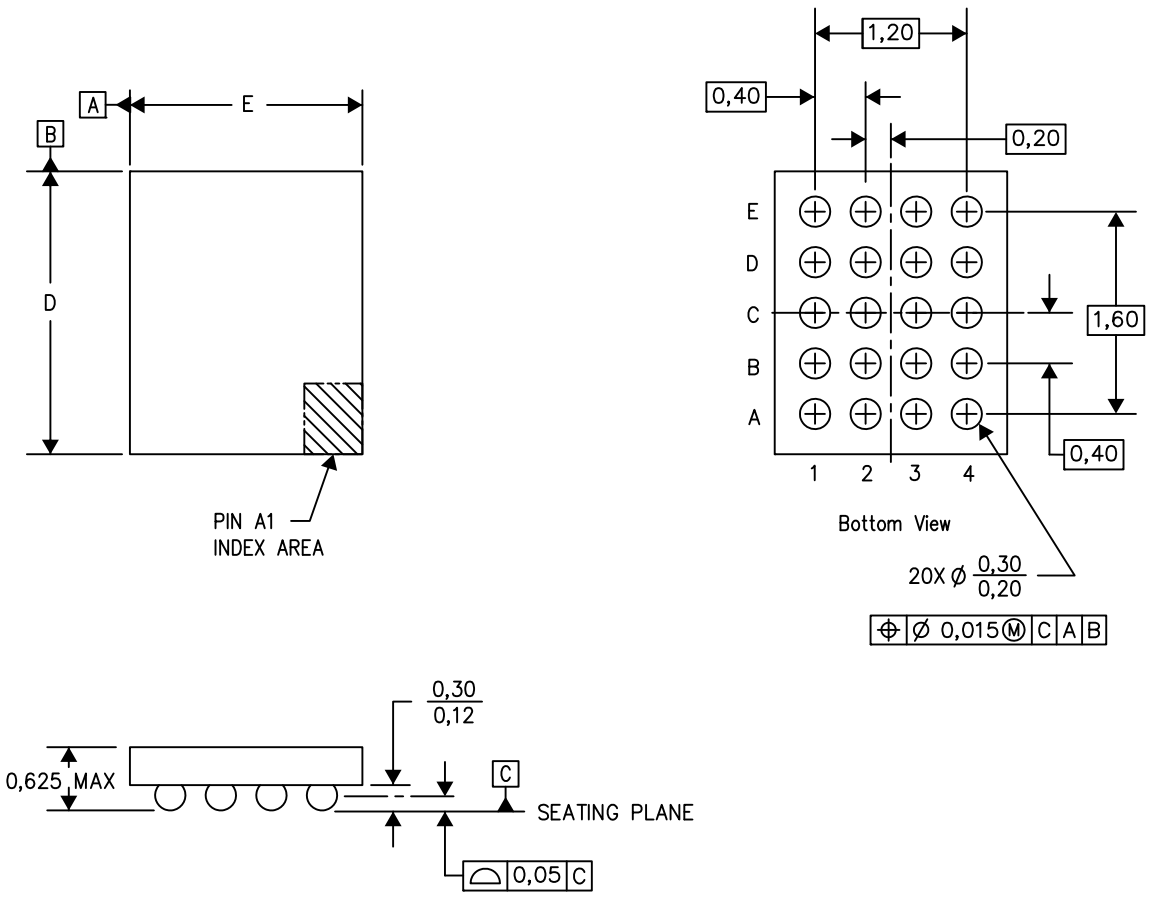
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61310YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS61310YFFR	DSBGA	YFF	20	3000	220.0	220.0	35.0
TPS61310YFFT	DSBGA	YFF	20	250	220.0	220.0	35.0
TPS61310YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0
TPS61311YFFR	DSBGA	YFF	20	3000	220.0	220.0	35.0
TPS61311YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS61311YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0
TPS61311YFFT	DSBGA	YFF	20	250	220.0	220.0	35.0

YFF (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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