DRV8850 Low-Voltage H-Bridge IC With LDO Voltage Regulator

1 Features

- H-Bridge Motor Driver
  - Drives a DC Motor, One Winding of a Stepper Motor, or Other Loads
  - Low MOSFET On-Resistance: 65 mΩ HS + LS at 4.2V, 25°C
- 5-A Continuous 8-A Peak-Drive Current
- Internal Current Sensing With Current Sense Output
- 2 to 5.5-V Operating Supply Voltage Range
- Overvoltage and Undervoltage Lockout
- Low-Power Sleep Mode
- 100-mA Isolated Low-Dropout (LDO) Voltage Regulator
- 24-Pin VQFN Package

2 Applications

- Battery-Operated Applications With High Start-Up Torque, such as:
  - Personal Hygiene (Electric Toothbrushes, Shavers)
  - Toys
  - RC Helicopters and Cars
  - Robotics

3 Description

The DRV8850 device provides a motor driver plus LDO voltage regulator solution for consumer products, toys, and other low-voltage or battery-powered motion-control applications. The device has one H-bridge driver to drive a DC motor, a voice-coil actuator, one winding of a stepper motor, a solenoid, or other devices. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the load. An internal charge pump generates the needed gate-drive voltages.

The DRV8850 device supplies up to 5 A of continuous output current (with proper PCB heat sinking) and up to 8-A peak current. It operates on a supply voltage from 2 V to 5.5 V.

A low-dropout linear voltage regulator is integrated with the motor driver to supply power to microcontrollers or other circuits. The LDO voltage regulator can be active in device sleep mode, so that the driver may be shut down without removing power to any devices powered by the LDO voltage regulator.

Internal shutdown functions provide overcurrent, short circuit, undervoltage, overvoltage, and overtemperature protection. In addition, the device also has built-in current sensing for accurate current measurement.

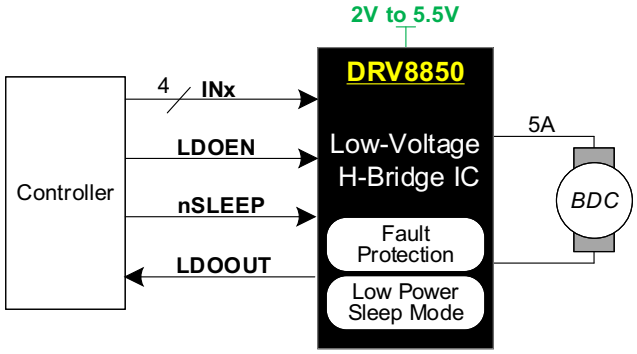
The DRV8850 device is packaged in a 24-pin VQFN (3.5-mm × 5.5-mm) package (Eco-friendly: RoHS and no Sb/Br).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8850	VQFN (24)	5.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 6
6.7 Typical Characteristics ... 7
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 11
7.3 Feature Description ... 12
7.4 Device Functional Modes ... 17
8 Application and Implementation ... 18
8.1 Application Information ... 18
8.2 Typical Application ... 18
9 Power Supply Recommendations ... 20
9.1 Bulk Capacitance ... 20
10 Layout ... 20
10.1 Layout Guidelines ... 20
10.2 Layout Example ... 21
10.3 Thermal Considerations ... 21
11 Device and Documentation Support ... 22
11.1 Documentation Support ... 22
11.2 Receiving Notification of Documentation Updates ... 22
11.3 Community Resources ... 22
11.4 Trademarks ... 22
11.5 Electrostatic Discharge Caution ... 22
11.6 Glossary ... 22
12 Mechanical, Packaging, and Orderable Information ... 22

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2016) to Revision D — **Page**

- Changed Pin Functions table's Pin No. of OUT2 to 21, 22, 23 ... 3
- Changed Pin Functions table's Pin No. of VCC to 18, 19, 20 ... 3
- Changed Table 1 table's Pin No. of VCC to 18, 19, 20 ... 12

Changes from Revision B (December 2015) to Revision C — **Page**

- Updated the RDS(ON) value and added the condition on the front page *Features* section ... 1
- Added maximum values for the HS and LS FET on resistance parameters (at T_A = 25°C, 85°C) in the *Electrical Characteristics* table ... 5
- Added the *Documentation Support* and *Receiving Notification of Documentation Updates* sections ... 22

Changes from Revision A (January 2014) to Revision B — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed HTSSOP package. ... 1

Changes from Original (November 2013) to Revision A — **Page**

- Removed product preview banner ... 1

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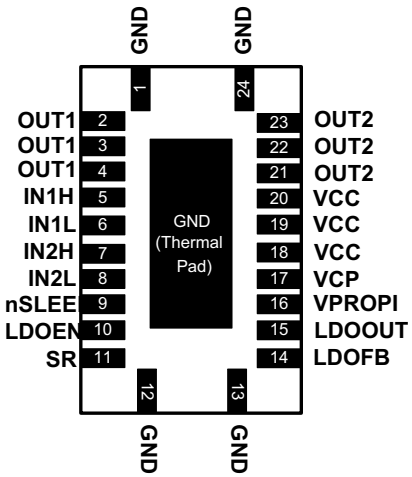
5 Pin Configuration and Functions

RGY Package
24-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND	1, 12, 13, 24, Thermal pad	—	Device ground	
LDOOUT	15	—	LDO regulator output	Bypass to GND with a 2.2-μF 6.3-V ceramic capacitor
VCC	18, 19, 20	—	Device supply	Bypass to GND with 0.1-μF and 10-μF 6.3-V ceramic capacitors
VCP	17	—	Charge pump	Connect a 0.1-μF 6.3-V ceramic capacitor to VCC
CONTROL				
IN1H	5	I	Input 1 HS FET enable	Active high enables HS FET for output 1 Internal pulldown resistor
IN1L	6	I	Input 1 LS FET enable	Active high enables LS FET for output 1 Internal pulldown resistor
IN2H	7	I	Input 2 HS FET enable	Active high enables HS FET for output 2 Internal pulldown resistor
IN2L	8	I	Input 2 LS FET enable	Active high enables LS FET for output 2 Internal pulldown resistor
LDOEN	10	I	LDO regulator enable	Logic low disables LDO regulator Logic high enables LDO regulator Internal pulldown resistor
LDOFB	14	I	LDO regulator feedback	Resistor divider from LDOOUT sets LDO output voltage May be connected to LDOIN to enable LDO
nSLEEP	9	I	Sleep mode input	Logic low puts device in low-power sleep mode Logic high for typical operation Internal pulldown resistor
SR	11	IO	Slew rate control	Resistor to ground sets output slew rate
OUTPUT				
OUT1	2, 3, 4	O	Output 1	Connect to motor winding
OUT2	21, 22, 23	O	Output 2	
VPROPI	16	O	Current sense output	Output current is proportional to H-bridge current. 1 kΩ, 1% resistor to GND for 2-A maximum current with VCC at 2 V. See Equation 1 if more current is required

(1) Directions: I = input, O = output, OZ = 3-state output, OD = open-drain output, IO = input or output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
	Power supply voltage, VCC	–0.3	7	V
	Charge pump, VCP	–0.3	VCC + 7	V
	Digital pin voltage, LDOEN, IN1H, IN1L, IN2H, IN2L, nSLEEP	–0.5	7	V
	Other pins, OUT1, OUT2, SR, LDOUT, LDOFB, VPROPI	–0.3	7	V
	Peak motor drive output current, OUT1, OUT2	Internally Limited		A
	LDO output current, LDOOUT	Internally Limited		A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCC	Device power supply voltage	2	5.5	V
V_{IN}	Logic level input voltage	0	VCC	V
I_{OUT}	H-bridge continuous output current(1)	0	5	A
I_{OUT}	H-bridge peak output current(1)	0	8	A
f_{PWM}	Externally applied PWM frequency	0	50	kHz
T_A	Ambient temperature	–40	85	°C

(1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC(1)		DRV8850 RGY (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
POWER SUPPLIES (VCC)						
I_{VCC}	VCC operating supply current, LDO regulator and driver enabled	VCC = 4.2 V, nSLEEP = LDOEN = VCC		2.9		mA
I_{VCQ1}	VCC sleep mode supply current	VCC = 4.2 V, nSLEEP = LDOEN = 0 V, INXH = INXL = 0 V			1	µA
I_{VCQ2}	VCC operating supply current, LDO regulator enabled, driver disabled (1)	VCC = 4.2 V, nSLEEP = 0 V, LDOEN = VCC, INXH = INXL = 0 V		40		µA
I_{VCQ3}	VCC operating supply current LDO voltage regulator disabled, driver enabled	VCC = 4.2 V, nSLEEP = VCC, LDOEN = 0 V		2.9		mA
V_{UVLO}	VCC undervoltage lockout voltage	VCC rising			2	V
		VCC falling			1.95	
V_{OVLO}	VCC overvoltage lockout voltage	VCC rising	5.6			V
		VCC falling	5.5			
LOGIC-LEVEL INPUTS (LDOEN, IN1H, IN1L, IN2H, IN2L, nSLEEP)						
V_{IL}	Input low voltage		0		0.2 × VCC	V
V_{IH}	Input high voltage		0.5 × VCC		VCC	V
V_{HYS}	Input hysteresis			0.08 × VCC		V
I_{IL}	Input low current	V_{IN} = 0	–1		1	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
R_{PD}	Pulldown resistance	LDOEN		3.5		MΩ
		nSLEEP		400		kΩ
		INXH, INXL		200		kΩ
VPROPI OUTPUT (VPROPI)						
I_{VPROPI}	VPROPI output current	VCC = 4.2 V, resistor chosen to keep VPROPI ≤ (VCC – 1 V) / I_{OUT} 500 mA ≤ I_{OUT} ≤ 5 A		I_{OUT} / 2000		A
H-BRIDGE FETS (OUT1, OUT2)						
$R_{DS(ON)}$	HS FET on resistance	VCC = 4.2 V, I_{OUT} = 2 A, T_A = 25°C		35	45	mΩ
		VCC = 4.2 V, I_{OUT} = 2 A, T_A = 85°C			49	
	LS FET on resistance	VCC = 4.2 V, I_{OUT} = 2 A, T_A = 25°C		30	40	mΩ
		VCC = 4.2 V, I_{OUT} = 2 A, T_A = 85°C			44	
I_{OFF}	Off-state leakage current	VOUT = 0 V	–1		1	µA
LDO REGULATOR (LDOOUT)						
V_{FB}	LDO feedback (reference) voltage		0.76	0.8	0.84	V
V_{DO}	LDO regulator dropout voltage	VCC = 4.2 V, I_{OUT} = 100 mA, T_A = 25°C		150		mV
		VCC = 4.2 V, I_{OUT} = 100 mA, T_A = 85°C		175		mV
ΔV_{LINE}	LDO line regulation	VCC from 4.2 to 5.5 V, VOUT = 3.3 V	–2.5%		2.5%	
ΔV_{LOAD}	LDO load regulation	VOUT = 3.3 V, I_{OUT} from 1 to 100 mA	–2.5%		2.5%	
I_{CL}	LDO output current limit	VCC = 4.2 V, VOUT = 3.3 V, T_A ≥ 25°C	275			mA

(1) Does not include the current consumption from the feedback resistors.

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Electrical Characteristics (continued)

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level	VCC = 2.5 to 5.5 V	9.5			A
t_{OCP}	Overcurrent protection deglitch time			1		µs
t_{RETRY}	Overcurrent retry time			4		ms
t_{TSD}	Thermal shutdown temperature	Die temperature (rising)	150	160	180	°C
t_{HYS}	Thermal shutdown hysteresis	Temperature hysteresis		50		°C

6.6 Timing Requirements

T_A = 25°C, VCC = 4.2 V, RL = 2 Ω(1)

				MIN	NOM	MAX	UNIT
t_R, t_F	Rise and fall time (measured at OUTx)	RSR connected to GND			70		ns
		RSR = 24 kΩ			0.7		µs
		RSR = 2.4 MΩ			70		µs
t_{DELAY}	Propagation delay (measured as time between input edge to output change)	RSR connected to GND			500		ns
		RSR = 24 kΩ			750		ns
		RSR = 2.4 MΩ			50		µs
t_{DEAD}	Dead time (measured as time OUTx FET is Hi-Z)	Low-side slow decay LS OFF to HS ON	RSR short to GND		400		ns
			RSR = 24 kΩ		2.6		µs
			RSR = 2.4 MΩ		110		µs
		Low-side slow decay HS OFF to LS ON	RSR short to GND		400		ns
			RSR = 24 kΩ		2.6		µs
			RSR = 2.4 MΩ		110		µs
		High-side slow decay or fast decay HS OFF to LS ON	RSR short to GND		400		ns
			RSR = 24 kΩ		2.6		µs
			RSR = 2.4 MΩ		110		µs
		High-side slow decay or fast decay LS OFF to HS ON	RSR short to GND		600		ns
			RSR = 24 kΩ		3.9		µs
			RSR = 2.4 MΩ		165		µs

(1) Rise and fall time measured from 10 to 90% VCC

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6.7 Typical Characteristics

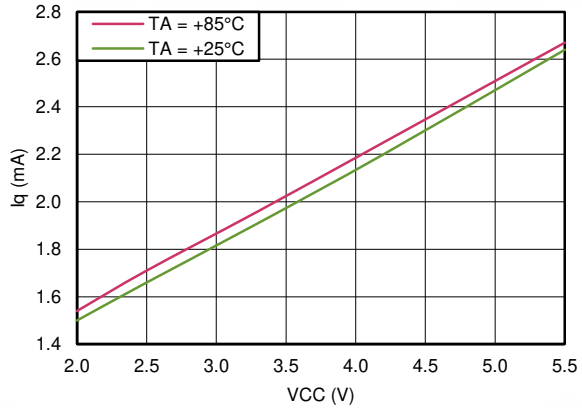

Figure 1. Quiescent Current With Motor Driver ON and LDO ON

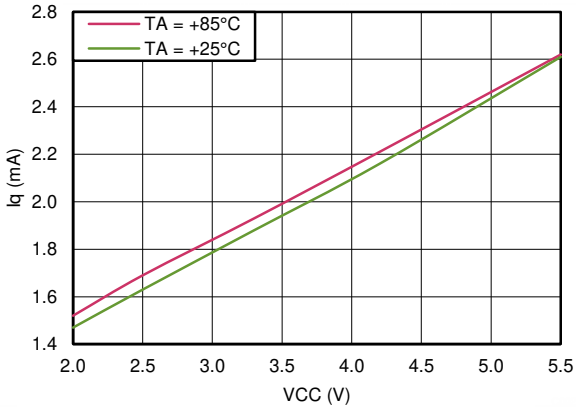

Figure 2. Quiescent Current With Motor Driver ON and LDO OFF

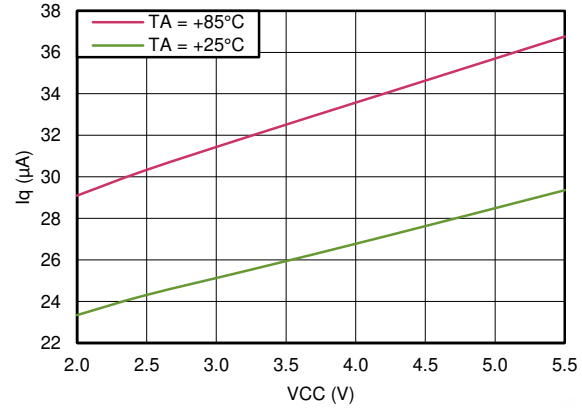

Figure 3. Quiescent Current With Motor Driver OFF and LDO ON

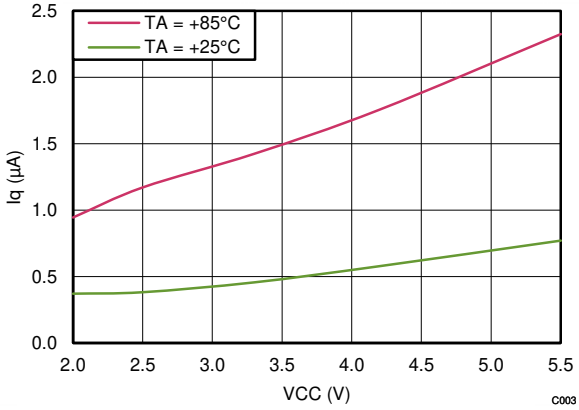

Figure 4. Quiescent Current With Motor Driver OFF and LDO OFF, Sleep Current

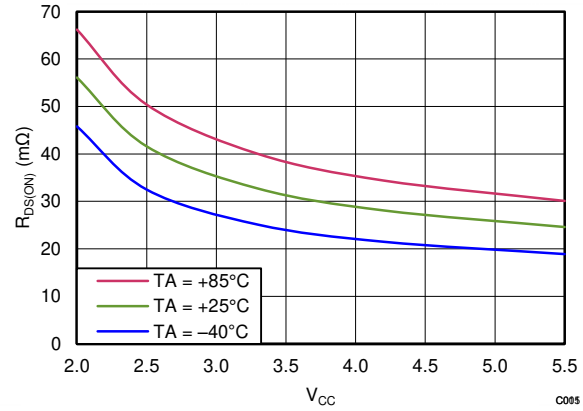

Figure 5. $R_{DS(ON)}$, HS – OUT1

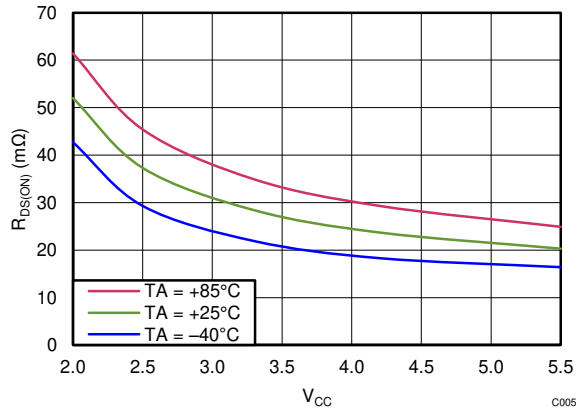

Figure 6. $R_{DS(ON)}$, HS – OUT2

Typical Characteristics (continued)

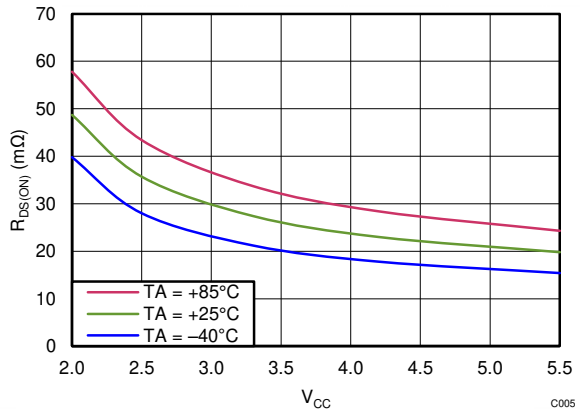

Figure 7. $R_{DS(ON)}$, LS – OUT1

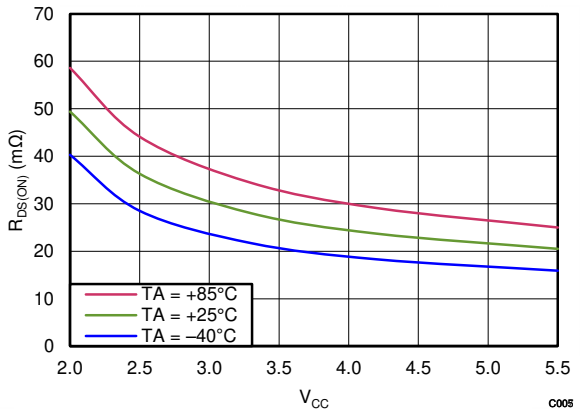

Figure 8. $R_{DS(ON)}$, LS – OUT2

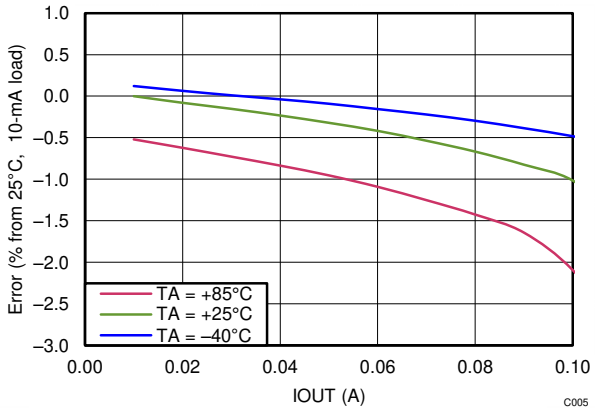

Figure 9. LDO Output, VCC = 3.5 V, LDOOUT = 3.3 V

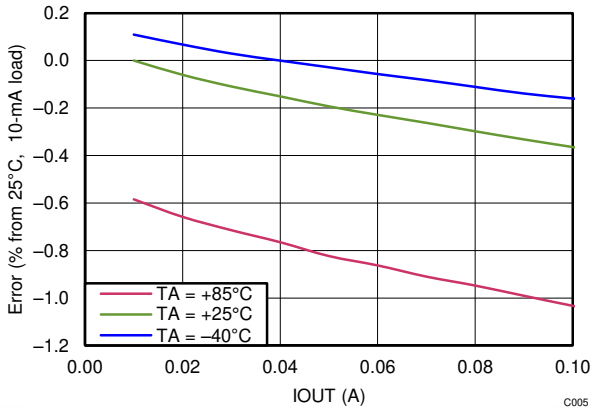

Figure 10. LDO Output, VCC = 4.2 V, LDOOUT = 3.3 V

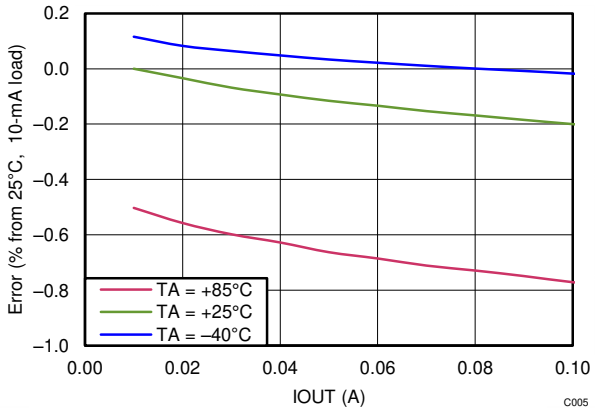

Figure 11. LDO Output, VCC = 5.5 V, LDOOUT = 3.3 V

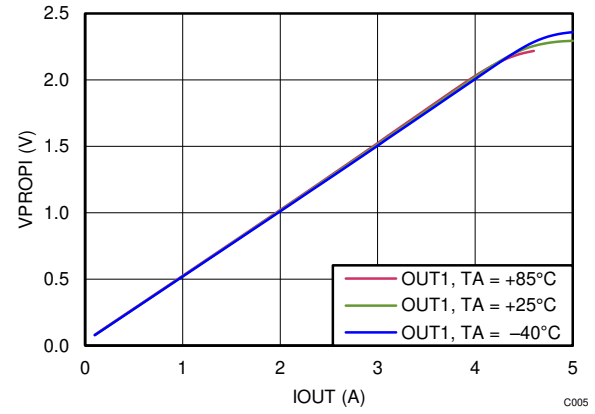

Figure 12. VPROPI Output, VCC = 4.2 V, OUT1 Overtemperature, 1 kΩ

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Typical Characteristics (continued)

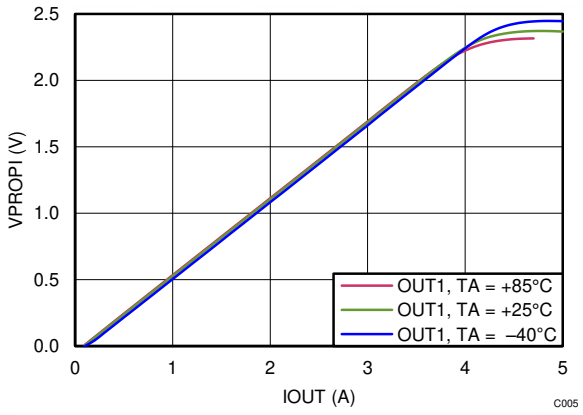

Figure 13. VPROPI Output, VCC = 4.2 V, OUT2 Overtemperature, 1 kΩ

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7 Detailed Description

7.1 Overview

The DRV8850 is an integrated motor driver solution for one DC motor. The device integrates one NMOS H-bridge, current regulation circuitry, and various protection circuitry. The DR8850 can be powered with a supply voltage range from 2 V to 5.5 V, and is capable of providing an output current up to 5-A peak current. Actual operable peak current will depend on the temperature, supply voltage, and PCB ground plane size. Between VM = 1.95 V and VM = 2 V the H-bridge outputs are shut down.

A simple 4 pin interface allows for individual control of each internal H-bridge FET. The condition where both HS and LS FETs are turned on at the same time is not allowed. During this input condition both the HS and LS FETs turn off.

The current monitoring is configurable from a range of 500 mA to 5 A. The VPROPI pin outputs an analog current that is proportional to the current flowing through the H-bridge. VPROPI is derived from the current through either of the high side FETs. Because of this, VPROPI does not represent H-bridge current when operating in a fast-decay mode or low-side slow-decay mode.

The LDO regulator integrated in the DRV8850 is typically used to provide the supply voltage for a low-power microcontroller. The output voltage is adjustable from 1.6 V to VCC – VLDO using external resistors. LDOEN pin is used to enable or disable the LDO regulator; when disabled the output is turned off and the LDO regulator enters a very-low-power state.

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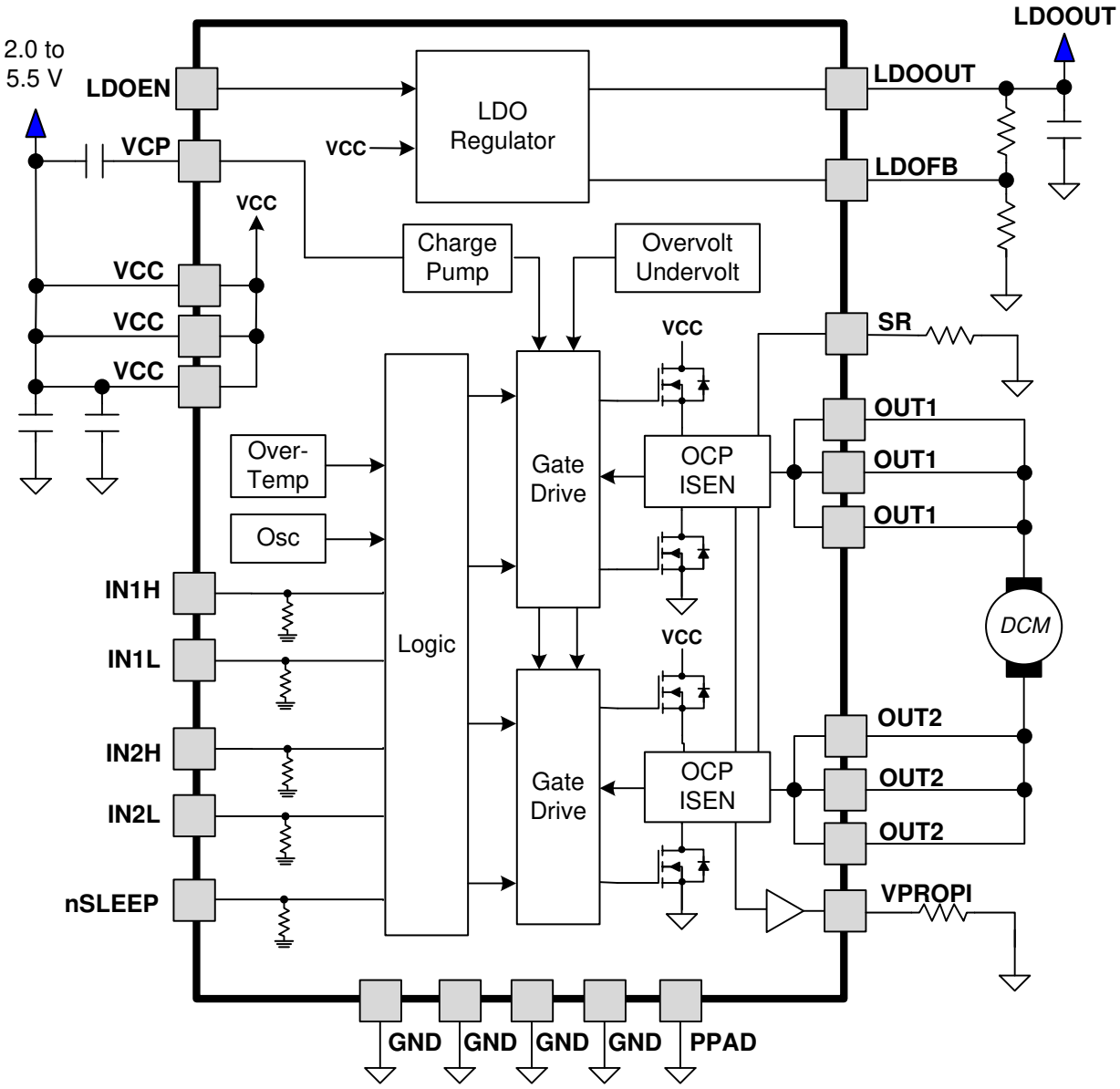
7.2 Functional Block Diagram



7.3 Feature Description

Table 1 lists the external components.

Table 1. External Components

PIN		DESCRIPTION	
NAME	NO.		
LDOFB	14	LDO regulator feedback	Resistor divider from LDOUT sets LDO output voltage.
LDOOUT	15	LDO regulator output	Bypass to GND with a 2.2-μF 6.3-V ceramic capacitor.
SR	11	Slew rate control	Resistor to ground sets output slew rate GND to 2.4 MΩ.
VCC	18, 19, 20	Device supply	Bypass to GND with 0.1-μF and 10-μF 6.3-V ceramic capacitors.
VCP	17	Charge pump	Connect a 0.1-μF 6.3-V ceramic capacitor to VCC
VPROPI	16	Current sense output	Output current is proportional to H-bridge current. 1 kΩ, 1% resistor to GND for 2-A max current with VCC at 2 V. See Equation 1 for if more current is required.

7.3.1 Power Supervisor

The LDO regulator can be active independent of the nSLEEP pin. This independence allows a microcontroller, or other device, to be powered by the LDO voltage regulator, while retaining the ability to put the DRV8850 device into sleep mode.

Because of this functionality, nSLEEP and LDOEN must both be brought logic low to minimize power consumption in sleep mode. If the LDO regulator remains active in sleep mode, a quiescent current of I_{VCQ2} (typically 50 μA plus current through the external feedback resistors) is drawn from the supply.

Table 2 lists the operation mode logic for the DRV8850 device.

Table 2. DRV8850 Device Operation Mode Logic(1)

nSLEEP	LDOEN	LDO REGULATOR	DRIVER
0	0	Off	Sleep
0	1	Active	Sleep
1	0	Off	Active
1	1	Active	Active

(1) A state must be active for a minimum of 1 ms before a new state is commanded.

7.3.2 Bridge Control

A corresponding input pin controls the individual FETs in the DRV8850 device. Shoot-through (the condition when both HS and LS FETs are turned on at the same time) is not allowed; with this input condition, both the HS and LS FETs turn off.

Table 3 lists the logic for the DRV8850 device.

Table 3. DRV8850 Device Logic

INxL	INxH	OUTx
0	0	Z
0	1	H
1	0	L
1	1	Z

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7.3.3 Current Sensing – VPROPI

The VPROPI pin outputs an analog current that is proportional to the current flowing in the H-bridge. The output current is typically 1 / 2000 of the current in both high side FETs. VPROPI is derived from the current through either of the high side FETs. Because of this, VPROPI does not represent the H-bridge current when operating in a fast-decay mode or low-side slow-decay mode. VPROPI represents the H-bridge current under forward drive, reverse drive, and high-side slow decay. VPROPI output is delayed by roughly 2 µs after the high side FET is switched on and it has reached approximately VCC (including the deglitch on the HSon). Select the external resistor so that the voltage on VPROPI is less than (VCC – 1 V), so the resistor must be sized less than:

$$2000 \; x \; (VCC \; - \; 1 \; V) \; / \; I_{OUT} \tag{1}$$

where I_{OUT} is the maximum drive current to be monitored

The range of current that can be monitored is 500 mA to 5 A, assuming the external resistor meets Equation 1.

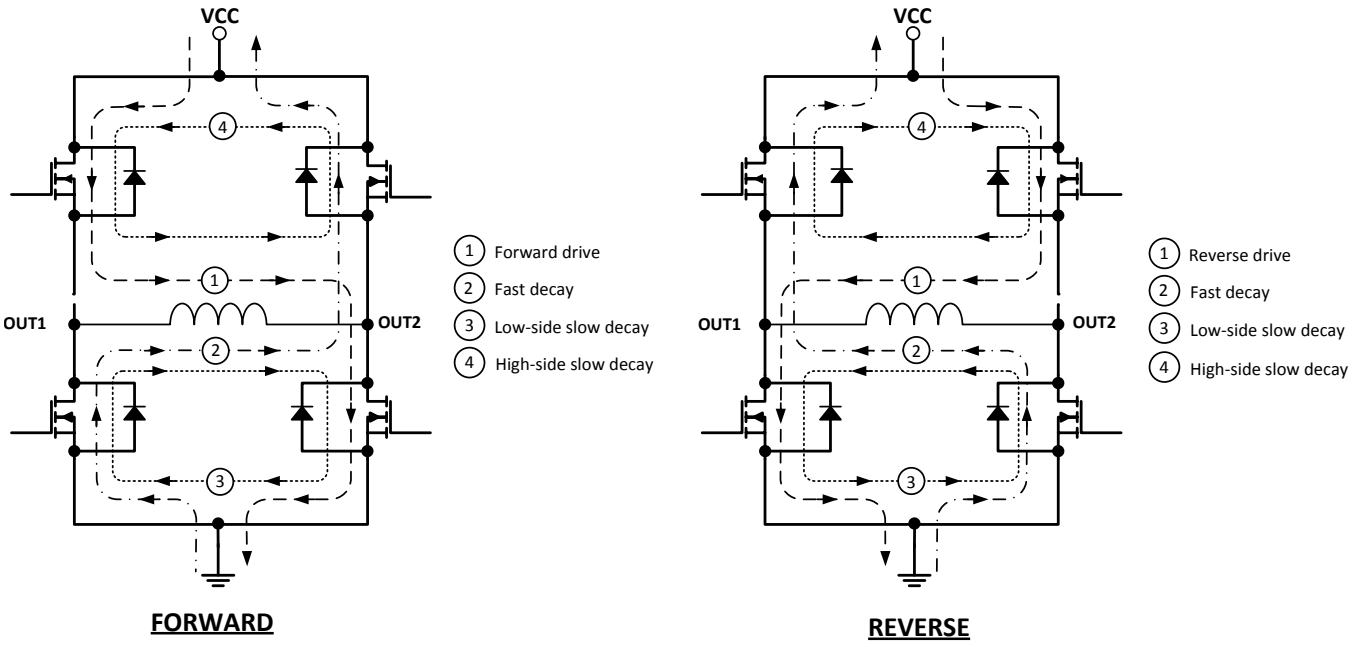

Figure 14. Forward and Reverse Operation

When using an independent half-bridge as a high-side driver, VPROPI does not output a current measurement during slow decay. During typical operation, VPROPI represents the total current flowing to loads connected to OUT1 and OUT2.

VPROPI is nonfunctional when implemented as a low-side driver.

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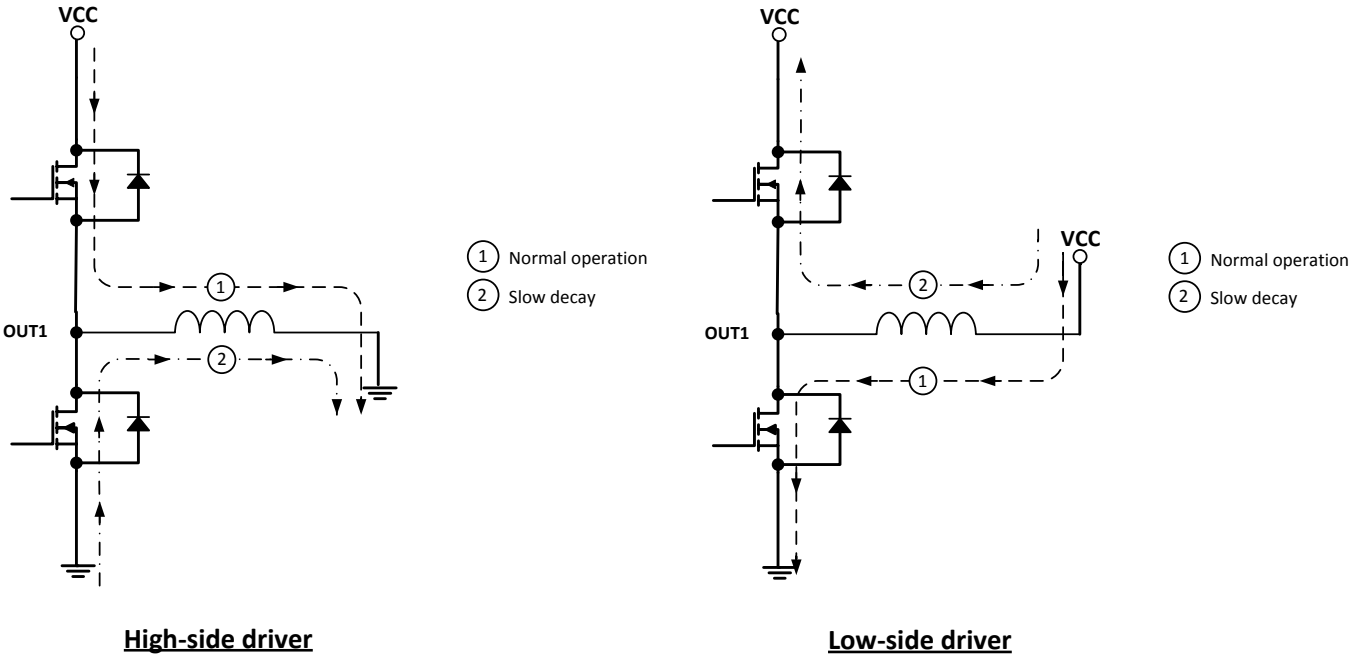

Figure 15. High-Side and Low-Side Drivers

7.3.4 Slew-Rate Control

The rise and fall times (t_R and t_F) of the outputs can be adjusted by the value of an external resistor connected from the SR pin to ground. The output slew rate is adjusted internally by the DRV8850 device by controlling the ramp rate of the driven FET gate.

The typical voltage on the SR pin is 0.6 V driven internally. Changing the resistor value monotonically increases the slew rates from approximately 100 ns to 100 µs. Recommended values for the external resistor are from GND to 2.4 MΩ. If the SR pin is grounded then the slew rate is 100 ns.

7.3.5 Dead Time

The dead time (t_{DEAD}) is measured as the time when OUTx is Hi-Z between turning off one of the H-bridge FETs and turning on the other. For example, the output is Hi-Z between turning off the high-side FET and turning on the low-side FET. When driving current out of the pin, the output is observed to fall to one diode drop below ground during dead time. When driving current into the pin, the output is observed to rise to one diode drop above VCC.

The DRV8850 has an analog dead time of approximately 100 ns. In addition to this analog dead time, the output is Hi-Z when the FET gate voltage is less than the threshold voltage. The total dead time depends on the SR resistor setting because a portion of the FET gate ramp includes the observable dead time.

7.3.6 Propagation Delay

The propagation delay time (t_{DELAY}) is measured as the time between an input edge to an output change. This time is composed of two parts: an input deglitcher and output slewing delay. The input deglitcher prevents noise on the input pins from affecting the output state.

The output slew rate also contributes to the delay time. For the output to change state during typical operation, first one FET must be turned off. The FET gate is ramped down according to the SR resistor selection, and the observed propagation delay ends when the FET gate falls to less than the threshold voltage.

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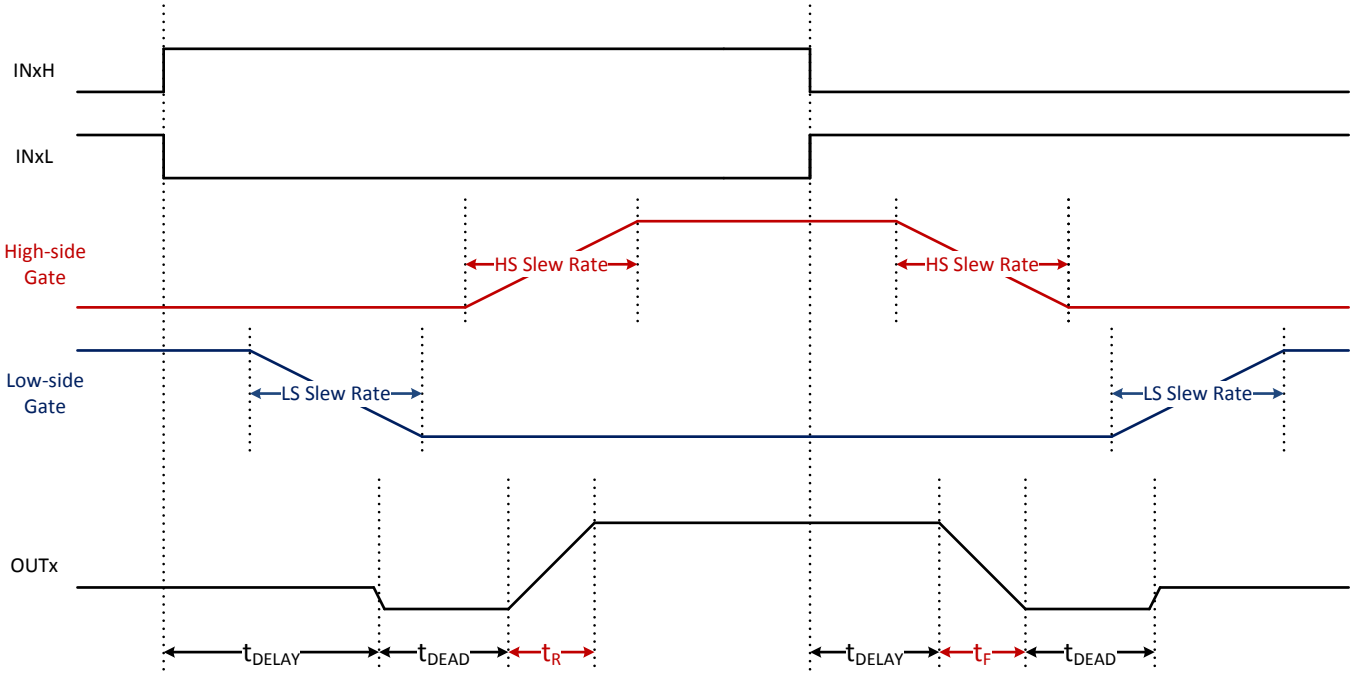

Figure 16. Low-Side Slow Decay Operation – Current Sourced from OUTx

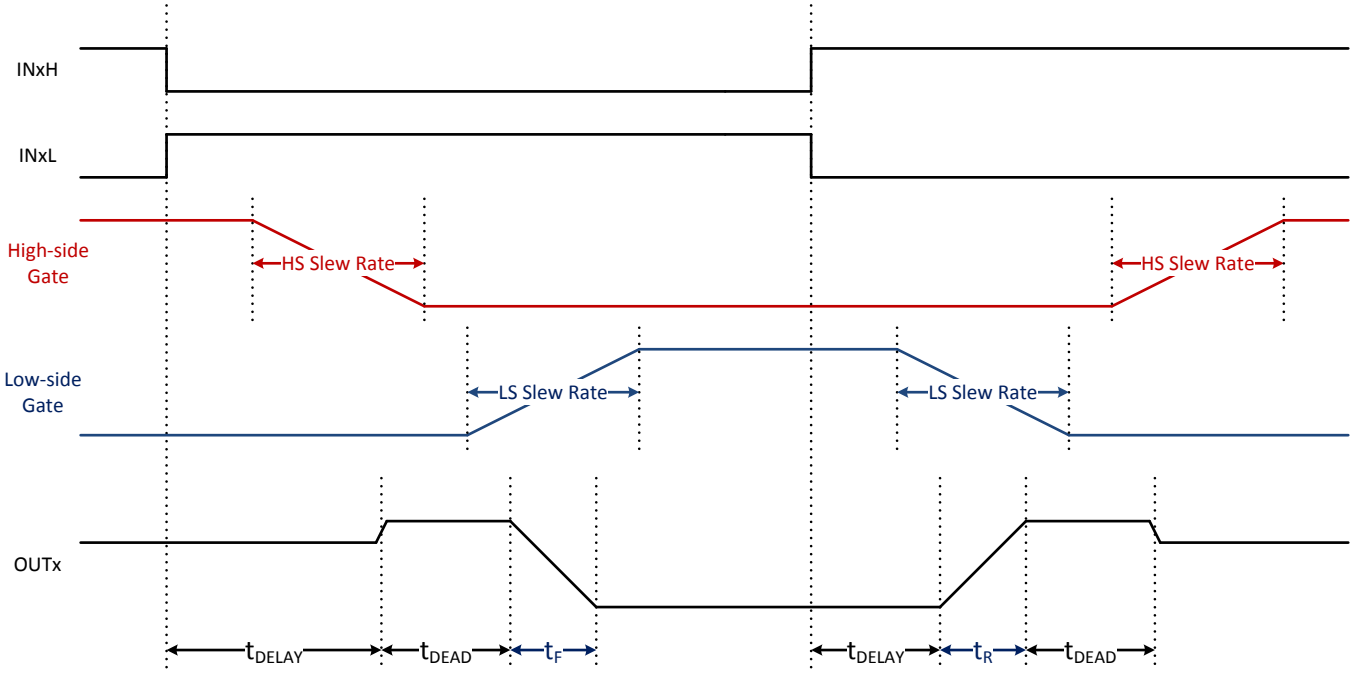

Figure 17. High-Side Slow Decay or Fast Decay Operation – Current Sunk into OUTx

7.3.7 Power Supplies and Input Pins

An internal charge pump generates a voltage greater than VCC that is used to drive the internal N-channel power MOSFETs. The charge pump requires a capacitor between the VCP and VCC pins. TI recommends bypassing VCC to ground with 0.1-µF and 10-µF ceramic capacitors, placing them as close as possible to the IC. Each input pin has a weak pulldown resistor to ground (see *Electrical Characteristics* for more details).

The input pins should not be driven to more than 0.6 V without the VCC power supply removed.

7.3.8 LDO Voltage Regulator

An LDO regulator is integrated into the DRV8850 device. The LDO regulator is typically used to provide the supply voltage for a low-power microcontroller. For proper operation, bypass the LDOOUT pin to GND using a ceramic capacitor. The recommended value for this component is 2.2 µF.

Two external resistors are used to set the LDO voltage (V_{LDO}) by creating a voltage divider between LDOOUT and LDOFB. The LDO output voltage can be given by:

$$V_{LDO} = V_{FB} \times (1 + R1 / R2) V \quad (2)$$

where

- R1 is located between LDOOUT and LDOFB
- R2 is between LDOFB and GND

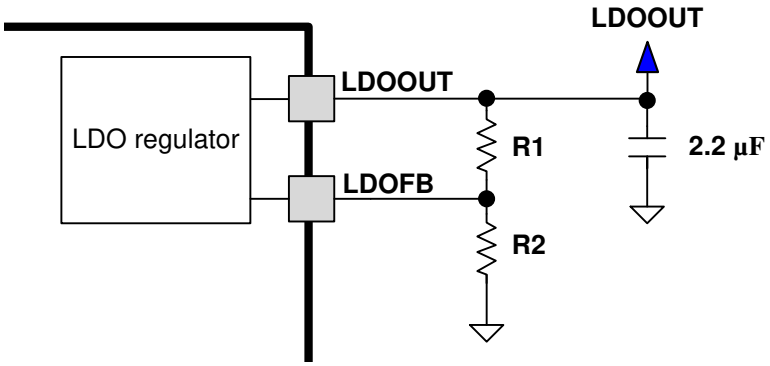

Figure 18. LDO Regulator Schematic

The output voltage is adjustable from 1.6 V to VCC – V_{LDO} using external resistors. The LDOEN pin is used to enable or disable the LDO regulator; when disabled, the output is turned off and the LDO regulator enters a very-low-power state.

When the LDO current load exceeds I_{CL}, the LDO regulator behaves like a constant current source. The LDO output voltage drops significantly with currents greater than I_{CL}.

7.3.9 Protection Circuits

The DRV8850 device is protected against undervoltage, overvoltage, overcurrent, and overtemperature events.

7.3.9.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{OCP}, all FETs in the H-bridge are disabled. After approximately t_{RETRY}, the bridge reenables automatically.

Overcurrent conditions on both high and low-side devices, that is, a short to ground, supply, or across the motor winding result in an overcurrent shutdown.

7.3.9.2 Thermal Shutdown (TSD)

If the die temperature exceeds t_{TSD}, all FETs in the H-bridge are disabled. Once the die temperature has fallen below t_{TSD} – t_{HYS}, the H-bridge automatically reenables.

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7.3.9.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls to less than the undervoltage lockout threshold voltage, all circuitry in the device is disabled and internal logic resets. Operation resumes when VCC rises to greater than the UVLO threshold.

7.3.9.4 Overvoltage Lockout (OVLO)

If at any time the voltage on the VCC pins rises to more than V_{OVLO}, the output FETs are disabled (outputs are high-Z). Operation resumes when VCC falls below the V_{OVLO}.

CAUTION

VCC must remain less than the absolute maximum rating for the device, or damage to the device may occur.

7.4 Device Functional Modes

The DRV8850 internal logic and charge pump are operating unless nSLEEP is pulled low. The LDO regulator can be active independent of the nSLEEP pin. This independence allows a microcontroller or other device to be powered by the LDO regulator while retaining the ability to put the DRV8850 into sleep mode.

If LDOEN and nSLEEP are both brought logic low the device will minimize current consumption in sleep mode. While the LDO regulator remains active n sleep mode, a quiescent current (typically 50 µA plus current through the external feedback resistors) is drawn from the supply.

Each FET inside the device is controlled by a corresponding input pin on the DRV8850. The condition where both HS and LS FETs are turned on at the same time is not allowed. During this input condition both the HS and LS FETs turn off.

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8 Application and Implementation

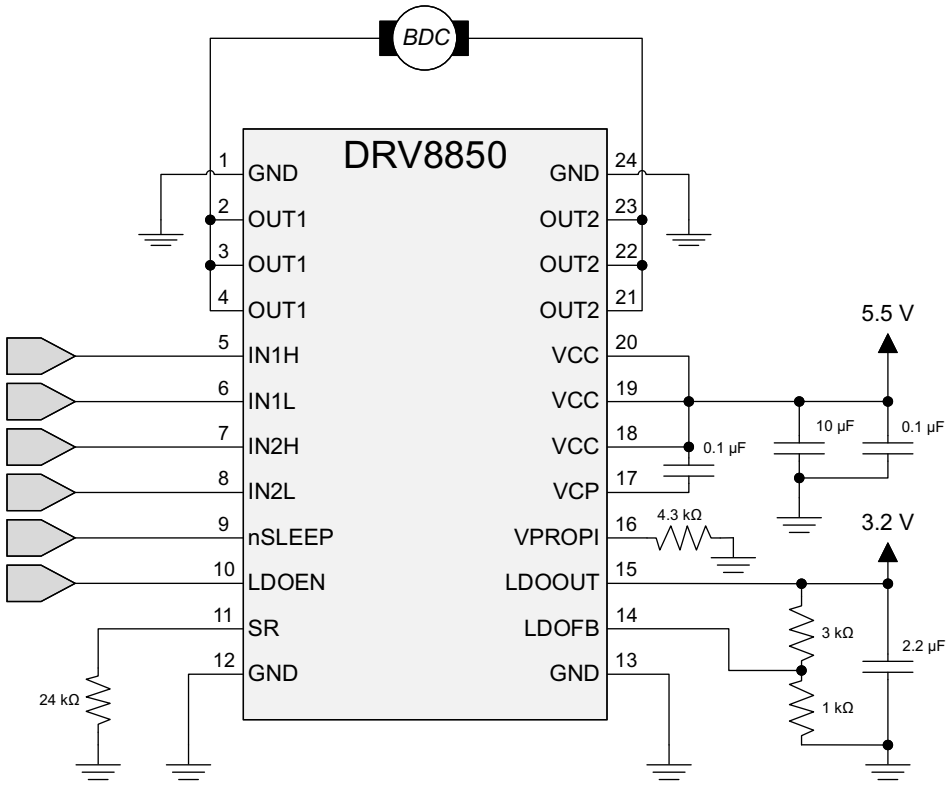
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8850 can be used to drive a DC motor.

8.2 Typical Application



8.2.1 Design Requirements

Table 4 lists the parameters for this design example.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_M	5.5 V
LDO output voltage	V_{LDO}	3.2 V
Slew rate	SR	700 ns
HS FET on resistance	$R_{DS(ON)_HS}$	35 mΩ
LS FET on resistance	$R_{DS(ON)_LS}$	30 mΩ
Motor rated current	I_M	2 A

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8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Drive Current

The current path is through the high-side sourcing DMOS power driver, motor winding, and low-side sinking DMOS power driver. Power dissipation losses in one source and sink DMOS power driver are shown in the following equation.

$$P_D = I^2 (R_{DS(ON)_HS} + R_{DS(ON)_LS}) \quad (3)$$

The DRV8850 has been measured to be capable of 5-A RMS current at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on PCB design and the ambient temperature.

8.2.3 Application Curves

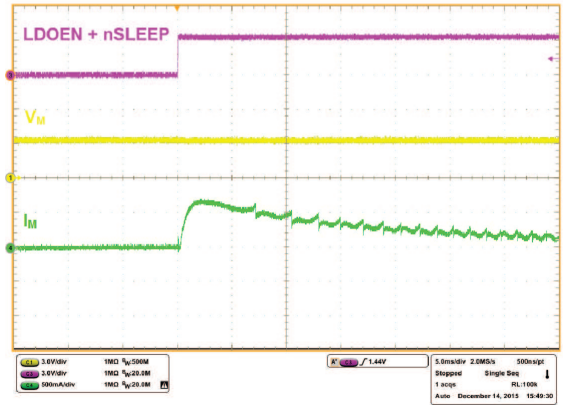

Figure 19. I_M Start-Up after LDOEN and nSLEEP Toggle

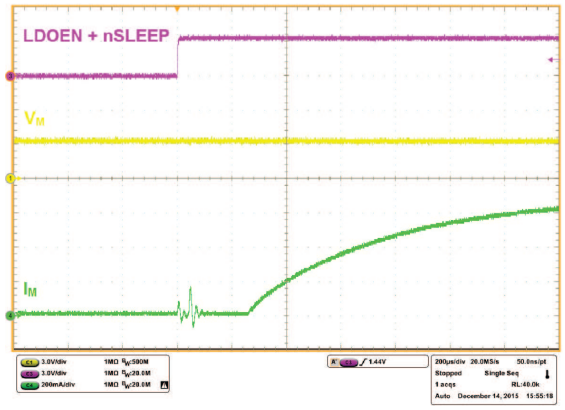

Figure 20. I_M Start-Up Delay after LDOEN and nSLEEP Toggle

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

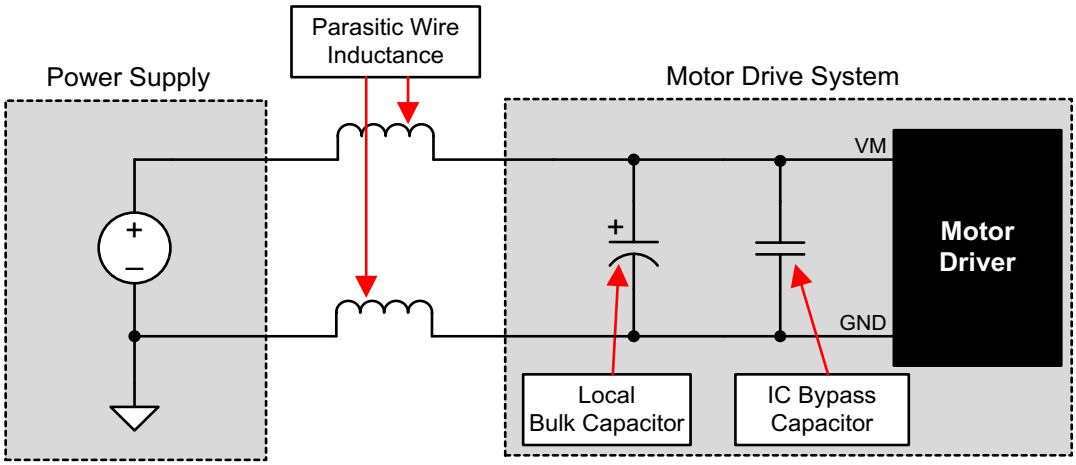

Figure 21. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

- The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.
- Small-value capacitors should be ceramic, and placed close to the device pins.
- The high-current device outputs should use wide metal traces.
- The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

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10.2 Layout Example

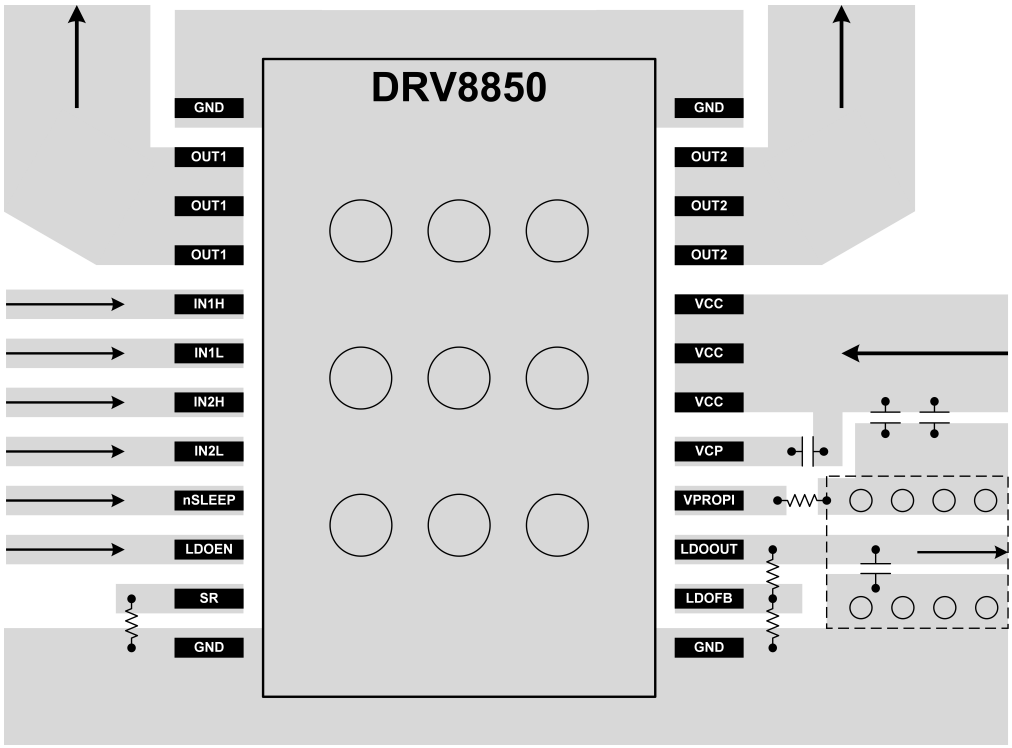

Figure 22. Layout Recommendation

10.3 Thermal Considerations

The DRV8850 device has thermal shutdown (TSD) as described in the *Thermal Shutdown (TSD)* section. If the die temperature exceeds approximately t_{TSD}, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

Power dissipation in the DRV8850 device is the sum of the motor driver power dissipation and the LDO voltage regulator dissipation.

The LDO dissipation is calculated simply by $(V_{IN} – V_{OUT}) \times I_{OUT}$.

The power dissipation in the motor driver is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Power dissipation can be estimated by:

$$P_{TOT} = \left(LS_R_{DS(ON)} + HS_R_{DS(ON)}\right) x \left(I_{OUT(RMS)}\right)^2 \quad (4)$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of each FET
- $I_{OUT(RMS)}$ is the RMS output current being driven

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heat sinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

DRV8850EVM User's Guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8850RGYR	ACTIVE	VQFN	RGY	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8850	Samples
DRV8850RGYT	ACTIVE	VQFN	RGY	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8850	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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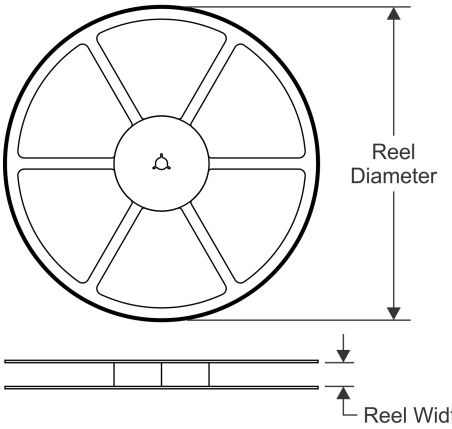
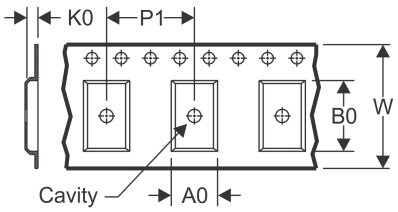
TAPE AND REEL INFORMATION

REEL DIMENSIONS

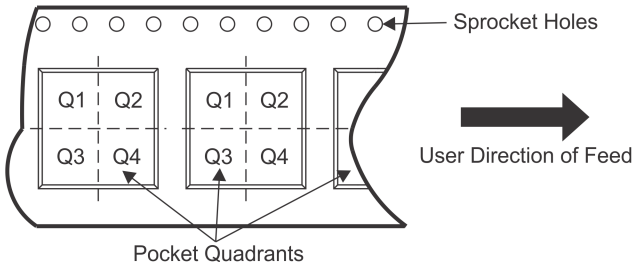


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

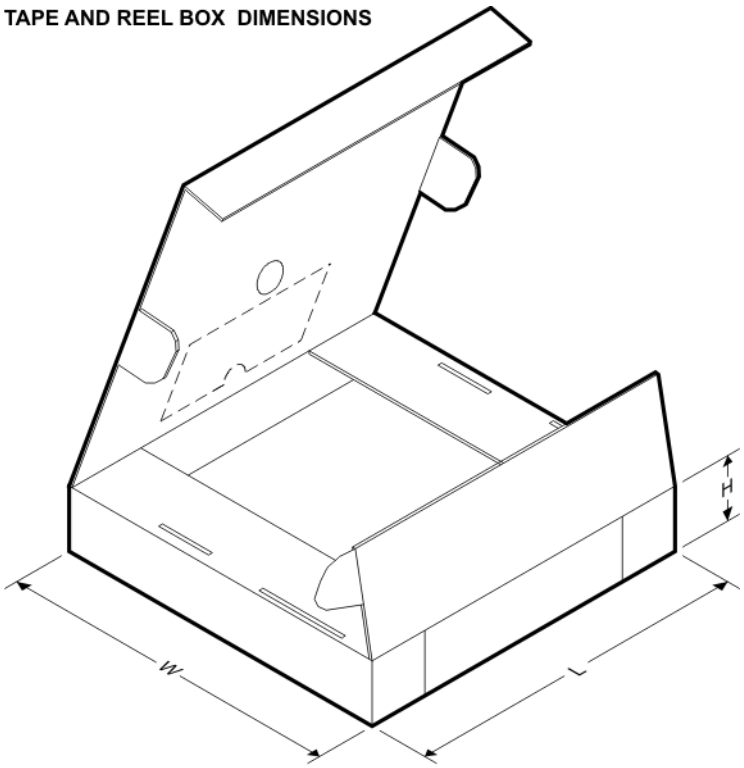
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8850RGYR	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
DRV8850RGYT	VQFN	RGY	24	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

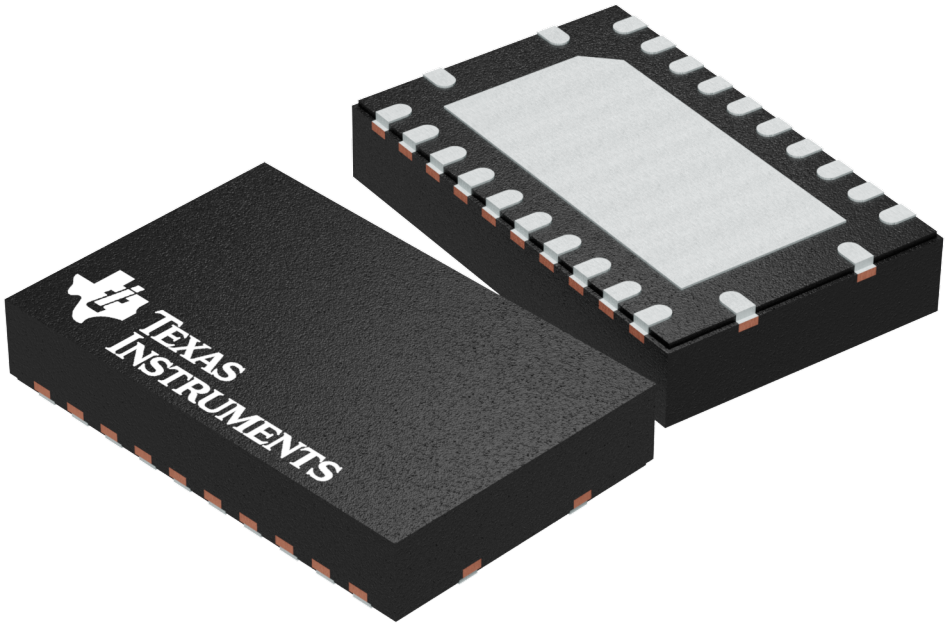
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8850RGYR	VQFN	RGY	24	3000	367.0	367.0	35.0
DRV8850RGYT	VQFN	RGY	24	250	210.0	185.0	35.0

RGY 24

VQFN - 1 mm max height

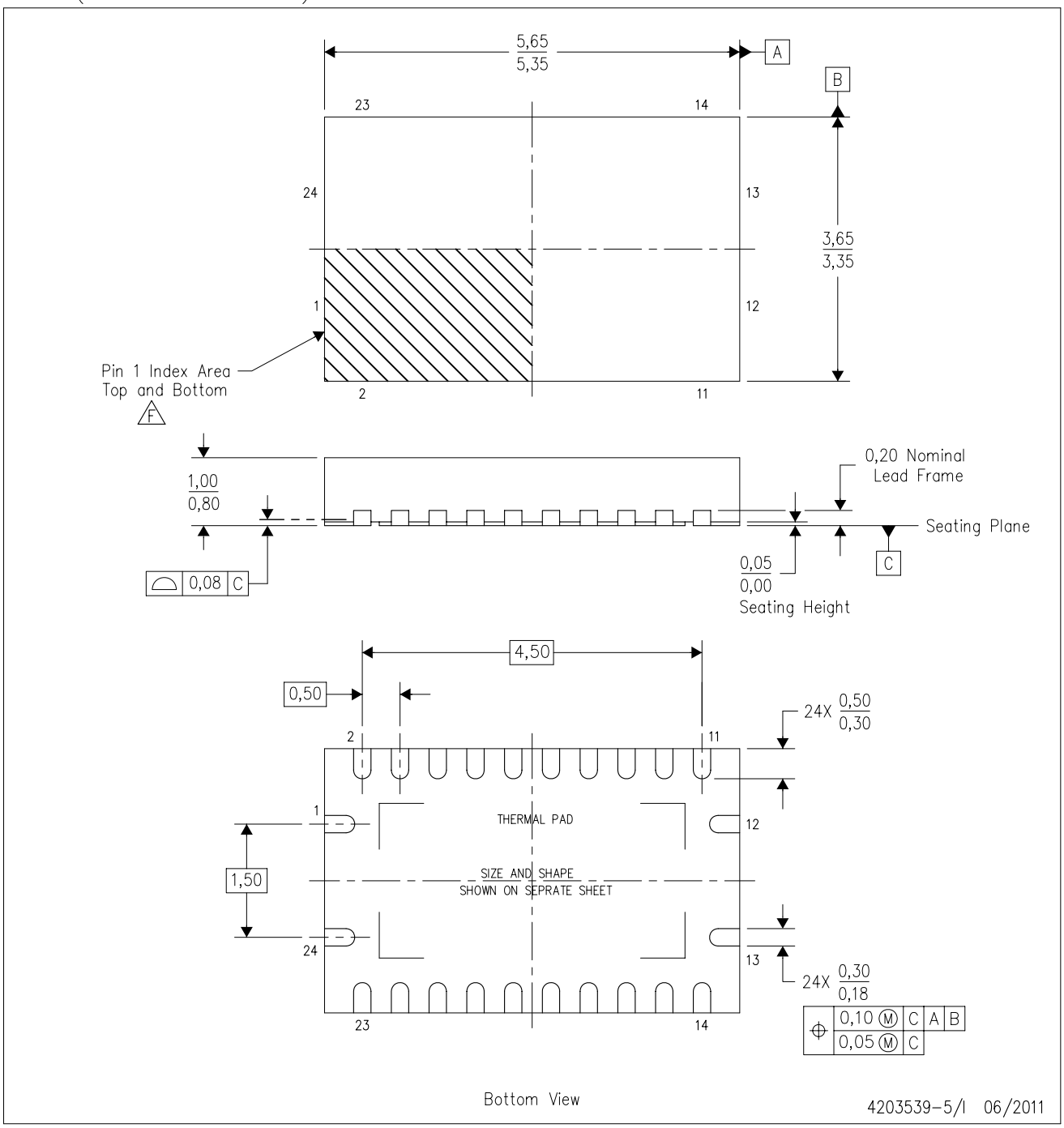
5.5 x 3.5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGY (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

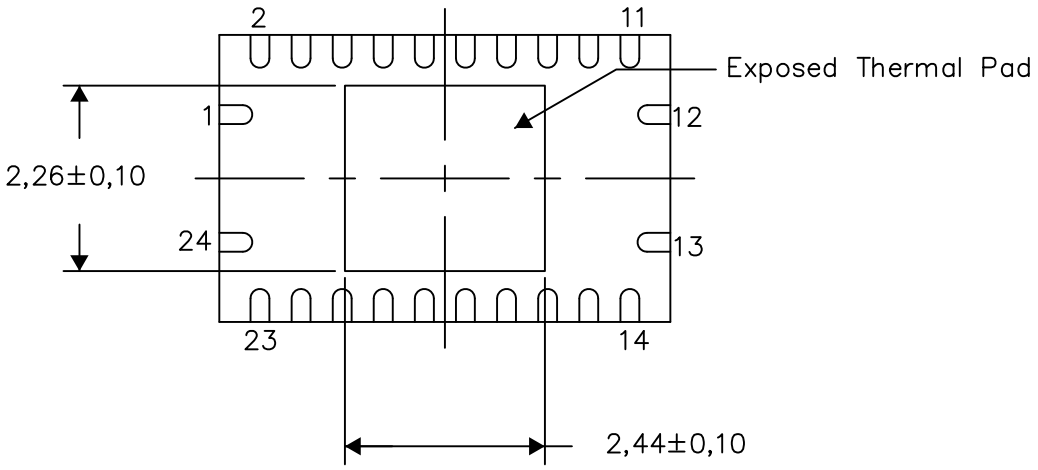
RGY (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353–7/P 03/14

NOTE: All linear dimensions are in millimeters

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