



# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

## General Description

The MAX5175/MAX5177 low-power, serial, voltage-output, 12-bit digital-to-analog converters (DACs) feature a precision output amplifier in a space-saving 16-pin QSOP package. The MAX5175 operates from a single +5V supply, and the MAX5177 operates from a single +3V supply. The output amplifier's inverting input is available to allow specific gain configurations, remote sensing, and high output current capability. This makes the MAX5175/MAX5177 ideal for a wide range of applications, including industrial process control. Both devices draw only 260 $\mu$ A of supply current, which reduces to 1 $\mu$ A in shutdown mode. In addition, the programmable power-up reset feature allows for a user-selectable output voltage state of either 0 or midscale.

The 3-wire serial interface is compatible with SPI™, QSPI™, and MICROWIRE™ standards. An input register followed by a DAC register provides a double-buffered input, allowing the registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include software and hardware shutdown, shutdown lockout, a hardware reset pin, and a reference input capable of accepting DC and offset AC signals. These devices provide a programmable digital output pin for added functionality and a serial-data output pin for daisy-chaining. All logic inputs are TTL/CMOS compatible and are internally buffered with Schmitt triggers to allow direct interfacing to optocouplers.

The MAX5175/MAX5177 incorporate a proprietary on-chip circuit that keeps the output voltage virtually "glitch free," limiting the glitches to a few millivolts during power-up.

Both devices come in 16-pin QSOP packages and are specified for the extended (-40°C to +85°C) temperature range. The MAX5171/MAX5173 are 14-bit pin-compatible upgrades to the MAX5175/MAX5177. For pin-compatible DACs with an internal reference, see the 13-bit MAX5132/MAX5133 and 12-bit MAX5122/MAX5123.

## Applications

- Digitally Programmable 4–20mA Current Loops
- Industrial Process Controls
- Digital Offset and Gain Adjustment
- Motion Control
- Automatic Test Equipment (ATE)
- Remote Industrial Controls
- $\mu$ P-Controlled Systems

**Functional Diagram appears at end of data sheet.**

*SPI and QSPI are trademarks of Motorola, Inc.*

*MICROWIRE is a trademark of National Semiconductor Corp.*

*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*

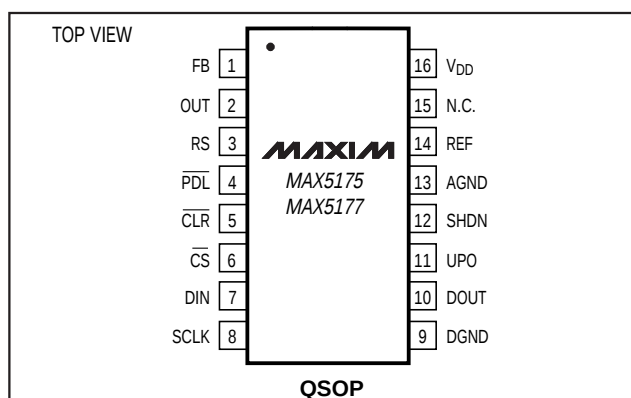
## Features

- ♦  $\pm 1$  LSB INL
- ♦ 1 $\mu$ A Shutdown Current
- ♦ "Glitch Free" Output Voltage at Power-Up
- ♦ Single-Supply Operation
  - +5V (MAX5175)
  - +3V (MAX5177)
- ♦ Full-Scale Output Range
  - +2.048V (MAX5177, VREF = +1.25V)
  - +4.096V (MAX5175, VREF = +2.5V)
- ♦ Rail-to-Rail® Output Amplifier
- ♦ Adjustable Output Offset
- ♦ Low THD (-80dB) in Multiplying Operation
- ♦ SPI/QSPI/MICROWIRE-Compatible 3-Wire Serial Interface
- ♦ Programmable Shutdown Mode and Power-Up Reset (0 or midscale)
- ♦ Buffered Output Capable of Driving 4–20mA or 5k $\Omega$  || 100pF Loads
- ♦ User-Programmable Digital Output Pin Allows Serial Control of External Components
- ♦ 14-Bit Upgrades Available (MAX5171/MAX5173)

## Ordering Information

| PART        | TEMP. RANGE    | PIN-PACKAGE | INL (LSB) |
|-------------|----------------|-------------|-----------|
| MAX5175AEEE | -40°C to +85°C | 16 QSOP     | $\pm 1$   |
| MAX5175BEEE | -40°C to +85°C | 16 QSOP     | $\pm 2$   |
| MAX5177AEEE | -40°C to +85°C | 16 QSOP     | $\pm 2$   |
| MAX5177BEEE | -40°C to +85°C | 16 QSOP     | $\pm 4$   |

## Pin Configuration



Maxim Integrated Products 1

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MAX5175/MAX5177

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

## ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub> to AGND, DGND .....-0.3V to +6V  
 AGND to DGND.....-0.3V to +0.3V  
 Digital Inputs to DGND.....-0.3V to +6V  
 DOUT, UPO to DGND .....-0.3V to (V<sub>DD</sub> + 0.3V)  
 FB, OUT REF to AGND.....-0.3V to (V<sub>DD</sub> + 0.3V)  
 Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
 16-Pin QSOP (derate 8mW/°C above +70°C).....667mW  
 Operating Temperature Range.....-40°C to +85°C  
 Storage Temperature Range.....-65°C to +150°C  
 Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—MAX5175

(V<sub>DD</sub> = +5V ±10%, V<sub>REF</sub> = 2.5V, AGND = DGND, FB = OUT, R<sub>L</sub> = 5kΩ, C<sub>L</sub> = 100pF referenced to ground, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

| PARAMETER                             | SYMBOL           | CONDITIONS                                                                  | MIN | TYP                   | MAX                   | UNITS  |
|---------------------------------------|------------------|-----------------------------------------------------------------------------|-----|-----------------------|-----------------------|--------|
| <b>STATIC PERFORMANCE</b>             |                  |                                                                             |     |                       |                       |        |
| Resolution                            |                  |                                                                             | 12  |                       |                       | Bits   |
| Integral Nonlinearity (Note 1)        | INL              | MAX5175A                                                                    |     |                       | ±1                    | LSB    |
|                                       |                  | MAX5175B                                                                    |     |                       | ±2                    |        |
| Differential Nonlinearity             | DNL              |                                                                             |     |                       | ±1                    | LSB    |
| Offset Error (Note 2)                 | V <sub>OS</sub>  |                                                                             |     |                       | ±10                   | mV     |
| Gain Error                            | GE               | R <sub>L</sub> = ∞                                                          |     | -0.6                  | ±4                    | LSB    |
|                                       |                  | R <sub>L</sub> = 5kΩ                                                        |     | -1.6                  | ±8                    |        |
| Power-Supply Rejection Ratio          | PSRR             |                                                                             |     | 10                    | 120                   | μV/V   |
| Output Noise Voltage                  |                  | f = 100kHz                                                                  |     | 1                     |                       | LSBp-p |
| Output Thermal Noise Density          |                  |                                                                             |     | 50                    |                       | nV/√Hz |
| <b>REFERENCE INPUT</b>                |                  |                                                                             |     |                       |                       |        |
| Reference Input Range                 | V <sub>REF</sub> |                                                                             | 0   |                       | V <sub>DD</sub> - 1.4 | V      |
| Reference Input Resistance            | R <sub>REF</sub> |                                                                             | 18  |                       |                       | kΩ     |
| <b>MULTIPLYING-MODE PERFORMANCE</b>   |                  |                                                                             |     |                       |                       |        |
| Reference -3dB Bandwidth              |                  | V <sub>REF</sub> = 0.5Vp-p + 2.5V <sub>DC</sub> , slew-rate limited         |     | 350                   |                       | kHz    |
| Reference Feedthrough                 |                  | V <sub>REF</sub> = 3.6Vp-p + 1.8V <sub>DC</sub> , f = 1kHz, code = all 0s   |     | -84                   |                       | dB     |
| Signal-to-Noise Plus Distortion Ratio | SINAD            | V <sub>REF</sub> = 1.4Vp-p + 2.5V <sub>DC</sub> , f = 10kHz, code = FFF hex |     | 84                    |                       | dB     |
| <b>DIGITAL INPUTS</b>                 |                  |                                                                             |     |                       |                       |        |
| Input High Voltage                    | V <sub>IH</sub>  |                                                                             | 3   |                       |                       | V      |
| Input Low Voltage                     | V <sub>IL</sub>  |                                                                             |     |                       | 0.8                   | V      |
| Input Hysteresis                      | V <sub>HYS</sub> |                                                                             |     | 200                   |                       | mV     |
| Input Leakage Current                 | I <sub>IN</sub>  | V <sub>IN</sub> = 0 or V <sub>DD</sub>                                      |     | 0.001                 | ±1                    | μA     |
| Input Capacitance                     | C <sub>IN</sub>  |                                                                             |     | 8                     |                       | pF     |
| <b>DIGITAL OUTPUTS</b>                |                  |                                                                             |     |                       |                       |        |
| Output High Voltage                   | V <sub>OH</sub>  | I <sub>SOURCE</sub> = 2mA                                                   |     | V <sub>DD</sub> - 0.5 |                       | V      |
| Output Low Voltage                    | V <sub>OL</sub>  | I <sub>SINK</sub> = 2mA                                                     |     | 0.13                  | 0.4                   | V      |

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

MAX5175/MAX5177

## ELECTRICAL CHARACTERISTICS—MAX5175 (continued)

(V<sub>DD</sub> = +5V ±10%, V<sub>REF</sub> = 2.5V, AGND = DGND, FB = OUT, R<sub>L</sub> = 5kΩ, C<sub>L</sub> = 100pF referenced to ground, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

| PARAMETER                                    | SYMBOL           | CONDITIONS                                                                                | MIN  | TYP  | MAX             | UNITS |
|----------------------------------------------|------------------|-------------------------------------------------------------------------------------------|------|------|-----------------|-------|
| <b>DYNAMIC PERFORMANCE</b>                   |                  |                                                                                           |      |      |                 |       |
| Voltage Output Slew Rate                     | SR               |                                                                                           |      | 0.6  |                 | V/μs  |
| Output Settling Time                         |                  | To ±0.5LSB, from 10mV to full-scale                                                       |      | 12   |                 | μs    |
| Output Voltage Swing (Note 3)                |                  |                                                                                           | 0    |      | V <sub>DD</sub> | V     |
| Current into FB                              |                  |                                                                                           | -0.1 | 0    | 0.1             | μA    |
| Time Required to Exit Shutdown               |                  |                                                                                           |      | 40   |                 | μs    |
| Digital Feedthrough                          |                  | $\overline{CS}$ = V <sub>DD</sub> ; f <sub>SCLK</sub> = 100kHz, V <sub>SCLK</sub> = 5Vp-p |      | 1    |                 | nV-s  |
| <b>POWER SUPPLIES</b>                        |                  |                                                                                           |      |      |                 |       |
| Positive Supply Voltage                      | V <sub>DD</sub>  |                                                                                           | 4.5  |      | 5.5             | V     |
| Power-Supply Current (Note 4)                | I <sub>DD</sub>  |                                                                                           |      | 0.26 | 0.35            | mA    |
| Shutdown Current (Note 4)                    |                  |                                                                                           |      | 1    | 10              | μA    |
| <b>TIMING CHARACTERISTICS</b>                |                  |                                                                                           |      |      |                 |       |
| SCLK Clock Period                            | t <sub>CP</sub>  |                                                                                           | 100  |      |                 | ns    |
| SCLK Pulse Width High                        | t <sub>CH</sub>  |                                                                                           | 40   |      |                 | ns    |
| SCLK Pulse Width Low                         | t <sub>CL</sub>  |                                                                                           | 40   |      |                 | ns    |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | t <sub>CSS</sub> |                                                                                           | 40   |      |                 | ns    |
| SCLK Rise to $\overline{CS}$ Rise Hold Time  | t <sub>CSH</sub> |                                                                                           | 0    |      |                 | ns    |
| SDI Setup Time                               | t <sub>DS</sub>  |                                                                                           | 40   |      |                 | ns    |
| SDI Hold Time                                | t <sub>DH</sub>  |                                                                                           | 0    |      |                 | ns    |
| SCLK Rise to DOUT Valid Propagation Delay    | t <sub>DO1</sub> | C <sub>LOAD</sub> = 200pF                                                                 |      |      | 80              | ns    |
| SCLK Fall to DOUT Valid Propagation Delay    | t <sub>DO2</sub> | C <sub>LOAD</sub> = 200pF                                                                 |      |      | 80              | ns    |
| SCLK Rise to $\overline{CS}$ Fall Delay      | t <sub>CS0</sub> |                                                                                           | 10   |      |                 | ns    |
| $\overline{CS}$ Rise to SCLK Rise Hold Time  | t <sub>CS1</sub> |                                                                                           | 40   |      |                 | ns    |
| $\overline{CS}$ Pulse Width High             | t <sub>CSW</sub> |                                                                                           | 100  |      |                 | ns    |

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

## ELECTRICAL CHARACTERISTICS—MAX5177

( $V_{DD}$  = +2.7V to +3.6V,  $V_{REF}$  = 1.25V, AGND = DGND, FB = OUT,  $R_L$  = 5k $\Omega$ ,  $C_L$  = 100pF referenced to ground,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A$  = +25°C.)

| PARAMETER                             | SYMBOL    | CONDITIONS                                                         | MIN            | TYP            | MAX      | UNITS           |
|---------------------------------------|-----------|--------------------------------------------------------------------|----------------|----------------|----------|-----------------|
| <b>STATIC PERFORMANCE</b>             |           |                                                                    |                |                |          |                 |
| Resolution                            |           |                                                                    | 12             |                |          | Bits            |
| Integral Nonlinearity (Note 5)        | INL       | MAX5177A                                                           |                |                | $\pm 2$  | LSB             |
|                                       |           | MAX5177B                                                           |                |                | $\pm 4$  |                 |
| Differential Nonlinearity             | DNL       |                                                                    |                |                | $\pm 1$  | LSB             |
| Offset Error (Note 2)                 | $V_{OS}$  |                                                                    |                |                | $\pm 10$ | mV              |
| Gain Error                            | GE        | $R_L = \infty$                                                     |                | -0.6           | $\pm 4$  | LSB             |
|                                       |           | $R_L = 5k\Omega$                                                   |                | -1.6           | $\pm 8$  |                 |
| Power-Supply Rejection Ratio          | PSRR      |                                                                    |                | 10             | 120      | $\mu V/V$       |
| Output Noise Voltage                  |           | $f = 100kHz$                                                       |                | 2              |          | LSBp-p          |
| Output Thermal Noise Density          |           |                                                                    |                | 50             |          | nV/ $\sqrt{Hz}$ |
| <b>REFERENCE</b>                      |           |                                                                    |                |                |          |                 |
| Reference Input Range                 | $V_{REF}$ |                                                                    | 0              | $V_{DD} - 1.4$ |          | V               |
| Reference Input Resistance            | $R_{REF}$ |                                                                    | 18             |                |          | k $\Omega$      |
| <b>MULTIPLYING-MODE PERFORMANCE</b>   |           |                                                                    |                |                |          |                 |
| Reference -3dB Bandwidth              |           | $V_{REF} = 0.5V_{p-p} + 1.25V_{DC}$ , slew-rate limited            |                | 350            |          | kHz             |
| Reference Feedthrough                 |           | $V_{REF} = 1.6V_{p-p} + 0.8V_{DC}$ , $f = 1kHz$ , code = all 0s    |                | -84            |          | dB              |
| Signal-to-Noise Plus Distortion Ratio | SINAD     | $V_{REF} = 0.9V_{p-p} + 1.25V_{DC}$ , $f = 10kHz$ , code = FFF hex |                | 78             |          | dB              |
| <b>DIGITAL INPUTS</b>                 |           |                                                                    |                |                |          |                 |
| Input High Voltage                    | $V_{IH}$  |                                                                    | 2.2            |                |          | V               |
| Input Low Voltage                     | $V_{IL}$  |                                                                    |                |                | 0.8      | V               |
| Input Hysteresis                      | $V_{HYS}$ |                                                                    |                | 200            |          | mV              |
| Input Leakage Current                 | $I_{IN}$  | $V_{IN} = 0$ or $V_{DD}$                                           |                | 0.001          | $\pm 1$  | $\mu A$         |
| Input Capacitance                     | $C_{IN}$  |                                                                    |                | 8              |          | pF              |
| <b>DIGITAL OUTPUTS</b>                |           |                                                                    |                |                |          |                 |
| Output High Voltage                   | $V_{OH}$  | $I_{SOURCE} = 2mA$                                                 | $V_{DD} - 0.5$ |                |          | V               |
| Output Low Voltage                    | $V_{OL}$  | $I_{SINK} = 2mA$                                                   |                | 0.13           | 0.4      | V               |

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

MAX5175/MAX5177

## ELECTRICAL CHARACTERISTICS—MAX5177 (continued)

( $V_{DD} = +2.7V$  to  $+3.6V$ ,  $V_{REF} = 1.25V$ ,  $AGND = DGND$ ,  $FB = OUT$ ,  $R_L = 5k\Omega$ ,  $C_L = 100pF$  referenced to ground,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

| PARAMETER                                    | SYMBOL    | CONDITIONS                                                                             | MIN  | TYP  | MAX      | UNITS      |
|----------------------------------------------|-----------|----------------------------------------------------------------------------------------|------|------|----------|------------|
| <b>DYNAMIC PERFORMANCE</b>                   |           |                                                                                        |      |      |          |            |
| Voltage Output Slew Rate                     | SR        |                                                                                        |      | 0.6  |          | V/ $\mu s$ |
| Output Settling Time                         |           | To $\pm 0.5LSB$ , from 10mV to full-scale                                              |      | 12   |          | $\mu s$    |
| Output Voltage Swing (Note 3)                |           |                                                                                        | 0    |      | $V_{DD}$ | V          |
| Current into FB                              |           |                                                                                        | -0.1 | 0    | 0.1      | $\mu A$    |
| Time Required to Exit Shutdown               |           |                                                                                        |      | 40   |          | $\mu s$    |
| Digital Feedthrough                          |           | $\overline{CS} = V_{DD}$ , $DIN = 50kHz$ , $f_{SCLK} = 100kHz$ , $V_{SCLK} = 3V_{p-p}$ |      | 1    |          | nV-s       |
| <b>POWER SUPPLIES</b>                        |           |                                                                                        |      |      |          |            |
| Positive Supply Voltage                      | $V_{DD}$  |                                                                                        | 2.7  |      | 3.6      | V          |
| Power-Supply Current (Note 4)                | $I_{DD}$  |                                                                                        |      | 0.26 | 0.35     | mA         |
| Shutdown Current (Note 4)                    |           |                                                                                        |      | 1    | 10       | $\mu A$    |
| <b>TIMING CHARACTERISTICS</b>                |           |                                                                                        |      |      |          |            |
| SCLK Clock Period                            | $t_{CP}$  |                                                                                        | 150  |      |          | ns         |
| SCLK Pulse Width High                        | $t_{CH}$  |                                                                                        | 75   |      |          | ns         |
| SCLK Pulse Width Low                         | $t_{CL}$  |                                                                                        | 75   |      |          | ns         |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS}$ |                                                                                        | 60   |      |          | ns         |
| SCLK Rise to $\overline{CS}$ Rise Hold Time  | $t_{CSH}$ |                                                                                        | 0    |      |          | ns         |
| SDI Setup Time                               | $t_{DS}$  |                                                                                        | 60   |      |          | ns         |
| SDI Hold Time                                | $t_{DH}$  |                                                                                        | 0    |      |          | ns         |
| SCLK Rise to DOUT Valid Propagation Delay    | $t_{DO1}$ | $C_{LOAD} = 200pF$                                                                     |      |      | 200      | ns         |
| SCLK Fall to DOUT Valid Propagation Delay    | $t_{DO2}$ | $C_{LOAD} = 200pF$                                                                     |      |      | 200      | ns         |
| SCLK Rise to $\overline{CS}$ Fall Delay      | $t_{CS0}$ |                                                                                        | 10   |      |          | ns         |
| $\overline{CS}$ Rise to SCLK Rise Hold Time  | $t_{CS1}$ |                                                                                        | 75   |      |          | ns         |
| $\overline{CS}$ Pulse Width High             | $t_{CSW}$ |                                                                                        | 150  |      |          | ns         |

**Note 1:** INL guaranteed between codes 16 and 4095.

**Note 2:** Offset is measured at the code that comes closest to 10mV.

**Note 3:** Accuracy is better than 1LSB for  $V_{OUT} = 10mV$  to  $V_{DD} - 180mV$ . Guaranteed by PSR test on end points.

**Note 4:**  $R_L$  = open and digital inputs are either  $V_{DD}$  or  $DGND$ .

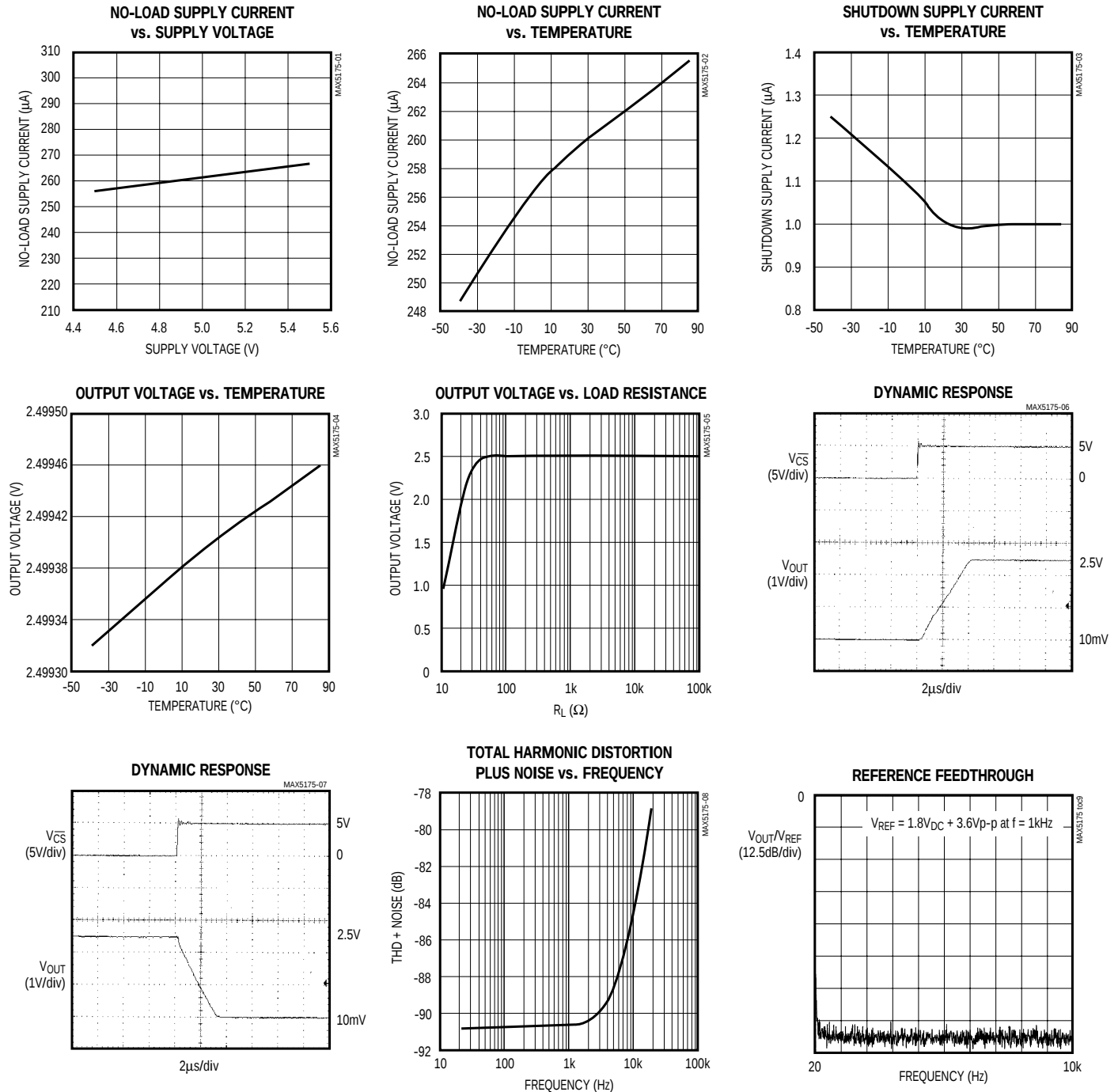
**Note 5:** INL guaranteed between codes 32 and 4095.

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

## Typical Operating Characteristics

(MAX5175:  $V_{DD} = +5V$ ,  $V_{REF} = 2.5V$ ; MAX5177:  $V_{DD} = +3V$ ,  $V_{REF} = 1.25V$ ;  $C_L = 100pF$ ,  $FB = OUT$ , code = FFF hex,  $T_A = +25^\circ C$ , unless otherwise noted.)

### MAX5175

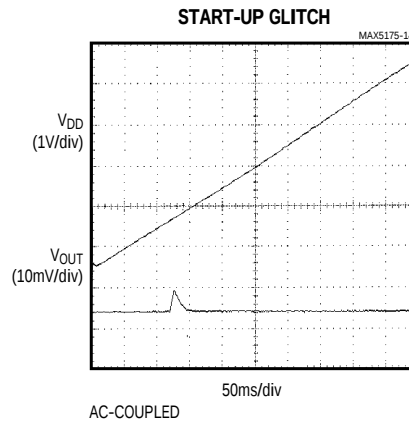
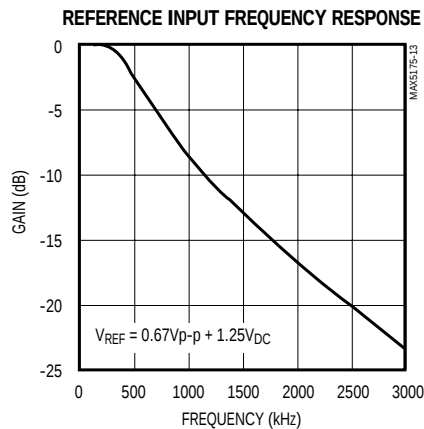
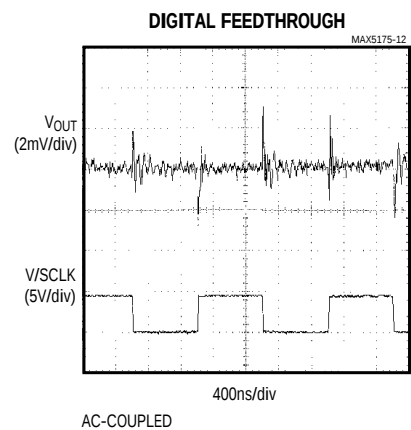
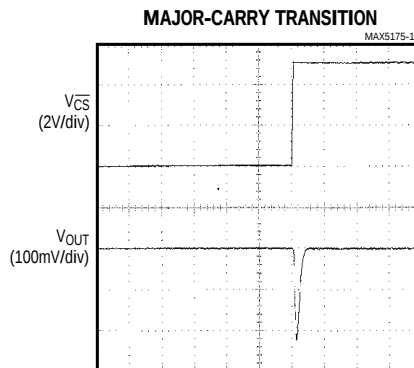
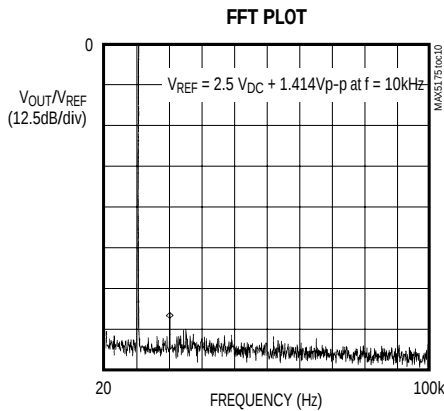


# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

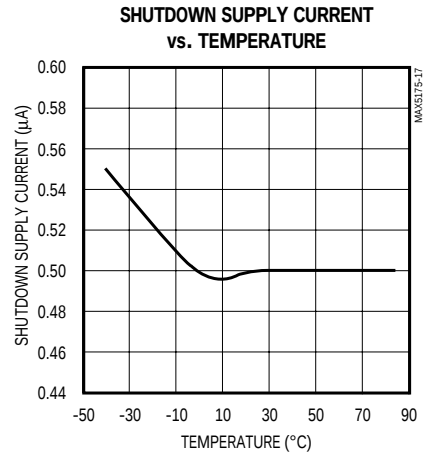
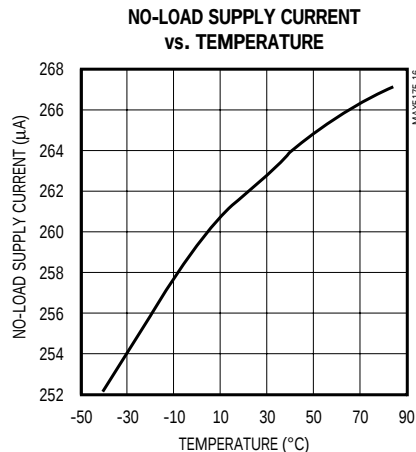
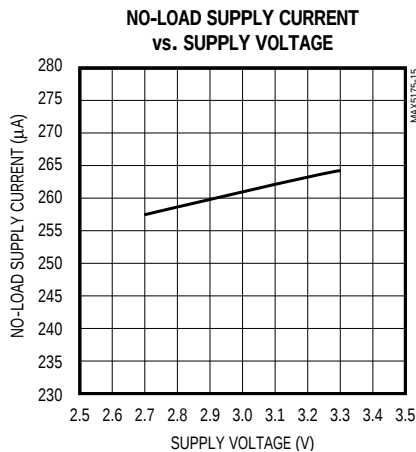
## Typical Operating Characteristics (continued)

(MAX5175:  $V_{DD} = +5V$ ,  $V_{REF} = 2.5V$ ; MAX5177:  $V_{DD} = +3V$ ,  $V_{REF} = 1.25V$ ;  $C_L = 100pF$ ,  $FB = OUT$ , code = FFF hex,  $T_A = +25^\circ C$ , unless otherwise noted.)

### MAX5175



### MAX5177



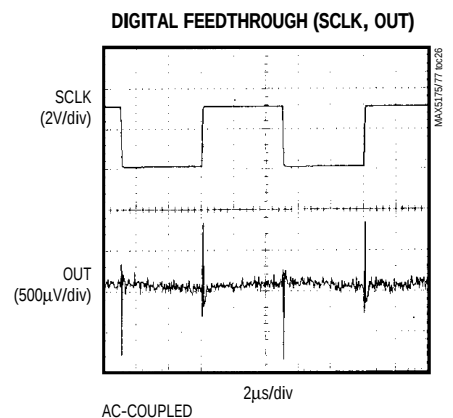
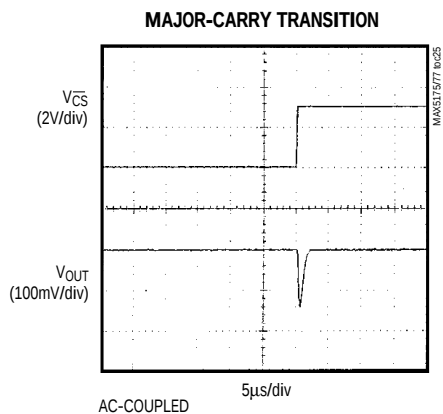
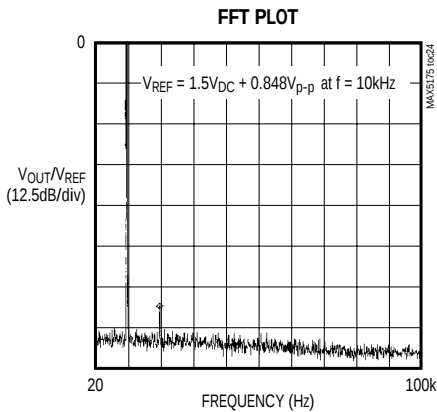
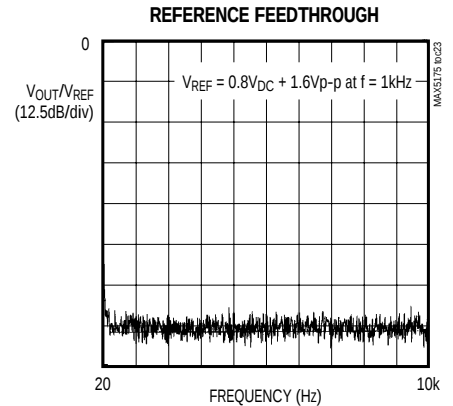
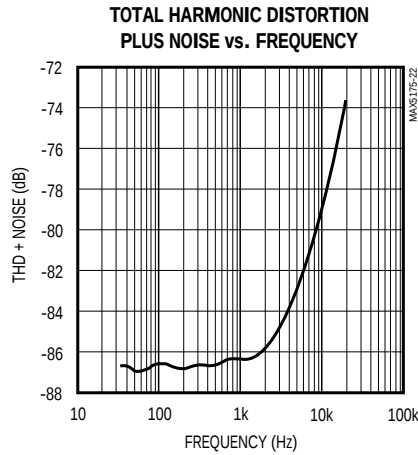
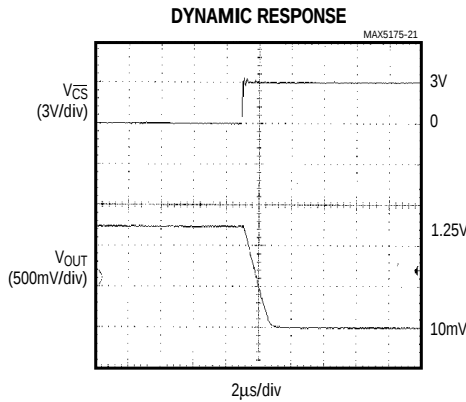
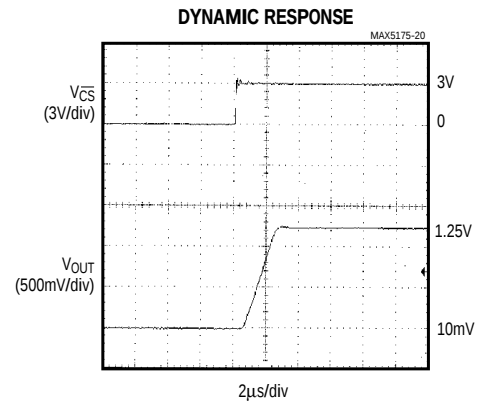
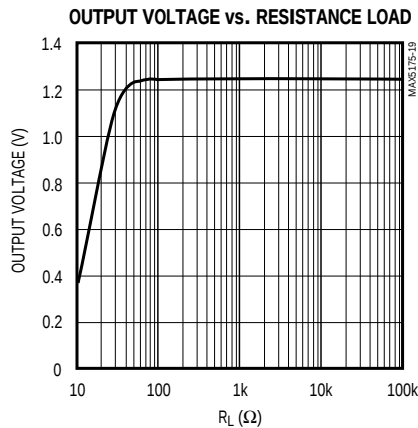
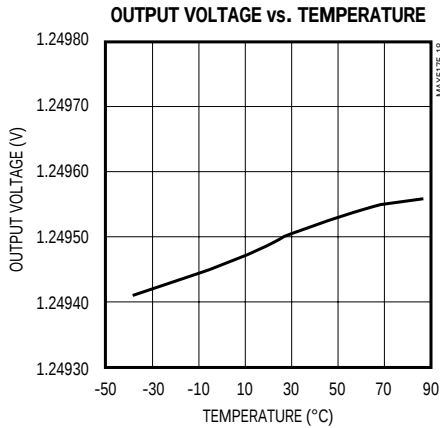
MAX5175/MAX5177

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

## Typical Operating Characteristics (continued)

(MAX5175:  $V_{DD} = +5V$ ,  $V_{REF} = 2.5V$ ; MAX5177:  $V_{DD} = +3V$ ,  $V_{REF} = 1.25V$ ;  $C_L = 100pF$ ,  $FB = OUT$ , code = FFF hex,  $T_A = +25^\circ C$ , unless otherwise noted.)

### MAX5177

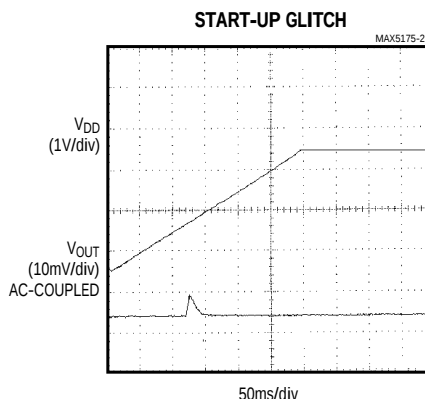
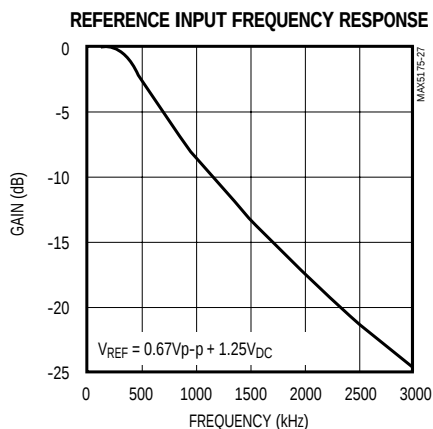


# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

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### MAX5177



## Pin Description

| PIN | NAME             | FUNCTION                                                                                                                                              |
|-----|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | FB               | Feedback Input                                                                                                                                        |
| 2   | OUT              | Voltage Output. High impedance in shutdown. Output voltage is limited to $V_{DD}$ .                                                                   |
| 3   | RS               | Reset Mode Select (digital input). Connect to $V_{DD}$ to select midscale reset output value. Connect to DGND to select 0 reset output value.         |
| 4   | $\overline{PDL}$ | Power-Down Lockout (digital input). Connect to $V_{DD}$ to allow shutdown. Connect to DGND to disable shutdown.                                       |
| 5   | $\overline{CLR}$ | Clear DAC (digital input). Clears the DAC to its predetermined output state as set by RS.                                                             |
| 6   | $\overline{CS}$  | Chip-Select Input (digital input). DIN is ignored when $\overline{CS}$ is high.                                                                       |
| 7   | DIN              | Serial-Data Input (digital input). Data is clocked in on the rising edge of SCLK.                                                                     |
| 8   | SCLK             | Serial Clock Input (digital input)                                                                                                                    |
| 9   | DGND             | Digital Ground                                                                                                                                        |
| 10  | DOUT             | Serial-Data Output                                                                                                                                    |
| 11  | UPO              | User-Programmable Output. State is set by the serial input.                                                                                           |
| 12  | SHDN             | Shutdown (digital input). Pulling SHDN high when $\overline{PDL} = V_{DD}$ places the chip in shutdown with a maximum shutdown current of $10\mu A$ . |
| 13  | AGND             | Analog Ground                                                                                                                                         |
| 14  | REF              | Reference Input. Maximum $V_{REF}$ is $V_{DD} - 1.4V$ .                                                                                               |
| 15  | N.C.             | No Connect                                                                                                                                            |
| 16  | $V_{DD}$         | Positive Supply. Bypass to AGND with a $4.7\mu F$ capacitor in parallel with a $0.1\mu F$ capacitor.                                                  |

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

## Detailed Description

The MAX5175/MAX5177 12-bit, serial, voltage-output DACs operate with a 3-wire serial interface. These devices include a 16-bit shift register and a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition, the negative terminal of the output amplifier is available. The DACs are designed with an inverted R-2R ladder network (Figure 1) that produces a weighted voltage proportional to the reference voltage.

### Reference Inputs

The reference input accepts both AC and DC values with a voltage range extending from 0 to  $V_{DD} - 1.4V$ . The following equation represents the resulting output voltage:

$$V_{OUT} = \frac{V_{REF} \cdot N \cdot GAIN}{4096}$$

where N is the numeric value of the DAC's binary input code (0 to 4095),  $V_{REF}$  is the reference voltage, and Gain is the externally set voltage gain. The maximum output voltage is  $V_{DD}$ . The reference pin has a minimum impedance of 18k $\Omega$  and is code dependent.

### Output Amplifier

The MAX5175/MAX5177's DAC output is internally buffered by a precision amplifier with a typical slew rate of 0.6V/ $\mu$ s. Access to the output amplifier's inverting input provides flexibility in output gain setting and signal conditioning (see *Applications Information*).

The output amplifier settles to  $\pm 0.5$ LSB from a full-scale transition within 12 $\mu$ s, when loaded with 5k $\Omega$  in parallel with 100pF. Loads less than 2k $\Omega$  degrade performance.

### Shutdown Mode

The MAX5175/MAX5177 feature a software- and hardware-programmable shutdown mode that reduces the typical supply current to 1 $\mu$ A. Enter shutdown by writing the appropriate input-control word as shown in Table 1 or by using the hardware shutdown function. In shutdown mode, the reference input and the amplifier output become high impedance and the serial interface remains active. Data in the input register is saved, allowing the MAX5175/MAX5177 to recall the prior output state when returning to normal operation. Exit shutdown by reloading the DAC register from the shift register, by simultaneously loading the input and DAC registers, or by toggling  $\overline{PDL}$ . When returning from shutdown, wait 40 $\mu$ s for the output to settle.

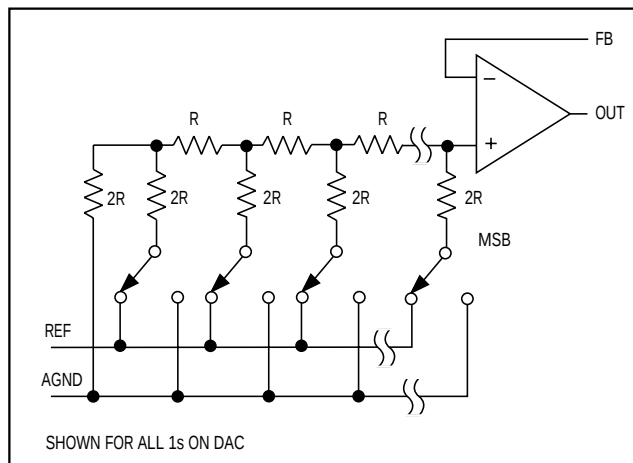


Figure 1. Simplified DAC Circuit Diagram

### Power-Down Lockout

Power-down lockout disables the software/hardware shutdown mode. A high-to-low transition on  $\overline{PDL}$  brings the device out of shutdown, returning the output to its previous state.

### Shutdown

Pulling SHDN high while  $\overline{PDL}$  is high places the MAX5175/MAX5177 in shutdown. Pulling SHDN low does not take the device out of shutdown. A high-to-low transition on  $\overline{PDL}$  or an appropriate command from the serial data line (see Table 1 for commands) is required to exit shutdown.

### Serial Interface

The 3-wire serial interface is compatible with SPI, QSPI (Figure 2), and MICROWIRE (Figure 3) interface standards. The 16-bit serial input word consists of two control bits, 12 bits of data (MSB to LSB), and two sub-bits.

The control bits determine the MAX5175/MAX5177's response as outlined in Table 1. The digital inputs are double buffered, which allows any of the following:

- Loading the input register without updating the DAC register
- Updating the DAC register from the input register
- Updating the input and DAC registers simultaneously.

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

The MAX5175/MAX5177 accept one 16-bit packet or two 8-bit packets sent while  $\overline{CS}$  remains low. The devices allow the following to be configured:

- Clock edge on which serial data output (DOUT) is clocked out
- State of the user-programmable logic output
- Reset state.

Specific commands for setting these are shown in Table 1.

The general timing diagram in Figure 4 illustrates how the MAX5175/MAX5177 acquire data.  $\overline{CS}$  must go low at least  $t_{CSS}$  before the rising edge of the serial clock (SCLK). With  $\overline{CS}$  low, data is clocked into the register on the rising edge of SCLK. The maximum serial clock frequency guaranteed for proper operation is 10MHz for the MAX5175 and 6MHz for the MAX5177. See Figure 5 for a detailed timing diagram of the serial interface.

**Table 1. Serial-Interface Programming Commands**

| 16-BIT SERIAL WORD |    |                   |        | FUNCTION                                                                                                   |
|--------------------|----|-------------------|--------|------------------------------------------------------------------------------------------------------------|
| C1                 | C0 | D11.....D0        | S1, S0 |                                                                                                            |
| 0                  | 0  | 12-bit DAC data   | 00     | Load input register; DAC registers are unchanged.                                                          |
| 0                  | 1  | 12-bit DAC data   | 00     | Load input register; DAC registers are updated (start up DAC with new data).                               |
| 1                  | 0  | xxxx xxxx xxxx    | xx     | Update DAC register from input register (start up DAC with data previously stored in the input registers). |
| 1                  | 1  | 0 0 x x xxxx xxxx | xx     | No operation (NOP).                                                                                        |
| 1                  | 1  | 0 1 x x xxxx xxxx | xx     | Shut down DAC (provided $\overline{PDL} = 1$ ).                                                            |
| 1                  | 1  | 1 0 0 x xxxx xxxx | xx     | UPO goes low (default).                                                                                    |
| 1                  | 1  | 1 0 1 x xxxx xxxx | xx     | UPO goes high.                                                                                             |
| 1                  | 1  | 1 1 0 x xxxx xxxx | xx     | Mode 1, DOUT clocked out on SCLK's rising edge.                                                            |
| 1                  | 1  | 1 1 1 x xxxx xxxx | xx     | Mode 0, DOUT clocked out on SCLK's falling edge (default).                                                 |

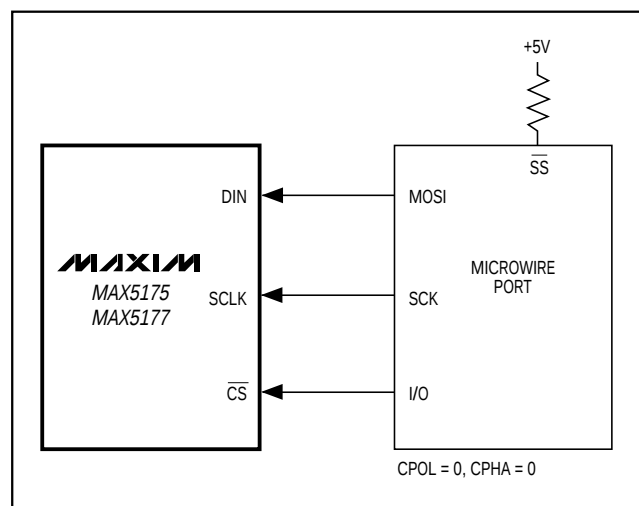


Figure 2. Connections for SPI/QSPI Standards

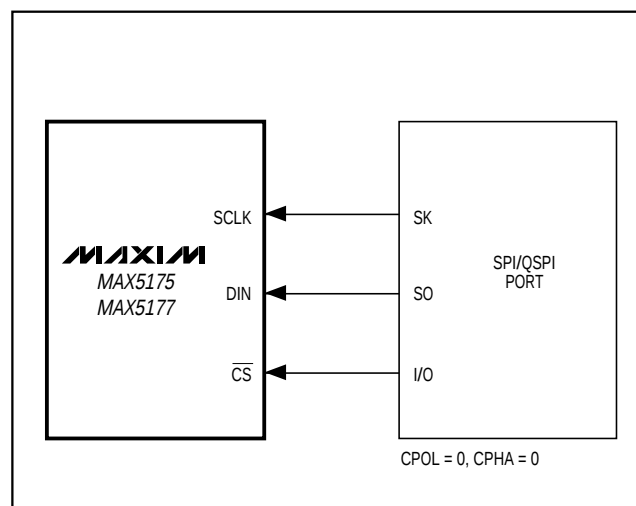


Figure 3. Connections for MICROWIRE

## Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

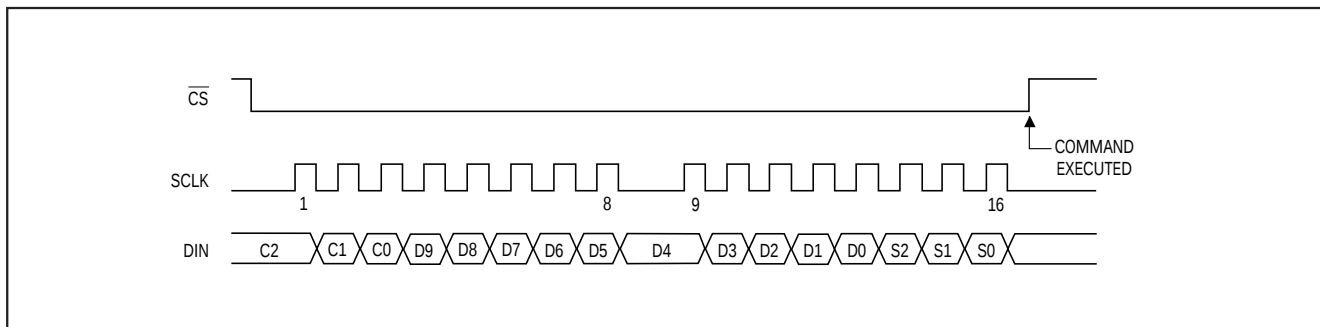


Figure 4. Serial-Interface Timing Diagram

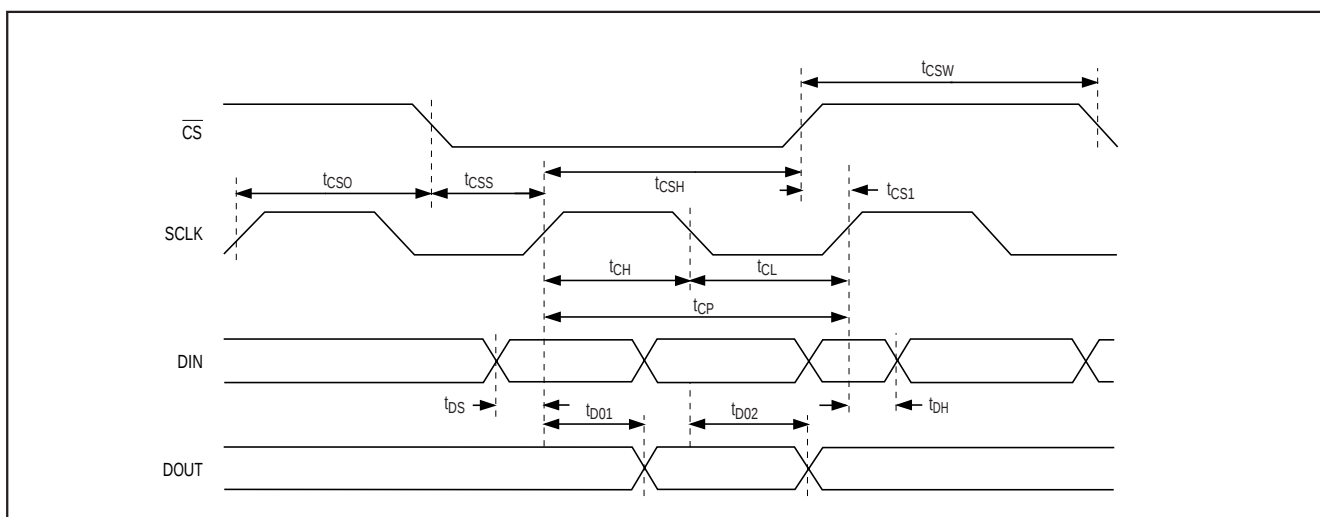


Figure 5. Detailed Serial-Interface Timing Diagram

### Serial-Data Output (DOUT)

The serial-data output (DOUT) is the internal shift register's output and allows for daisy-chaining of multiple devices as well as data readback (see *Applications Information*). By default upon start-up, data shifts out of DOUT on the serial clock's rising edge (Mode 0) and provides a lag of 16 clock cycles, thus maintaining SPI, QSPI, and MICROWIRE compatibility. However, if the device is programmed for Mode 1, then the output data lags DIN by 16.5 clock cycles and is clocked out on the serial clock's rising edge. During shutdown, DOUT retains its last digital state prior to shutdown.

### User-Programmable Logic Output (UPO)

The UPO allows control of an external device through the serial interface, thereby reducing the number of microcontroller I/O pins required. During power-down, this output will retain its digital state prior to shutdown.

When  $\overline{\text{CLR}}$  is pulled low, UPO will reset to its programmed default state. See Table 1 for specific commands to control the UPO.

### Reset (RS) and Clear ( $\overline{\text{CLR}}$ )

The MAX5175/MAX5177 offers a clear pin ( $\overline{\text{CLR}}$ ) which resets the output voltage. If  $\text{RST} = \text{DGND}$ , then  $\overline{\text{CLR}}$  resets the output voltage to the minimum voltage (0 if no offset is introduced). If  $\text{RST} = \text{VDD}$ , then  $\overline{\text{CLR}}$  resets the output voltage to midscale. In either case,  $\overline{\text{CLR}}$  will reset UPO to its programmed default state.

## MAX5175/MAX5177

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

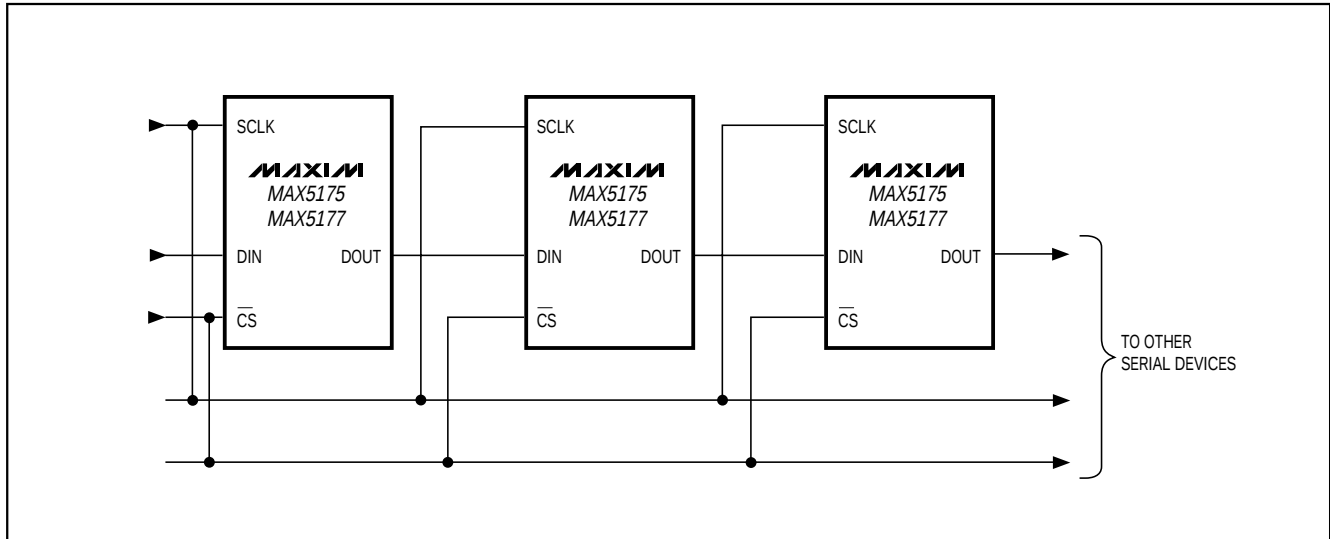


Figure 8. Daisy-Chaining MAX5175/MAX5177s

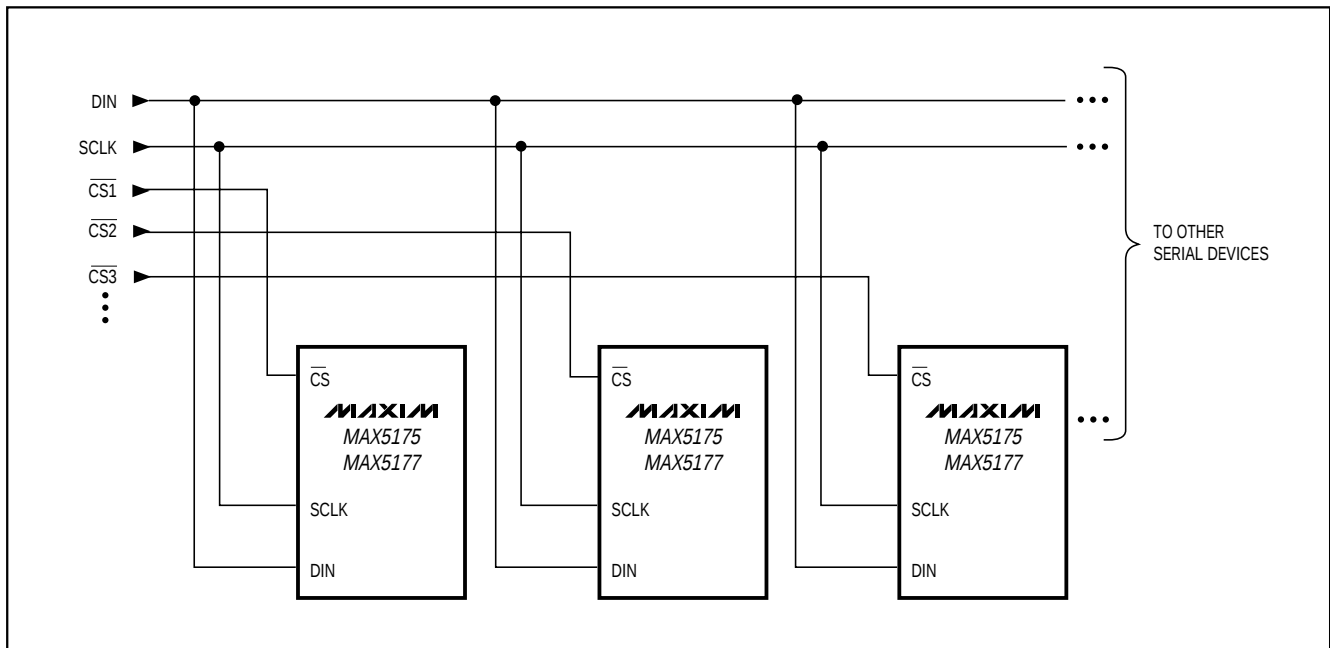


Figure 9. Multiple MAX5175/MAX5177s Sharing Common DIN and SCLK Lines

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

## Using an AC Reference

The MAX5175/MAX5177 accept reference voltages containing AC components, as long as the reference voltage remains between 0 and  $V_{DD} - 1.4V$ . Figure 10 shows a technique for applying a sine-wave signal to REF. The reference voltage must remain above AGND.

## Digitally Programmable Current Source

The circuit of Figure 11 places an NPN transistor (2N3904 or similar) within the op amp feedback loop to implement a digitally programmable, unidirectional current source. The output current is calculated with the following equation:

$$I_{OUT} = \frac{V_{REF} \cdot N}{R \cdot 4096}$$

where N is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 11.

## Power-Supply and Layout Considerations

Wire-wrap boards are not recommended. For optimum system performance, use printed circuit boards with separate analog and digital ground planes. Connect the two ground planes together at the low-impedance

power-supply source. Connect DGND and AGND pins together at the IC. The best ground connection is achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may infiltrate the DAC's analog portion.

Bypass the power supply with a  $4.7\mu F$  capacitor in parallel with a  $0.1\mu F$  capacitor to AGND. Minimize capacitor lead lengths to reduce inductance. If noise becomes an issue, use shielding and/or ferrite beads to increase isolation.

In order to maintain INL and DNL performance, as well as gain drift, it is extremely important to provide the lowest possible reference output impedance at the DAC reference input pin. INL degrades if the series resistance on the REF pin exceeds  $0.1\Omega$ . The same consideration must be made for the AGND pin.

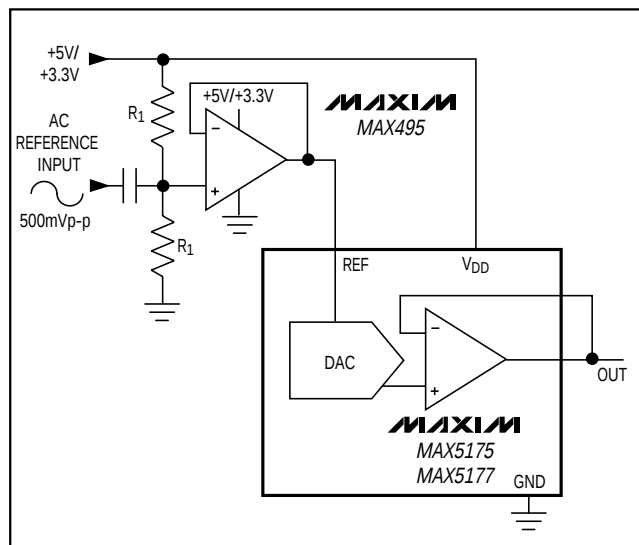


Figure 10. AC Reference Input Circuit

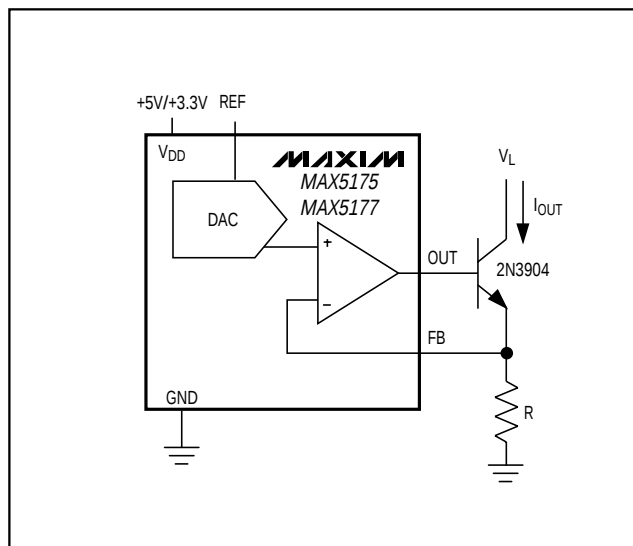
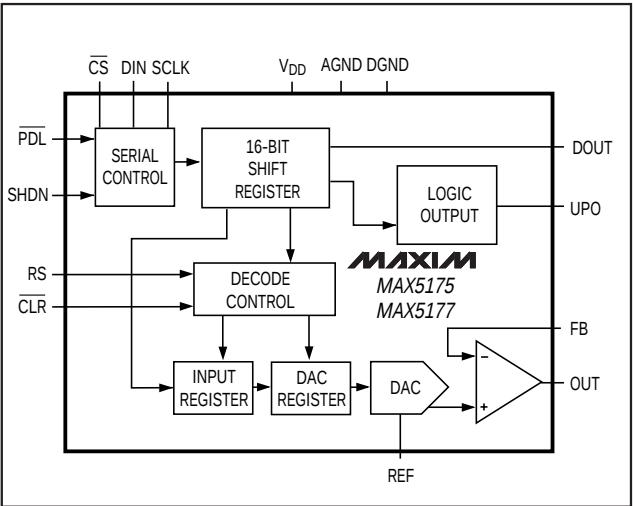


Figure 11. Digitally Programmable Current Source

# Low-Power, Serial, 12-Bit DACs with Force/Sense Voltage Output

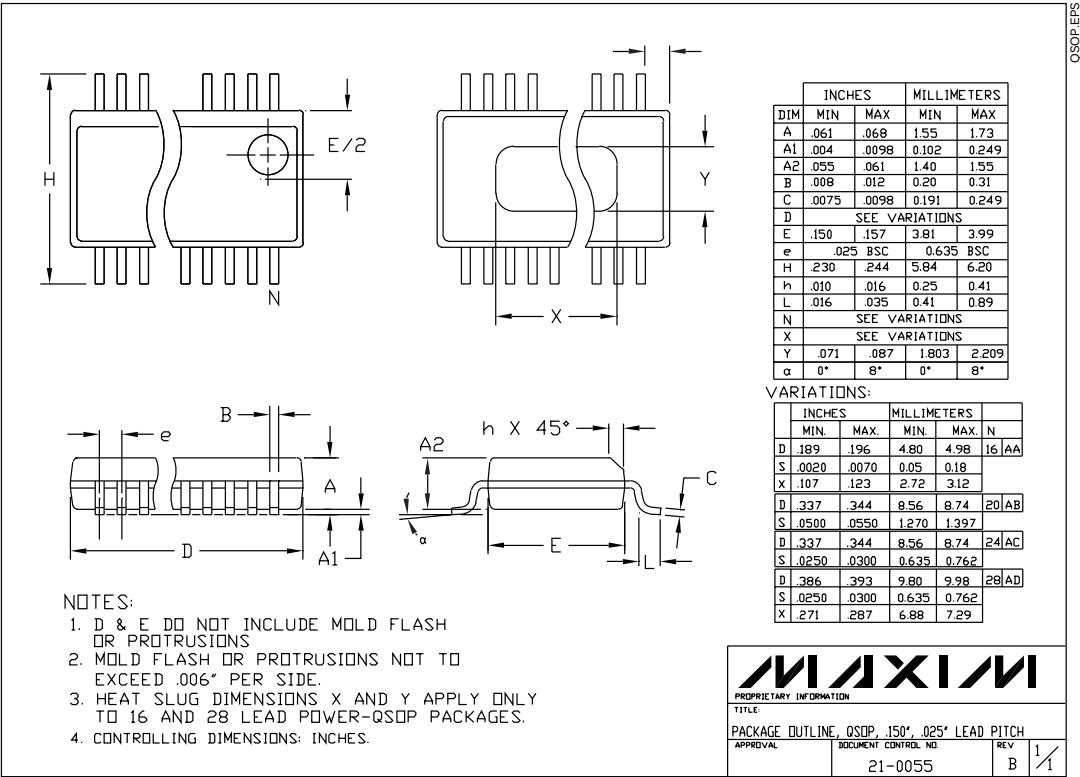
## Functional Diagram



## Chip Information

TRANSISTOR COUNT: 3457

## Package Information



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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