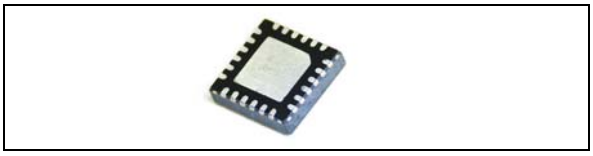
STUSB1700

USB Type-C™ source controller with high voltage protections

Datasheet - preliminary data



Features

- Single power role support: source mode
- Type-C attach and cable orientation detection
- Configurable current advertising through external control pins
- Configurable start-up profiles through NVM
- Integrated V_{BUS} voltage monitoring and discharge path
- Short-to-V_{BUS} protections on CC pins (22 V) and V_{BUS} pins (28 V)
- High and/or low voltage power supply:
  - V_{SYS} = [3.0 V; 5.5 V]
  - V_{DD} = [4.1 V; 22 V]
- Integrated power switch for V_{CONN} supply:
  - programmable current limit up to 600 mA
  - overcurrent, overvoltage and thermal protection
  - undervoltage lockout
- Integrated V_{CONN} discharge path
- Accessory mode support
- I^2C interface and interrupt (optional connection to MCU)
- Temperature range: -40 °C up to 105 °C
- ESD: 4 kV HBM - 1.5 kV CDM
- AEC-Q100 qualified
- Certification test ID 1100100

Applications

- Automotive: USB car chargers (single and dual port), 12 V car chargers accessories, infotainment systems
- Smart plugs, wall adapters and chargers
- Power hubs and docking stations
- Notebook host port
- LCD monitors & TV
- Power bank
- Any Type-C source device

Description

The STUSB1700 is an IC controller, fully compliant with the USB Type-C cable and connector specification (rev. 1.2), which addresses 5 V USB Type-C port management on the host side. It is fully autonomous and allows the advertising of the current capability to be managed by external pins. It is suited to implement power sharing capabilities, or external temperature protection mechanism with current capability adjustment.

The STUSB1700 is designed for a broad range of applications and can handle the following USB Type-C functions: attach detection, plug orientation detection, host to device connection, V_{CONN} support, and V_{BUS} configuration. Thanks to its 20 V technology, it implements high voltage protection features against short-circuits to V_{BUS} up to 28 V. The device is fully customizable thanks to an integrated non-volatile memory.

Table 1. Device summary

Order code	AEC-Q100	USB Type-C	Package	Marking
STUSB1700YQTR	Yes	Rev 1.2 +ECR	QFN24 EP 4x4 mm wettable flanks	1700Y

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Functional description

The STUSB1700 is a USB Type-C controller IC. It is designed to interface with the Type-C receptacle on the host side. It is used to establish and manage the source-to-sink connection between two USB Type-C host and device ports.

The STUSB1700 major role is to:

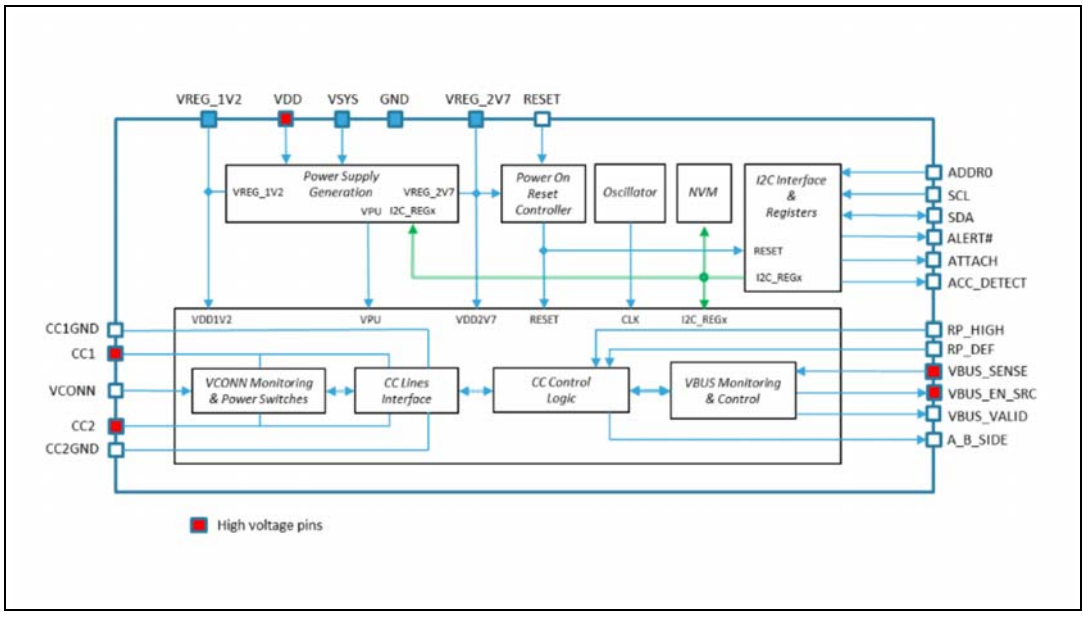
1. Detect the connection between two USB Type-C ports (attach detection).
2. Establish a valid source-to-sink connection.
3. Determine the attached device mode: sink or accessory.
4. Resolve cable orientation and twist connections to establish USB data routing (mux control).
5. Configure and monitor V_{BUS} power path.
6. Manage V_{BUS} power capability: USB default, Type-C medium or Type-C high current mode.
7. Configure V_{CONN} when required.

The STUSB1700 also provides:

- Low power standby mode
- I^2C interface and interrupt (optional connection to the MCU)
- Start-up configuration customization: static through NVM and/or dynamic through I^2C
- High voltage protection
- Accessory mode detection

1.1 Block overview

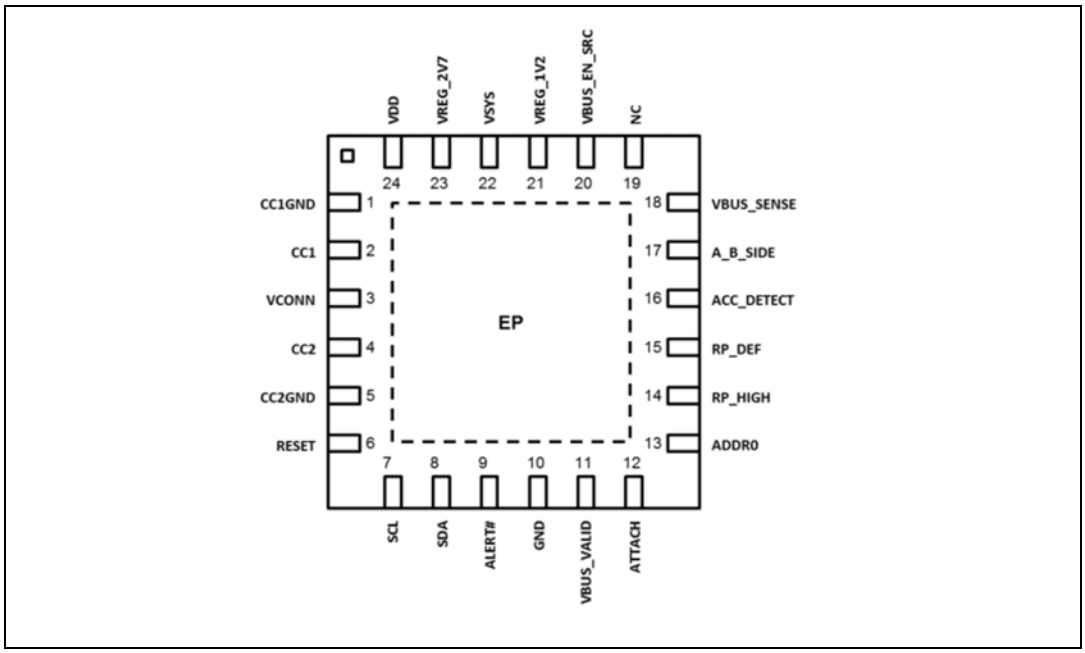
Figure 1. Functional block diagram



2 Inputs / Outputs

2.1 Pinout

Figure 2. STUSB1700 pin connections



2.2 Pin list

Table 2. Pin function list

Pin	Name	Type	Description	Typical connection
1	CC1GND	GND	Ground reference channel 1	Ground
2	CC1	HV AIO	Type-C configuration channel 1	Type-C receptacle A5
3	VCONN	PWR	Power input for active plug	5 V power source
4	CC2	HV AIO	Type-C configuration channel 2	Type-C receptacle B5
5	CC2GND	GND	Ground reference channel 2	Ground
6	RESET	DI	Reset input (active high)	
7	SCL	DI	I^2C clock input	To I²C master, ext. pull-up
8	SDA	DI/OD	I^2C data input/output, active low open drain	To I²C master, ext. pull-up
9	ALERT#	OD	I^2C interrupt, active low open drain	To I²C master, ext. pull-up
10	GND	GND	Ground	Ground
11	VBUS_VALID	OD	V_{BUS} detection, active low open drain	To MCU if any, ext. pull-up
12	ATTACH	OD	Attachment detection, active low open drain	To MCU if any, ext. pull-up
13	ADDR0	DI	I²C device address setting (see *Section 4: I²C interface*)	Static
14	RP_HIGH	DI	Logic level input to select between 1.5 A and 3.0 A USB Type-C current advertising	Static or to MCU if any
15	RP_DEF	DI	Logic level input to select between USB default current (500 mA or 900mA) or USB Type-C current advertising	Static or to MCU if any
16	ACC_DETECT	OD	Accessory device detection, active low open drain	To MCU if any, ext. pull-up
17	A_B_SIDE	OD	Cable orientation, active low open drain	USB super speed mux select, ext. pull-up
18	VBUS_SENSE	HV AI	V_{BUS} voltage monitoring and discharge path	From V_{BUS}
19	NC	-	-	Floating
20	VBUS_EN_SRC	HV OD	V_{BUS} source power path enable, active low open drain	To switch or power system, ext. pull-up
21	VREG_1V2	PWR	1.2 V internal regulator output	1 µF typ. decoupling capacitor
22	VSYS	PWR	Power supply from system	From power system, connect to ground if not used

Table 2. Pin function list

Pin	Name	Type	Description	Typical connection
23	VREG_2V7	PWR	2.7 V internal regulator output	1 µF typ. decoupling capacitor
24	VDD	HV PWR	Power supply from USB power line	From V_{BUS}
-	EP	GND	Exposed pad is connected to ground	To ground

Table 3. Pin function descriptions

Type	Description
D	Digital
A	Analog
O	Output pad
I	Input pad
IO	Bidirectional pad
OD	Open drain output
PD	Pull-down
PU	Pull-up
HV	High voltage
PWR	Power
GND	Ground

2.3 Pin description

2.3.1 CC1 / CC2

CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable.

2.3.2 CC1GND / CC2GND

CC1GND and CC2GND are used as a reference to ground and must be connected to ground.

2.3.3 V_{CONN}

This power input is connected to a power source that can be a 5 V power supply, or a lithium battery. It is used to provide power supply to the local plug. It is internally connected to power switches that are protected against short circuit and overvoltage. This does not require any protection on the input side. When a valid source-to-sink connection is determined and V_{CONN} power switches enabled, V_{CONN} is provided by the source to the unused CC pin (see *Section 3.3: VCONN supply*).

2.3.4 RESET

Active high reset.

2.3.5 I²C interface pins

Table 4. I²C interface pins list

Name	Description
SCL	I²C clock – need external pull-up
SDA	I²C data – need external pull-up
ALERT#	I²C interrupt – need external pull-up
ADDR0	I²C device address bit (see *Section 4: I²C interface*)

2.3.6 GND

Ground.

2.3.7 VBUS_VALID

This pin is asserted during attachment when V_{BUS} is detected on VBUS_SENSE pin and VBUS voltage is within the valid operating range. The V_{BUS} valid state is also advertised in a dedicated I²C register bit (see *Section 5.1: Register description*).

2.3.8 ATTACH

This pin is asserted when a valid source-to-sink connection is established. It is also asserted when a connection to an accessory device is detected. The attachment state is also advertised in a dedicated I^2C register bit (see *Section 5.1: Register description*).

2.3.9 RP_HIGH / RP_DEF

These input pins are used to adjust externally the Rp value on the CC pins to advertise the current capability the source can supply as defined in the USB Type-C standard specification. These pins can be used dynamically to implement systems with power-sharing capabilities or with external temperature protection mechanism to adapt the current capability to the system temperature.

Table 5. USB Type-C current advertising with RP control pins

USB Type-C Rp value	RP_DEF Logic level	RP_HIGH Logic level	Source current capability
Rp = Default USB	0	X	Default USB current (500 mA or 900 mA)
Rp = 1.5 A	1	0	1.5 A USB Type-C current
Rp = 3 A	1	1	3.0 A USB Type-C current

2.3.10 ACC_DETECT

This pin is asserted when an audio accessory device or a debug accessory device is detected (see *Section 3.7: Accessory modes detection*).

2.3.11 A_B_SIDE

This output pin provides cable orientation. It is used to establish USB SuperSpeed signals routing. The cable orientation is also provided by an internal I^2C register (see *Section 5.1: Register description*. This signal is not required in case of USB 2.0 support.

Table 6. USB data mux select

Value	CC pin position
HiZ	CC1 pin is attached to CC line
0	CC2 pin is attached to CC line

2.3.12 VBUS_SENSE

This input pin is used to sense V_{BUS} presence, monitor V_{BUS} voltage and discharge V_{BUS} on USB Type-C receptacle side.

2.3.13 VBUS_EN_SRC

This pin allows the outgoing V_{BUS} power to be enabled when the connection to a sink is established and V_{BUS} is in the valid operating range. The open drain output allows a PMOS transistor to be directly driven. The logic value of the pin is also advertised in a dedicated I^2C register bit (see *Section 5.1: Register description*).

2.3.14 VREG_1V2

This pin is used only for external decoupling of 1.2 V internal regulator. The recommended decoupling capacitor is: 1 µF typ. (0.5 µF min; 10 µF max).

2.3.15 VSYS

This is the low power supply from the system, if any. It can be connected directly to a single cell Lithium battery or to the system power supply delivering 3.3 V or 5 V. It is recommended to connect the pin to ground when it is not used.

2.3.16 VREG_2V7

This pin is used only for external decoupling of 2.7 V internal regulator. The recommended decoupling capacitor: 1 µF typ. (0.5 µF min; 10 µF max).

2.3.17 VDD

This is the power supply from the USB power line for applications powered by V_{BUS}.

This pin can be used to sense the voltage level of the main power supply providing the V_{BUS}. It allows UVLO and OVLO thresholds to be considered independently on the VDD pin as additional conditions to enable the V_{BUS} power path through VBUS_EN_SRC pin (see *Section 3.2.3: VBUS power path assertion*). When the UVLO threshold detection is enabled, the VDD pin must be connected to the main power supply to establish the connection and to assert the V_{BUS} power path.

3 Features description

3.1 CC interface

The STUSB1700 controls the connection to the configuration channel (CC) pins, CC1 and CC2, through two main blocks, the CC line interface block and the CC control logic block.

The CC lines interface block is used to:

- Configure the pull-up termination mode on the CC pins
- Monitor the CC pin voltage values relative to the attachment detection thresholds
- Configure V_{CONN} on the unconnected CC pin when required
- Protect the CC pins against over voltage

The CC control logic block is used to:

- Execute the Type-C FSM relative to the Type-C source power mode
- Determine the electrical state for each CC pin relative to the detected thresholds
- Evaluate the conditions relative to the CC pin states and the V_{BUS} voltage value to transition from one state to another in the Type-C FSM
- Detect and establish a valid source-to-sink connection
- Determine the attached device mode: sink or accessory
- Determine cable orientation to allow external routing of the USB data
- Manage V_{BUS} power capability: USB default, Type-C medium or Type-C high current mode
- Handle hardware faults.

The CC control logic block implements the Type-C FSM corresponding to the source power role with accessory support.

3.2 V_{BUS} power path control

3.2.1 V_{BUS} monitoring

The V_{BUS} monitoring block supervises from the VBUS_SENSE pin the V_{BUS} voltage on the USB Type-C receptacle side.

It is used to check that V_{BUS} is within a valid voltage range:

- to establish a valid source-to-sink connection according to USB Type-C standard specification,
- to enable safely the V_{BUS} power path through VBUS_EN_SRC pin.

It allows to detect unexpected V_{BUS} voltage conditions such as under voltage or over voltage relative to the valid V_{BUS} voltage range. When such conditions occur, the STUSB1700 reacts as follows:

- at attachment, it prevents the source-to-sink connection and the V_{BUS} power path assertion,
- after attachment, it deactivates the source-to-sink connection, disables the V_{BUS} power path and goes into error recovery state.

The valid V_{BUS} voltage range is defined from the V_{BUS} nominal voltage by a high threshold voltage and a low threshold voltage whose nominal values are respectively V_{BUS}+5% and V_{BUS}-5%. The nominal threshold limits can be shifted by fraction of V_{BUS} from +1% to +15% for the high threshold voltage and from -1% to -15% for the low threshold voltage. It means the threshold limits can vary from V_{BUS}+5% to V_{BUS}+20% for the high limit and from V_{BUS}-5% to V_{BUS}-20% for the low limit.

The threshold limits are preset by default in the NVM with different shift coefficients (see *Section 8.3: Electrical and timing characteristics*). The threshold limits can be changed independently through NVM programming (see *Section 6: Start-up configuration*) and also by software during attachment through the I^2C interface (see *Section 5.1: Register description*).

3.2.2 V_{BUS} discharge

The monitoring block also handles the internal VBUS discharge path connected to the VBUS_SENSE pin. The discharge path is activated at detachment, or when the device goes into the error recovery state (see *Section 3.6: Hardware fault management*).

The V_{BUS} discharge path is enabled by default in the NVM and can be disabled through NVM programming only (see *Section 6: Start-up configuration*). The discharge time duration is also preset by default in the NVM (see *Section 8.3: Electrical and timing characteristics*). The discharge time duration can be changed through NVM programming (see *Section 6: Start-up configuration*) and also by software through the I^2C interface (see *Section 5.1: Register description*).

3.2.3 V_{BUS} power path assertion

The STUSB1700 can control the assertion of the V_{BUS} power path on the USB Type-C port, directly or indirectly, through the VBUS_EN_SRC pin.

The tables below summarize the configurations of the STUSB1700 and the operation conditions that determine the electrical value of the VBUS_EN_SRC pin during system operation.

Table 7. Conditions for V_{BUS} power path assertion in source power role

Pin	Electrical value	Operation conditions			
		Type-C attached state	VDD **pin monitoring**	**VBUS_SENSE pin monitoring**	**Comment**
VBUS_EN_SRC	0	Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC	$V_{DD} > V_{DDUVLO}$ if UVLO threshold detection enabled and/or $V_{DD} < V_{DDOVLO}$ if OVLO threshold detection enabled	$V_{BUS} < V_{MONUSBH}$ and $V_{BUS} > V_{MONUSBL}$ if V_{BUS} voltage range detection enabled or $V_{BUS} > V_{THUSB}$ if V_{BUS} voltage range detection disabled	The signal is asserted only if all the valid operation conditions are met.
	HiZ	Any other state	$V_{DD} < V_{DDUVLO}$ if UVLO threshold detection enabled or $V_{DD} > V_{DDOVLO}$ if OVLO threshold detection enabled	$V_{BUS} > V_{MONUSBH}$ or $V_{BUS} < V_{MONUSBL}$ if V_{BUS} voltage range detection enabled or $V_{BUS} < V_{THUSB}$ if V_{BUS} voltage range detection disabled	The signal is de-asserted when at least one non valid operation condition is met.

As specified in the USB Type-C standard specification, the attached state “Attached.SRC” is reached only if the voltage on the V_{BUS} receptacle side is at vSafe0V condition when a connection is detected.

"Type-C attached state” refers to the Type-C FSM states as defined in the USB Type-C standard specification and as described in the I^2C register CC_OPERATION_STATUS (see *Section 5.1: Register description*).

“VDD pin monitoring” refers to the UVLO and OVLO thresholds detection on VDD pin that can be activated through NVM programming (see *Section 6: Start-up configuration*) and also by software through the I^2C interface (see *Section 5.1: Register description*). When the UVLO and/or OVLO threshold detection is activated, the VBUS_EN_SRC pin is asserted only if the device is attached and the valid threshold conditions on VDD are met. Once the VBUS_EN_SRC pin is asserted, the V_{BUS} monitoring is done on VBUS_SENSE pin instead of the VDD pin.

“VBUS_SENSE pin monitoring” relies, by default, on a valid V_{BUS} voltage range defined by a high limit $V_{MONUSBH}$ and a low limit $V_{MONUSBL}$. The voltage range condition can be disabled to consider UVLO threshold detection instead. The monitoring condition of the V_{BUS} voltage can be changed through NVM programming (see *Section 6: Start-up configuration*) and also by software through the I^2C interface (see *Section 5.1: Register description*). The VBUS_EN_SRC pin is maintained asserted as long as the device is attached and a valid voltage condition on the V_{BUS} is met.

See *Section 8.3: Electrical and timing characteristics* for the threshold voltages description and value on VDD and VBUS_SENSE pins.

3.3 V_{CONN} supply

3.3.1 V_{CONN} input voltage

V_{CONN} is a regulated supply used to power circuits in the plug of USB3.1 full-featured cables and other accessories. V_{CONN} nominal operating voltage is 5.0 V +/- 5%.

3.3.2 V_{CONN} application conditions

The VCONN pin of the STUSB1700 is connected to each CC pin (CC1 and CC2) across independent power switches.

The STUSB1700 applies V_{CONN} only to the CC pin not connected to the CC wire when all below conditions are met:

- V_{CONN} power switches are enabled
- A valid connection to a sink is achieved
- Ra presence is detected on the unwired CC pin
- A valid power source is applied to the V_{CONN} pin with respect to a predefined UVLO threshold.

3.3.3 V_{CONN} monitoring

The V_{CONN} monitoring block detects whether V_{CONN} power supply is available on the VCONN pin. It is used to check that V_{CONN} voltage is above a pre-defined under-voltage lockout (UVLO) threshold to allow the enabling of the V_{CONN} power switches.

The default value of the UVLO threshold is 4.65 V typical for powered cables operating at 5 V. It can be changed by software to 2.65 V typical to support V_{CONN}-powered accessories that are operating down to 2.7 V (see *Section 5.1: Register description*).

3.3.4 V_{CONN} discharge

The behavior of Type-C FSMs is extended with an internal V_{CONN} discharge path capability on CC pins in Source power role. The discharge path is activated during 250 ms from Sink detachment detection. This feature is disabled by default. It can be activated through NVM programming (see *Section 6: Start-up configuration*) and also by software through the I^2C interface (see *Section 5.1: Register description*).

3.3.5 V_{CONN} control and status

The supplying conditions of V_{CONN} across STUSB1700 are managed through the I^2C interface. Different I^2C registers and bits are used specifically for this purpose (see *Section 5.1: Register description*).

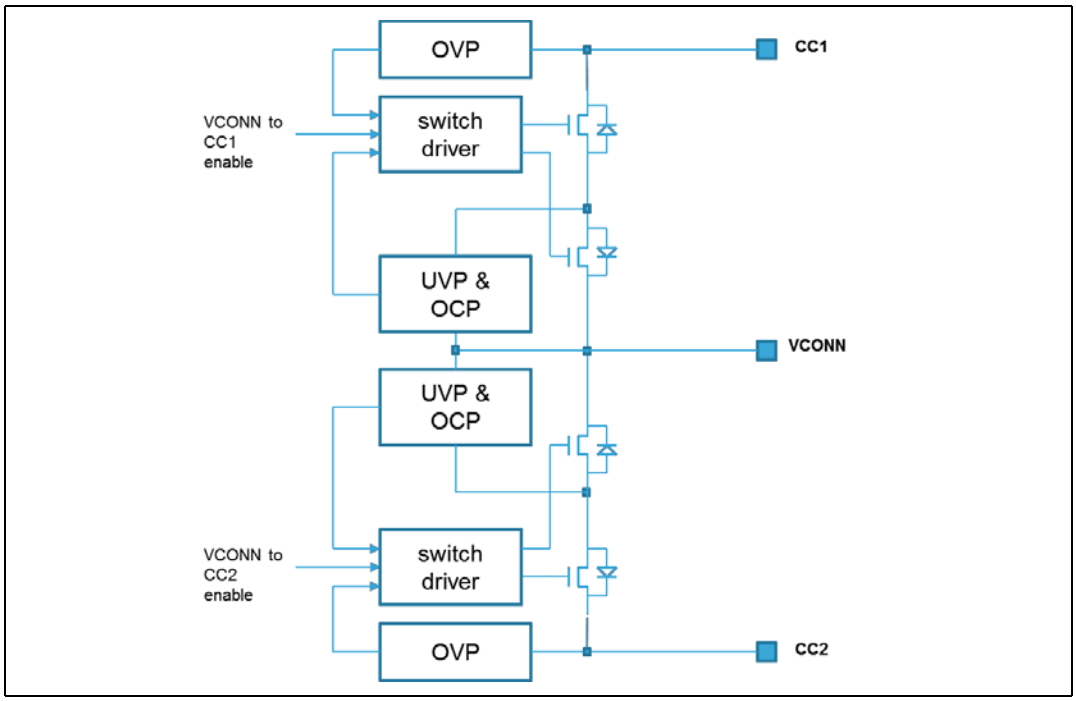
3.3.6 V_{CONN} power switches

The STUSB1700 integrates two current limited high-side power switches with protections that tolerate high voltage up to 22 V on the CC pins.

Each V_{CONN} power switch is presenting the following features:

- Soft-start to limit inrush current
- Constant current mode over-current protection
- Adjustable current limit
- Thermal protection
- Under-voltage and over-voltage protections
- Reverse current and reverse voltage protections

Figure 3. V_{CONN} to CC1 and CC2 power switches protections



Current limit programming

The current limit can be set within the range 100 mA to 600 mA by step of 50 mA. The default current limit is programmed through NVM programming (see *Section 6: Start-up configuration*) and can be changed by software through I^2C interface (see *Section 5.1: Register description*). At power-on or after a reset, the current limit takes the default value preset in the NVM.

Fault management

The table below summarizes the different fault conditions that could occur during operation of the switch and the associated responses. An I^2C alert is generated when a fault condition happens (see *Section 5.1: Register description*).

Table 8. Fault management conditions

Fault types	Fault conditions	Expected actions
Short-circuit	CC output pin shorted to ground via very low resistive path causing rapid current surge.	Power switch limits the current and reduces the output voltage. I^2C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits.
Over-current	CC output pin connected to a load that sinks current above programmed limit.	Power switch limits the current and reduces the output voltage. I^2C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits.
Over-heating	Junction temperature exceeding 145 °C due to any reason.	Power switch is disabled immediately until the temperature falls below 145 ° minus hysteresis of 15 °C. I^2C alert is asserted immediately thanks to THERMAL_FAULT bit. STUSB1700 goes into transient error recovery state.
Under-voltage	V_{CONN} input voltage drops below UVLO threshold minus hysteresis.	Power switch is disabled immediately until the input voltage rises above the UVLO threshold. I^2C alert is asserted immediately thanks to VCONN_PRESENCE bit.
Over-voltage	CC output pin voltage exceeds maximum operating limit of 6.0 V.	Power switch is opened immediately until the voltage falls below the voltage limit. I^2C alert is asserted immediately thanks to VCONN_SW_OVP_FAULT bits.
Reverse current	CC output pin voltage exceeds V_{CONN} input voltage when the power switch is turned-off.	The reverse biased body diode of the back-to-back MOS switches is naturally disabled preventing current to flow from the CC output pin to the input.
Reverse voltage	CC output pin voltage exceeds V_{CONN} input voltage of more than 0.35 V for 5 V when the power switch is turned-on.	Power switch is opened immediately until the voltage difference falls below the voltage limit. I^2C alert is asserted immediately thanks to VCONN_SW_RVP_FAULT bits.

3.4 Low power standby mode

The STUSB1700 proposes a standby mode to reduce the device power consumption when no device is connected to the USB Type-C port. It is disabled by default and can be activated through NVM programming (see *Section 6: Start-up configuration*).

When activated, the STUSB1700 enters in standby mode at power up, or after a reset, or after a disconnection. In this mode, the CC interface and the voltages monitoring blocks are turned off. Only a monitoring circuitry is maintained active on the CC pins to detect a connection. When the connection is detected, all the internal circuits are turned on to allow normal operation.

3.5 High voltage protection

The STUSB1700 can be safely used in systems or connected to systems that handle high voltage on the V_{BUS} power path. The device integrates an internal circuitry on the CC pins that tolerate high voltage and ensures protection up to 22 V in case of unexpected short

circuits with the V_{BUS} or in case of a connection to a device supplying high voltage on the V_{BUS}.

3.6 Hardware fault management

The STUSB1700 handles hardware fault conditions related to the device itself and to the V_{BUS} power path during system operation.

When such conditions happen, the circuit goes into a transient error recovery state named ErrorRecovery in the Type-C FSM. The error recovery state is equivalent to force a detach event.

When entering in this state, the device de-asserts the VBUS power path by disabling VBUS_EN_SRC pin, and it removes the terminations from the CC pins during several tens of milliseconds. Then, it transitions to the unattached state.

The STUSB1700 goes into error recovery state when at least one condition listed below is met:

- If an over-temperature is detected, the “THERMAL_FAULT” bit set to 1b
- If an internal pull-up voltage on CC pins is below UVLO threshold, the “VPU_VALID” bit set to 0b
- If an over-voltage is detected on the CC pins, the “VPU_OVP_FAULT” bit set to 1b
- If the VBUS voltage is out of the valid voltage range during attachment, the “VBUS_VALID” bit set to 0b
- If an under-voltage is detected on the VDD pin during attachment when UVLO detection is enabled, the “VDD_UVLO_DISABLE” bit set to 0b
- If an over-voltage is detected on the VDD pin during attachment when OVLO detection is enabled, the “VDD_OVLO_DISABLE” bit set to 0b

The I^2C register bits mentioned into brackets give either the state of the hardware fault when it occurs, or the setting condition to detect the hardware fault (see *Section 5.1: Register description*).

3.7 Accessory modes detection

The STUSB1700 supports the detection of audio accessory mode and debug accessory mode as defined in the USB Type-C standard specification.

3.7.1 Audio accessory mode detection

The STUSB1700 detects an audio accessory device when both CC1 and CC2 pins are pulled down to the ground by a Ra resistor from connected device. The audio accessory detection is advertised by the ACC_DETECT pin as well as through the CC_ATTACHED_MODE bits of I^2C register CC_CONNECTION_STATUS (see *Section 5.1: Register description*).

3.7.2 Debug accessory mode detection

The STUSB1700 detects a connection to a debug and test system (DTS). The debug accessory detection is advertised by the ACC_DETECT pin as well as through the CC_ATTACHED_MODE bits of the I^2C register CC_CONNECTION_STATUS (see

Section 5.1: Register description). The VBUS_EN_SRC pin is also asserted to allow enabling the VBUS power path as defined in the USB Type-C standard specification.

A debug accessory device is detected when both the CC1 and CC2 pins are pulled down to ground by a Rd resistor from the connected device. The orientation detection is performed in two steps as described in the table below. The A_B_SIDE pin indicates the orientation of the connection. The orientation detection is advertised through TYPEC_FSM_STATE bits of the I^2C register CC_OPERATION_STATUS (see *Section 5.1: Register description*).

Table 9. Orientation detection

#	CC1 pin (CC2 pin)	CC2 pin (CC1 pin)	Detection process	A_B_SIDE pin CC1/CC2 (CC2/CC1)	Orientation detection state TYPEC_FSM_STATE bits value
1	Rd	Rd	1st step: debug accessory mode detected	HiZ (HiZ)	UnorientedDebugAccessory.SRC
2	Rd	≤ Ra	2nd step: orientation detected (DTS presents a resistance to GND with a value ≤ Ra on its CC2 pin)	HiZ (0)	OrientedDebugAccessory.SRC

4 I²C interface

4.1 Read and write operations

The I²C interface is used to configure, control and read the operation status of the device. It is compatible with the Philips I²C Bus® (version 2.1). The I²C is a slave serial interface based on two signals:

- SCL - Serial clock line: input clock used to shift data
- SDA - Serial data line: input/output bidirectional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity.

The bidirectional data line supports transfers up to 400 Kbit/s (fast mode). The data are shifted to and from the chip on the SDA line, MSB first.

The first bit must be high (START) followed by the 7-bit device address and the read/write control bit.

Two 7-bit device addresses are available for STUSB1700 thanks to external programming of DevADDR0 through ADDR0 pin setting, i.e. 0x28 or 0x29. It allows to connect two STUSB1700 devices on the same I²C bus.

Table 10. Device address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DevADDR6	DevADDR5	DevADDR4	DevADDR3	DevADDR2	DevADDR1	DevADDR0	R/W
0	1	0	1	0	0	ADDR0	0/1

Table 11. Register address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RegADDR7	RegADDR6	RegADDR5	RegADDR4	RegADDR3	RegADDR2	RegADDR1	RegADDR0

Table 12. Register data format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 4. Read operation

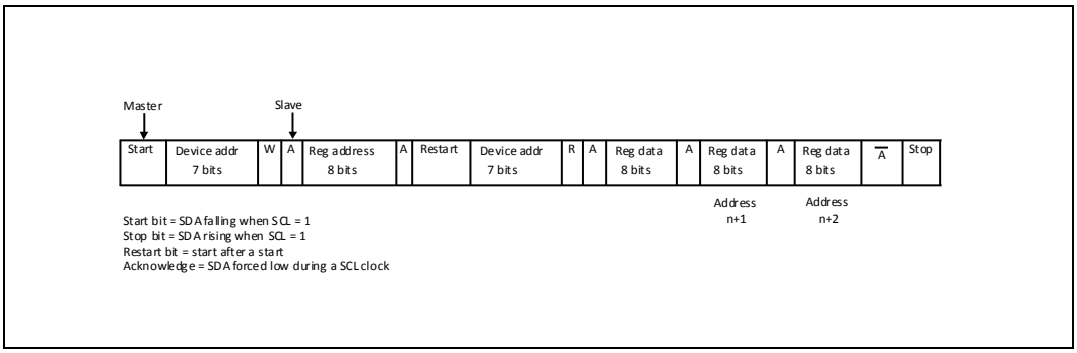
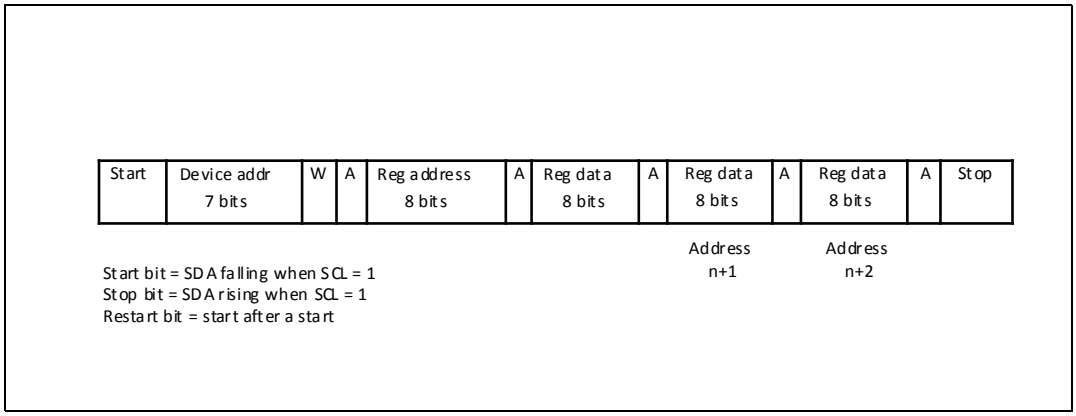


Figure 5. Write operation



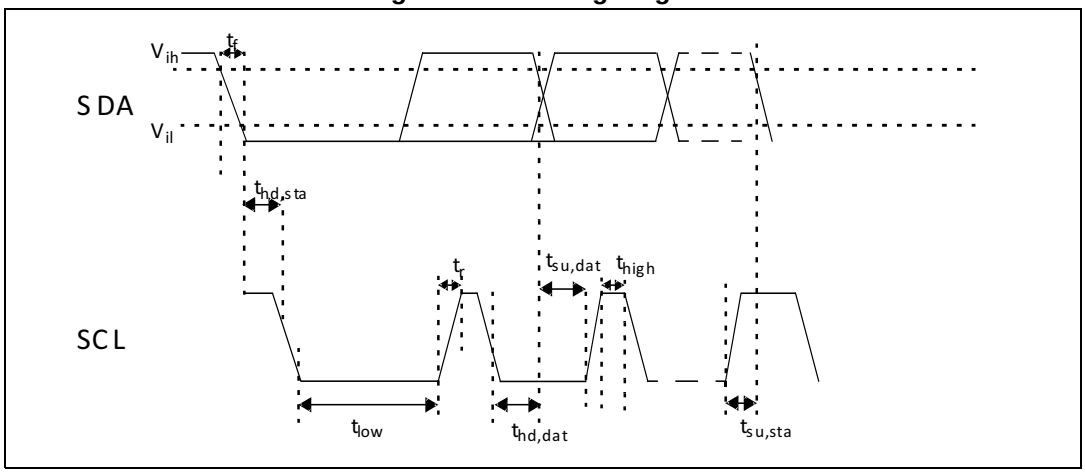
4.2 Timing specifications

The device uses a standard slave I²C channel at speed up to 400 kHz.

Table 13. I²C timing parameters - VDD = 5 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{scl}	SCL clock frequency	0	-	400	kHz
$t_{hd,sta}$	Hold time (repeated) START condition	0.6	-	-	µs
t_{low}	LOW period of the SCL clock	1.3	-	-	µs
t_{high}	HIGH period of the SCL clock	0.6	-	-	µs
$t_{su,dat}$	Setup time for repeated START condition	0.6	-	-	µs
$t_{hd,dat}$	Data hold time	0.04	-	0.9	µs
$t_{su,dat}$	Data setup time	100	-	-	µs
t_r	Rise time of both SDA and SCL signals	20 + 0.1 C_b	-	300	ns
t_f	Fall time of both SDA and SCL signals	20 + 0.1 C_b	-	300	ns
$t_{su,sto}$	Setup time for STOP condition	0.6	-	-	µs
t_{buf}	Bus free time between a STOP and START condition	1.3	-	-	µs
C_b	Capacitive load for each bus line	-	-	400	pF

Figure 6. I²C timing diagram



5 I²C register map

Table 14. Register access legend

Access code	Expanded name	Description
RO	Read only	Register can be read only
R/W	Read/write	Register can be read or written
RC	Read and clear	Register can be read and is cleared after read

Table 15. STUSB1700 register map overview

Address	Register name	Access	Description
00h to 0Ah	Reserved	RO	Do not use
0Bh	ALERT_STATUS	RC	Alerts register linked to transition registers
0Ch	ALERT_STATUS_MASK_CTRL	R/W	Allows the interrupt mask on the ALERT_STATUS register to be changed
0Dh	CC_CONNECTION_STATUS_TRANS	RC	Alerts about transition in CC_CONNECTION_STATUS register
0Eh	CC_CONNECTION_STATUS	RO	Gives status on CC connection
0Fh	MONITORING_STATUS_TRANS	RC	Alerts about transition in MONITORING_STATUS register
10h	MONITORING_STATUS	RO	Gives status on V_{BUS} and V_{CONN} voltage monitoring
11h	CC_OPERATION_STATUS	RO	Gives status on CC operation modes
12h	HW_FAULT_STATUS_TRANS	RC	Alerts about transition in HW_FAULT_STATUS register
13h	HW_FAULT_STATUS	RO	Gives status on hardware faults
14h to 17h	Reserved	RO	Do not use
18h	CC_CAPABILITY_STATUS_CTRL	R/W	Gives status on the advertised current capability, and allows the V_{CONN} supply capabilities to be changed
19h to 1Dh	Reserved	RO	Do not use
1Eh	CC_VCONN_SWITCH_CTRL	R/W	Allows the current limit of V_{CONN} power switches to be changed
1Fh	Reserved	RO	Do not use

Table 15. STUSB1700 register map overview (continued)

Address	Register name	Access	Description
20h	VCONN_MONITORING_CTRL	R/W	Allows the monitoring conditions of V_{CONN} voltage to be changed
21h	Reserved	RO	Do not use
22h	VBUS_MONITORING_RANGE_CTRL	R/W	Allows the voltage range for V_{BUS} monitoring to be changed
23h	RESET_CTRL	R/W	Controls the device reset by software
24h	Reserved	RO	Do not use
25h	VBUS_DISCHARGE_TIME_CTRL	R/W	Allows the V_{BUS} discharge time to be changed
26h	VBUS_DISCHARGE_STATUS	RO	Gives status on V_{BUS} discharge path activation
27h	VBUS_ENABLE_STATUS	RO	Gives status on V_{BUS} power path activation
28h to 2Dh	Reserved	RO	Do not use
2Eh	VBUS_MONITORING_CTRL	R/W	Allows the monitoring conditions of V_{BUS} voltage to be changed
2Fh	Reserved	RO	Do not use

5.1 Register description

The reset column specified in the registers description below defines the default value of the registers at power-up or after a reset. The reset values with (NVM) index correspond to the user-defined parameters that can be customized by NVM re-programming if needed (see *Section 6: Start-up configuration*).

5.1.1 ALERT_STATUS

Address: 0Bh

Access: RC

Note: This register indicates an Alert has occurred.

Table 16. ALERT_STATUS register

Bit	Field name	Reset	Description
7	Reserved	0b	Do not use
6	CC_CONNECTION_STATUS_AL	0b	0b: cleared 1b: change occurred on CC_CONNECTION_STATUS_TRANS register
5	MONITORING_STATUS_AL	1b	0b: cleared 1b: change occurred on MONITORING_STATUS_TRANS register
4	HW_FAULT_STATUS_AL	0b	0b: cleared 1b: change occurred on HW_FAULT_STATUS_TRANS register
3:0	Reserved	0000b	Do not use

When a bit value change occurs on one of the mentioned transition register, it automatically sets the corresponding alert bit in ALERT_STATUS register.

5.1.2 ALERT_STATUS_MASK_CTRL

Address: 0Ch

Access: R/W

Note: This register is used to mask event interrupt and prevent the assertion of the alert bit in the ALERT_STATUS register when the corresponding bit defined below is set to 1.

Table 17. ALERT_STATUS_MASK_CTRL register

Bit	Field name	Reset	Description
7	Reserved	1b	Do not use
6	CC_CONNECTION_STATUS_AL_MASK	1b (NVM)	0b: interrupt unmasked 1b: interrupt masked
5	MONITORING_STATUS_AL_MASK	1b (NVM)	0b: interrupt unmasked 1b: interrupt masked
4	HW_FAULT_STATUS_AL_MASK	1b (NVM)	0b: interrupt unmasked 1b: interrupt masked
3:0	Reserved	1111b	Do not use

The condition for generating an active-low ALERT signal is:

[ALERT_STATUS bitwise AND (NOT ALERT_STATUS_MASK)] <> 0

5.1.3 CC_CONNECTION_STATUS_TRANS

Address: 0Dh

Access: RC

Note: This register indicates a bit value change has occurred in CC_CONNECTION_STATUS register.

Table 18. CC_CONNECTION_STATUS_TRANS register

Bit	Field name	Reset	Description
7:1	Reserved	0000000b	Do not use
0	CC_ATTACH_TRANS	0b	0b: cleared 1b: transition occurred on CC_ATTACH bit

5.1.4 CC_CONNECTION_STATUS

Address: 0Eh

Access: RO

Note: This register gives the connection state of the CC pins and on associated operating modes of the device.

Table 19. CC_CONNECTION_STATUS register

Bit	Field name	Reset	Description
7:5	CC_ATTACHED_MODE	000b	000b: no device attached 001b: sink attached 010b: do not use 011b: debug accessory attached 100b: audio accessory attached 101b: do not use 110b: do not use 111b: do not use
4	DEVICE_POWER_MODE	0b (NVM)	0b: operating in normal power mode 1b: operating in standby power mode
3	CC_POWER_ROLE	0b	0b: not operating 1b: operating as a source
2	Reserved	0b	Do not use
1	CC_VCONN_SUPPLY	0b	0b: V_{CONN} is not supplied on CC pin 1b: V_{CONN} is supplied on CC pin
0	CC_ATTACH	0b	0b: not attached 1b: attached

The DEVICE_POWER_MODE bit indicates the power consumption mode of the device at start-up and during operation:

- In normal mode, all the internal circuits are turned on
- In standby mode, the CC interface and the voltage monitoring blocks remain off until a connection is detected.

The standby power mode is disabled by default and can be activated through NVM programming (see *Section 6: Start-up configuration*).

The CC_POWER_ROLE bit is relevant only when a connection is established and the device is attached.

5.1.5 MONITORING_STATUS_TRANS

Address: 0Fh

Access: RC

Note: This register indicates a bit value change has occurred in MONITORING_STATUS register.

Table 20. MONITORING_STATUS_TRANS register

Bit	Field name	Reset	Description
7:4	Reserved	0000b	Do not use
3	VBUS_VALID_TRANS	0b	0b: cleared 1b: transition occured on VBUS_VALID bit
2	VBUS_VSAFE0V_TRANS	0b	0b: cleared 1b: transition occured on VBUS_VSAFE0V bit
1	VBUS_PRESENCE_TRANS	0b	0b: cleared 1b: transition occured on VBUS_PRESENCE bit
0	VCONN_PRESENCE_TRANS	0b	0b: cleared 1b: transition occured on VCONN_PRESENCE bit

5.1.6 MONITORING_STATUS

Address: 10h

Access: RO

Note: This register informs on the current status of V_{BUS} and V_{CONN} voltages monitoring done respectively on VBUS_SENSE pin and V_{CONN} pin.

Table 21. MONITORING_STATUS register

Bit	Field name	Reset	Description
7:4	Reserved	0000b	Do not use
3	VBUS_VALID	0b	0b: V_{BUS} is outside valid voltage range 1b: V_{BUS} is within valid voltage range
2	VBUS_VSAFE0V	1b	0b: V_{BUS} is above vSafe0V threshold 1b: V_{BUS} is below VSafe0V threshold
1	VBUS_PRESENCE	0b	0b: V_{BUS} is below UVLO threshold 1b: V_{BUS} is above UVLO threshold
0	VCONN_PRESENCE	0b or 1b	0b: V_{CONN} is below UVLO threshold 1b: V_{CONN} is above UVLO threshold

The default value of the valid V_{BUS} voltage range can be changed in the VBUS_MONITORING_RANGE_CTRL register during operation.

The V_{BUS} vSafe0V threshold is set in the VBUS_MONITORING_CTRL register. It is used in source power role as a Type-C FSM condition to establish a valid device attachment.

The V_{BUS} UVLO threshold is set by hardware.

The V_{CONN} UVLO threshold is set in the VCONN_MONITORING_CTRL register.

The reset value of the VCONN_PRESENCE bit is:

- 0b when V_{CONN} is not supplied on the VCONN pin, or when V_{CONN} is supplied and the voltage level is below the UVLO threshold, or when the VCONN threshold detection circuit is disabled.
- 1b when V_{CONN} is supplied on the VCONN pin and the voltage level is above UVLO threshold.

See *Section 8.3: Electrical and timing characteristics* for the threshold voltages description and value on VBUS_SENSE and VCONN pins.

5.1.7 CC_OPERATION_STATUS

Address: 11h

Access: RO

Note: This register informs on the current status of the device operating modes with respect to the Type-C FSM states as defined in the USB Type-C standard specification. This status is informative only and is not used to trigger any alert.

Table 22. CC_OPERATION_STATUS register

Bit	Field name	Reset	Description
7	CC_PIN_ATTACHED	0b	0b: CC1 is attached
			1b: CC2 is attached
6:5	Reserved	00b	Do not use
4:0	TYPEC_FSM_STATE	08h	00h: reserved
			01h: reserved
			02h: reserved
			03h: reserved
			04h: reserved
			05h: reserved
			06h: reserved
			07h: reserved
			08h: Unattached.SRC
			09h: AttachWait.SRC
			0Ah: Attached.SRC
			0Bh: reserved
			0Ch: reserved
			0Dh: Unattached.Accessory
			0Eh: AttachWait.Accessory
			0Fh: AudioAccessory
			10h: UnorientedDebugAccessory.SRC
			11h: reserved
			12h: reserved
			13h: ErrorRecovery
			14h: reserved
			15h: reserved
			16h: reserved
			17h: reserved
			18h: UnattachedWait.SRC (V_{CONN} intermediate discharge state)
			19h: OrientedDebugAccessory.SRC

Table 22. CC_OPERATION_STATUS register (continued)

Bit	Field name	Reset	Description
4:0	TYPEC_FSM_STATE	08h	1Ah: reserved
			1Bh: reserved
			1Ch: reserved
			1Dh: reserved
			1Eh: reserved
			1Fh: reserved

The CC_PIN_ATTACHED bit indicates which CC pin is connected to the CC line. Its value is consistent with the logic level of the A_B_SIDE output pin providing cable orientation. The TYPEC_FSM_STATE bits indicate the current state of the Type-C FSM corresponding to the power mode defined in the CC_POWER_MODE_CTRL register.

5.1.8 HW_FAULT_STATUS_TRANS

Address: 12h

Access: RC

Note: This register indicates a bit value change has occurred in HW_FAULT_STATUS register. It alerts also when the over-temperature condition is met.

Table 23. HW_FAULT_STATUS_TRANS register

Bit	Field name	Reset	Description
7	THERMAL_FAULT	0b	0b: cleared 1b: junction temperature is above temperature threshold of 145° C
6	Reserved	0b	Do not use
5	VPU_OVP_FAULT_TRANS	0b	0b: cleared 1b: transition occured on VPU_OVP_FAULT bit
4	VPU_VALID_TRANS	0b	0b: cleared 1b: transition occured on VPU_VALID bit
3	Reserved	0b	Do not use
2	VCONN_SW_RVP_FAULT_TRANS	0b	0b: cleared 1b: transition occured on VCONN_SW_RVP_FAULT bits
1	VCONN_SW_OCP_FAULT_TRANS	0b	0b: cleared 1b: transition occured on VCONN_SW_OCP_FAULT bits
0	VCONN_SW_OVP_FAULT_TRANS	0b	0b: cleared 1b: transition occured on VCONN_SW_OVP_FAULT bits

5.1.9 HW_FAULT_STATUS

Address: 13h

Access: RO

Note: This register provides information on hardware fault conditions related to the internal pull-up voltage in Source power role and to the V_{CONN} power switches.

Table 24. HW_FAULT_STATUS register

Bit	Field name	Reset	Description
7	VPU_OVP_FAULT	0b	0b: voltage on CC pins is below OVP threshold of 6.0 V 1b: voltage on CC pins is above OVP threshold of 6.0 V
6	VPU_VALID	0b	0b: pull-up voltage on CC pins is below UVLO threshold of 2.8 V 1b: pull-up voltage on CC pins is above UVLO threshold of 2.8 V (safe condition)
5	VCONN_SW_RVP_FAULT_CC1	0b	0b: no reverse voltage on V_{CONN} power switch connected to CC1 1b: reverse voltage detected on V_{CONN} power switch connected to CC1
4	VCONN_SW_RVP_FAULT_CC2	0b	0b: no reverse voltage on V_{CONN} power switch connected to CC2 1b: reverse voltage detected on V_{CONN} power switch connected to CC2
3	VCONN_SW_OCP_FAULT_CC1	0b	0b: no short circuit or over current on V_{CONN} power switch connected to CC1 1b: short circuit or over current detected on V_{CONN} power switch connected to CC1
2	VCONN_SW_OCP_FAULT_CC2	0b	0b: no short circuit or over current on V_{CONN} power switch connected to CC2 1b: short circuit or over current detected on V_{CONN} power switch connected to CC2
1	VCONN_SW_OVP_FAULT_CC1	0b	0b: no over voltage on V_{CONN} power switch connected to CC1 1b: over voltage detected on V_{CONN} power switch connected to CC1
0	VCONN_SW_OVP_FAULT_CC2	0b	0b: no over voltage on V_{CONN} power switch connected to CC2 1b: over voltage detected on V_{CONN} power switch connected to CC2

The VPU_VALID and VPU_OVP_FAULT bits are related to the internal pull-up voltage applied on the CC pins when the device is operating in source power role. They give information on an internal supply issue that could prevent the device to detect a valid connection to a distant device.

5.1.10 CC_CAPABILITY_STATUS_CTRL

Address: 18h

Access: R/W

Note: This register gives the current capability that is advertised through the RP pins and allows the default V_{CONN} supply capability to be changed.

Table 25. CC_CAPABILITY_STATUS_CTRL register

Bit	Field name	Reset	Description
7:6	CC_CURRENT_ADVERTISED	00b	00b: default USB current (500 mA or 900 mA) 01b: 1.5 A USB Type-C current 10b: 3.0 A USB Type-C current 11b: do not use
5	Reserved	1b	Do not use
4	CC_VCONN_DISCHARGE_EN	0b (NVM)	0b: V_{CONN} discharge disabled on CC pin 1b: V_{CONN} discharge enabled for 250 ms on CC pin
3:1	Reserved	000b	Do not use
0	CC_VCONN_SUPPLY_EN	1b (NVM)	0b: V_{CONN} supply capability disabled on CC pin 1b: V_{CONN} supply capability enabled on CC pin

5.1.11 CC_VCONN_SWITCH_CTRL

Address: 1Eh

Access: R/W

Note: This register allows the default current limit of the power switches supplying V_{CONN} on the CC pins to be changed.

Table 26. CC_VCONN_SWITCH_CTRL register

Bit	Field name	Reset	Description
7:4	Reserved	0000b	Do not use
3:0	CC_VCONN_SWITCH_ILIM	0000b (NVM)	0000b: 350 mA (default) 0001b: 300 mA 0010b: 250 mA 0011b: 200 mA 0100b: 150 mA 0101b: 100 mA 0110b: 400 mA 0111b: 450 mA 1000b: 500 mA 1001b: 550 mA 1010b: 600 mA

5.1.12 VCONN_MONITORING_CTRL

Address: 20h

Access: R/W

Note: This register allows the default voltage monitoring conditions for VCONN to be modified.

Table 27. VCONN_MONITORING_CCTRL register

Bit	Field name	Reset	Description
7	VCONN_MONITORING_EN	1b	0b: disables UVLO threshold detection on V_{CONN} pin 1b: enables UVLO threshold detection on V_{CONN} pin
6	VCONN_UVLO_THRESHOLD	0b	0b: selects high UVLO threshold (default) 1b: selects low UVLO threshold (case where V_{CONN}-powered accessories are operating down to 2.7 V)
5	Reserved	1b	Do not use
4	Reserved	0b	Do not use
3:0	Reserved	0000b	Do not use

Disabling the UVLO threshold detection on the V_{CONN} pin deactivates the V_{CONN} power path and sets the VCONN_PRESENCE bit to 0b in the MONITORING_STATUS register.

See *Section 8.3: Electrical and timing characteristics* for the threshold voltages description and value on VCONN pin.

5.1.13 VBUS_MONITORING_RANGE_CTRL

Address: 22h

Access: R/W

Note: This register allows the low and high limits of the V_{BUS} monitoring voltage range to be changed during attachment.

Table 28. VBUS_MONITORING_RANGE_CTRL register

Bit	Field name	Reset	Description
7:4	SHIFT_HIGH_VBUS_LIMIT	0000b (NVM)	Binary coded V_{SHUSBH} coefficient to shift up the nominal high voltage limit from 1% (0001b) to 15% (1111b) of V_{BUS} voltage by step of 1%
3:0	SHIFT_LOW_VBUS_LIMIT	0000b (NVM)	Binary coded V_{SHUSBL} coefficient to shift down the nominal low voltage limit from 1% (0001b) to 15% (1111b) of V_{BUS} voltage by step of 1%

The V_{BUS} voltage is fixed at 5.0 V. The nominal values of the high and low limits of the V_{BUS} monitoring voltage range are respectively V_{BUS}+5% and V_{BUS}-5%. Each coefficient V_{SHUSBH} and V_{SHUSBL} represents the fraction of V_{BUS} voltage that is either added or subtracted to the nominal value of the corresponding limit to determine the V_{BUS} monitoring voltage limits (see *Section 8.3: Electrical and timing characteristics*).

When the STUSB1700 is in the unattached state, the register takes the reset values. When a device is attached, the register takes the values set in the NVM (see *Section 6: Start-up configuration*) or the new ones set by software during attachment.

5.1.14 RESET_CTRL

Address: 23h

Access: R/W

Note: This register allows the device to be reset by software.

Table 29. RESET_CTRL register

Bit	Field name	Reset	Description
7:1	Reserved	0000000b	Do not use
0	SW_RESET_EN	0b	0b: device reset is performed from hardware RESET pin 1b: forces the device reset as long as this bit value is set

The SW_RESET_EN bit acts as the hardware RESET pin except that I^2C control registers are not reset to default value. They keep the last value change. The SW_RESET_EN bit does not command the RESET pin.

5.1.15 VBUS_DISCHARGE_TIME_CTRL

Address: 25h

Access: R/W

Note: This register contains the parameter used to define the V_{BUS} discharge time when the internal V_{BUS} discharge path is activated on VBUS_SENSE pin.

Table 30. VBUS_DISCHARGE_TIME_CTRL register

Bit	Field name	Reset	Description
7:4	VBUS_DISCHARGE_TIME_TO_0V	0110b (NVM)	Binary coded $T_{DISPARAM}$ coefficient used to compute the V_{BUS} discharge time to 0 V: T_{DISUSB} = 84 ms (typical) * $T_{DISPARAM}$
3:0	Reserved	1111b	Do not use

5.1.16 VBUS_DISCHARGE_STATUS

Address: 26h

Access: RO

Note: This register gives information, during operation, on the activation state of the internal V_{BUS} discharge path on the VBUS_SENSE pin.

Table 31. VBUS_DISCHARGE_STATUS register

Bit	Field name	Reset	Description
7	VBUS_DISCHARGE_EN	0b	0b: V_{BUS} discharge path is deactivated 1b: V_{BUS} discharge path is activated
6:1	Reserved	0000000b	Do not use

5.1.17 VBUS_ENABLE_STATUS

Address: 27h

Access: R0

Note: This register gives information, during operation, on the activation state of the V_{BUS} power path through VBUS_EN_SRC pin.

Table 32. VBUS_ENABLE_STATUS register

Bit	Field name	Reset	Description
7:1	Reserved	0b	Do not use
0	VBUS_SOURCE_EN	0b	0b: V_{BUS} source power path is disabled 1b: V_{BUS} source power path is enabled

5.1.18 VBUS_MONITORING_CTRL

Address: 2Eh

Access: R/W

Note: This register allows to modify the default monitoring conditions of V_{BUS} voltage over the power path from VDD and VBUS_SENSE pins.

Table 33. VBUS_MONITORING_CTRL register

Bit	Field name	Reset	Description
7	Reserved	0b	Do not use
6	VDD_OVLO_DISABLE	0b (NVM)	0b: enables OVLO threshold detection on VDD pin 1b: disables OVLO threshold detection on VDD pin
5	Reserved	0b	Do not use
4	VBUS_VALID_RANGE_DISABLE	0b (NVM)	0b: enables valid V_{BUS} voltage range detection 1b: disables valid V_{BUS} voltage range detection (V_{BUS} UVLO threshold detection used instead)
3	Reserved	0b	Do not use
2:1	VBUS_VSAFE0V_THRESHOLD	00b (NVM)	00b: V_{BUS} vSafe0V threshold = 0.6 V 01b: V_{BUS} vSafe0V threshold = 0.9 V 10b: $_{VBUS}$ vSafe0V threshold = 1.2 V 11b: V_{BUS} vSafe0V threshold = 1.8 V
0	VDD_UVLO_DISABLE	1b (NVM)	0b: enables UVLO threshold detection on VDD pin 1b: disables UVLO threshold detection on VDD pin

The VBUS_VALID_RANGE_DISABLE and VBUS_VSAFE0V_THRESHOLD bits are defining monitoring conditions applicable to the VBUS_SENSE pin connected to the USB Type-C receptacle side.

The VBUS_VALID_RANGE_DISABLE bit allows the valid V_{BUS} voltage range condition to be substituted by the V_{BUS} UVLO threshold condition to establish a valid device attachment and to assert the V_{BUS} power path.

The VBUS_VSAFE0V_THRESHOLD bit indicates the voltage value of the V_{BUS} vSafe0V threshold used as a Type-C FSM condition to establish a valid device attachment.

The VDD_UVLO_DISABLE and VDD_OVLO_DISABLE bits are defining monitoring conditions applicable to the VDD supply pin when it is connected to the main power supply:

- When UVLO detection is enabled, the VBUS_EN_SRC pin is asserted only if the voltage on the VDD pin is above V_{DDUVLO} threshold.
- When OVLO detection is enabled, the VBUS_EN_SRC pin is asserted only if the voltage on the VDD pin is below V_{DDOVLO} threshold.

See *Section 8.3: Electrical and timing characteristics* for the threshold voltages description and value on VDD and VBUS_SENSE pins.

6 Start-up configuration

6.1 User-defined parameters

The STUSB1700 has a set of user-defined parameters that can be customized by NVM re-programming and/or by software through I^2C interface. It allows the customer to change the preset configuration of USB Type-C interface and to define a new configuration to meet specific customer requirements addressing various applications, use cases or specific implementations.

The NVM re-programming overrides the initial default setting to define a new default setting that will be used at power-up or after a reset. The default value is copied at power-up, or after a reset, from the embedded NVM into dedicated I^2C register bits (see *Section 5.1: Register description*). The NVM re-programming is possible with a customer password.

When a default value is changed during functioning by software, the new setting remains in effect as long as the STUSB1700 is operating or when it is changed again. But after power-off and power-up, or after a reset, STUSB1700 takes back default values defined in the NVM.

Please refer to the NVM access and programming application note in order to read and change the default values of the parameters customizable by NVM if needed.

6.2 Default start-up configuration

The following table lists the user-defined parameters and indicates the default start-up configuration of the STUSB1700.

Three types of user-defined parameters are specified in the table with respect to the “Customization type” column:

- SW: indicates parameters that can be customized only by software through the I^2C interface during system operation,
- NVM: indicates parameters that can be customized only by NVM re-programming,
- NVM/SW: indicates parameters that can be customized by NVM re-programming and/or by software through the I^2C interface during system operation.

Table 34. STUSB1700 user-defined parameters and default setting

Customization type	Parameter	Default value and description	I^2C register address
NVM/SW	CC_CONNECTION_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM/SW	MONITORING_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM/SW	HW_FAULT_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM	STANDBY_POWER_MODE_DISABLE	1b: disables standby power mode	N/A
NVM/SW	CC_VCONN_DISCHARGE_EN	0b: V_{CONN} discharge disabled on CC pin	18h

Table 34. STUSB1700 user-defined parameters and default setting (continued)

Customization type	Parameter	Default value and description	I^2C register address
NVM/SW	CC_VCONN_SUPPLY_EN	1b: V_{CONN} supply capability enabled on CC pin	18h
NVM/SW	CC_VCONN_SWITCH_ILIM	0000b: 350 mA	1Eh
SW	VCONN_MONITORING_EN	1b: enables UVLO threshold detection on VCONN pin	20h
SW	VCONN_UVLO_THRESHOLD	0b: high UVLO threshold of 4.65 V	20h
NVM/SW	SHIFT_HIGH_VBUS_LIMIT	0101b: V_{SHUSBH} = 5% of V_{BUS}, high voltage limit $V_{MONUSBH}$ Source = VBUS+10%	22h
NVM/SW	SHIFT_LOW_VBUS_LIMIT	0101b: V_{SHUSBL} = 5% of V_{BUS}, low voltage limit $V_{MONUSBL}$ Source = V_{BUS}-10%	22h
SW	SW_RESET_EN	0b: device reset is performed from hardware RESET pin	23h
NVM/SW	VBUS_DISCHARGE_TIME_TO_0V	0110b: $T_{DISPARAM}$ = 6, discharge time T_{DISUSB} = 504 ms	25h
NVM	VBUS_DISCHARGE_DISABLE	0b: enables V_{BUS} discharge path	N/A
NVM/SW	VDD_OVLO_DISABLE	0b: enables OVLO threshold detection on VDD pin	2Eh
NVM/SW	VBUS_VALID_RANGE_DISABLE	0b: enables valid V_{BUS} voltage range detection	2Eh
NVM/SW	VBUS_VSAFE0V_THRESHOLD	00b: V_{BUS} vSafe0V threshold = 0.6 V	2Eh
NVM/SW	VDD_UVLO_DISABLE	1b: disables UVLO threshold detection on VDD pin	2Eh

7 Application

The following sections are not part of ST product specification. This part is intended to give a generic application overview to be used by the customer as a starting point for further implementation and customization. ST does not warrant compliancy with customer specification. Full system implementation and validation are under customer responsibility.

7.1 General information

7.1.1 Power supplies

The STUSB1700 can be supplied in three different ways depending on the targeted application:

- Through the VDD pin only for applications powered by V_{BUS},
- Through the VSYS pin only for AC applications with a system power supply delivering 3.3 V or 5 V,
- Through VDD and VSYS pins for applications powered by V_{BUS} with a system power supply delivering 3.3 V or 5 V. When both VDD and VSYS power supplies are present, the low power supply VSYS is selected when VSYS voltage is above 3.1 V otherwise VDD is selected.

7.1.2 Connection to MCU or application processor

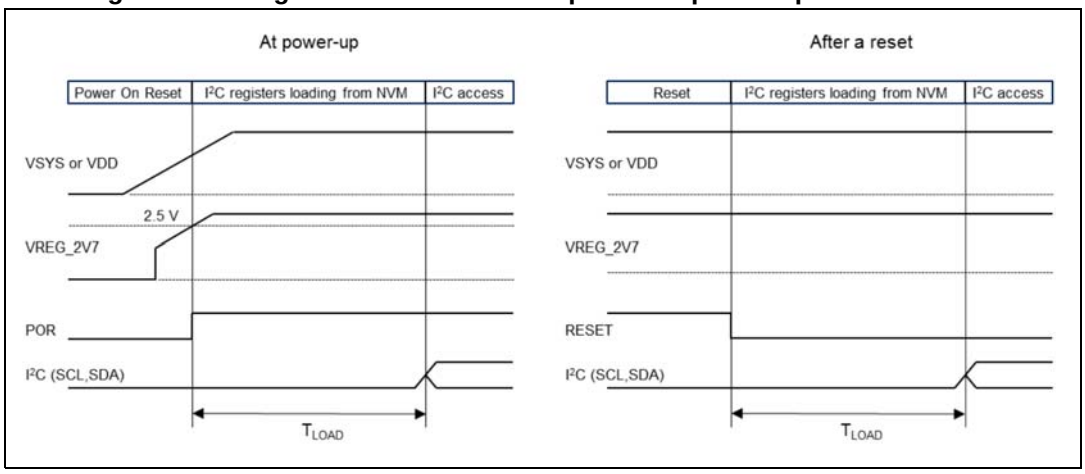
The connection to an MCU or an application processor is optional.

When a connection through I²C interface is implemented, it provides extensive functionality during system operation. For instance, it may be used to:

1. Define the port configuration during system boot (in case the NVM parameters are not customized during manufacturing),
2. Change the default configuration at any time during operation
3. Adjust the port power capability according to contextual power availability and/or the power partitioning with other ports,
4. Save system power by shutting down the DC-DC converter according to the attachment detection state,
5. Provide a diagnostic of the Type-C connection and the V_{BUS} power path in real time.

At power-up or after a reset, the first software access to the I^2C registers of STUSB1700 can be done only after T_{LOAD} as shown in the figure below. T_{LOAD} corresponds to the time required to initialize the I^2C registers with the default values from the embedded NVM. At power-up, the loading phase starts when the voltage level on the VREG_2V7 output pin of the 2.7 V internal regulator reaches 2.5 V to release the internal POR signal. After a reset, the loading phase starts when the signal on the RESET pin is released.

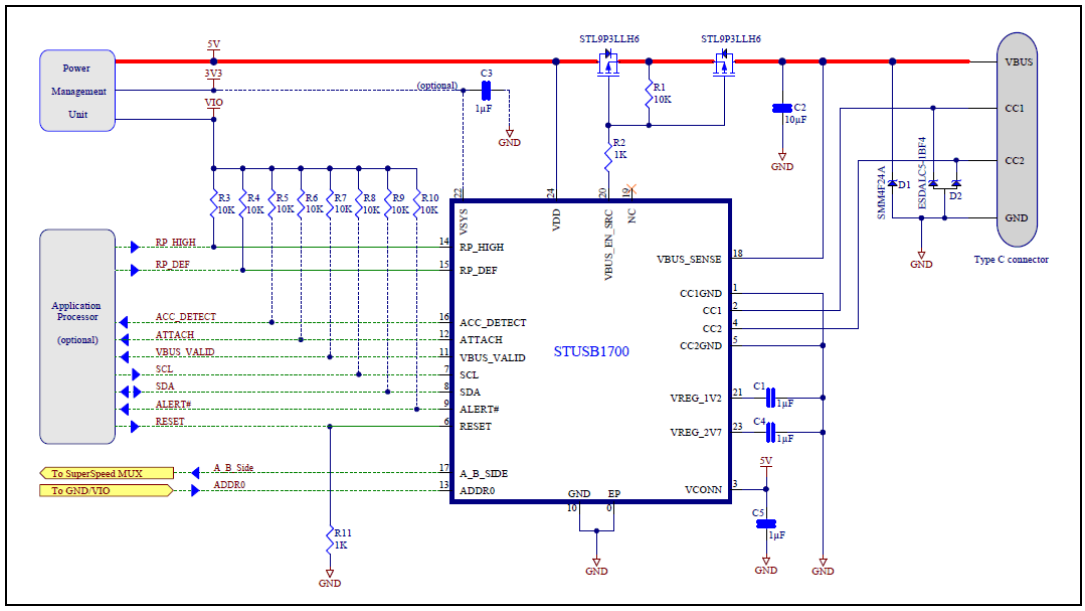
Figure 7. I²C registers initialization sequence at power-up or after a reset



7.2 USB Type-C typical applications

7.2.1 Source type application with Rp = 3A

Figure 8. Typical STUSB1700 implementation in source type application with Rp=3A



Note: Dashed lines correspond to optional connections (depends on application requirements).

7.2.2 V_{BUS} power path assertion

Table 35. Conditions for V_{BUS} power path assertion with STUSB1700 default configuration

Pin	Electrical value	Operation conditions			Comment
		Type-C attached state	VDD pin monitoring	VBUS_SENSE pin monitoring	
VBUS_EN_SRC	0	Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC	V_{DD} < V_{DDOVLO} if VDD pin is supplied	V_{BUS} is within valid voltage range	The signal is asserted only if all the valid operation conditions are met
	HiZ	Any other state	V_{DD} > V_{DDOVLO} if VDD pin is supplied	V_{BUS} is out of valid voltage range	The signal is de-asserted when at least one non valid operation condition is met.

7.2.3 Device state according to connection state

Table 36. Source power role with accessory support

Connection state	CC1 pin	CC2 pin	Type-C device state CC_OPERATION_STATUS register @11h	A_B_SIDE pin	V_{CONN} supply	VBUS_EN_SRC pin	CC_CONNECTION_STATUS register @0Eh
Nothing attached	Open	Open	Unattached.SRC	HiZ	OFF	HiZ	00h
Sink attached	Rd	Open	Attached.SRC	HiZ	OFF	0	2Dh
	Open	Rd		0	OFF	0	2Dh
Powered cable without sink attached	Open	Ra	Unattached.SRC	HiZ	OFF	HiZ	00h
	Ra	Open		HiZ	OFF	HiZ	00h
Powered cable with sink attached or Vconn-powered accessory attached	Rd	Ra	Attached.SRC	HiZ	CC2	0	2Fh
	Ra	Rd		0	CC1	0	2Fh
Debug accessory mode attached source role	Rp	Rp	Unattached.SRC	HiZ	OFF	HiZ	00h
Debug accessory mode attached sink role	Rd	Rd	UnorientedDebug Accessory.SRC	HiZ	OFF	0	6Dh

Table 36. Source power role with accessory support (continued)

Connection state	CC1 pin	CC2 pin	Type-C device state CC_OPERATION_STATUS register @11h	A_B_SIDE pin	V_{CONN} supply	VBUS_EN_SRC pin	CC_CONNECTION_STATUS register @0Eh
Debug accessory mode attached sink role	Rd	≤ Ra	OrientedDebug Accessory.SRC	HiZ	OFF	0	6Dh
	≤ Ra	Rd		0	OFF	0	6Dh
Audio adapter accessory mode attached	Ra	Ra	AudioAccessory	HiZ	OFF	HiZ	81h

The value of the CC1 and CC2 pins is defined from a termination perspective and corresponds to the termination presented by the connected device. The CC_CONNECTION_STATUS register can report other values than the one presented in *Table 36*. In this table, it reflects the state transitions in Type-C FSM that can be ignored from the application stand point.

8 Electrical characteristics

8.1 Absolute maximum rating

All voltages are referenced to GND.

Table 37. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage on VDD pin	28	V
V_{SYS}	Supply voltage on VSYS pin	6	
V_{CC1}, V_{CC2}	High voltage on CC pins	22	
$V_{VBUS_EN_SRC}$ V_{VBUS_SENSE}	High voltage on V_{BUS} pins	28	
V_{SCL}, V_{SDA} $V_{ALERT\#}$ V_{RESET} V_{ATTACH} $V_{A_B_SIDE}$ V_{VBUS_VALID} V_{ACC_DETECT} V_{RP_DEF} V_{RP_HIGH}	Operating voltage on I/O pins	-0.3 to 6	
V_{CONN}	V_{CONN} voltage	6	
T_{STG}	Storage temperature	-55 to 150	°C
T_J	Maximum junction temperature	145	
ESD	HBM	4	kV
	CDM	1.5	

8.2 Operating conditions

Table 38. Operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage on VDD pin	4.1 to 22	V
V_{SYS}	Supply voltage on VSYS pin	3.0 to 5.5	
V_{CC1}, V_{CC2}	CC pins	0 to 5.5	
$V_{VBUS_EN_SRC}$ V_{VBUS_SENSE}	High voltage pins	0 to 22	
V_{SCL}, V_{SDA} $V_{ALERT\#}$ V_{RESET} V_{ATTACH} $V_{A_B_SIDE}$ V_{VBUS_VALID} V_{ACC_DETECT} V_{RP_DEF} V_{RP_HIGH}	Operating voltage on I/O pins	0 to 4.5	
V_{CONN}	V_{CONN} voltage	2.7 to 5.5	
I_{CONN}	V_{CONN} rated current (default = 0.35 A)	0.1 to 0.6	A
T_A	Operating temperature	-40 to 105	°C

8.3 Electrical and timing characteristics

Unless otherwise specified: V_{DD} = 5 V, T_A = +25 °C, all voltages are referenced to GND.

Table 39. Electrical and timing characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DD\ (SRC)}$	Current consumption	Device idle as a SOURCE (not connected, no communication) V_{SYS} @ 3.3 V V_{DD} @ 5.0 V				
				158		µA
				188		µA
I_{STDBY}	Standby current consumption	Device in standby (not connected, low power) V_{SYS} @ 3.3 V V_{DD} @ 5.0 V				
				33		µA
				53		µA
T_{LOAD}	I^2C registers loading time from NVM	At power-up or after a reset			30	ms
CC1 and CC2 pins						
I_{P-USB}	CC current sources	CC pin voltage, V_{CC} = 0 to 2.6 V, -40 °C < T_A < +105 °C	-20%	80	20%	µA
$I_{P-1.5}$			-8%	180	8%	µA
$I_{P-3.0}$			-8%	330	8%	µA
V_{CCO}	CC open pin voltage	CC unconnected, V_{DD} = 3.0 to 5.5 V	2.75			V
R_{INCC}	CC input impedance	Terminations off	200			kΩ
$V_{TH0.2}$	Detection threshold 1	Max R_a detection by source at $I_P = I_{P–USB}$	0.15	0.2	0.25	V
$V_{TH0.4}$	Detection threshold 2	Max R_a detection by source at $I_P = I_{P-1.5}$	0.35	0.4	0.45	V
$V_{TH0.8}$	Detection threshold 3	Max R_a detection by source at $I_P = I_{P-3.0}$	0.75	0.8	0.85	V
$V_{TH1.6}$	Detection threshold 4	Max R_d detection by source at $I_P = I_{P-USB}$ and $I_P = I_{P-1.5}$	1.5	1.6	1.65	V
$V_{TH2.6}$	Detection threshold 5	Max R_d detection by source at $I_{P-3.0}$, max CC voltage for connected sink	2.45	2.6	2.75	V
VCONN pin and power switches						
R_{VCONN}	V_{CONN} power path resistance	I_{VCONN} = 0.2 A	0.25	0.5	0.975	Ω
		-40 °C < T_A < 105 °C				

Table 39. Electrical and timing characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OCP}	Overcurrent protection	Programmable current limit threshold (from 100 mA to 600 mA by step of 50 mA)	85	100	125	mA
			300	350	400	
			550	600	650	
V_{OVP}	Overvoltage protection on CC output pins		5.9	6	6.1	V
V_{UVP}	Undervoltage protection on VCONN input pin	Low UVLO threshold	2.6	2.65	2.7	V
		High UVLO threshold (default)	4.6	4.65	4.8	
VDD pin monitoring						
V_{DDOVLO}	Overvoltage lockout	OVLO threshold detection enabled, VDD pin supplied	5.8	6	6.2	V
V_{DDUVLO}	Undervoltage lockout	UVLO threshold detection enabled, VDD pin supplied	3.8	3.9	4	V
VBUS_SENSE pin monitoring and driving						
V_{THUSB}	V_{BUS} presence threshold (UVLO)	V_{SYS} = 3.0 to 5.5 V	3.8	3.9	4	V
V_{TH0V}	V_{BUS} safe 0V threshold (vSafe0V)	V_{SYS} = 3.0 to 5.5 V, threshold programmable from 0.6 V to 1.8 V, default V_{THOV} = 0.6 V	0.5	0.6	0.7	V
			0.8	0.9	1	V
			1.1	1.2	1.3	V
			1.7	1.8	1.9	V
R_{DISUSB}	V_{BUS} discharge resistor		600	700	800	Ω
T_{DISUSB}	V_{BUS} discharge time to 0V	Coefficient $T_{DISPARAM}$ programmable by NVM, default $T_{DISPARAM}$ = 6, T_{DISUSB} = 504 ms	70 *$T_{DISPARAM}$	84 *$T_{DISPARAM}$	100 *$T_{DISPARAM}$	ms
$V_{MONUSBH}$	V_{BUS} monitoring high voltage limit	Coefficient V_{SHUSBH} programmable by NVM from 1% to 15% of V_{BUS} by step of 1%, default $V_{MONUSBH}$ = V_{BUS}+10%		V_{BUS}+5%+ V_{SHUSBH}		V
$V_{MONUSBL}$	V_{BUS} monitoring low voltage limit	Coefficient V_{SHUSBL} programmable by NVM from 1% to 15% of V_{BUS} by step of 1%, default $V_{MONUSBL}$ = V_{BUS}-10%		VBUS-5% -V_{SHUSBL}		V
Digital input/output (SCL, SDA, ALERT#, RESET, ATTACH, A_B_SIDE, VBUS_VALID, ACC_DETECT, RP_DEF, RP_HIGH)						
V_{IH}	High level input voltage		1.2			V
V_{IL}	Low level input voltage				0.35	V

Table 39. Electrical and timing characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V
20 V open drain output (VBUS_EN_SRC)						
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

9.1 QFN-24 EP (4 x 4 mm) Wet Flk package information

Figure 9. QFN-24 EP 4x4 mm Wet Flk package outline

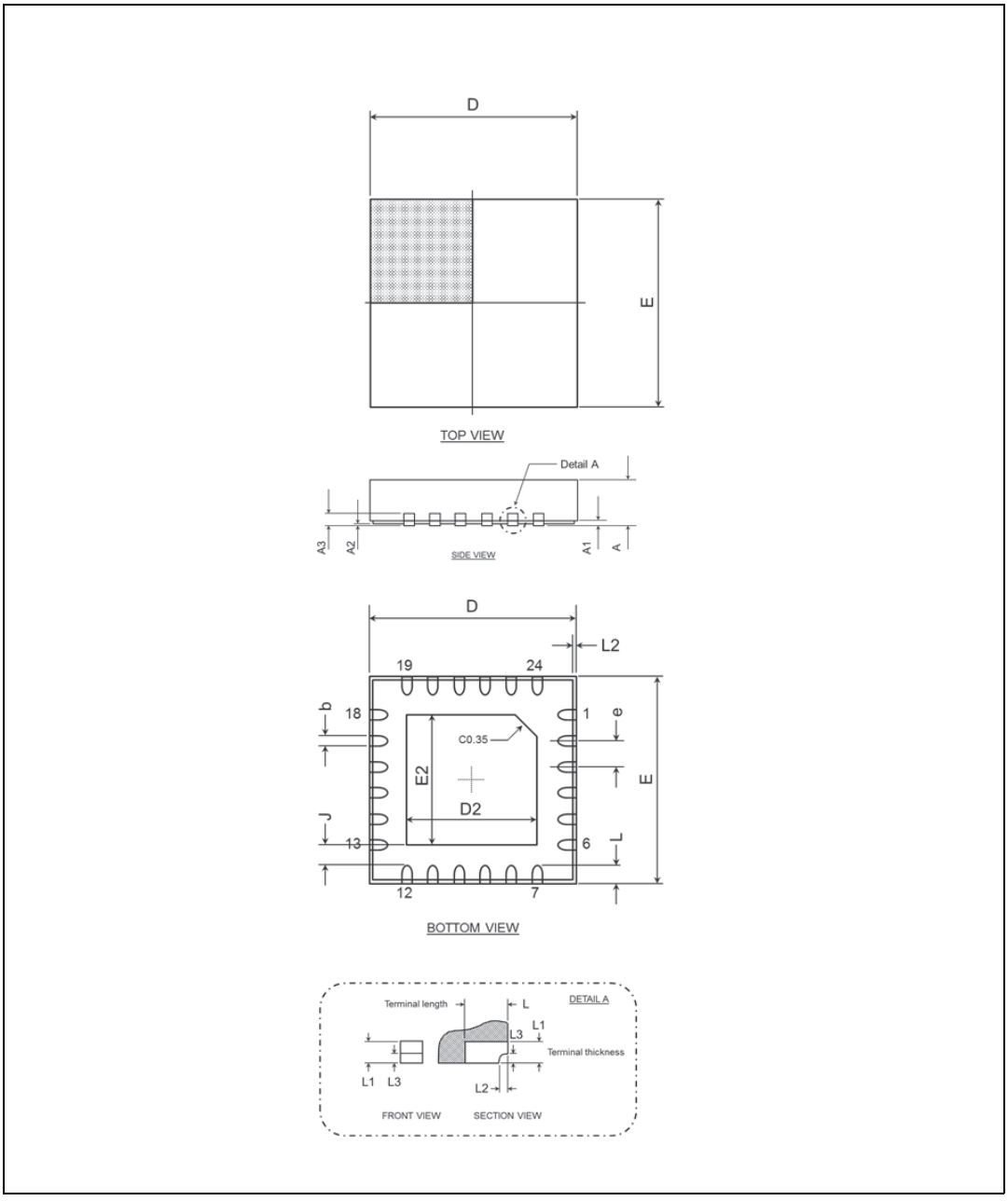
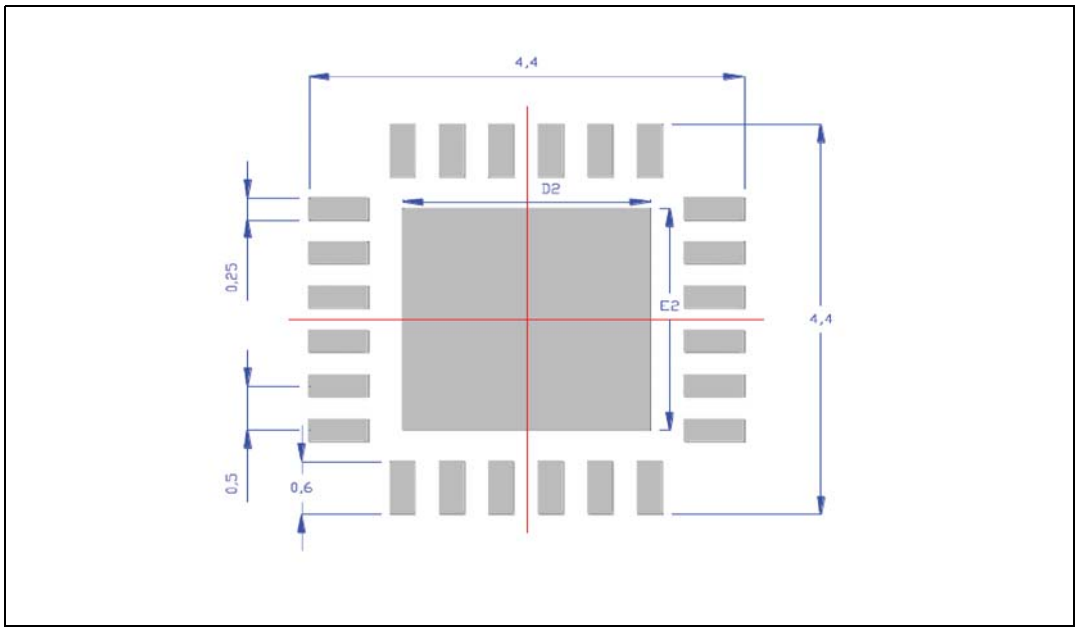


Table 40. QFN24 EP 4x4 Wet Flk mm mechanical data

Symbol	Dimensions (mm)		
	Min	Typ	Max
A	0.90	0.95	1.00
A1		0.10	
A2	0.00	0.02	0.05
A3		0.20	
b	0.20	0.25	0.30
D	3.85	4.00	4.15
D2	2.40	2.50	2.60
E	3.85	4.00	4.15
E2	2.40	2.50	2.60
e		0.50	
J		0.35	
L	0.30	0.40	0.50
L1		0.20	
L2		0.05	
L3		0.10	

Figure 10. QFN24 EP 4x4 mm Wet Flk recommended footprint



9.2 Thermal information

Table 41. Thermal information

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	37	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	5	°C/W

10 Terms and abbreviations

Table 42. List of terms and abbreviations

Term	Description
Accessory modes	Audio adapter accessory mode. It is defined by the presence of Ra/Ra on CC1/CC2 pins.
	Debug accessory mode. It is defined by the presence of Rd/Rd on CC1/CC2 pins.
DFP	Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically the ports on a HOST or the ports on a hub to which devices are connected. In its initial state, the DFP sources V_{BUS} and V_{CONN}, and supports data.
DRP	Dual-role port. A port that can operate as either a Source or a Sink. The port's role may be changed dynamically.
Sink	Port asserting Rd on CC pins and consuming power from V_{BUS}; most commonly a Device.
Source	Port asserting Rp on CC pins and providing power over V_{BUS}; most commonly a Host or Hub DFP.
UFP	Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks V_{BUS} and supports data.

11 Revision history

Table 43. Document revision history

Date	Revision	Changes
13-Dec-2017	1	Initial release.

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