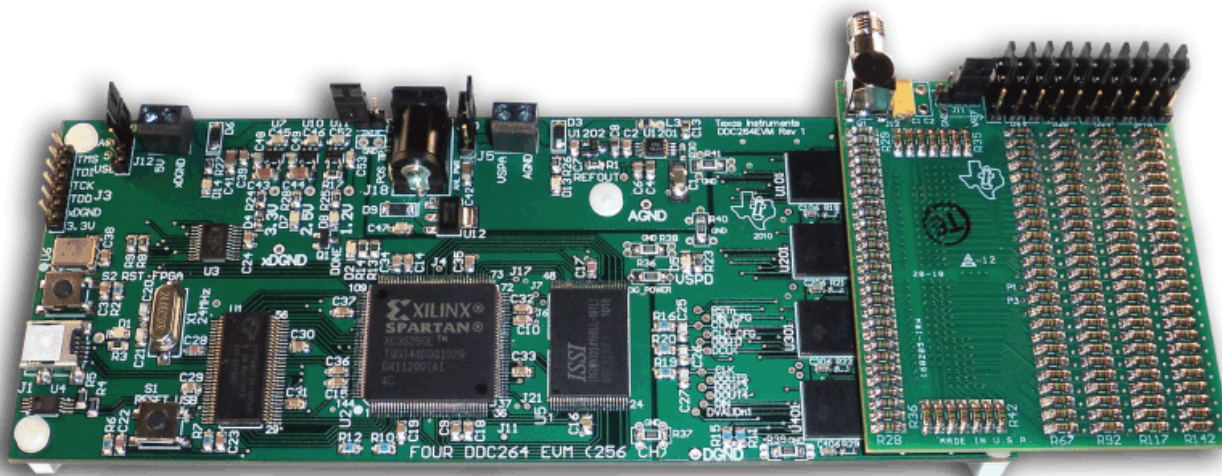


DDC264EVM User's Guide



DDC264EVM

This user's guide describes the characteristics, operation, and use of the DDC264EVM. This evaluation module (EVM) is an evaluation kit for evaluating the [DDC264](#), a 64-channel, current input, 20-bit analog-to-digital (A/D) converter. The EVM consists of four DDC264 devices, a USB device for interfacing to a PC, an FPGA for device communication, 16 MB of memory for temporary data storage, and a high-density socket to allow connection to the analog inputs. Easy-to-use software for the Microsoft® Windows® operating system is included that allows performance evaluation of each device. A socketed analog input board (AIB) is attached to the high-density DDC264EVM socket for device analysis. Complete circuit descriptions, schematic diagrams, and bills of material are included in this user's guide.

The following related documents are available through the Texas Instruments web site at www.ti.com.

EVM-Compatible Device Data Sheets

Device	Literature Number	Device	Literature Number
DDC264	SBAS368	REG1117-5	SBVS001
OPA350	SBOS099	REG113	SBVS031
REF3040	SBVS032	SN105125	SLVS418

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1 Introduction

The DDC264EVM provides an easy-to-use platform for evaluating the DDC264 charge-digitizing A/D converters. A PC interface board (DDC264EVM) and an analog input daughterboard (AIB) for the DDC264 devices are included along with software that makes analysis and testing of this device simple.

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the DDC264EVM.

2 DDC264

The DDC264 is a 20-bit, 64-channel, current-input analog-to-digital (A/D) converter (see [Figure 1](#)). It combines both current-to-voltage and A/D conversion so that 64 separate low-level current output devices, such as photodiodes, can be directly connected to its inputs and digitized. For each of the 64 inputs, the DDC264 uses the proven dual switched-integrator front-end. This design allows for continuous current integration: while one integrator is being digitized by the onboard A/D converter, the other is integrating the input current. Adjustable full-scale ranges from 12.5pC to 150pC and adjustable integration times from 160μs to 1s allow currents from fAs to μAs to be continuously measured with outstanding precision. Low-level linearity is ±1.0ppm of the full-scale range and noise is 6.3ppm of the full-scale range.

There are four different capacitor configurations available on-chip for both sides of every channel in the DDC264. These internal capacitors are trimmed in production to achieve the specified performance for range error of the DDC264. The range control bits (Range[1:0]) set the capacitor value for all integrators. Consequently, all inputs and both sides of each input always have the same full-scale range. [Table 1](#) shows the capacitor value selected for each range selection.

Table 1. Range Selection

Range	Range Control Bits		C _F	Input Range
	Range[1]	Range[0]		
0	0	0	3pF	–0.04 to 12.5pC
1	0	1	12.5pF	–0.2 to 50.0pC
2	1	0	25pF	–0.4 to 100pC
3	1	1	37.5pF	–0.6 to 150pC

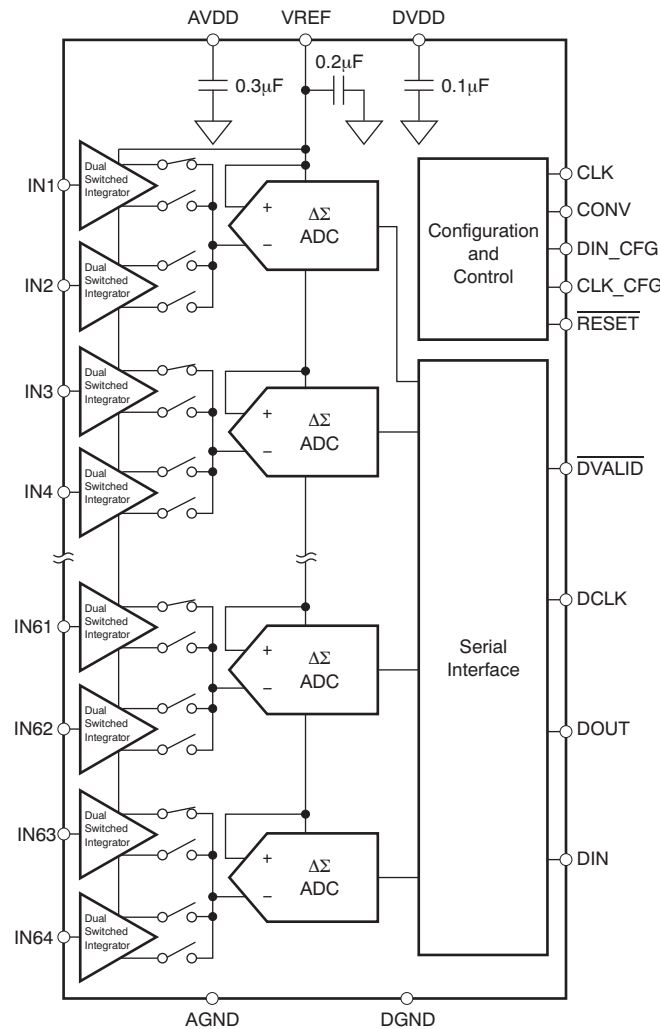


Figure 1. DDC264 Functional Block Diagram

3 DDC264EVM Hardware Description

The DDC264EVM is a device-under-test (DUT) board that contains four DDC264 devices on the analog portion of the board. Also included on the analog portion is a 4.096V reference and buffer, a high-density analog input socket, and decoupling capacitors. An analog input board (AIB) is connected to the high-density socket, and drives the 256 possible device channels (see [Figure 22](#) for layout artwork and appended schematic).

The digital portion of the DDC264EVM contains voltage regulators, decoupling capacitors, interface connectors, reset switches, oscillators, a USB interface, a Xilinx Spartan™-3 FPGA, and 16MB of memory. The FPGA generates all the timing signals that are sent to the DDC264s as well as handles the communication of data between the DDC264s and the PC.

The DDC264EVM connects to a PC via J1. J1 accepts a USB mini-B cable. The USB communication can be reset by pressing reset switch S1. LED D1 should be lit if the cable is connected properly.

The DDC264EVM board is carefully laid out to ensure low-noise evaluations. Note that the digital portion of the board is separate from the analog portion. All the analog device channels inputs are on the right hand portion of the board, and have a short trace length to the DDC264 devices. Even though the DDC264EVM is designed for optimal performance, it may be necessary to add shielding around the board to eliminate any extraneous environmental noise sources.

3.1 Power-Supply Circuit

Four power-supply connections are provided on the DDC264EVM. The primary power for both the analog and digital portions of the EVM operates on 5VDC. The 5V digital supply can be applied at terminal block J12, or can come from the USB connection. When using the USB-supplied voltage, jumper J19 must have the jumper across the bottom two positions. When using J5, remove the J19 jumper. The analog supply can be applied with 5V at terminal block J5. When using J12, make sure to remove jumper J20.

It is possible to power the board from a single source, such as an ac/dc wall supply connection at J18. If using a single-supply source from the ac/dc adapter, then jumpers J19, J20, and J22 must be attached. J19 must be in the appropriate position depending on which source is used. Connect the top two pins of J19 if using the ac/dc adapter (jack) to power the board. To isolate analog and digital supplies, remove J19, J20, and J22 (default position) and supply 5VDC to J12 and J5. Green LEDs that represent the required voltages should be lit when the DDC264EVM is powered correctly. The 5VDC supply is regulated to 3.3V, 2.5V, and 1.2V for use on the digital portion. The analog portion operates from 5VDC.

To use an ac/dc wall supply adapter at J18, the following conditions must be observed:

- J18 only accepts dc voltages from 7V to 10V.
- The center conductor should be the positive side of the supply, while the outer barrel is the negative.
- The size of the inner conductor is 2.5mm; the outer conductor size is 5.5mm.

When the supply is connected to J18, U12 regulates the voltage to the necessary 5VDC.

3.2 Reference Circuit

The 4.096V reference that has been installed on the DDC264EVM has been carefully selected because of its low-noise performance. The REF3040 provides a 4.096V (nominal) reference. At the reference output, a single pole (3.386Hz) low-pass filter is inserted in the reference signal path. This filter is then followed by an amplifier configured as a buffer. The output of the amplifier has been loaded with 140μF of bulk capacitance. A small value of series resistance is added with each of the bulk capacitors to prevent possible oscillation of the amplifier output.

If jumper J16 is installed, the reference voltage can be applied to J14 pins A15, A16, B15, and B16. This configuration can be useful for applying the reference voltage as an input to the AIB card.

The reference circuit can be powered by either connecting 5V to J5, or by connecting an ac/dc wall supply adapter to J18. J18 accepts dc voltages from 7V to 10V.

3.3 Clock Options

Two clocks are used on the DDC264EVM: a clock for the USB microcontroller, and a clock for the FPGA. The FPGA generates all clocking signals for the DDC264 devices. The USB microprocessor uses a 24MHz crystal (X1), while the FPGA (U2) uses a 80MHz crystal oscillator (U6).

3.4 Motherboard Switches

Switch S1, RESET_USB, resets the USB controller. Pushing this switch may be necessary if the DDC264EVM is not recognized by your PC when connecting it to the DDC264EVM.

Switch S2, RESET_FPGA, resets the FPGA. Normally, it should not be necessary to use this switch. Pressing this switch resets the FPGA to power-up conditions.

3.5 Hardware LEDs

A number of LED indicators are on the DDC264EVM. These indicators allow ease of monitoring the operational state of the EVM. Refer to [Table 2](#) for a summary of these indicators.

Table 2. DDC264EVM LED Indicator Functions

LED	Function Indicator
D1	USB bus power detected.
D2	FPGA configuration is done.
D14	5V digital power is available.
D4	3.3V power to board available.
D7	2.5V power to board available.
D8	1.2V power to board available.
D5	3.3V digital supply to the DDC264 power is connected.
D13	5V analog power is connected

4 Analog Input Board Hardware Description

The AIB allows basic test configurations to be used for inputs to the various DDC264 devices. The AIB consists of a high-density interconnect socket that allows the daughterboard to be connected to the DDC264EVM. The AIB also contains 256 10MΩ resistors to be used as current-limiting devices. There is one resistor for each device channel. One end of the resistor connects to a DDC264 device channel, and the other end connects to a bank of parallel resistors that connect to other DDC264 device channels.

A voltage can be applied to the resistors by several methods. The method used depends on the jumper settings along the top edge of the AIB card and the specific bank of resistors to which the jumper is connected.

When the top two jumper positions are connected together on jumpers J1 through J10, the input to the resistor bank comes from the SMA connector J12. If the bottom two jumper positions are connected, the input to the resistor bank is determined by the selection of jumper J11.

Connecting the center pin of J11 to the left-most pin connects the selected resistor bank input to ground. If the J11 center pin is connected to the right-most pin, the resistor bank is connected to the reference voltage of the DDC264EVM that is determined by jumper J16 (located at the upper right corner of the EVM). Jumper J16, by default, is not installed. If V_{REF} from the DDC264EVM is to be used as the reference voltage for the AIB, then J16 must be installed. [Table 3](#) shows the relationship of the resistor banks to the DDC264 device channels.

Table 3. Resistor Banks and Device Channels Configuration

Jumper	AIB Resistors	Device Channels			
		U101	U201	U301	U401
J1	R1-R28	31, 57, 62	1, 4, 12, 16, 20, 24, 26, 38, 40, 55, 63	2, 19, 25, 30, 34, 39, 41, 45, 51, 58, 64	28, 33, 35
J2	R29-R42, R243-R256	12, 16, 20, 23, 25, 26, 51, 55, 58, 63	33, 34, 35, 39	26, 31, 62, 63	8, 12, 19, 34, 38, 39, 40, 41, 45, 51
J3	R43-R67	17, 40, 45, 47, 48, 54	5, 9, 22, 25, 43, 58, 61	11, 21, 23, 33, 35, 50, 57	5, 11, 16, 44, 48
J4	R218-R242	4, 5, 14, 32, 34, 35, 37, 42, 59	3, 17, 21, 60	9, 29, 37, 52, 56, 59	21, 26, 53, 56, 57, 60
J5	R68-R92	21, 22, 27, 38, 41	13, 19, 28, 32, 36, 51, 52, 53	42, 43, 44, 48, 49, 61	10, 42, 43, 46, 55, 58
J6	R193-R217	1, 2, 3, 10, 13, 33, 36, 43, 46	6, 50, 54	3, 14, 18, 60	17, 22, 24, 29, 31, 32, 54, 61, 64
J7	R93-R117	18, 19, 28, 49, 61	11, 15, 18, 30, 41, 45, 64	7, 8, 10, 13, 22, 27, 53, 54	13, 20, 25, 49, 50
J8	R168-R192	6, 7, 9, 11, 39, 44	10, 27, 37, 42, 44, 59	6, 32, 36, 47	3, 27, 28, 30, 37, 52, 59, 62, 63
J9	R118-R142	8, 15, 24, 29, 30, 52, 60	8, 29, 47, 48, 57, 62	1, 5, 12, 17, 24, 28, 40, 55	1, 9, 15, 47
J10	R143-R167	50, 53, 56, 64	2, 7, 14, 23, 31, 46, 49, 56	4, 15, 16, 20, 38, 46	2, 4, 6, 14, 18, 23, 36

5 DDC264EVM Kit Operation

This section provides information on using the DDC264EVM, including setup, program installation, and program usage.

5.1 Minimum Requirements

Before installing the software please verify that the PC meets the following minimum requirements:

- Microsoft Windows XP® operating system with Service Pack 2 (SP2) installed
- 1024 x 768 screen resolution
- USB 2.0 compatible port

Other configurations may work; however, they are not tested. Users should be advised that when capturing larger data sets, PCs equipped with faster processors and ample memory tend to perform best.

5.2 Installing the Software

Application software can be downloaded from the [DDC264EVM product folder](#). Unzip the downloaded file into a known location.

Before installing the DDC264EVM application software, the USB drivers must be installed. This step is best accomplished by letting Windows find the drivers when the hardware connects. The drivers are located in the driver directory. To begin, connect a power supply to the DDC264EVM. If the wizard has trouble finding the driver files, point to the location where the application software was unzipped. Connect a USB cable from the computer to the DDC264EVM through J1.

Use the Windows *Found New Hardware Wizard* to install the drivers. The DDC264EVM requires a boot driver and an application driver; therefore, new setups require going through the Found New Hardware Wizard twice. [Figure 2](#) through [Figure 7](#) show the first driver screens that appear.



Figure 2. Initial Found New Hardware Wizard Screen

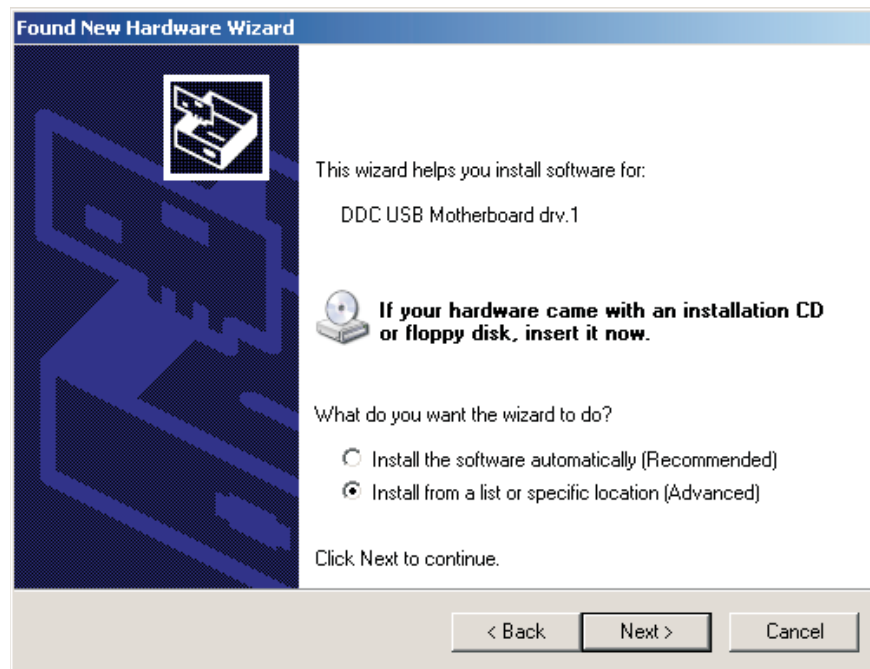


Figure 3. Driver Selection for DDC USB Motherboard drv.1

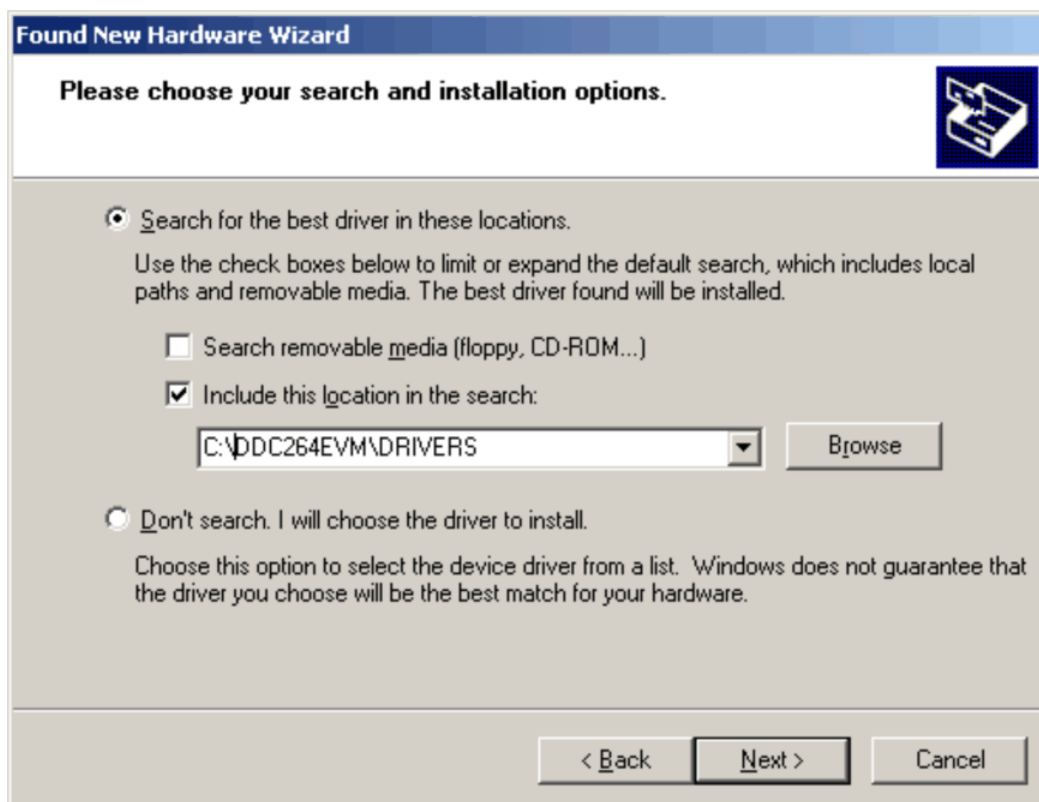


Figure 4. Select to Include This Location and Browse to Driver Location

NOTE: You may see notices (Figure 5) that the drivers are not digitally signed, and given the option to accept the drivers anyway. Choose *Continue Anyway*.



Figure 5. Driver Not Signed Notification—Choose Continue Anyway

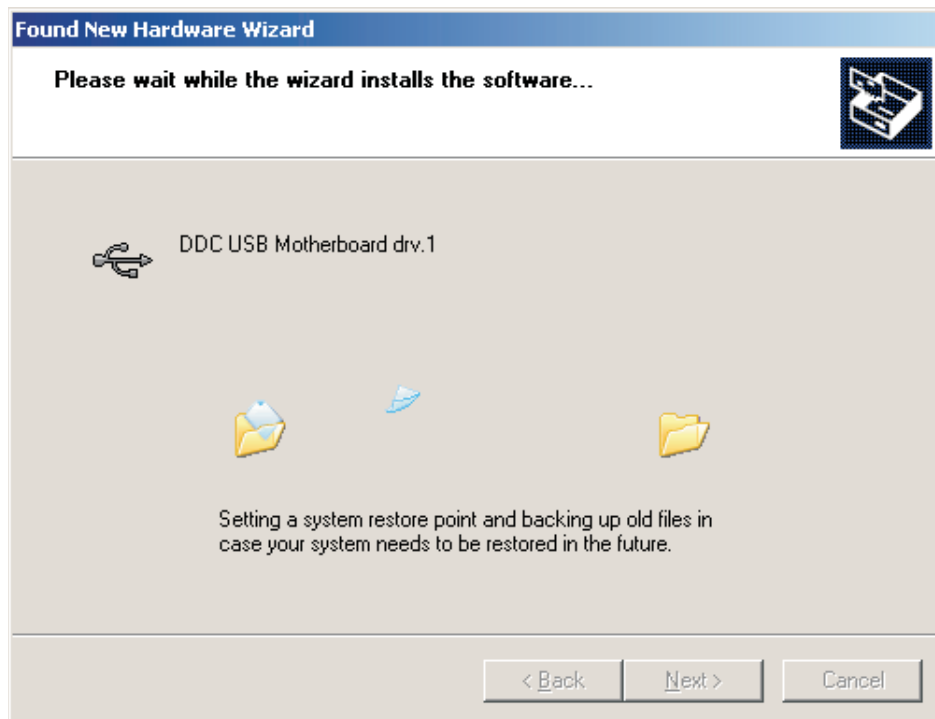


Figure 6. Copying Driver Files

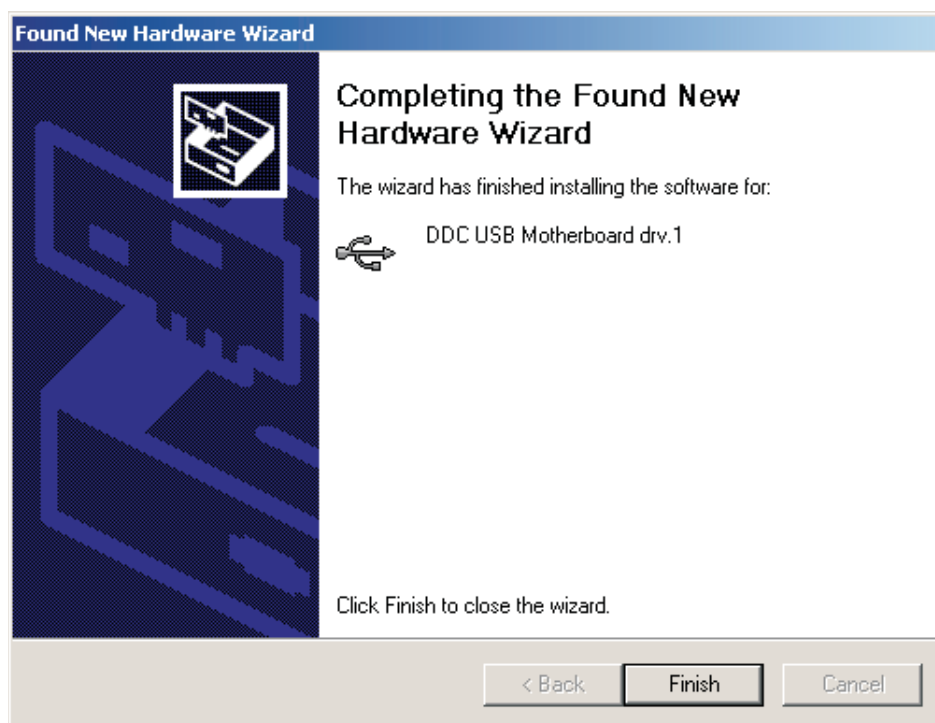


Figure 7. First Driver Installation Complete

After the first driver is installed, disconnect and reconnect the USB cable to the DDC264EVM, or press the **RESET_USB** button on the DDC264EVM. This step causes the second driver to be installed. You will then see screens similar to those in [Figure 8](#) through [Figure 10](#).

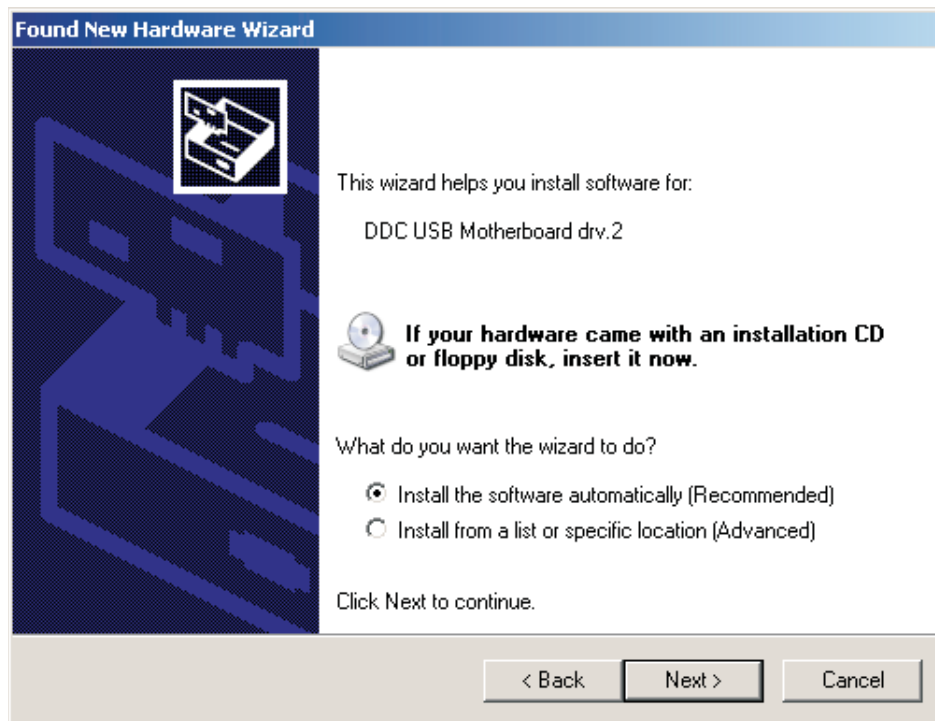


Figure 8. Driver Selection for DDC USB Motherboard drv.2

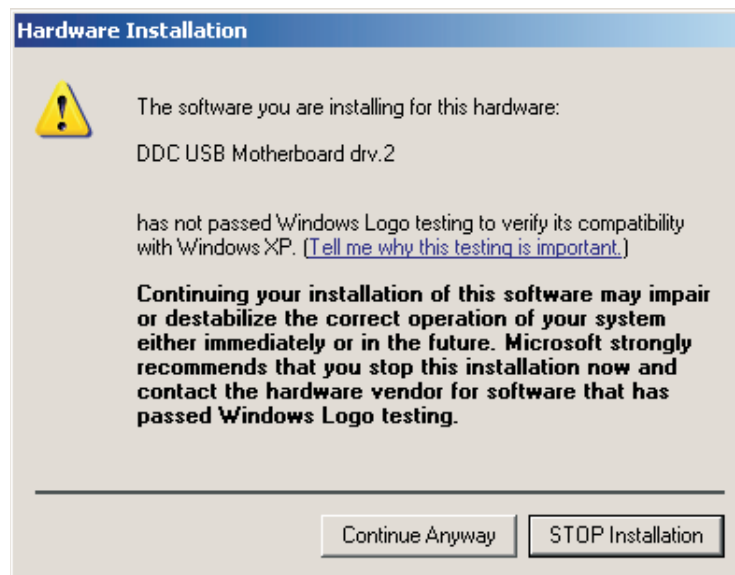


Figure 9. Second Driver Not Signed Notification—Choose Continue Anyway

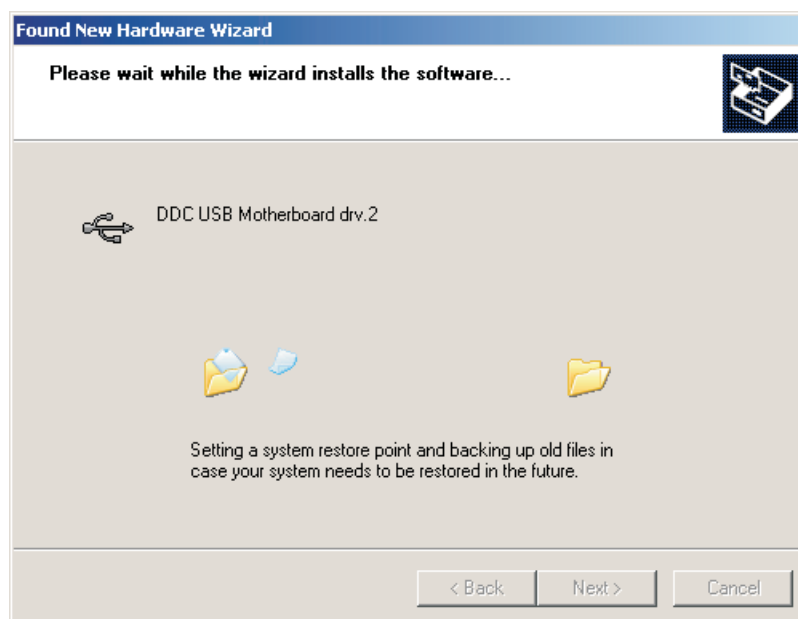


Figure 10. Copying Files for Additional Driver

Once the USB drivers are installed, you must copy the file **USB_IO_for_VB6.dll** from the software installation *Drivers* folder to the *Windows\System32* folder. After the copy process completes, the DDC264 Evaluation program can be installed. Double-click on setup.exe in the install directory. A screen similar to that shown in Figure 11 appears.

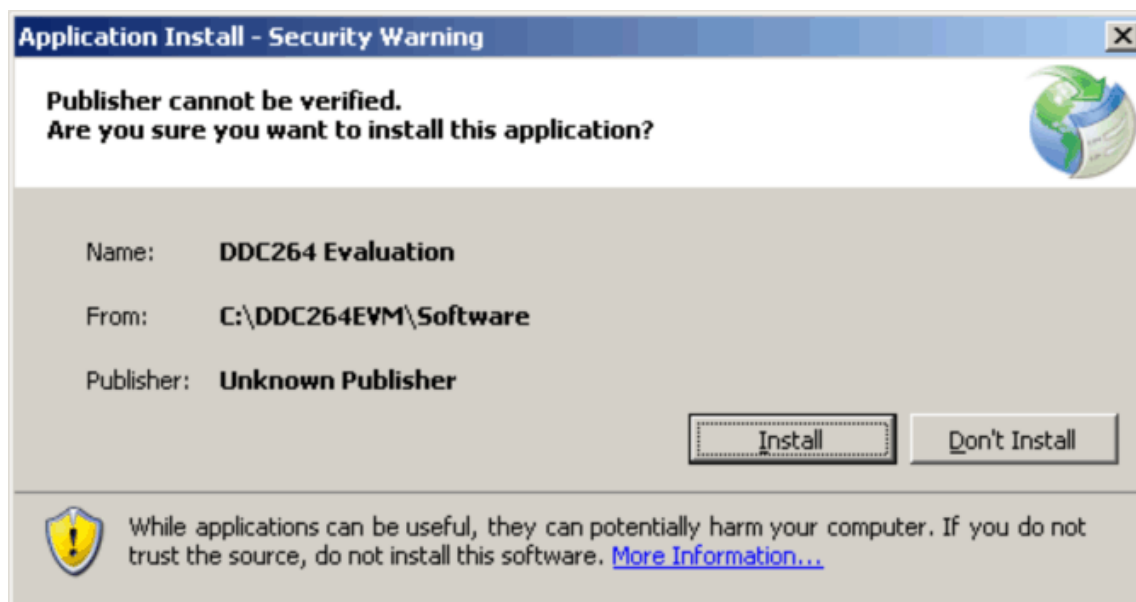


Figure 11. Initial Software Installer Screen

If you are ready to proceed with the installation, press the **Install** button to continue.

The screen shown in [Figure 12](#) appears and displays the installation progress.

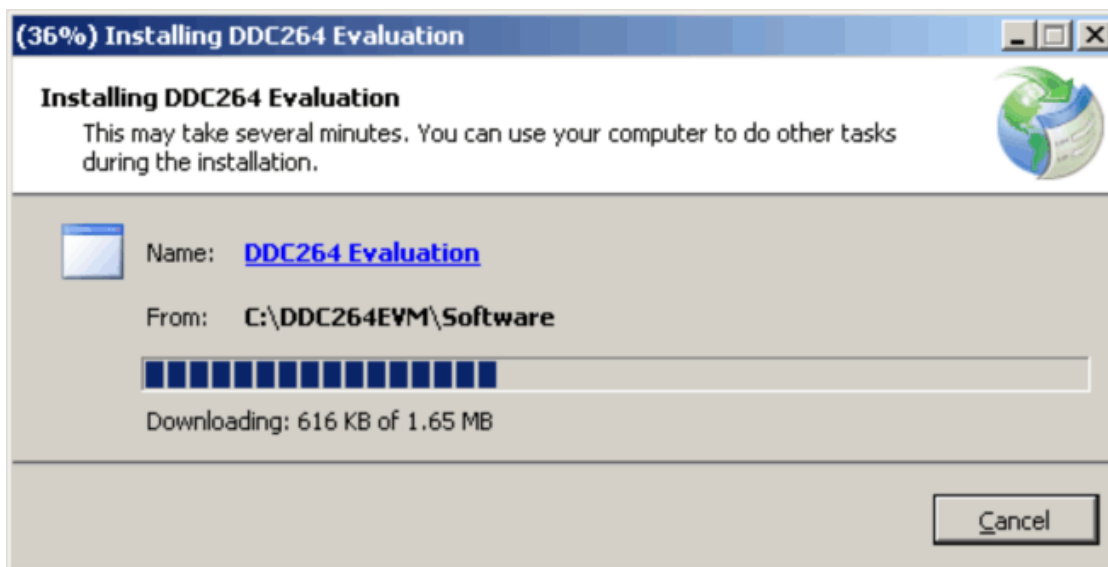


Figure 12. Software Installation Progress

The software installation is now complete. Disconnect power from the DDC264EVM and proceed to the next section.

5.3 ***Evaluating a DDC264 Device: Quick Start***

Set the jumpers J19, J20, and J22 to the appropriate positions for the desired manner of powering the DDC264EVM. The default position for J19, J20, and J22 is off. In this case, 5V must be applied to the J5 and J12 terminal blocks. Once the power is properly connected, turn the power on. Connect a USB2.0 mini-B type cable from the PC and plug it into connector J1 of the DDC264EVM.

Start the PC software from the Windows **Start** menu; select the *DDC264 Evaluation* program under the Texas Instruments dropdown menu. The program starts and displays a window as shown in Figure 13.

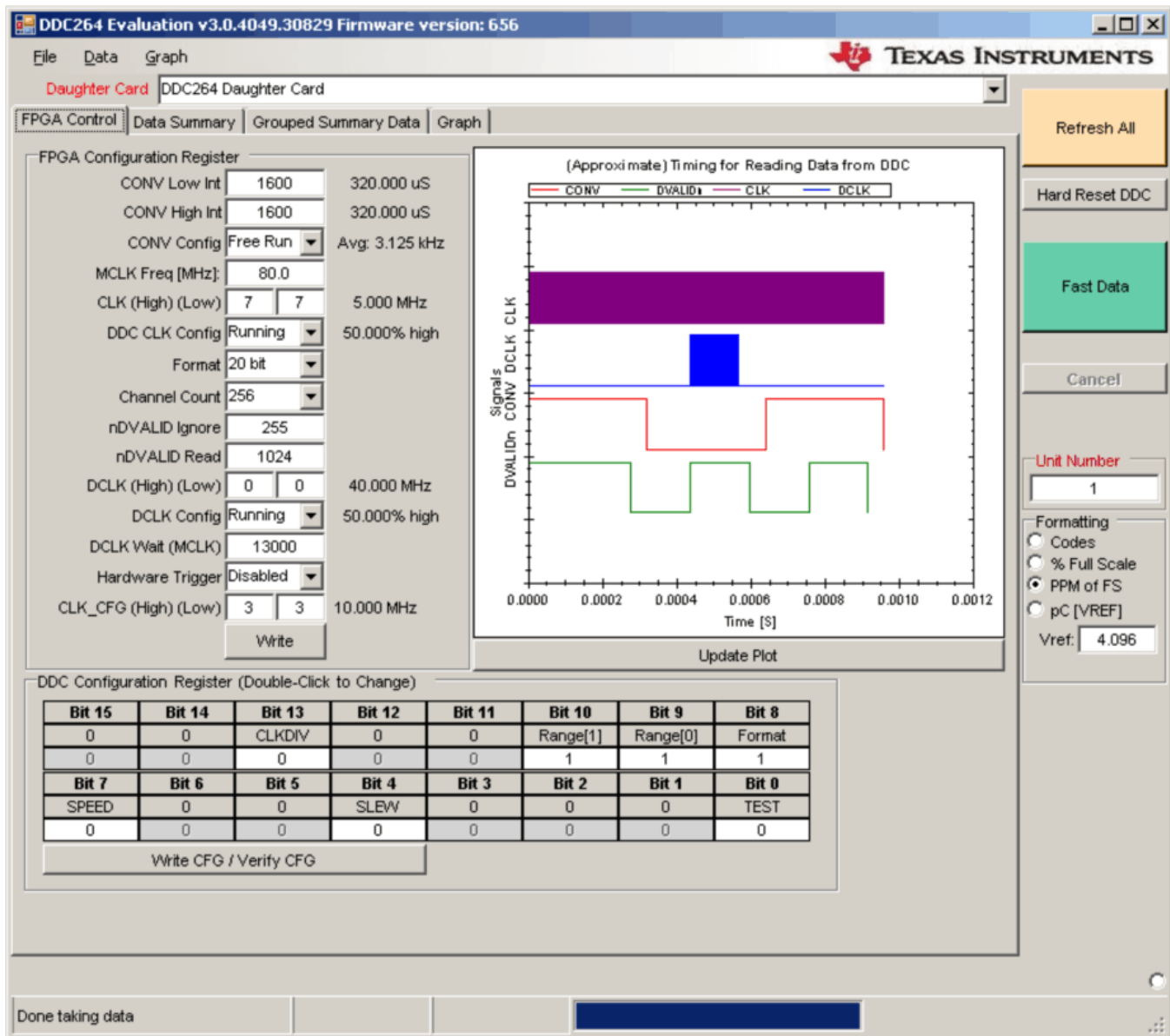


Figure 13. Initial Software Screen, FPGA Control Tab

Next, do a system refresh of the FPGA by clicking on the **Refresh All** button, located in the upper right corner of the screen. This action refreshes the system to the working default settings, and verifies communication with the FPGA. When communication is established, the **Fast Data** button is enabled. The software is now ready to receive data from the DDC264s.

5.3.1 Main Window Controls

A number of controls are always visible, regardless of the tab selected in the main tab control.

The **Refresh All** button updates the state of all FPGA registers, as well as the DDC configuration, to those states set in the FPGA control tab. The **Hard Reset DDC** button performs a hardware-resets of the DDC264 devices. **Fast Data** causes an acquisition cycle to occur and loads data into the program memory. **Cancel** stops the collection of data in process. **Unit Number** is information that can be appended to the data for use in sorting data saved to files. This information is merely text that can be used or ignored as desired.

Data can be displayed in a number of formats, selected with the **Formatting** controls. The options are:

- *Codes*: data are displayed in raw codes or counts
- *% Full Scale*: data are displayed as a percentage of the full scale range
- *PPM of FS*: data are displayed in units of parts per million (PPM) of the full-scale range
- *pC Scaled to Vref*: data are displayed in picocoulombs

The reference voltage can be set in the **Vref** text box control. The default value is 4.096V, which corresponds to the reference voltage provided by the onboard voltage reference on the DDC264EVM, but may be adjusted if a different reference voltage is used.

5.3.2 Main Window Menus

The Main window has three menus: **File**, **Data**, and **Graph**. This section describes the functions of each menu item.

File → *About*

This option displays a window that gives program version information.

Data: This menu has three sub-menu selections:

- *Load Data into Memory*
Saved data can be reloaded into memory for analysis review. These data are retrieved from a standard comma-separated value (CSV) formatted spreadsheet file.
- *Save Data from Memory*
Collected data can be saved to a standard comma-separated value (CSV) formatted spreadsheet file. No header data are written to the file; only raw data. The columns are written in this order: Channel Name, Reading #, Reading [codes], Range [0-7], Vref [V], # of Bits [16 or 20].
Once a reading is made, the data can be saved to a file using the *Save Data from Memory* menu item. The data can then be analyzed further in Microsoft Excel® or a similar spreadsheet application that can parse data in user-defined CSV format.
- *Save Summary Data*
A summary of the collected data can be saved to a standard CSV-formatted spreadsheet file. No header data are written to the file; only raw data. The columns are written in this order: Channel Name, Average Reading, RMS Noise, and Peak-to-Peak Noise.
Once a reading is made, the data can be saved to a file using the *Save Summary Data* menu item. The data can then be analyzed further in Microsoft Excel or a similar spreadsheet application that can parse data in user-defined CSV format.

Graph → *Plot Data on Graph*

If data are loaded into memory but not plotted on the graph (because the **Use Graph** check box is not checked under the Graph tab), selecting this menu item plots that data on the graph.

5.3.3 FPGA Control Tab

The controls on this tab (refer to [Figure 13](#)) directly affect the operating mode of the DDC264s being tested. This section explains the various fields and buttons that reside on this tab.

5.3.3.1 Registers Group Box

The fields in this box hold all the data that are used by the FPGA to generate the waveforms for the device under test and retrieve data. The following list summarizes all of the fields and the respective functions of each. Refer to the individual DDC device data sheets for further information on valid clock times and pin functions.

- **CONV Low Int:** This is the number of DDC System Clock Cycles for the CONV signal to remain low during integration. The actual time is listed next to the text box.
- **CONV High Int:** This is the number of DDC System Clock Cycles for the CONV signal to remain high during integration. The actual time is listed next to the text box.
- **CONV CONFIG:** The default value of this control is *Free Run*, and should be used in the data acquisition process. The other options should not be used.
- **MCLK Freq (MHz):** The master clock frequency used by the FPGA; the default value is 80MHz, which is the oscillator frequency installed on the EVM. This value should not be changed.
- **CLK (High) (Low):** This sets the high and low times of the DDC clock. The default value is 7 in both fields, representing the number of clock cycles that CLK will be high and low.
- **DDC CLK CONFIG:** Choose *Running* to enable the DDC clock or *Low* to disable the DDC clock.
- **FORMAT:** Choose how many bits wide the output word is on the DOUT line (16- or 20-bit). This setting should also match the setting of bit 8 of the DDC Configuration Register. A '1' corresponds to 20-bit word and '0' to 16-bit word.
- **Channel Count:** Number of channels to read back. The number of channels available for reading is in groups of powers of two. The maximum number of channels available on the EVM is 256.
- **nDVALID Ignore:** This is the number of nDVALID pulses to ignore, or rather the number of samples to initially discard from the device. Setting this number higher can help negate the effects of settling and give cleaner data from a dead conversion stop.
- **nDVALID Read:** This is the number of nDVALID pulses after which to capture data. The device has two sides to each integrator, so if there is a 4-channel device, 256 nDVALID Reads equate to 128 samples on four channels of both A and B sides. As a result of a limitation in the memory depth of the DDC264EVM, the maximum data capture for 256 channels is 1792 readings. To calculate other possible variations, two conditions must be met:
 1. $(\text{Channel Count}) * (2) * (\text{nDVALID Read}) < 1048576$; and
 2. $(\text{Channel Count}) * (2) * (\text{nDVALID Read}) / 131072$ must result as an integer.
- **DCLK (High) (Low):** The number of master clock cycles for DCLK to remain low and high during data readback. DCLK can be faster than the DDC System Clock, which is why DCLK is separate and may be much smaller than CLK Count. The divisor for the 80MHz clock is: $\text{DCLK(High)} + 1 + \text{DCLK(Low)} + 1$. In the case where DCLK(High) and DCLK(Low) are both equal to zero, then the divisor is: $2 (0 + 1 + 0 + 1)$, and the resulting clock is 40MHz, which is an acceptable data clock transfer rate.
- **DCLK Config:** The default position is *Running*, which enables the DCLK signal. The DCLK is disabled when the selection is *Low*.
- **DCLK Wait (MCLK):** This is the number of master clock cycles to wait after detecting an nDVALID signal. Once a signal is detected, the data are ready; in some applications, however, a delay is helpful in achieving desired results.
- **HARDWARE TRIGGER:** In normal operation, this should be *Disabled*. If *Enabled*, a pulse can be issued on J4 to start a conversion after **Fast Data** is pressed. If enabled and no pulse ever comes, the program appears to be frozen. If this condition happens, disable, cancel out the error messages, and refresh.
- **CLK_CFG (HI, LO):** This sets the number of master clock cycles to hold the DDC Data Clock (DCLK) high or low. The default value is '3' in both fields, and represents the number of clock cycles that DCLK will be high or low.

The **Write** button sends data from the PC to the FPGA, programming the settings in the FPGA to correspond to the settings listed above. When this button is pressed, the data are written and read back. If the data read back equal the data written, the screen appears as normal; however, if the data read back is different than the data set in the fields above, the text in those fields appears in a different color than black (on most systems, it appears in a dark red color).

5.3.3.2 DDC Configuration Register Box

The options in this box set and then read back the configuration register settings for the DDC264s installed on the DDC264EVM. Information regarding the specific register settings is described in the [DDC264 product data sheet](#). The available settings appear as white boxes. To change the bit value, double-click inside the box that contains the bit value to be changed. The bit then toggles to the opposite state displayed previously.

Pressing the **WriteCFG/Verify CFG** button sets the DDC264s to the desired configuration setting, and then verifies the setting by reading back the configuration register data. Any bit value displayed in **red** shows a conflict between the data written and the data read back.

5.3.3.3 (Approximate) Timing for Reading Data from DDC Box

This box shows a graphical representation of the approximate timing that is used based on the configuration information entered in the FPGA Configuration Register. The plot shows the approximate location of the DCLKs used for data readback with respect to CLK, CONV, and nDVALID signals. This timing plot can be used as a quick check to prevent timing violations as well as ensuring that data can be read within the time specified by the conversion clock. See the [product data sheet](#) for examples of when and how to set up timing for optimal data readback.

Pressing the **Update Plot** button resets the graphical display to the current values entered in the FPGA Configuration Register entry boxes.

5.3.4 Data Summary Tab

This tab, illustrated in Figure 14, displays the data in summary form. It displays all the channels, the average value measured by the channels, the RMS noise of the measured data, the peak-to-peak noise of the measured data, and the units that all these measurements are reported in. It also displays the RMS noise of all channels averaged together at the very top left.

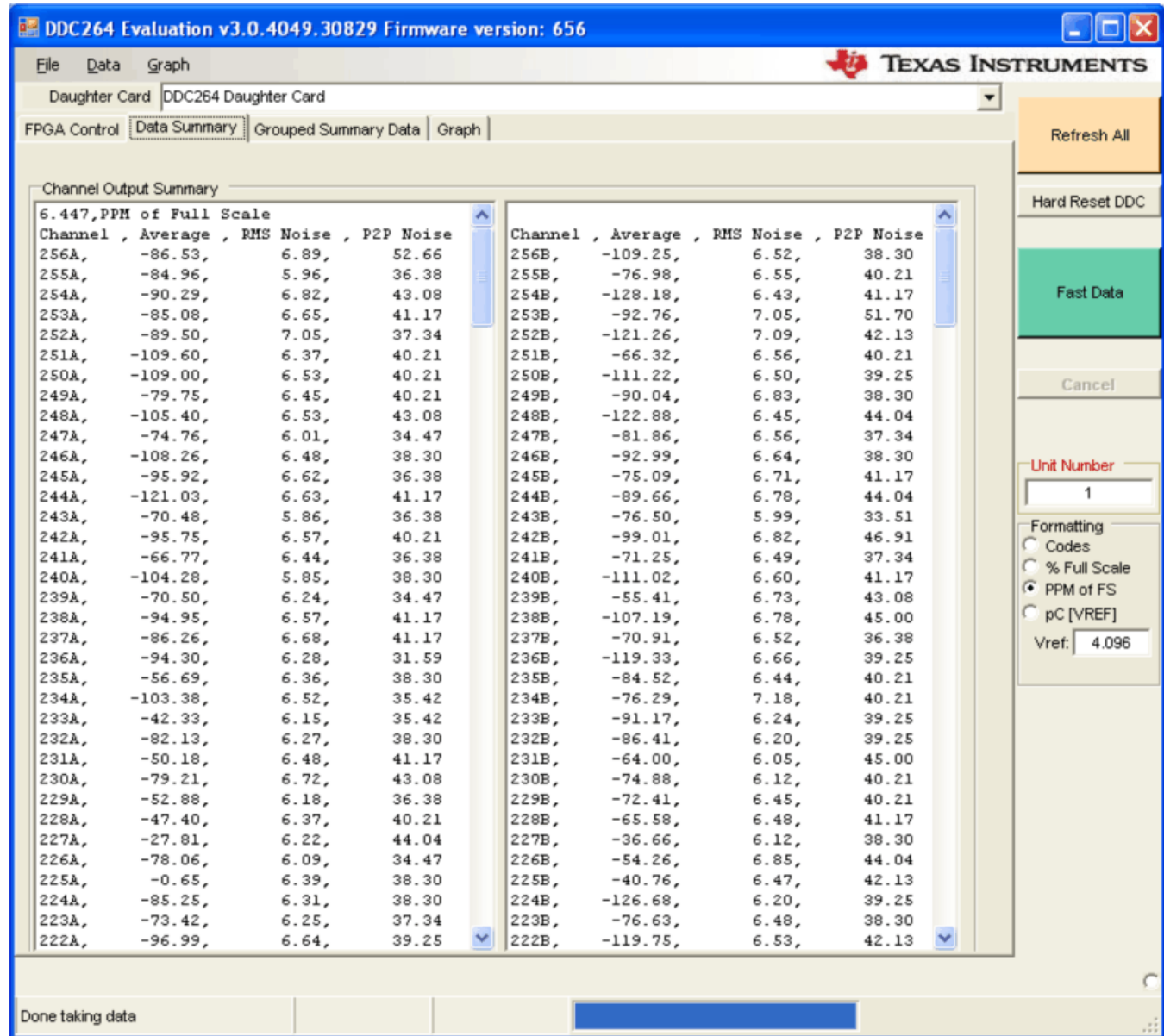


Figure 14. Data Summary Tab

The format that the data are displayed in is controlled by the formatting options set in the main window **Formatting** controls.

5.3.5 Grouped Summary Tab

This tab, shown in [Figure 15](#), summarizes the channel data as a grouping. The information displayed is based on the format selection and consists of channel averages for A-side, B-side, odd-channel, and even-channel noise.

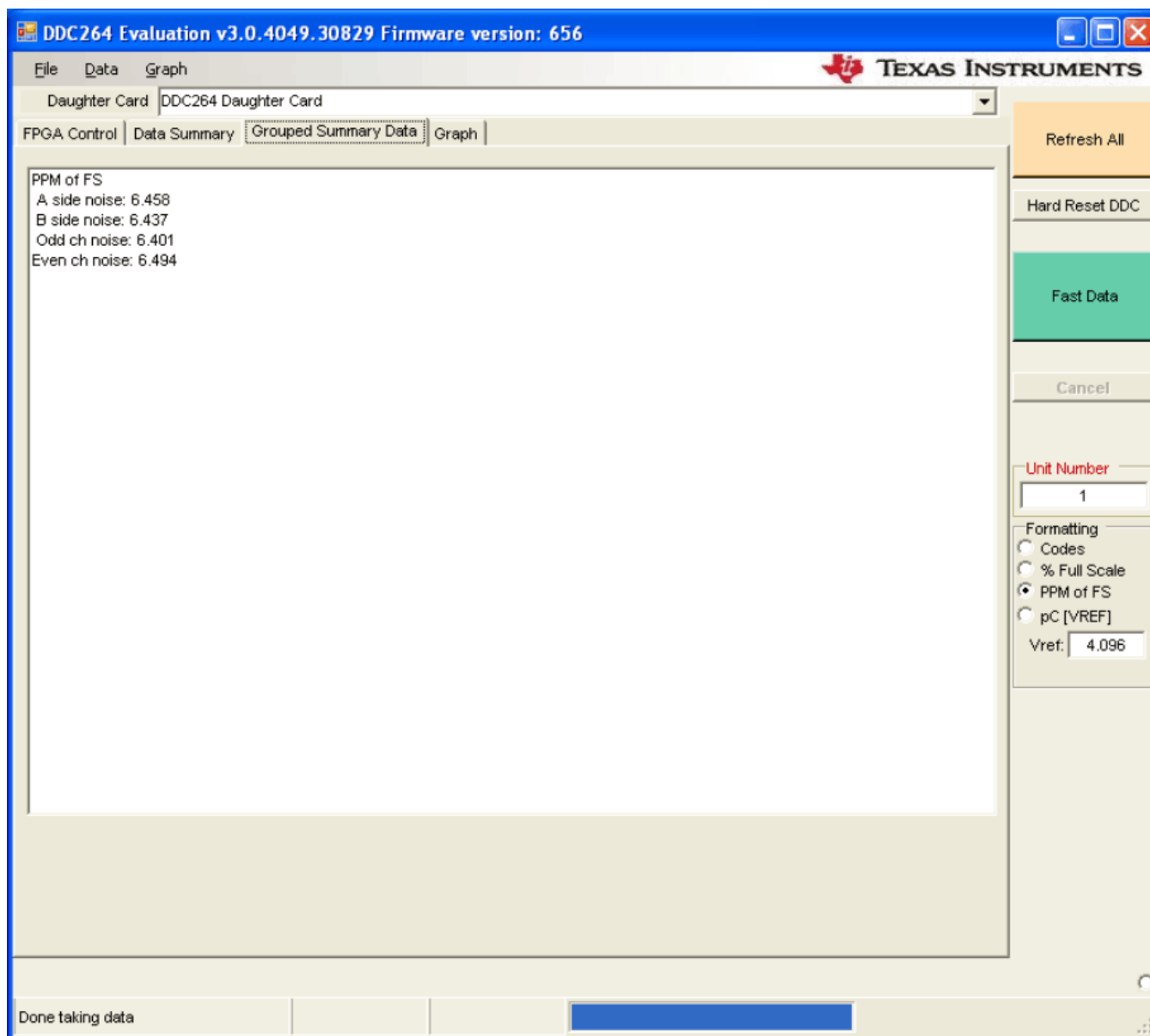


Figure 15. Grouped Summary Tab

5.3.6 Graph Tab

The graph tab allows for a quick visual representation of the data collected. Some of the data are presented for all device channels, while others only show the plot of a single device channel.

Some of the selections show results based on the Formatting setting, while others ignore the Formatting setting and report the result in the format shown in the graph.

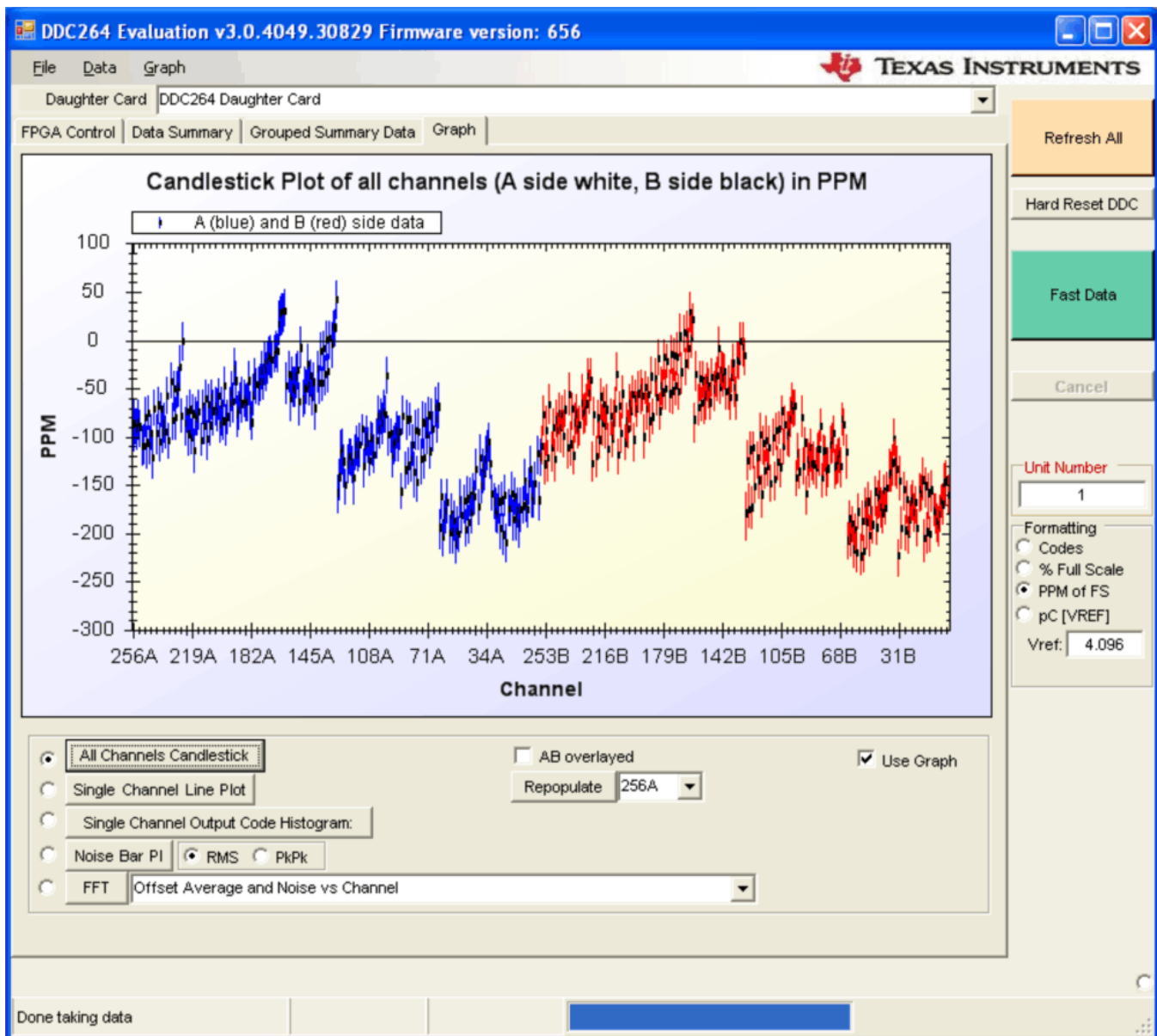


Figure 16. Graph Tab

Two check boxes appear in the selection portion beneath the graph. When checked, **AB Overlayed** shows both the A and B channel data. The **Use Graph** box, when checked, updates the graph as soon as new data are collected; otherwise, any new data are ignored.

The channel drop-down menu allows single channel data to be displayed. The entries that can be selected depend on the *Channel Count* entered in the *FPGA Channel Count* on the FPGA Control tab. Pressing the **Repopulate** button resets the graph to the most recent data, and regenerates the graph that is displayed.

Left-clicking and dragging a box within the graph window zooms in to the selected section of the graph.

Right-clicking on the graph brings up an option menu for limited zoom, format, print, copy, save, and display features.

5.3.6.1 All Channels Candlestick

Figure 17 shows the *All Channels Candlestick* graph, which presents the RMS noise. Channel A is presented in blue and channel B in red. Each channel candlestick marker is centered on the channel average. The red and blue lines extend out from the maximum to the minimum for each channel.

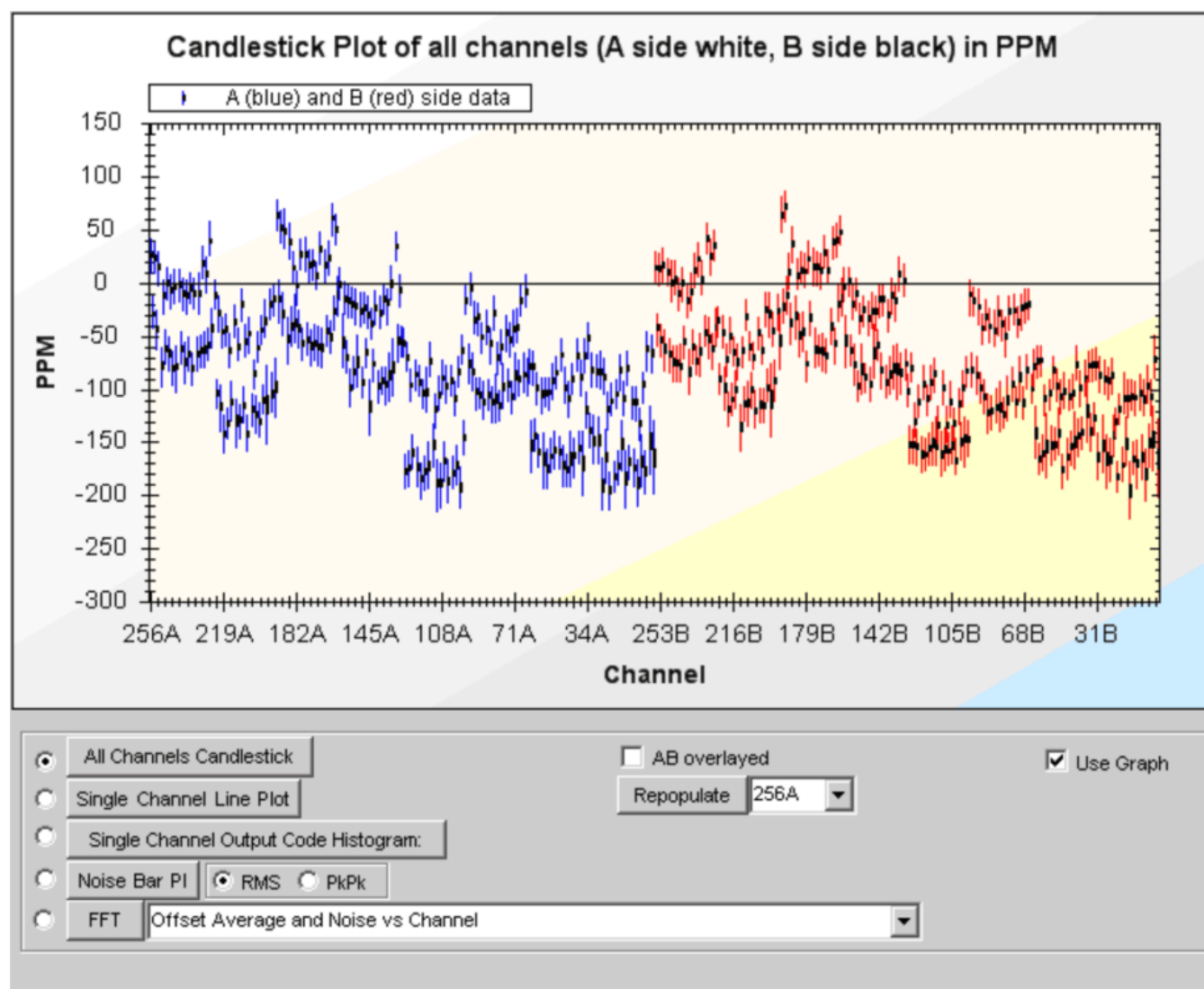


Figure 17. All Channels Candlestick Graph

5.3.6.2 Single Channel Line Plot

The plot (as shown in [Figure 18](#)) presents a sequential series of data for a single channel. The desired channel to be displayed can be selected from the drop-down menu.

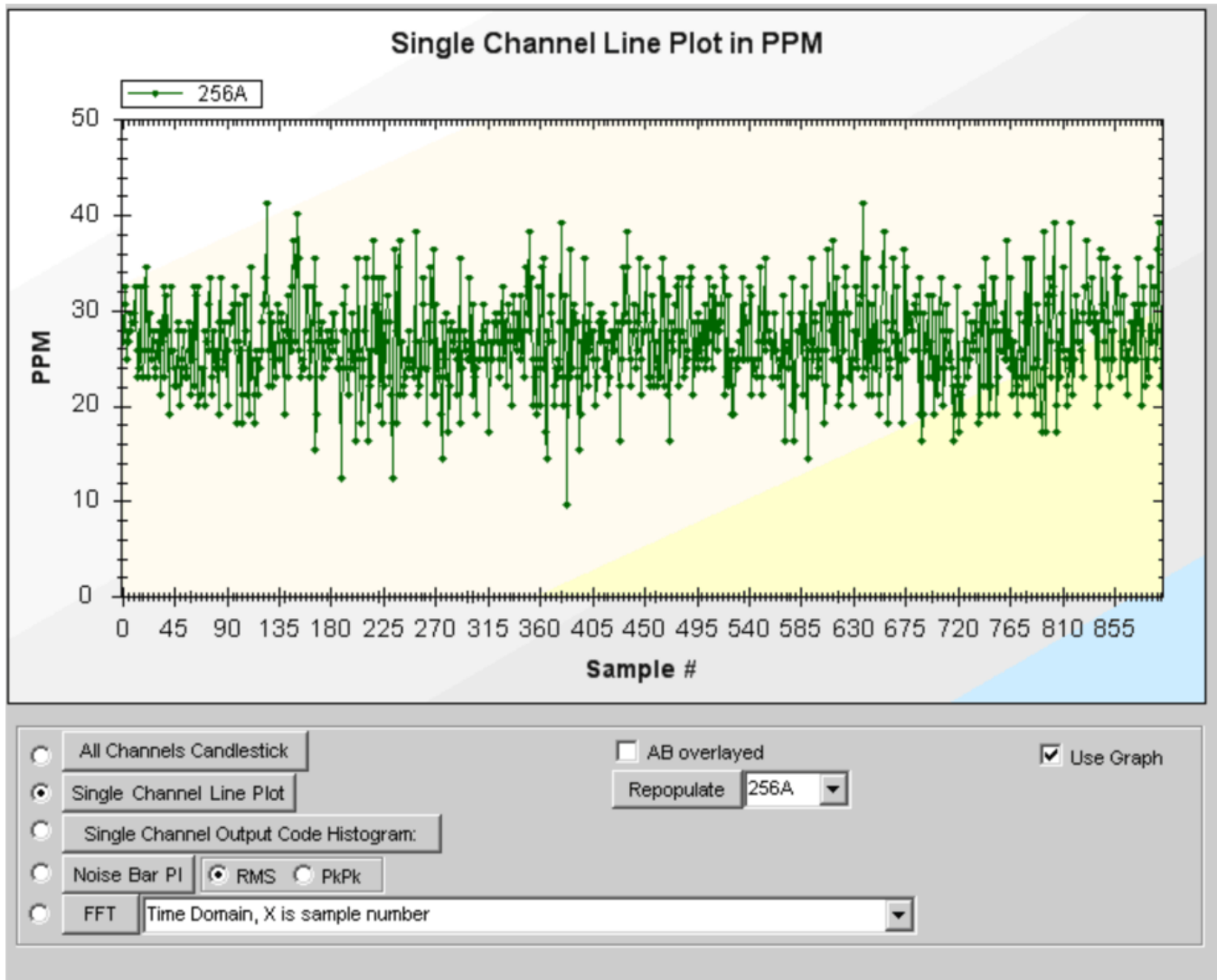


Figure 18. Single Channel Line Plot

5.3.6.3 Single Channel Output Code Histogram

This plot shows a single channel histogram result, as displayed in [Figure 19](#). The desired channel to be displayed can be selected from the drop-down menu. The result is displayed only in codes.

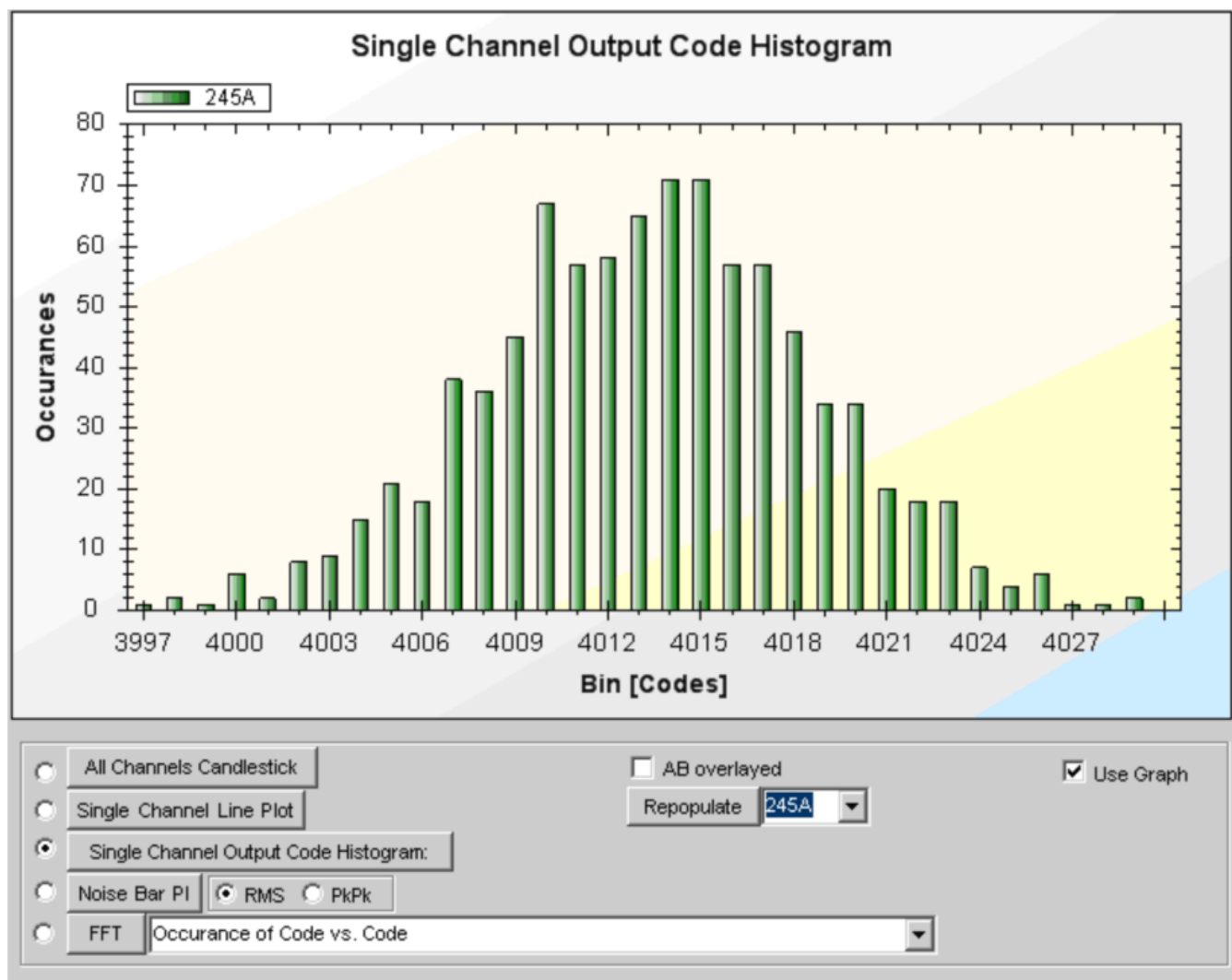


Figure 19. Single-Channel Output Code Histogram

5.3.6.4 Noise Bar Plot

The Noise Bar Plot (refer to [Figure 20](#)) displays results based on the selection of RMS or peak-to-peak (PkPk) values. The **RMS** button result is the RMS noise measurement for the channels displayed in parts-per-million of full-scale (ppm_{FS}). The **PkPk** button changes the result to peak-to-peak noise in ppm_{FS} .

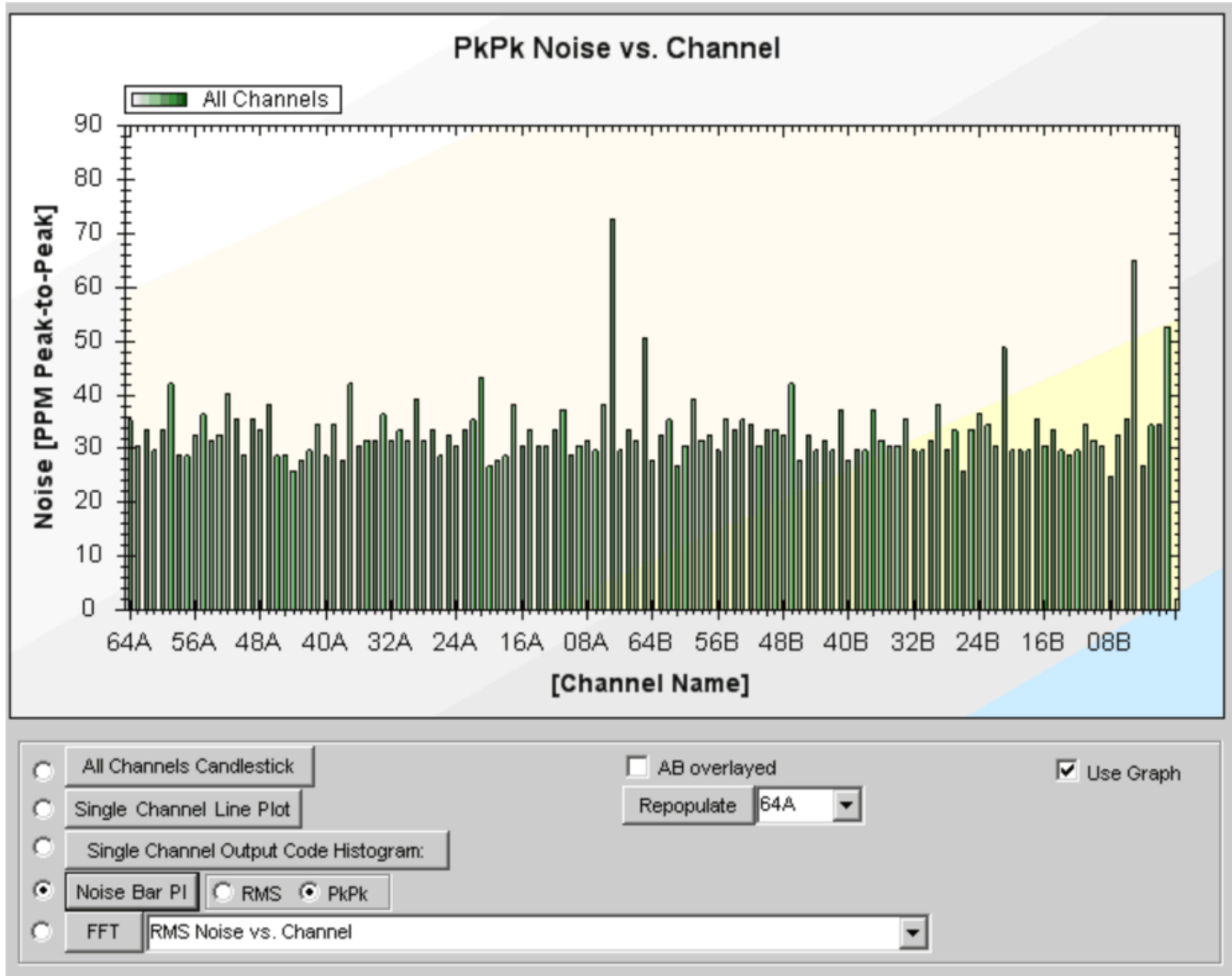


Figure 20. Noise Bar Plot

5.3.6.5 FFT

The FFT plot (illustrated in Figure 21) presents data for a single channel. The channel is selected from the channel drop-down menu. Five different windowing options can be selected from the drop-down menu next to the **FFT** button.

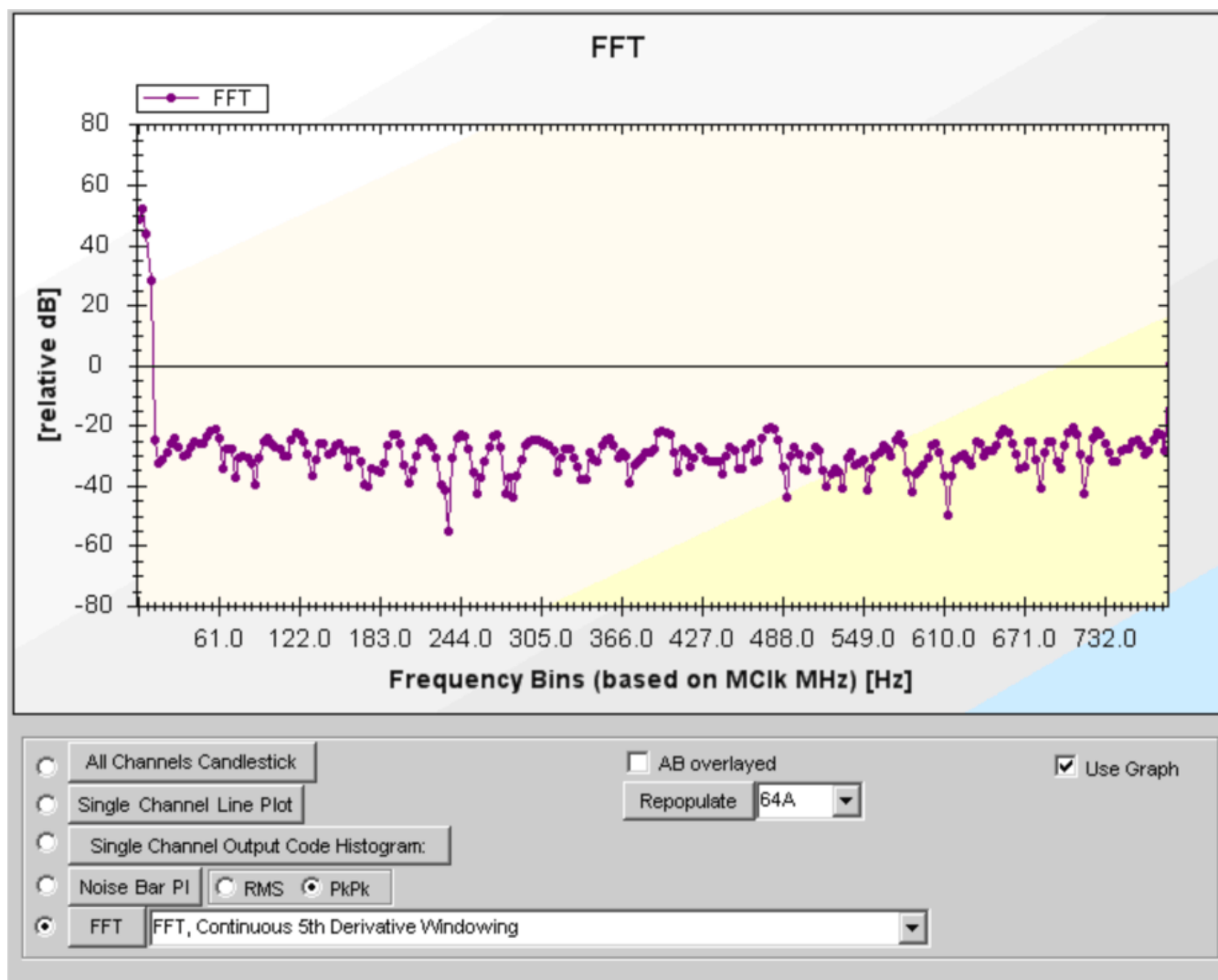


Figure 21. Example FFT Plot

5.4 Troubleshooting

If you see an error message on the main window status bar saying *Error Writing FPGA Registers*, this message indicates that the DDC264EVM is either not connected via USB or has not been properly detected by the system. Verify that the USB connection is good, or press the RESET_USB (S1) button on the DDC264EVM to allow communication to be established.

6 Schematics and Layout

Full-size schematics for the DDC264EVM board is appended to this user's guide. The bills of material is provided in [Section 6.1](#).

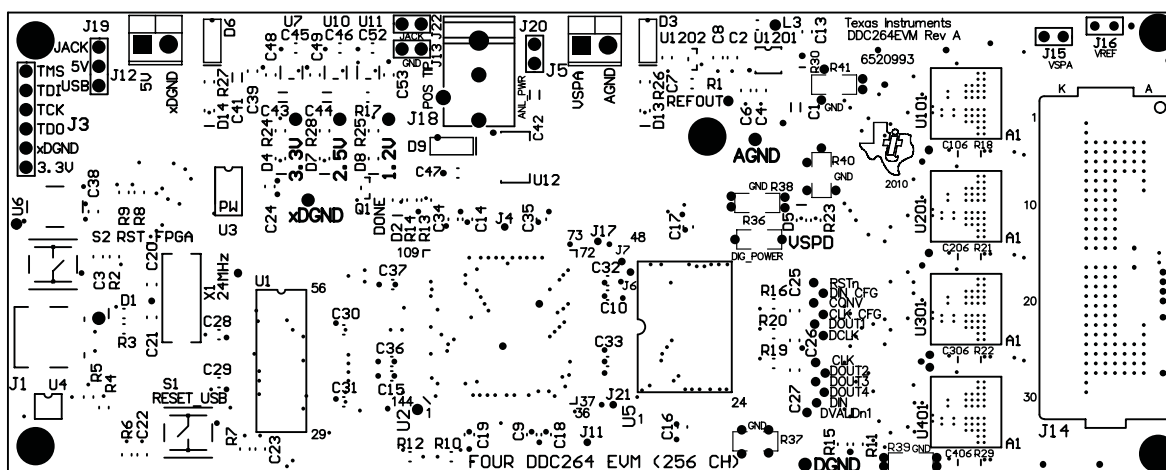


Figure 22. Top Silkscreen for DDC264EVM DUT Board

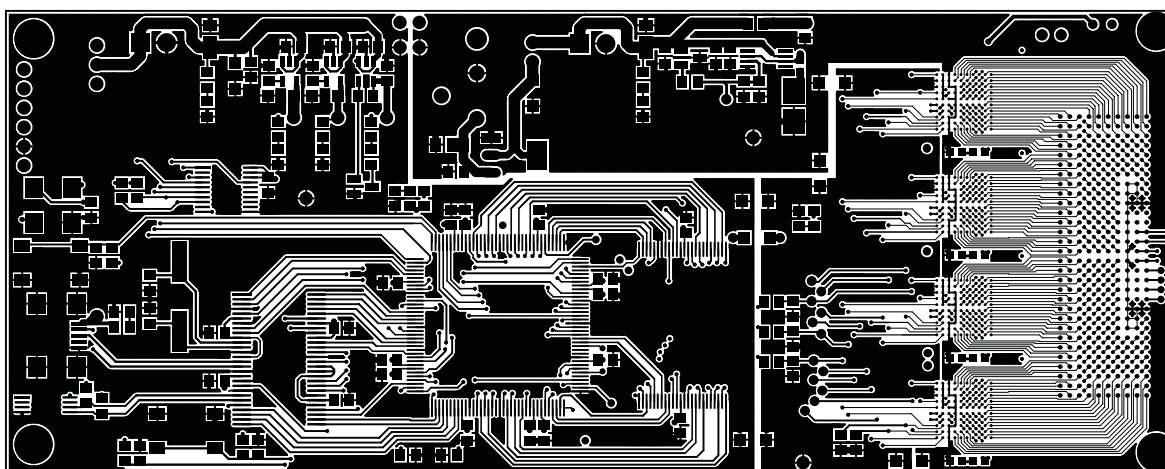


Figure 23. Top Layer of DDC264EVM DUT Board

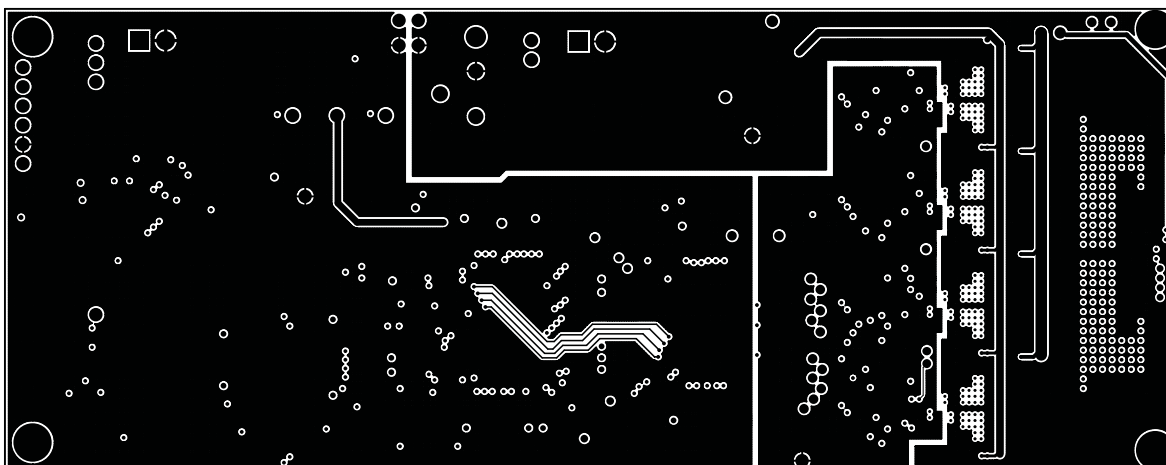


Figure 24. DDC264EVM DUT Board: Layer 2

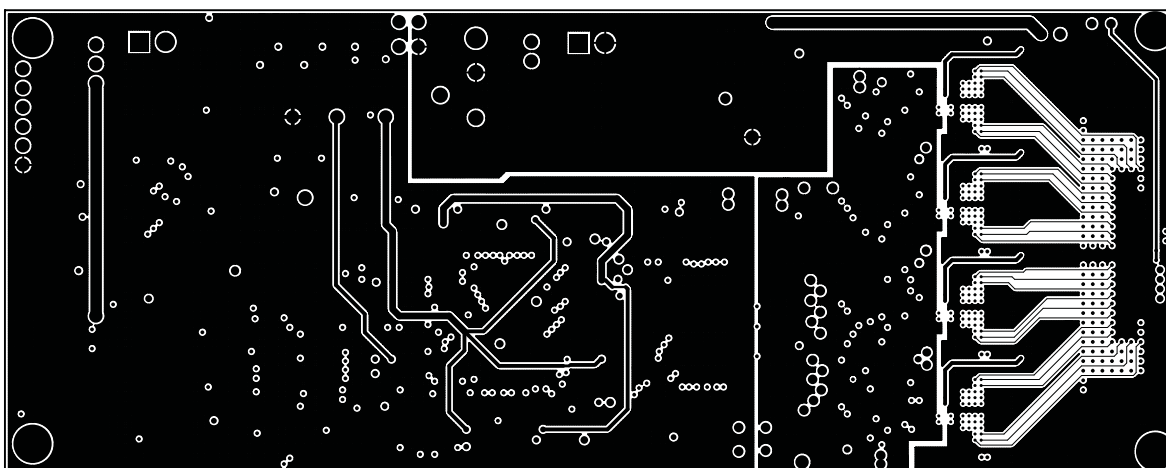


Figure 25. DDC264EVM DUT Board: Layer 3

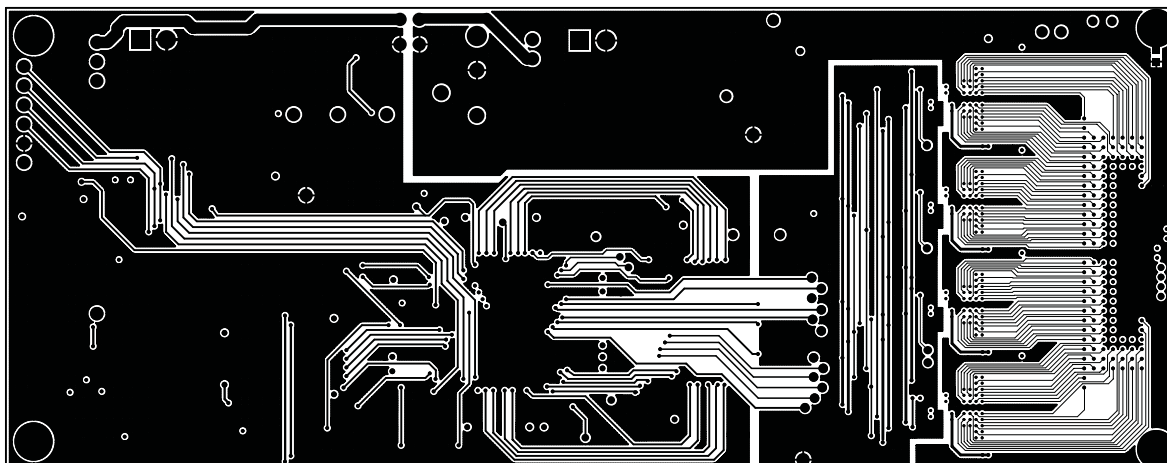


Figure 26. Bottom Layer of DDC264EVM DUT Board

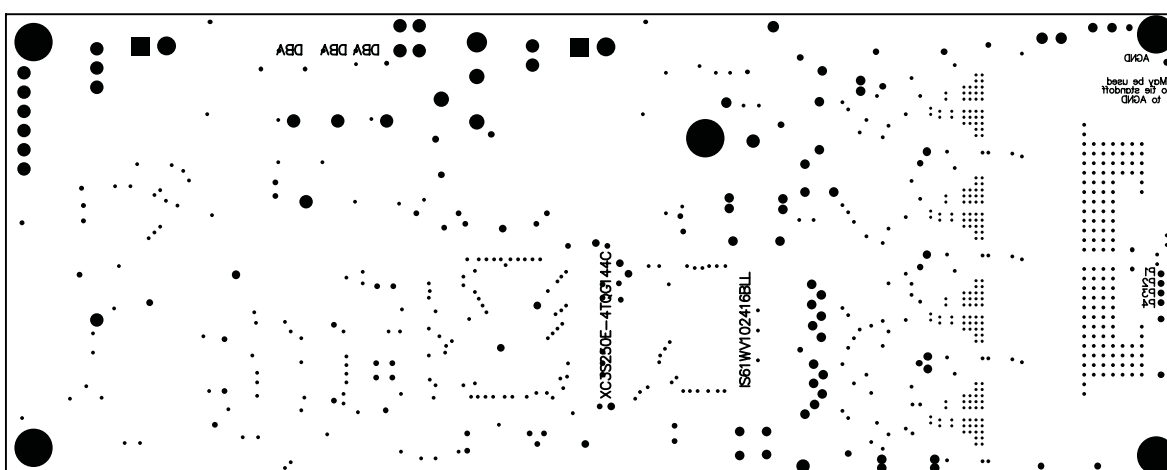


Figure 27. Bottom Silkscreen for DDC264EVM DUT Board

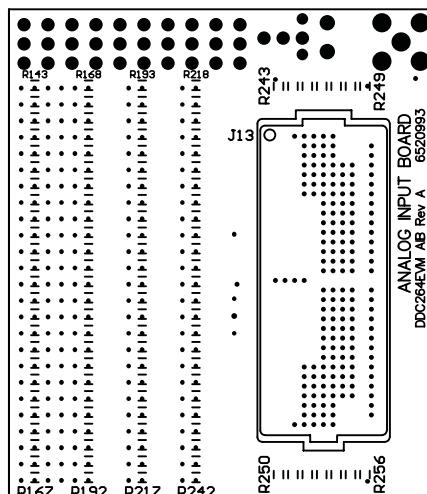


Figure 28. Top Silkscreen of Analog Interface Board

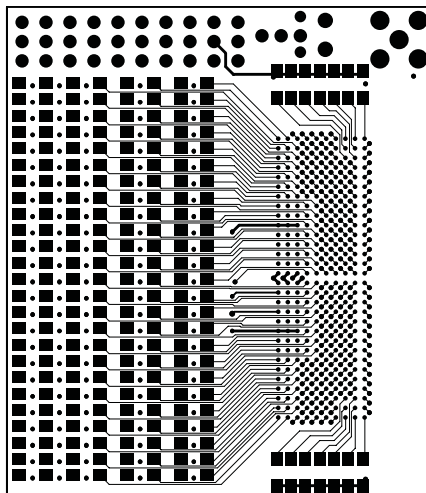


Figure 29. Top Layer of Analog Interface Board

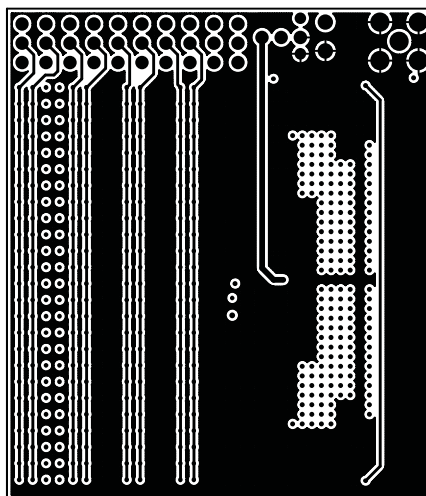


Figure 30. Analog Interface Board: Layer 2

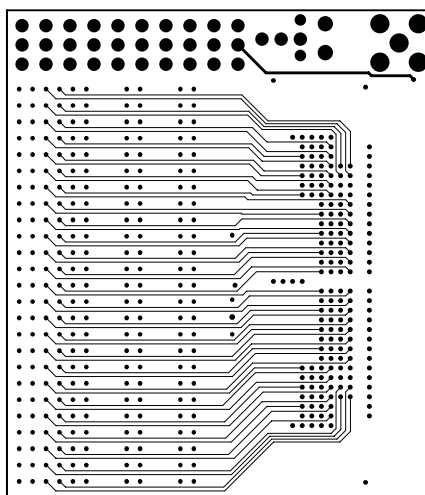


Figure 31. Analog Interface Board: Layer 3

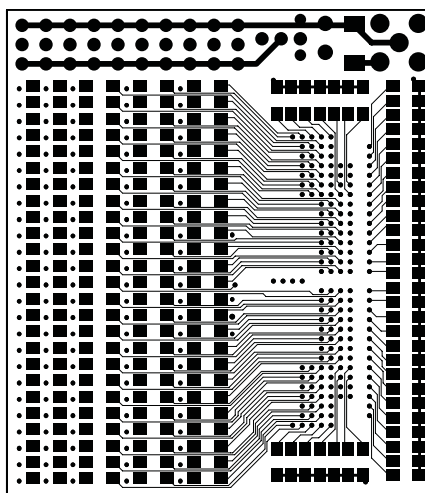


Figure 32. Bottom Layer of Analog Interface Board

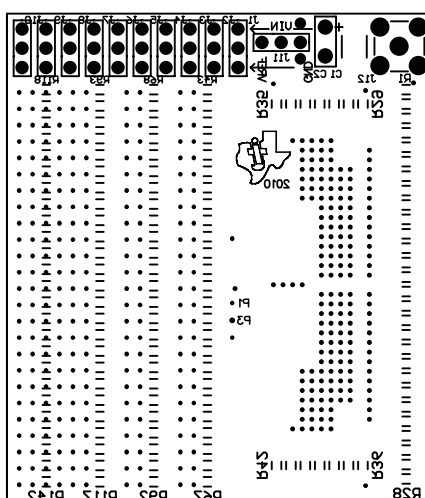


Figure 33. Bottom Silkscreen of Analog Interface Board

6.1 Bills of Material

NOTE: All components should be RoHS compliant. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS compliant.

Table 4. DDC264EVM Bill of Materials

Item	Qty	Ref Des	Description	Manufacturer	Part Number
1	1	N/A	Printed wiring board	TI	6520993
2	1	C1	Capacitor, ceramic 100µF 6.3V X5R 1206	Kemet	C1206C107M9PACTU
3	27	C2, C3, C6, C7, C9, C10, C14, C15, C16, C17, C18, C19, C22, C23, C24, C28 to C39	Capacitor, ceramic 0.10µF 50V X7R 0805	Kemet	C0805C104J5RACTU
4	1	C4	Capacitor, ceramic 47µF 6.3V X5R 0805	Taiyo Yuden	JMK212BJ476MG-T
5	2	C8, C13	Capacitor, ceramic 10µF 16V X5R 0805	Taiyo Yuden	EMK212BJ106KG-T
6	2	C20, C21	Capacitor, ceramic 10pF 630V X7R 0805	Kemet	C0805C100KBRACU
7	3	C25, C26, C27	Capacitor, ceramic 47pF 630V X7R 0805	Kemet	C0805C470KBRACU
8	4	C41, C42, C43, C44	Capacitor, ceramic 10µF 10V X7R 20% 1206	TDK	C3216X7R1A106M
9	3	C45, C46, C47	Capacitor, ceramic 0.33µF 10% 16V X7R 0805	AVX	0805YC334KAT2A
10	2	C48, C49	Capacitor, ceramic 10000pF 50V X7R 0805	Yageo	CC0805KRX7R9BB103
11	2	C52, C53	Capacitor, ceramic 1.0µF 16V X7R 0805	Murata	GRM21BR71C105KA01L
12	4	C106, C206, C306, C406	Capacitor, ceramic 10µF 6.3V X5R 0603	Taiyo Yuden	JMK107BJ106MA-T
13	8	D1, D2, D4, D5, D7, D8, D13, D14	LED Thin 565nm Grn Diff 0805 SMD	Lumex Opto	SML-LXT0805GW-TR
14	3	D3, D6, D9	Diode SBR 3A 40V Power DI123	Diodes Inc	SBR3U40P1-7
15	1	J1	Connector, receptor Mini USB 2.0 5-Position	Hirose Electric	UX60A-MB-5ST
16	1	J3	Connector, header 6-Position .100" SGL Gold	Samtec	TSW-106-07-G-S
17	0	J4, J6, J7, J11, J17, J21	Not installed		
18	2	J5, J12	Terminal block 3.5mm 2-Position PCB	On Shore	ED555/2DS
19	0	J13, J15, J16	Not installed		
20	1	J14	Connector, Meg-array 300 Position Plug Assy	FCI	84500-002LF
21	2	J20, J22	Connector, header 2-Position .100" SGL Gold	Samtec	TSW-102-07-G-S
22	1	J18	Connector, power jack 2.5X5.5MM High Current	CUI Inc	PJ-102BH
23	1	J19	Connector, header 3-Position 0.100" SGL Gold	Samtec	TSW-103-07-G-S
24	1	L3	Ferrite chip bead 600Ω 0805 SMD	TDK	MPZ2012S601A
25	1	Q1	MOSFET N-Channel 30V 2.2A SSOT3	Fairchild	FDN337N
26	1	R1	Resistor 1.00kΩ 1/8W 1% 0805 SMD	Panasonic	ERJ-6ENF1001V
27	3	R2, R6, R7	Resistor 100kΩ 1/8W 1% 0805 SMD	Rohm	MCR10EZH1003
28	3	R3, R13, R14	Resistor 499Ω 1/8W 1% 0805 SMD	Rohm	MCR10EZH4990

Table 4. DDC264EVM Bill of Materials (continued)

Item	Qty	Ref Des	Description	Manufacturer	Part Number
29	2	R4, R5	Resistor 2.21k Ω 1/8W 1% 0805 SMD	Rohm	MCR10EZHF2211
30	2	R8, R9	Resistor 4.99k Ω 1/8W 1% 0805 SMD	Yageo	RC0805FR-074K99L
31	4	R10, R11, R12, R15	Resistor 47.0k Ω 1/8W 1% 0805 SMD	Rohm	MCR10EZHF4702
32	3	R16, R19, R20	Resistor 33.0 Ω 1/8W 1% 0805 SMD	Rohm	MCR10EZHF33R0
33	1	R17	Resistor 10k Ω 1/8W 1% 0805 SMD	Rohm	MCR10EZPF1002
34	5	R18, R21, R22, R29, R30	Resistor 0.68 Ω 1/5W 1% 0603 SMD	Susumu	RP1608S-R68-F
35	2	R23, R24	Resistor 200 Ω 1/8W 1% 0805 SMD	Rohm	MCR10EZHF2000
36	3	R25, R26, R27	Resistor 402 Ω 1/8W 1% 0805 SMD	Rohm	MCR10EZHF4020
37	1	R28	Resistor 100 Ω 1/8W 1% 0805 SMD	Rohm	MCR10EZHF1000
38	6	R36 - R41	Resistor 0.0 Ω 1/4W 1206 SMD	Rohm	MCR18EZJ000
39	2	S1, S2	Switch Tact 6MM MOM SMD 100GF	Omron	B3FS-1000P
40	1	U1	IC MCU USB Peripheral HI SPD 56SSOP	Cypress	CY7C68013A-56PVXC
41	1	U2	IC Spartan-3E FPGA 250k 144TQFP	Xilinx	XC3S250E-4TQG144C
42	1	U3	IC PROM SRL for 4M GATE 20-TSSOP	XILINX	XCF04SVOG20C
43	1	U4	IC SRL EEPROM 128-Bit 5V 8-TSSOP	Microchip	24LC00-I/ST
44	1	U5	IC SRAM 16MB ASYNC 48-TSOP	ISSI	IS61WV102416BLL-10TLI
45	1	U6	OSC 80.0000MHz 3.3V $\pm$ 25PPM SMD	Connor-Winfield	CWX813-80.0M
46	1	U7	IC LDO regulator 3.3V 400mA SOT23-5	Texas Instruments	REG113NA-3.3
47	1	U10	IC LDO regulator 2.5V 400mA SOT23-5	Texas Instruments	REG113NA-2.5
48	1	U11	IC LDO regulator 1.2V 150mA SOT23-5	Texas Instruments	SN105125DBVR
49	1	U12	IC LDO 5.00V regulator SOT223-4	Texas Instruments	REG1117-5
50	4	U101, U201, U301, U401	64-Ch, Current-Input A/D Converter 100BGA	Texas Instruments	DDC264CKZW
51	1	U1201	IC Op Amp GP R-R 38MHz SGL 8MSOP	Texas Instruments	OPA350EA
52	1	U1202	IC Voltage Reference 4.096V LP SOT23-3	Texas Instruments	REF3040AIDBZT
53	1	X1	Crystal 24.000MHz 16pF SMD	ECS Inc	ECS-240-16-5PX-TR
54	5	N/A	Screw, Mach Philips 4-40x1/4 Nylon	B & F Fasteners	NY PMS 440 0025 PH
55	5	N/A	Standoff hex 0.25"L 4-40Thr Nylon	Keystone	1902A
56	3	N/A	0.100 Shunt—Black Shunts	Samtec	SNT-100-BK-G

Table 5. Analog Input Board (AIB) Bill of Materials

Item	Qty	Ref Des	Description	Manufacturer	Part Number
1	1	NA	DDC264EVM AIB Rev A Circuit Board	TI	6520993
2	1	C1	Capacitor, Tantalum 220 μ F 10V 20% 6032 SMD	Kemet	T491C227M010ZT
3	0	C2	Not installed		
4	11	J1 to J11	Connector, Header 3-Position 0.100" SGL Gold	Samtec	TSW-103-07-G-S
5	1	J12	Connector, Female R/A PCB MT	Linx Technologies Inc	CONSMA002
6	1	J13	Connector, Meg-array 300 Position 4mm	FCI	84501-101LF
7	256	R1 to R256	Resistor 10M Ω 1/4W 1% 0204 MELF	Vishay	2312 155 11006
8	0	TP1, TP2	Not installed		
9	1	N/A	Connector, ADT SMA Plug-BNC Jack	Amphenol Connex	242102
10	11	N/A	0.100 Shunt—Black Shunts	Samtec	SNT-100-BK-G

D



B

A

D

C

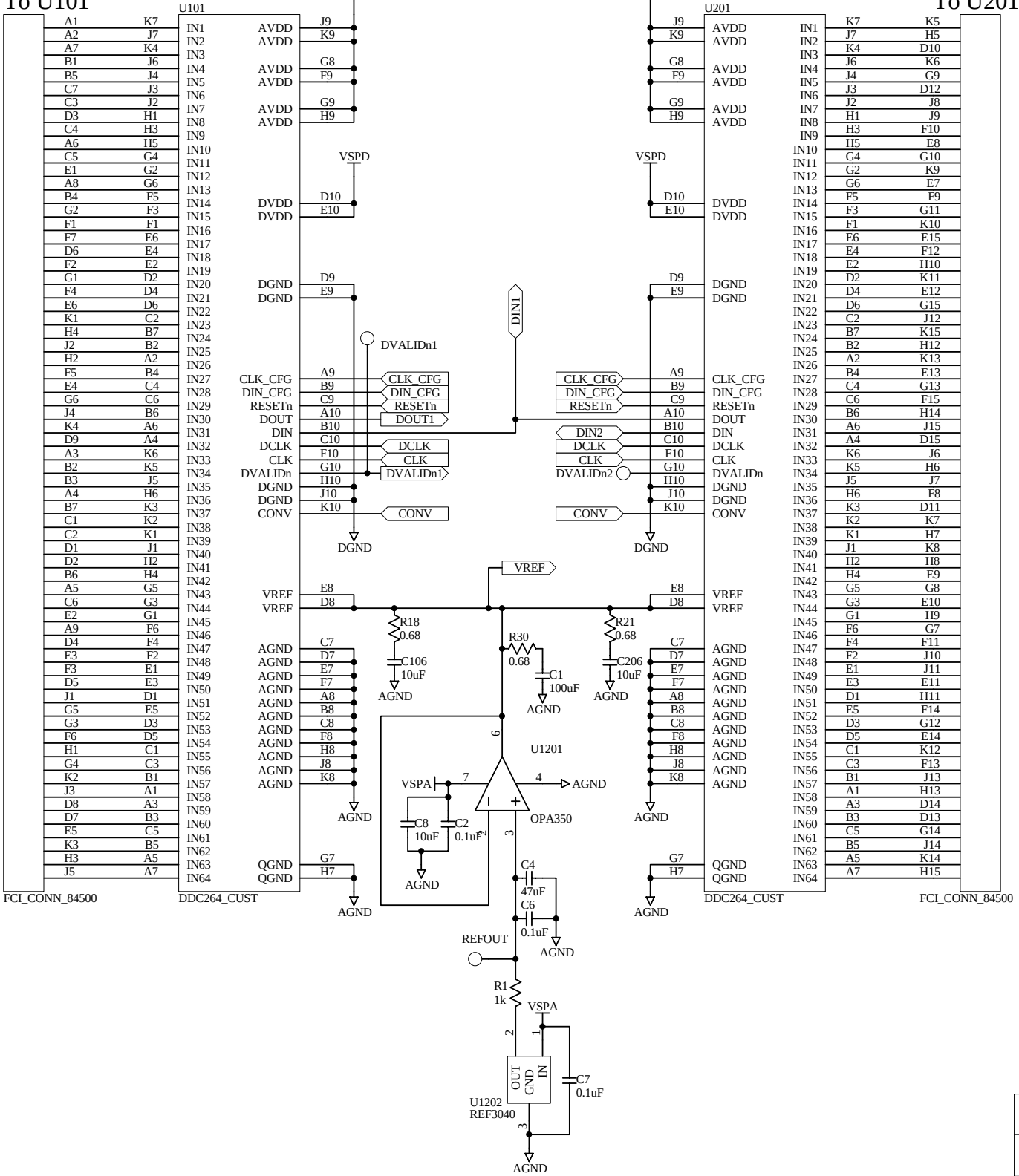
B

A

DDC264 1 and 2 and Support Circuitry

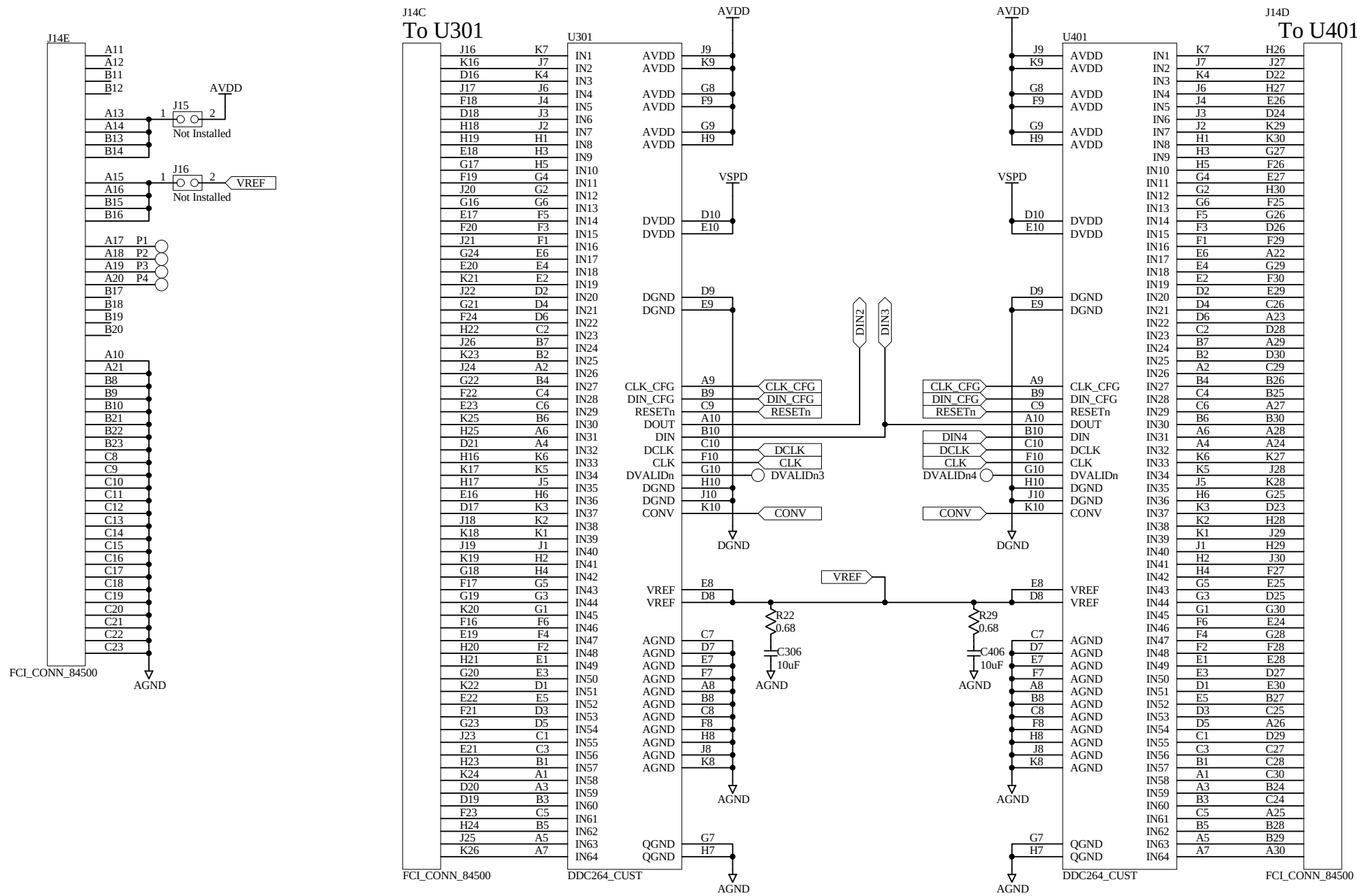
To U101

To U201



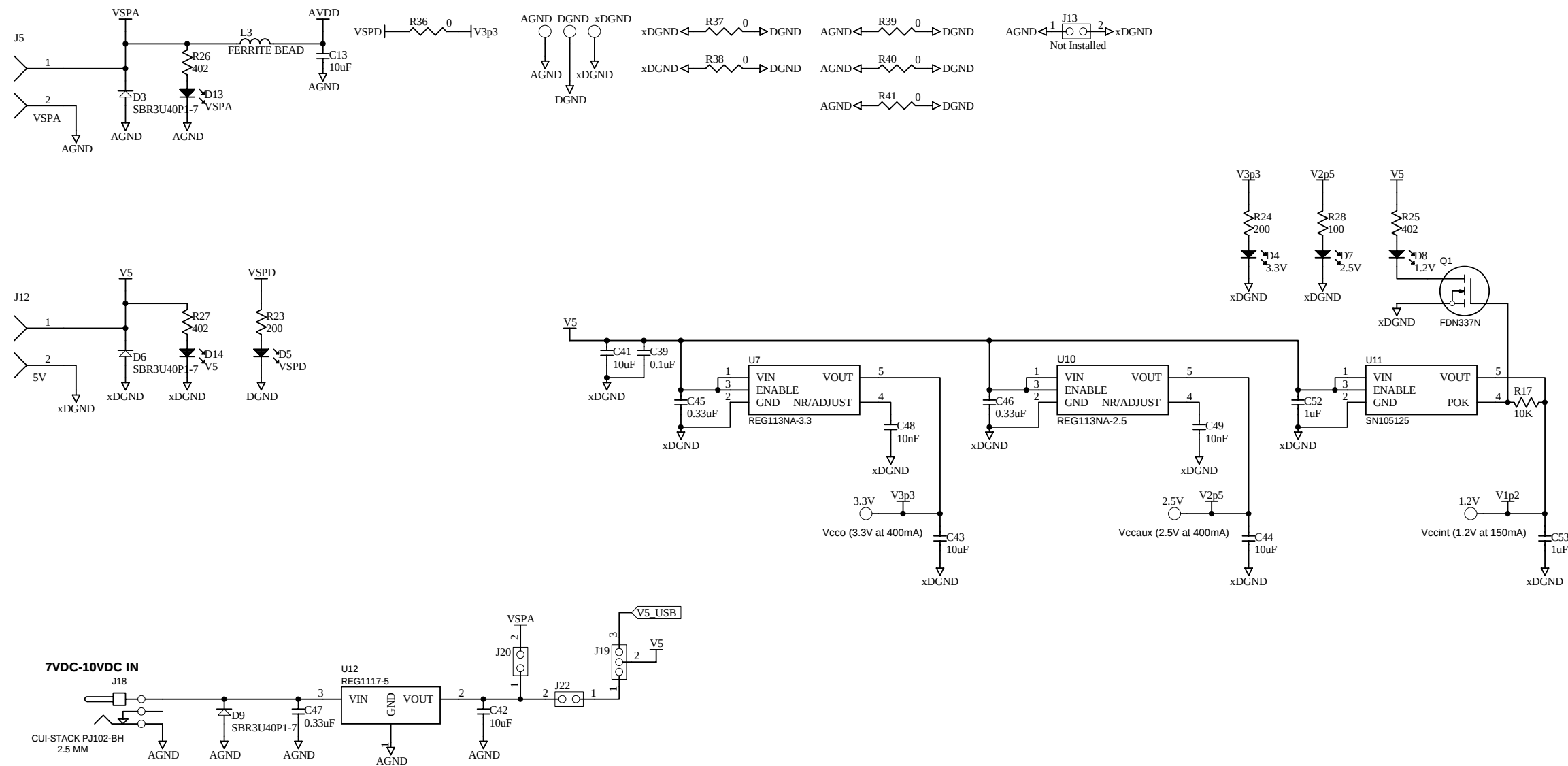
Title			DDC264EVM
Size	Number	Revision	
B	6520993	A	
Date:	28-Jan-2011	Sheet3 of 5	
File:	C:\Work\DDC264\DDC264_a.ddb	Drawn By:	

DDC264 3 and 4 and Support Circuitry



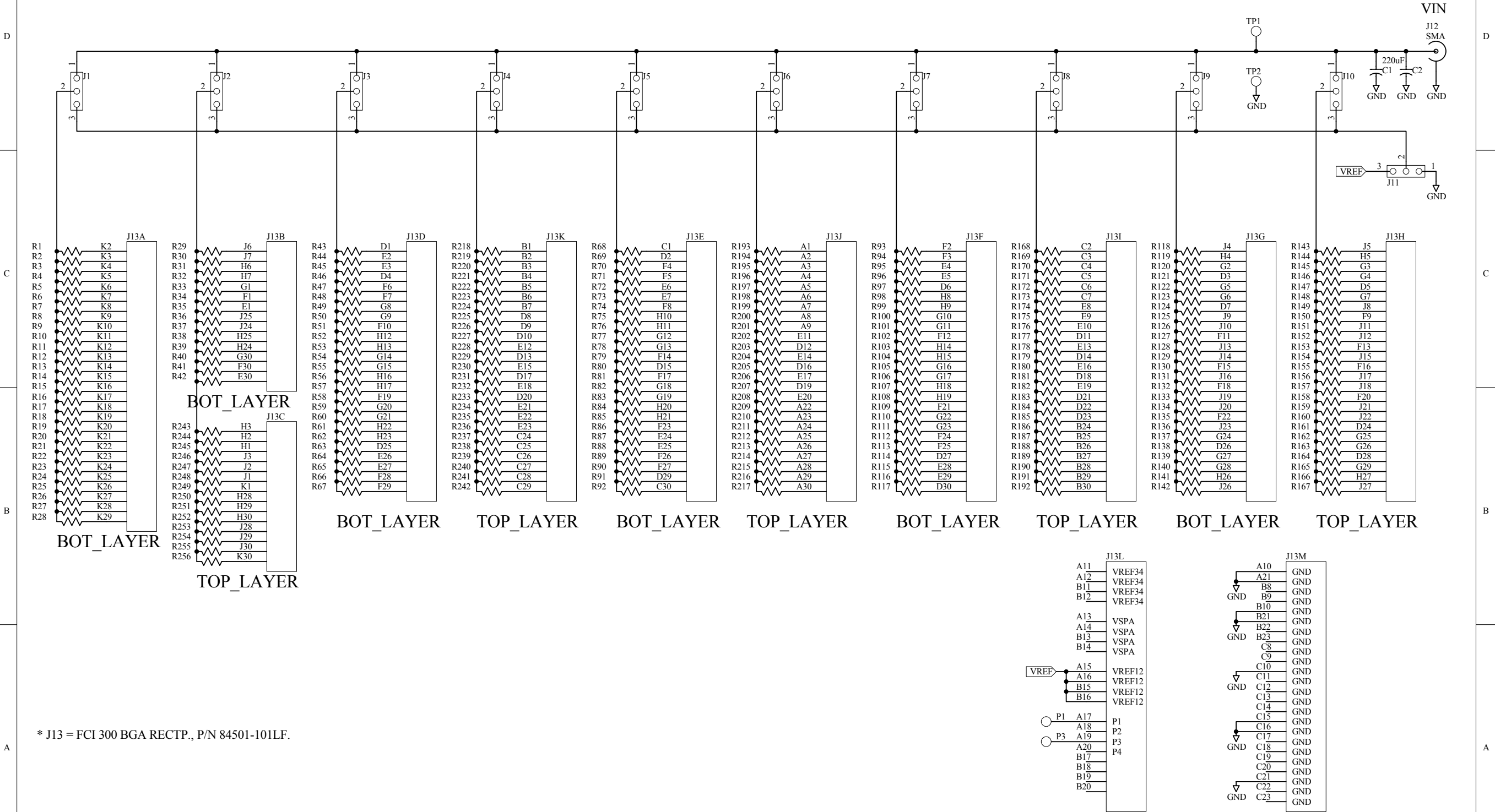
Title			DDC264EVM
Size	Number	Revision	
B	6520993	A	
Date:	28-Jan-2011	Sheet4 of 5	
File:	C:\Work\DDC264\DDC264_a.ddb	Drawn By:	

Power



Title				DDC264EVM			
Size B		Number 6520993				Revision A	
Date:		28-Jan-2011				Sheet 5 of 5	
File:		C:\Work\DDC264\DDC264_a.ddb				Drawn By:	

Analog Input Board



* J13 = FCI 300 BGA RECTP., P/N 84501-101LF.

* VREF COMES FROM DDC264 EVM

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0V to +10V and the output voltage range of 0V to +5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

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