ZL30136

GbE and Telecom Rate Network Interface Synchronizer

Short Form Data Sheet

July 2009

Features

- Provides synchronous clocks for network interface cards that support synchronous Ethernet (SyncE) in addition to telecom interfaces (T1/E1, DS3/E3, etc.)
- Supports the requirements of ITU-T G.8262 for Synchronous Ethernet equipment slave clocks (EEC option 1 and 2)
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz, and 155.52 MHz)
- Generates Ethernet clocks (12.5 MHz, 25 MHz, 50 MHz, 62.5 MHz, or 125 MHz)
- Programmable telecom synthesizer generates clock frequencies of any multiple of 8 kHz up to 100 MHz
- Selectable loop bandwidth of 14 Hz, 28 Hz, 890 Hz, or 0.1 Hz
- Generates several styles of output frame pulses with selectable pulse width, polarity and frequency
- Provides 3 sync inputs for output frame pulse alignment
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities

Ordering Information

ZL30136GGG	64 Pin CABGA	Trays
ZL30136GGG2	64 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Supports automatic hitless reference switching and short term holdover during loss of reference inputs
- DPLL can be configured to provide synchronous or asynchronous clock outputs
- Configurable through a serial interface (SPI or I^2C)
- Supports IEEE 1149.1 JTAG Boundary Scan

Applications

- GbE network interface cards that support synchronous Ethernet (SyncE)
- GPON ONT/ONU
- T1/E1 line cards
- DS3/E3 line cards

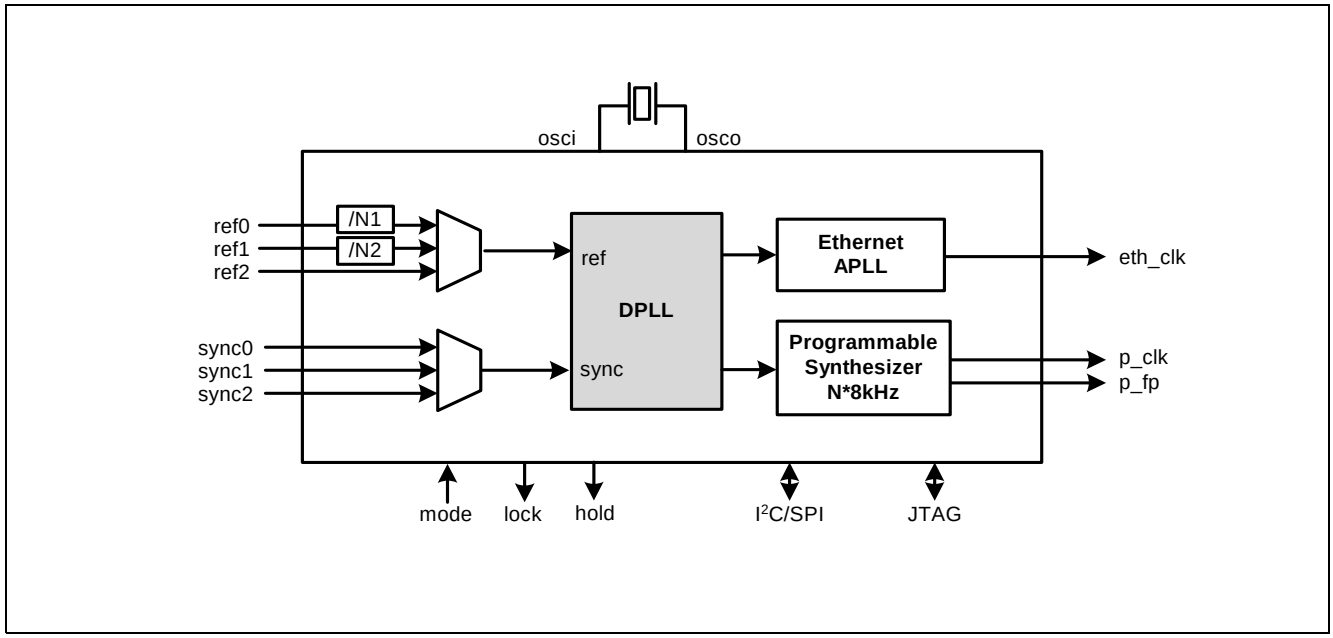


Figure 1 - Functional Block Diagram

1.0 Change Summary

Changes from September 2008 issue to July 2009 issue.

Page	Item	Change
3	p_clk maximum clock frequency	Changed max frequency of the P0 clock from 77.76 MHz to 100 MHz.

Changes from February 2008 issue to September 2008 issue.

Page	Item	Change
	Ordering Information	Corrected ordering part number.

Pin Description

Pin #	Name	I/O Type	Description
Input Reference			
B1 A3 B4	ref0 ref1 ref2	I_u	**Input References 2:0 (LVCMOS, Schmitt Trigger).** These input references are available to the DPLL for synchronizing output clocks. All three input references can lock to 2 kHz or any multiple of 8 kHz up to 77.76 MHz including 25 MHz and 50 MHz. Input ref0 and ref1 have additional configurable pre-dividers allowing input frequencies of 62.5 MHz, 125 MHz, and 155.52 MHz. These pins are internally pulled up to V_{dd}.
A1 A2 A4	sync0 sync1 sync2	I_u	**Frame Pulse Synchronization References 2:0 (LVCMOS, Schmitt Trigger).** These are optional frame pulse synchronization inputs associated with input references 0, 1 and 2. These inputs accept frame pulses in a clock format (50% duty cycle) or a basic frame pulse format with minimum pulse width of 5 ns. These pins are internally pulled up to $V_{dd.}$
Output Clocks and Frame Pulses			
D8	eth_clk	O	**Network Output Clock (LVCMOS).** This output can be configured to provide any of the Ethernet clock rates: 12.5 MHz, 25 MHz, 50 MHz, 62.5 MHz, or 125 MHz.
G8	p_clk	O	**Programmable Telecom Synthesizer - Output Clock (LVCMOS).** This output can be configured to provide telecom clock rates in multiples of 8 kHz up to 100 MHz. The default frequency for this output is 2.048 MHz.
G7	p_fp	O	**Programmable Telecom Synthesizer - Output Frame Pulse (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse. The default frequency for this frame pulse output is 8 kHz.
Control			
G5	rst_b	I	**Reset (LVCMOS, Schmitt Trigger).** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
B2	mode	I_u	**DPLL Mode Select (LVCMOS, Schmitt Trigger).** During reset, the level on this pin determines the default mode of operation for DPLL (Normal=0 or Freerun=1). After reset, the mode of operation can be controlled directly with this pin, or by accessing the dpll_modesel register (0x1F) through the serial interface. This pin is internally pulled up to Vdd.
Status			
E1	lock	O	**Lock Indicator (LVCMOS).** This is the lock indicator pin for DPLL. This output goes high when the DPLL's output is frequency and phase locked to the input reference.
H1	hold	O	**Holdover Indicator (LVCMOS).** This pin goes high when the DPLL enters the holdover mode.
Serial Interface (SPI/I^2C)			
C1	sck/scl	I/B	**Clock for Serial Interface (LVCMOS).** Serial interface clock. When i2c_en = 0, this pin acts as the sck pin for the serial interface. When i2c_en = 1, this pin acts as the scl pin (bidirectional) for the I^2C interface.

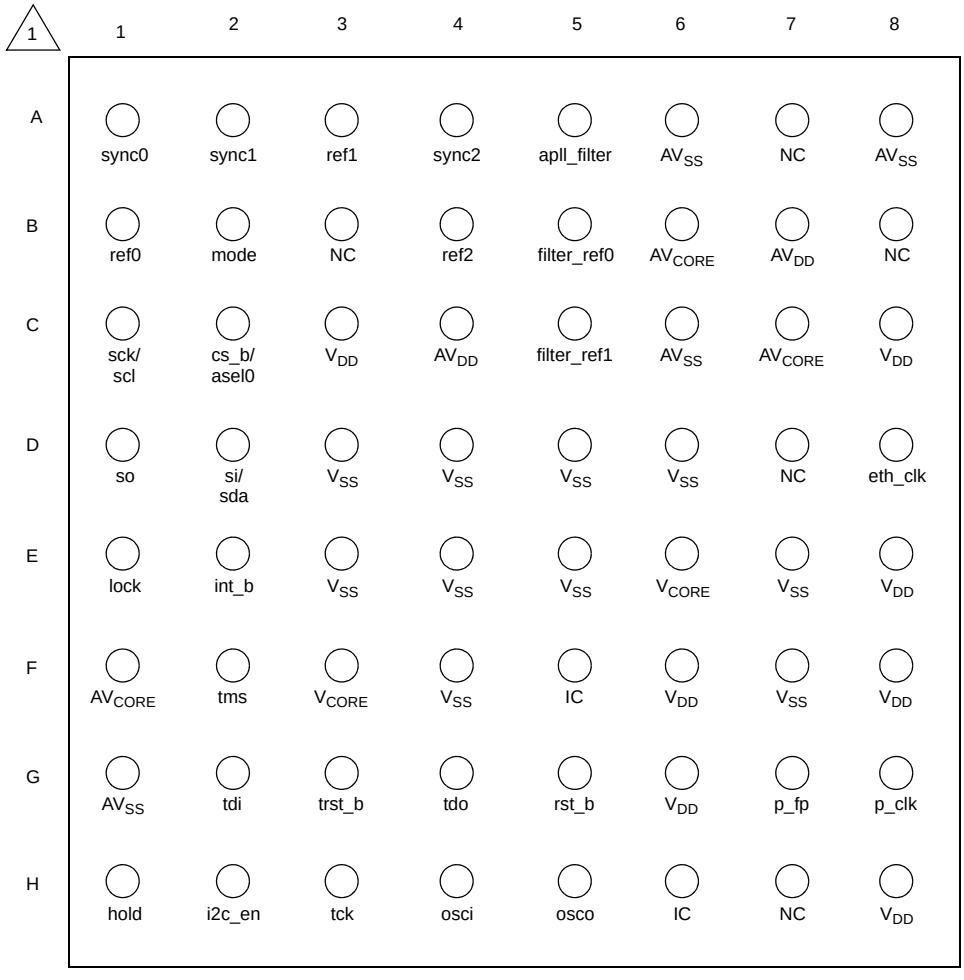
Pin #	Name	I/O Type	Description
D2	si/sda	I/B	**Serial Interface Input (LVCMOS).** Serial interface data pin. When i2c_en = 0, this pin acts as the si pin for the serial interface. When i2c_en = 1, this pin acts as the sda pin (bidirectional) for the I^2C interface.
D1	so	O	**Serial Interface Output (LVCMOS).** Serial interface data output. When i2c_en = 0, this pin acts as the so pin for the serial interface. When i2c_en = 1, this pin is unused and should be left unconnected.
C2	cs_b/asel0	I_u	**Chip Select for SPI/Address Select 0 for I^2C (LVCMOS).** When i2c_en = 0, this pin acts as the chip select pin (active low) for the serial interface. When i2c_en = 1, this pin acts as the asel0 pin for the I^2C interface.
E2	int_b	O	**Interrupt Pin (LVCMOS).** Indicates a change of device status prompting the processor to read the enabled interrupt service registers (ISR). This pin is an open drain, active low and requires an external pulled-up to Vdd.
H2	i2c_en	I_u	**I^2C Interface Enable (LVCMOS).** If set high, the I^2C interface is enabled, if set low the SPI interface is enabled. Internally pull-up to Vdd.
APLL Loop Filter			
A5	apll_filter	A	**External Analog PLL Loop Filter Terminal.**
B5	filter_ref0	A	**Analog PLL External Loop Filter Reference.**
C5	filter_ref1	A	**Analog PLL External Loop Filter Reference.**
JTAG and Test			
G4	tdo	O	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G2	tdi	I_u	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to Vdd. If this pin is not used then it should be left unconnected.
G3	trst_b	I_u	**Test Reset (LVCMOS).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to Vdd. If this pin is not used then it should be connected to GND.
H3	tck	I	**Test Clock (LVCMOS):** Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.
F2	tms	I_u	**Test Mode Select (LVCMOS).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
H4	osci	I	**Oscillator Master Clock Input (LVCMOS).** This input accepts a 20 MHz reference from a clock oscillator (XO) or crystal XTAL. The stability and accuracy of the clock at this input determines the free-run accuracy and the long term holdover stability of the output clocks.
H5	osco	O	**Oscillator Master Clock Output (LVCMOS).** This pin must be left unconnected when the osci pin is connected to a clock oscillator.

Pin #	Name	I/O Type	Description
Miscellaneous			
F5	IC		**Internal Connection.** Leave unconnected.
H6	IC		**Internal Connection.** Connect to ground.
A7 B3 B8 D7 H7	NC		**No Connection.** Leave unconnected.
Power and Ground			
C3 C8 E8 F6 F8 G6 H8	V_{DD}	P P P P P P P	**Positive Supply Voltage.** +3.3V_{DC} nominal.
E6 F3	V_{CORE}	P P	**Positive Supply Voltage.** +1.8V_{DC} nominal.
B7 C4	AV_{DD}	P P	**Positive Analog Supply Voltage.** +3.3V_{DC} nominal.
B6 C7 F1	AV_{CORE}	P P P	**Positive Analog Supply Voltage.** +1.8V_{DC} nominal.
D3 D4 D5 D6 E3 E4 E5 E7 F4 F7	V_{SS}	G G G G	**Ground.** 0 Volts.
A6 A8 C6 G1	AV_{SS}	G G G G	**Analog Ground.** 0 Volts.

I - Input
I_d - Input, Internally pulled down
I_u - Input, Internally pulled up
O - Output
A - Analog
P - Power
G - Ground

2.0 Pin Diagram

TOP VIEW



1 - A1 corner is identified by metallized markings.

3.0 High Level Overview

The ZL30136 GbE and Telecom Rate Network Interface Synchronizer is a highly integrated device that provides timing for network interface cards. The DPLL is capable of locking to one of three input references and provides standard Ethernet clock rates for synchronizing Ethernet PHYs, and a highly programmable clock and frame pulse for telecom interfaces such as T1/E1, DS3/E3, etc...

This device is ideally suited for systems with network interface cards that are synchronized to a centralized telecom backplane. The ZL30136 synchronizes to backplane clocks and generates a synchronized and jitter attenuated Ethernet clock and a PDH clock. A typical application is shown in Figure 2. In this application, the ZL30136 translates a 19.44 MHz clock from the telecom backplane to an Ethernet clock rate for the GbE PHY and filters the jitter to ensure compliance with related clock standards. A programmable synthesizer provides PDH clocks with multiples of 8 kHz for generating PDH interface clocks. The ZL30136 allows easy integration of Ethernet line rates with today's telecom backplanes.

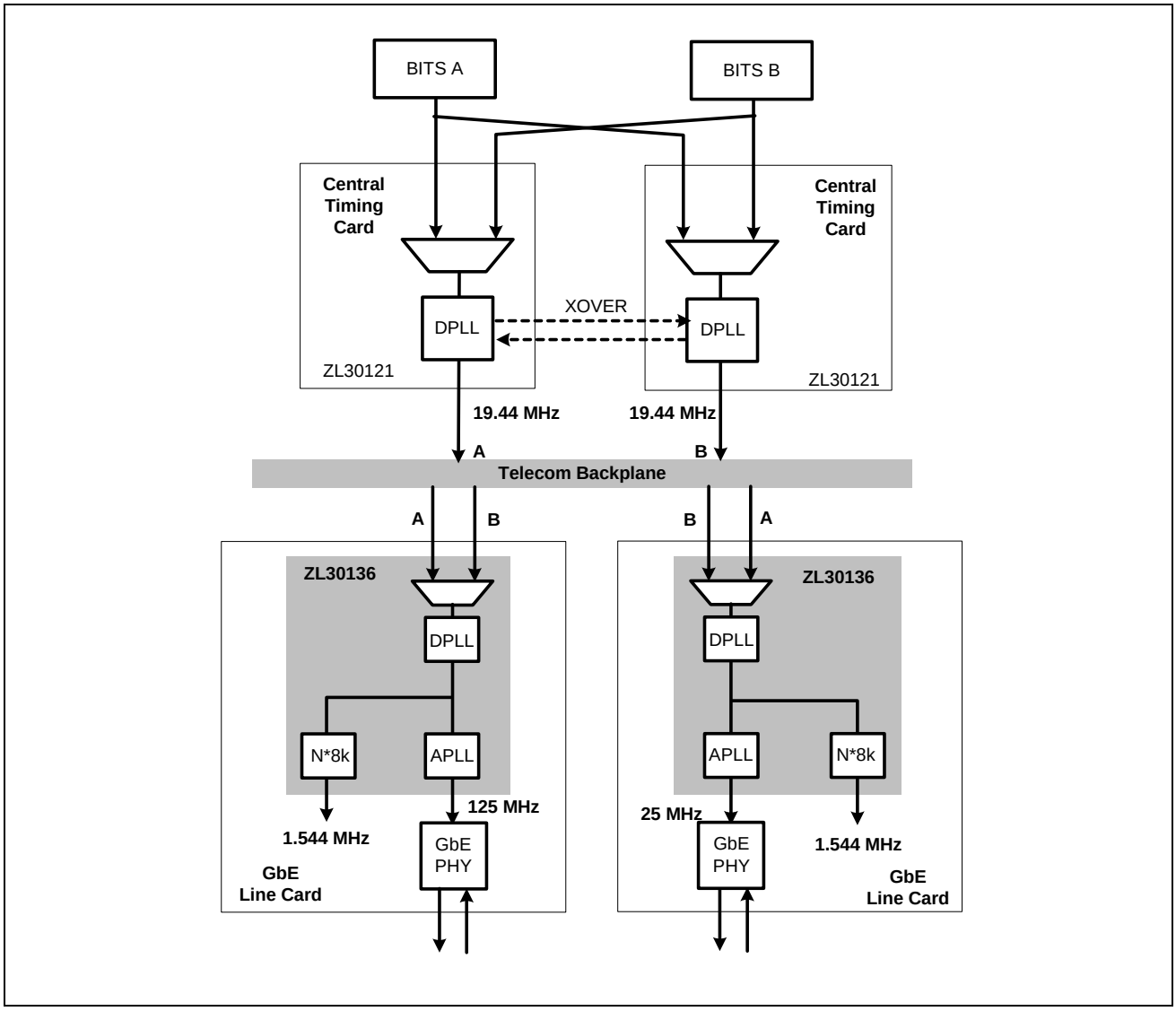
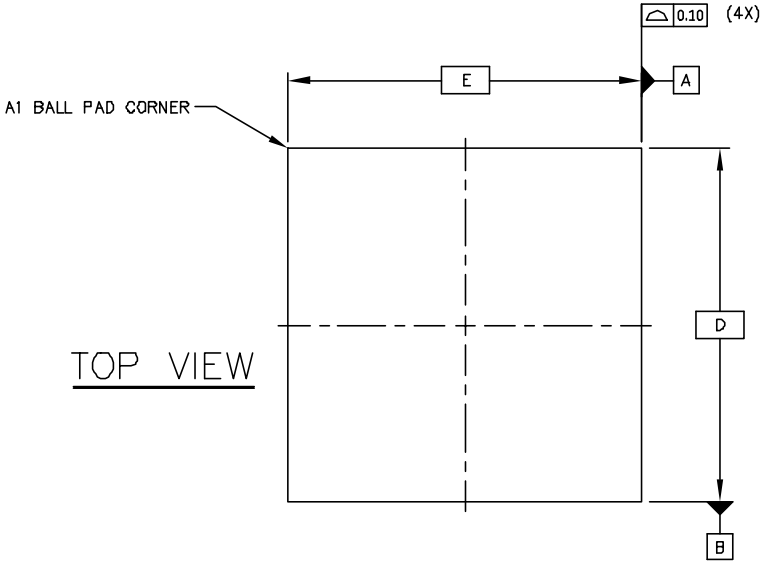
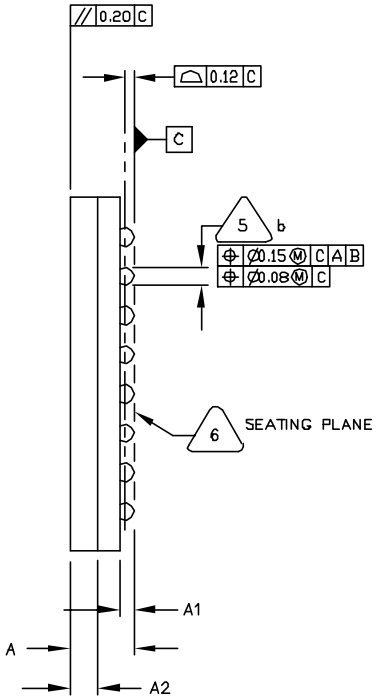


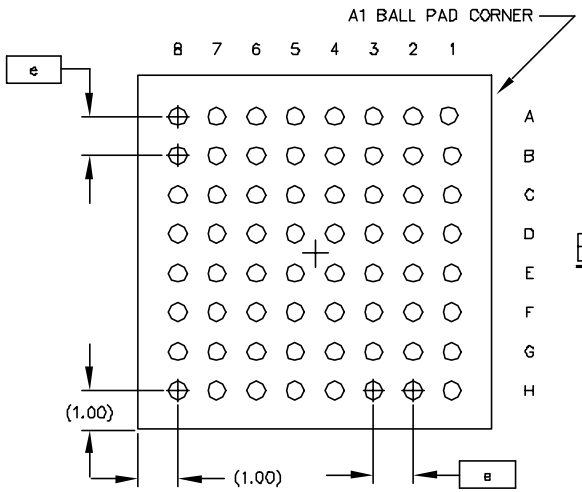
Figure 2 - Typical Application of the ZL30136



TOP VIEW



SIDE VIEW



BOTTOM VIEW

64 SOLDER BALLS

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b		0.46 Typ.	
D		9.00 REF.	
E		9.00 Ref.	
e		1.0 Ref	
n		64	

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1			
ACN	CDCA			
DATE	15April05			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

N/A

Package Code GG

Package Outline for 64ball 9x9mm, 1.0 mm Pitch, 4 layer, CABGA

111039

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