

4A Half-Bridge Driver

Features

- Floating High Side Driver with boot-strap Power supply along with a Low Side Driver.
- Fully operational to 650V
- $\pm 50\text{V/ns}$ dV/dt immunity
- Gate drive power supply range: 10 - 35V
- Undervoltage lockout for both output drivers
- Separate Logic power supply range: 3.3V to V_{CL}
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up protected over entire operating range
- High peak output current: 4A
- Matched propagation delay for both outputs
- Low output impedance
- Low power supply current
- Immune to negative voltage transients

Warning: The IX4R11 is ESD sensitive.

General Description

The IX4R11 Bridge Driver for N-channel MOSFETs and IGBTs with a high side and low side output, whose input signals reference the low side. The High Side driver can control a MOSFET or IGBT connected to a positive buss voltage up to 650V. The logic input stages are compatible with TTL or CMOS, have built-in hysteresis and are fully immune to latch up over the entire operating range. The IX4R11 can withstand dV/dt on the output side up to $\pm 50\text{V/ns}$.

The IX4R11 comes in either the 16-PIN SOIC package (IX4R11S3) or the 14-PIN DIP through-hole package (IX4R11P7)

Applications

- Driving MOSFETs and IGBTs in half-bridge circuits
- High voltage, high side and low side drivers
- Motor Controls
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Class D Switching Amplifiers

Figure 1. Typical Circuit Connection

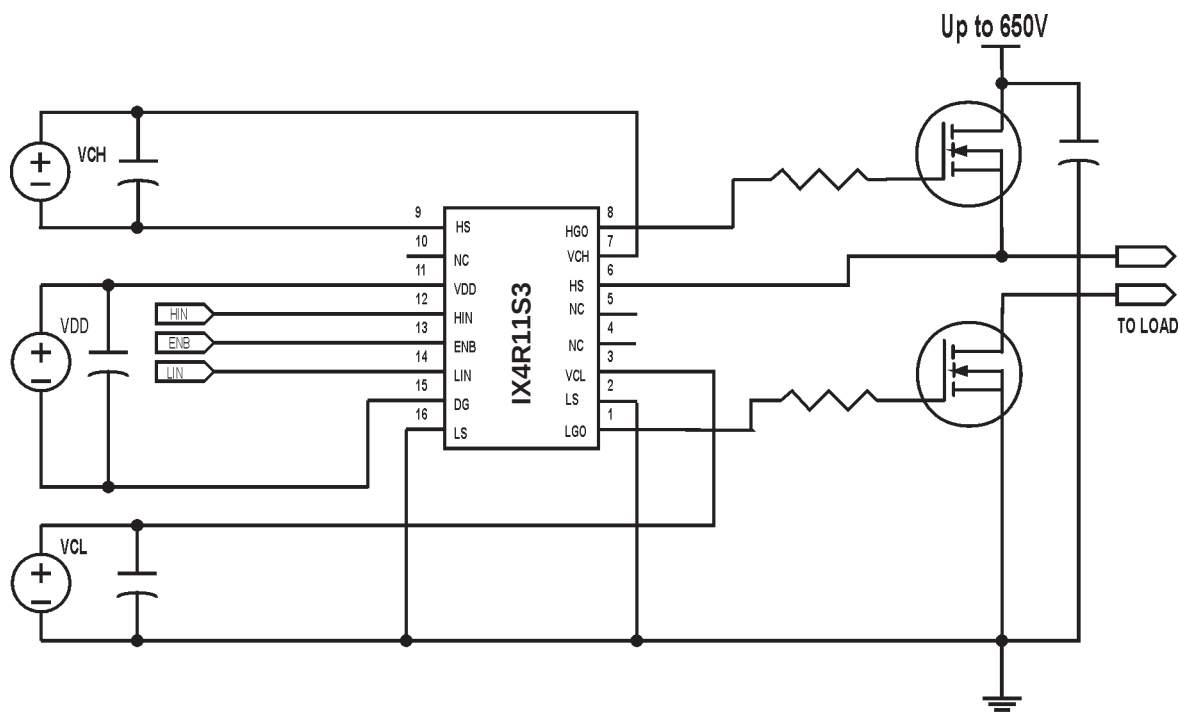
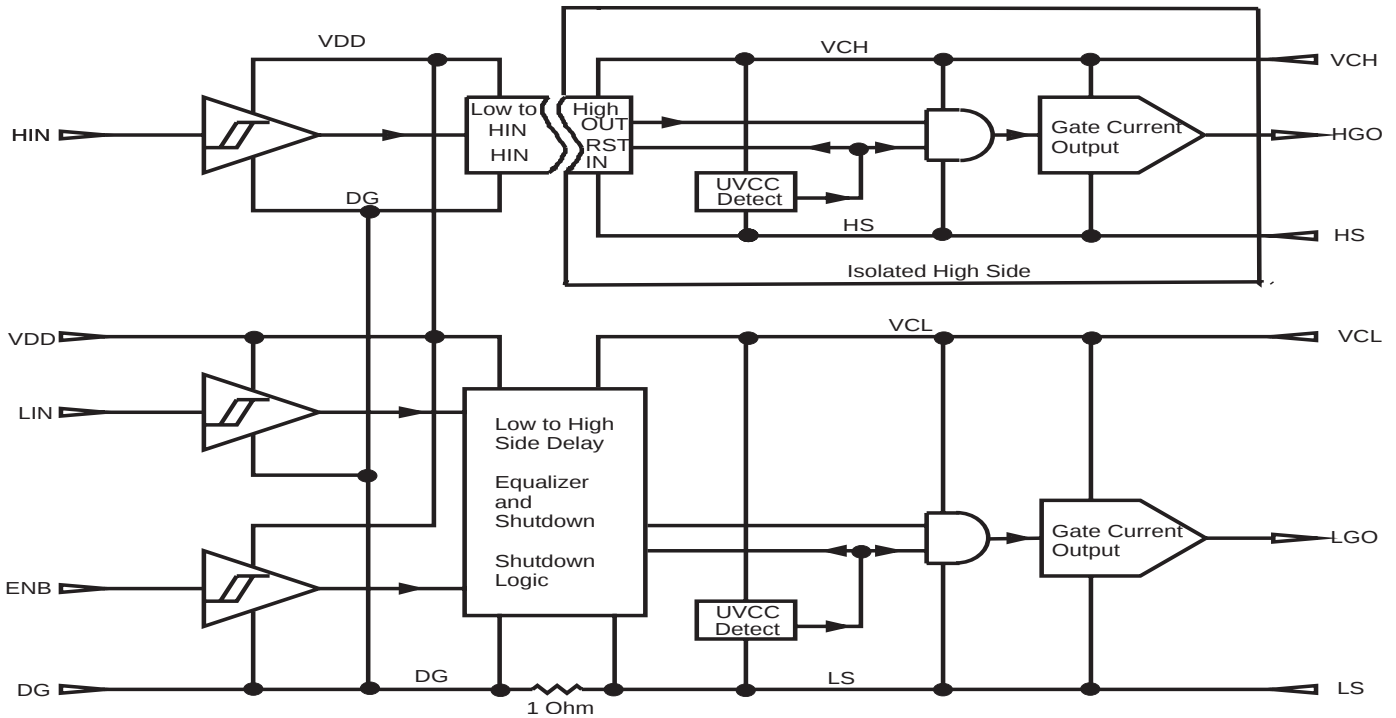


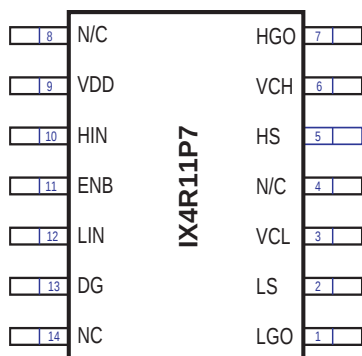
Figure 2 - IX4R11 Functional Block Diagram



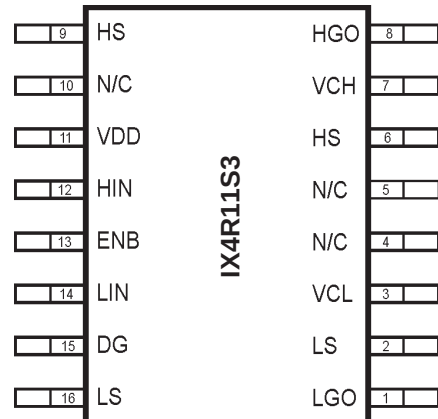
Pin Description And Configuration

SYMBOL	FUNCTION	DESCRIPTION
VDD	Logic Supply	Positive power supply for the chip CMOS functions
HIN	HS Input	High side Input signal, TTL or CMOS compatible; HGO in phase
LIN	LS Input	Low side Input signal, TTL or CMOS compatible; LGO in phase
ENB	Enable	Chip enable. When driven high, both outputs go low.
DG	Ground	Logic Reference Ground
VCH	Supply Voltage	High Side Power Supply
HGO	Output	High side driver output
HS	Return	High side voltage return pin
VCL	Supply Voltage	Low side power supply. This power supply provides power for both outputs. Voltage range is from 4.5 to 25V.
LGO	Output	Low side driver output
LS	Ground	Low side return

14-PIN DIP



16-PIN SOIC



Absolute Maximum Ratings

Symbol	Definition	Min	Max	Units
V_{CH}	High side floating supply voltage	-25	650	V
V_{HS}	High side floating supply offset voltage	$V_{CH}-200$	$V_{CH}+3$	V
V_{HGO}	High side floating output voltage	$V_{HS}-3$	$V_{CH}+3$	V
V_{CL}	Low side fixed supply voltage	-0.3	35	V
V_{LGO}	Low side output voltage	-0.3	$V_{CL}+3$	V
V_{DD}	Logic supply voltage	-0.3	$V_{DG}+35$	V
V_{DG}	Logic supply offset voltage	$V_{LS}-3.8$	$V_{LS}+3.8$	V
V_{IN}	Logic input voltage(HIN & LIN)	$V_{SS}-3$	$V_{DD}+3$	V
dV_S/dt	Allowable offset supply voltage transient		50	V/ns
P_D	Package power dissipation@ $T_A \leq 25C$		1.25	W
P_D	Package power dissipation@ $T_C \leq 25C$		2.5	W
R_{THJA}	Thermal resistance, junction-to-ambient		100	K/W
R_{THJC}	Thermal resistance, junction-to-case		50	K/W
T_J	Junction Temperature		150	°C
T_S	Storage temperature	-55	150	°C
T_L	Lead temperature (soldering, 10 s)		300	°C

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{CH}	High side floating supply absolute voltage	$V_{HS}+10$	$V_{HS}+20$	V
V_{HS}	High side floating supply offset voltage	-20	650	V
V_{HGO}	High side floating output voltage	V_{HS}	$V_{CH}+20$	V
V_{CL}	Low side fixed supply voltage	10	20	V
V_{LGO}	Low side output voltage	0	V_{CC}	V
V_{DD}	Logic supply voltage	$V_{DG}+3$	$V_{DG}+20$	V
V_{DG}	Logic supply voffset voltage	$V_{LS}-1$	$V_{LS}+1$	V
V_{IN}	Logic input voltage(HIN, LIN, ENbar)	V_{DG}	V_{DD}	V
T_A	Ambient Temperature	-40	125	°C

Ordering Information

Part Number	Package Type
IX4R11P7	14-PIN DIP
IX4R11S3	16-PIN SOIC

Dynamic Electrical Characteristics

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
t_{on}	Turn-on propagation delay	$V_{HS} = 0V, C_{load} = 2nF$		120		ns
t_{off}	Turn-off propagation delay	$V_{HS} = 600V, C_{load} = 2nF$		87		ns
t_{en}	Device enable delay			202		ns
t_r	Turn-on rise time	$C_{load} = 2nF$		23		ns
t_f	Turn-off fall time	$C_{load} = 2nF$		22		ns
t_{dm}	Delay matching, HS & LS turn-on/off	$C_{load} = 2nF$		10	20	ns

Static Electrical Characteristics

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
V_{INH}	Logic "1" input voltage	$V_{DD} = V_{CL} = 15V$	7.0			V
V_{INL}	Logic "0" input voltage	$V_{DD} = V_{CC} = 15V$			6	V
V_{HLGO} / V_{HHGO}	High level output voltage, $V_{CH} - V_{HGO}$ or $V_{CL} - V_{LGO}$	$I_o = 0A$		0.28		V
V_{LLGO} / V_{LHGO}	High level output voltage, V_{HGO} or V_{LGO}	$I_o = 0A$		.23		V
I_{HL}	HS to LS bias current.	$V_{HS} = V_{CH} = 600V$		.17		mA
I_{QHS}	Quiescent V_{CH} supply current	$V_{IN} = 0V$ or V_{DD}		.77		mA
I_{QLS}	Quiescent V_{CL} supply current	$V_{IN} = 0V$ or V_{DD}		.79		mA
I_{QDD}	Quiescent V_{DD} supply current	$V_{IN} = 0V$ or V_{DD}		36		uA
I_{IN}^+	Logic "1" input bias current	$V_{IN} = V_{DD}$		2		uA
I_{IN}^-	Logic "0" input voltage	$V_{IN} = 0V$		1		uA
V_{CHUV}^+	V_{CH} supply undervoltage positive going threshold.			8.3		V
V_{CHUV}^-	V_{CH} supply undervoltage negative going threshold.			8.2		V
V_{CLUV}^+	V_{CL} supply undervoltage positive going threshold			8.1		V
V_{CLUV}^-	V_{CL} supply undervoltage negative going threshold.			8.0		V
I_{GO}^+	HS or LS Output low short circuit current; $V_{GO} = 15V, V_{IN} = 0V, PW < 10\mu s$				+4	A
I_{GO}^-	HS or LS Output low short circuit current; $V_{GO} = 15V, V_{IN} = 0V, PW < 10\mu s$				-4	A

Timing Waveform Definitions

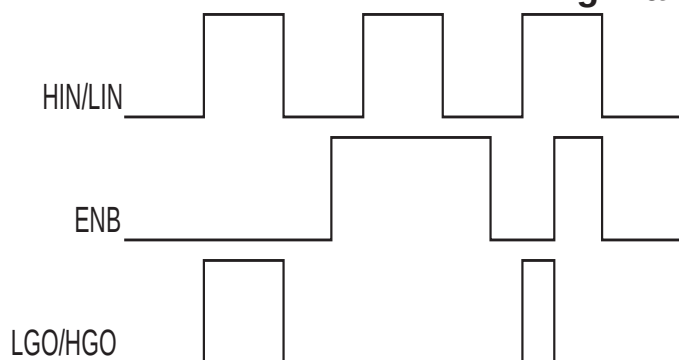


Figure 3. INPUT/OUTPUT Timing Diagram

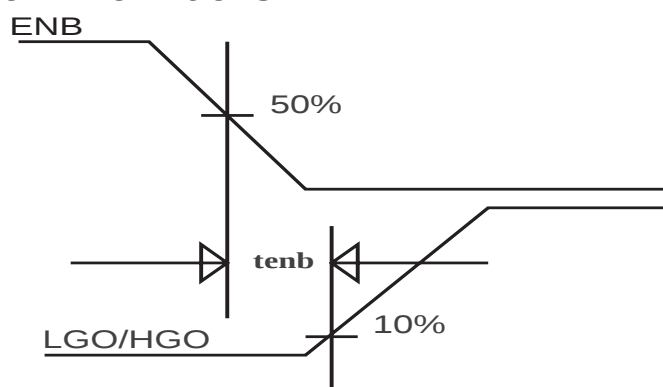
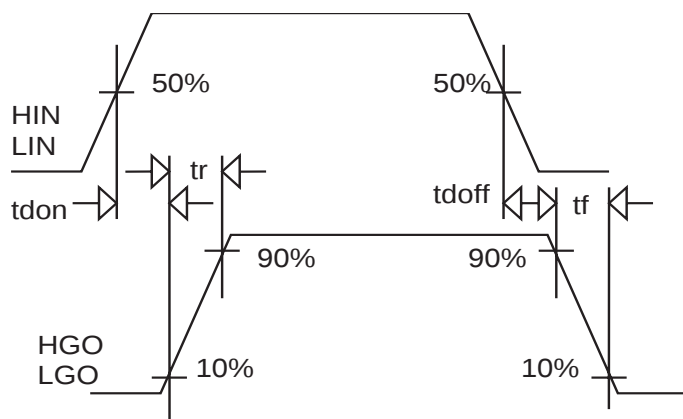


Figure 4. ENABLE Waveform Definitions

Figure 5. Definitions of Switching Time Waforms



The diagram illustrates the timing relationship between the Input Signal and the Outgoing Signal. The Input Signal is a trapezoidal pulse with 50% rise and fall times. The Outgoing Signal is a trapezoidal pulse with 10% rise and 90% fall times. The diagram includes labels for LGO (Logic Output), HGO (High Output), and tdm (Time Delay Measurement) points.

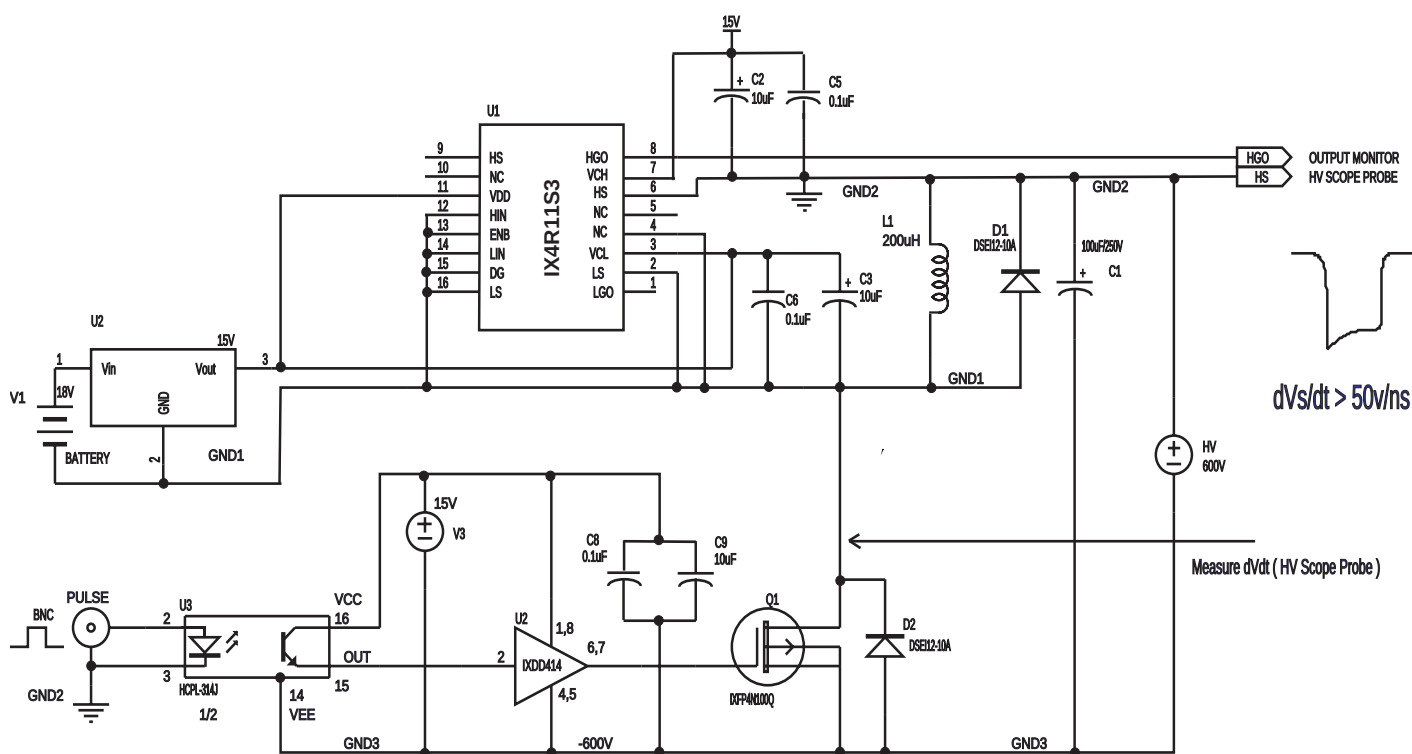
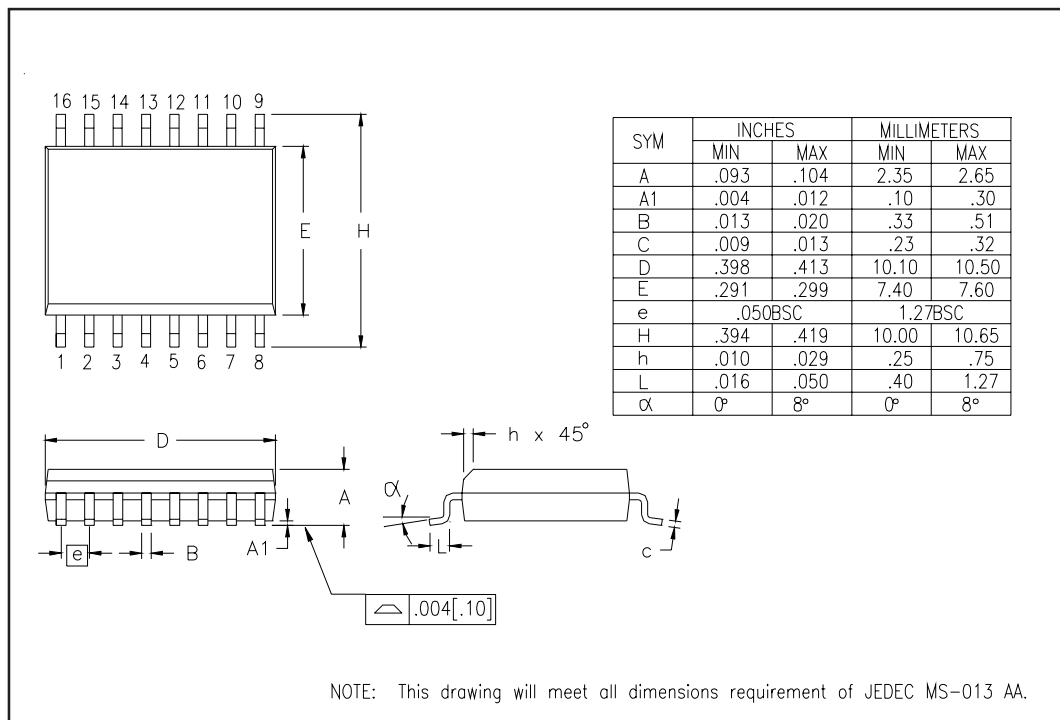


Figure 7. Test circuit for allowable offset supply voltage transient.

IX4R11S3 Package Outline



IX4R11P7 Package Outline

