

## Evaluating the **ADA4350**, a FET Input Analog Front End With ADC Driver Offered in a 28-Lead 9.8 mm × 6.4 mm TSSOP

### FEATURES

- Enables quick breadboarding/prototyping
- User defined circuit configuration
- Edge mounted SMA connector provisions
- Easy connection to test equipment and other circuits
- Guard ring to minimize leakage currents

### GENERAL DESCRIPTION

The **EVAL-ADA4350RUZ-P** evaluation board is designed to help users evaluate the **ADA4350** offered in a 28-lead, 9.8 mm × 6.4 mm thin shrink small outline package (TSSOP). The evaluation board is a populated board that enables users to quickly prototype the best configuration of the analog front end for their systems. Figure 1 shows the component side of the bare evaluation board, and Figure 2 shows the solder side of the bare evaluation board.

The evaluation board is a 6-layer printed circuit board (PCB) designed to minimize leakage currents with its guard ring features. It accepts SMA edge mounted connectors on the inputs and outputs for efficient connection to test equipment or other circuitry.

The evaluation board components are primarily SMT 0603 case size, with the exception of the electrolytic bypass capacitors (C9, C10, and C13), which are 1206 case size.

Figure 10 shows the **ADA4350** configured as a transimpedance amplifier with multiple gains when a dual supply is used.

Figure 3 and Figure 4 show the signal gain/noise gain of the board when configured as Figure 10. Figure 7 to Figure 9 show the guard ring details. Figure 11 shows the assembly drawing and Figure 12 shows the 6-layer stackup along with the dimensions for each layer. The bill of materials is listed in Table 2.

### DIGITAL PICTURES OF THE EVALUATION BOARD

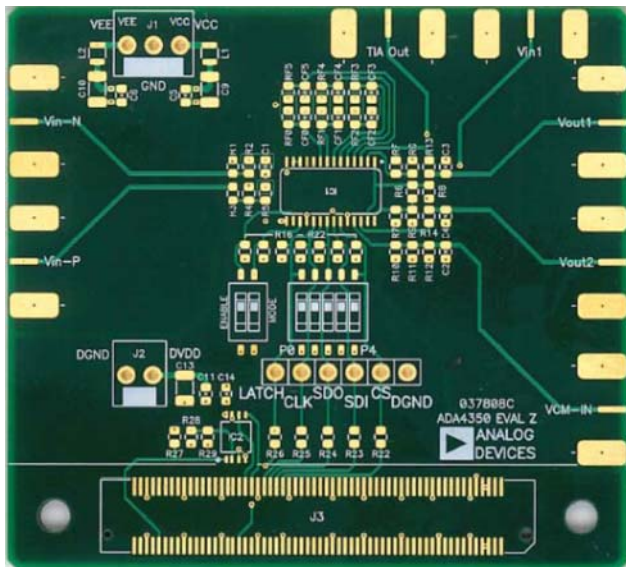


Figure 1. **ADA4350** Evaluation Board Component Side

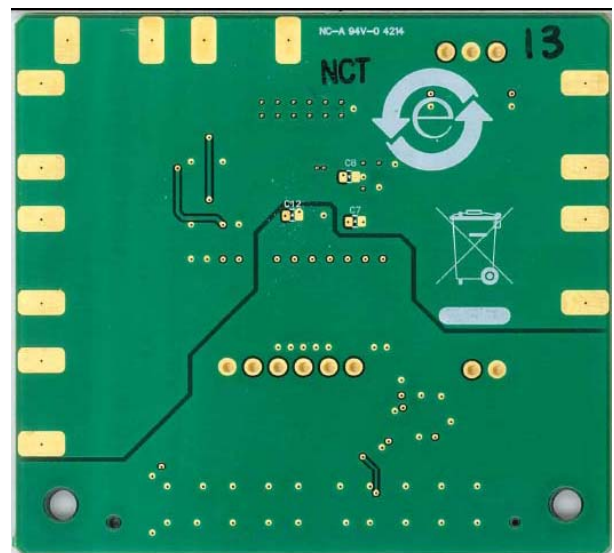


Figure 2. **ADA4350** Evaluation Board Solder Side

TABLE OF CONTENTS

|                                                |   |                                               |   |
|------------------------------------------------|---|-----------------------------------------------|---|
| Features .....                                 | 1 | Frequency Response .....                      | 3 |
| General Description .....                      | 1 | Evaluation Board Control .....                | 4 |
| Digital Pictures of the Evaluation Board ..... | 1 | Evaluation Board Electrostatic Guarding ..... | 5 |
| Revision History .....                         | 2 | Evaluation Board Schematic and Artwork.....   | 6 |
| Evaluation Board Hardware.....                 | 3 | Ordering Information.....                     | 8 |
| Power Supplies .....                           | 3 | Bill of Materials.....                        | 8 |
| Guard Ring Features .....                      | 3 |                                               |   |

REVISION HISTORY

5/15—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

### POWER SUPPLIES

The ADA4350 has two supplies. The analog supply is used to power up all the analog circuitries while the digital supply is used to power up all the digital controls. The two supplies have separate grounds inside the chip. Table 1 shows the supply range of the analog and digital supply, the voltages to be applied to the supply pins in different configurations, and their limitations.

### GUARD RING FEATURES

The ADA4350 evaluation board employs a two layer electrostatic guarding to minimize leakage currents from entering the TIA node.

Five mil wide guard rings encircle the inverting and noninverting input components on the top copper layer (see Figure 7 and Figure 9). The guard rings connect to the internal GND copper layer with 5 mil dia vias. Each component pad that connects to the TIA inverting and noninverting inputs is connected to an internal copper trace with 5 mil dia vias (see Figure 8 and Figure 9).

This electrostatic guarding scheme provides isolation from leakage currents but adds a 35 pF parasitic capacitance to the TIA inverting node.

### FREQUENCY RESPONSE

The ADA4350 evaluation board is configured for a simulated photodiode input. The photodiode capacitance is represented by C1, a 51 pF capacitor. The photodiode current is simulated by the input voltage  $V_{in-N}$  and R2, a 100 kΩ resistor.  $I_{PHOTODIODE} = (V_{in-N})/100\text{ k}\Omega$ .

The total capacitance (91 pF) seen by the TIA is the sum of the ADA4350 input capacitances (2 pF + 3 pF), the photodiode capacitance (51 pF), and the parasitic capacitance of the electrostatic guarding (35 pF).

The five feedback resistor values are approximately ½ decade apart. The five compensation capacitors are selected for maximum bandwidth and maximum gain flatness.

The normalized transimpedance and noise gain are shown in Figure 3 and Figure 4 with compensation capacitors installed and not installed.

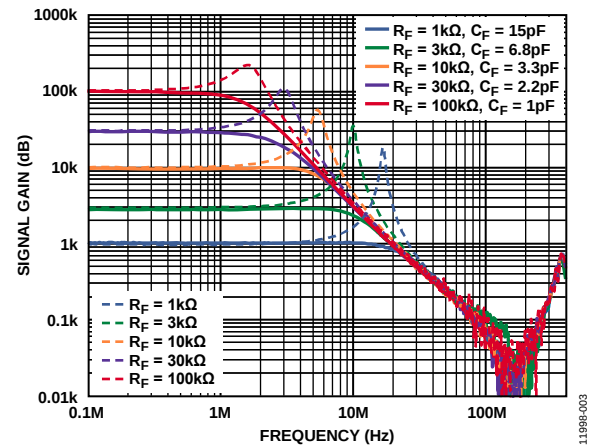


Figure 3. ADA4350 Signal Gain and Noise Gain Frequency Response

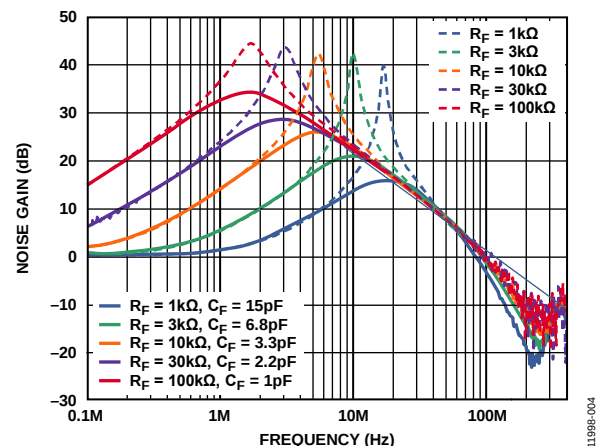


Figure 4. ADA4350 Signal Gain and Noise Gain Frequency Response

Table 1. Powering Up the Analog and Digital Supplies

| Supply  | Supply Range (V) | Dual Supplies ( $\pm V_S$ ) |     |        | Single Supplies ( $+V_S$ ) |     |     |
|---------|------------------|-----------------------------|-----|--------|----------------------------|-----|-----|
|         |                  | VCC                         | GND | VEE    | VCC                        | GND | VEE |
| Analog  | 3.3 to 12        | $+V_S$                      | 0   | $-V_S$ | $+V_S$                     | 0   | 0   |
| Digital | 3.3 to 5.5       | VCC to DGND                 |     |        | VCC to DGND                |     |     |
|         |                  | $\geq 3\text{ V}$           |     |        | $\geq 3\text{ V}$          |     |     |

## EVALUATION BOARD CONTROL

This user guide focuses on setting up the evaluation board. For logic tables of the different control modes and for an in depth analysis of the circuit, refer to the [ADA4350](#) data sheet.

### Manual Mode

The evaluation board is configured for manual gain selection using the DIP switches. The DIP switch on position represents Logic 0. To operate manually, set the enable switch to Logic 1 (off position), and set the MODE switch to Logic 1 (off position).

To select one gain, set all gain select switches, P0 to P4, to Logic 0 (on position) and select a gain by setting the corresponding gain select switch to Logic 1 (off position).

Note that only five feedback paths (FB0 to FB4) can be accessed in the manual mode and that selecting more than one gain connects all the selected feedback resistors in parallel.

### SPI Control (Parallel Mode)

The parallel mode works very similar to the manual mode except that five digital control lines (P0 to P4) are used instead of the manual switches. Set the enable switch to Logic 1 (off position), and set the MODE switch to Logic 1 (off position). Set the DIP switches (P0 to P4) to Logic 1 (off position), and connect the logic output of an external microcontroller or FPGA to the plated holes next to the P0 to P4 switches. A Logic 1 on each digital line selects the corresponding gain. Applying a Logic 1 to more than one line at a time connects all the selected gains in parallel.

### SPI Control (Serial Mode)

Set the MODE switch and LATCH switch to Logic 0 (on position), and the ENABLE switch to Logic 1 (off position). Set all other gain select switches (P1 to P4) to Logic 1 (off position), and perform the following steps:

1. Plug the Analog Devices, Inc., SDP-S controller board onto the 120-pin connector on the [ADA4350](#) evaluation board. The [SDP-S](#) control board can be purchased from Analog Devices.  
The user can also use an individual SPI interface through the 5-pin SPI connector on the evaluation board.
2. Download the LabVIEW® control panel from <http://www.analog.com/ada4350-demoinstaller>. Unzip the file, click **setup.exe**, and follow the installation prompts. If the installation is successful, the **ADA4350 Evaluation** icon appears under **Start > Programs > Analog Devices** (see Figure 5).

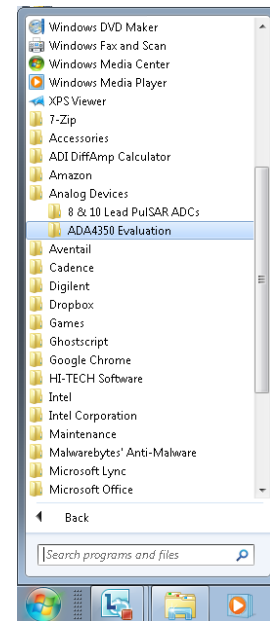


Figure 5. Location of the LabVIEW Control Panel Program

3. Open the LabVIEW control panel (see Figure 6). The control panel allows the user to open and close individual switches in the switch matrix of the [ADA4350](#). For example, to select the FB0 feedback path, click the S0 and S6 switches, then click the **Write New Configuration** button.

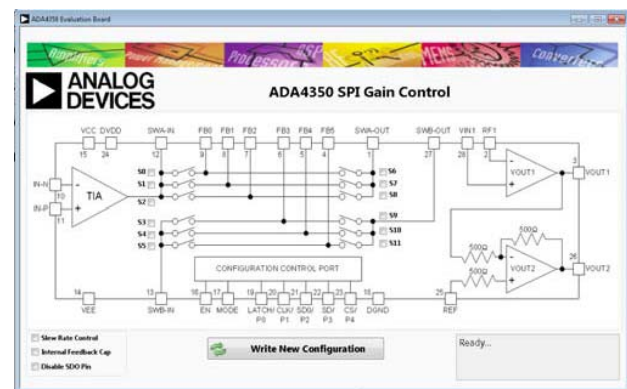


Figure 6. Labview Control Panel

### Switches

The gain select switches (S0 to S5) have around 350  $\Omega$  series internal resistance that appears as a resistance in series with the TIA output, while S6 to S11 has around 150  $\Omega$  switch resistances.

**EVALUATION BOARD ELECTROSTATIC GUARDING**

The guard ring is represented by the red enclosed area around the inputs. The evaluation board uses the guard ring to minimize leakage currents entering the inputs causing offsets.

Note that the guard ring is employed all the way from the top copper layer through the inner layers and into the ground layer.

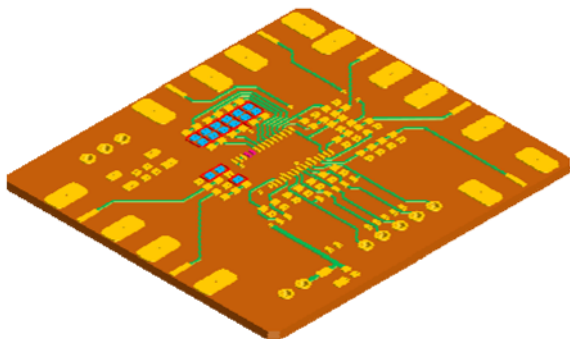


Figure 7. Top Layer Guard Ring Drawing

11998-007

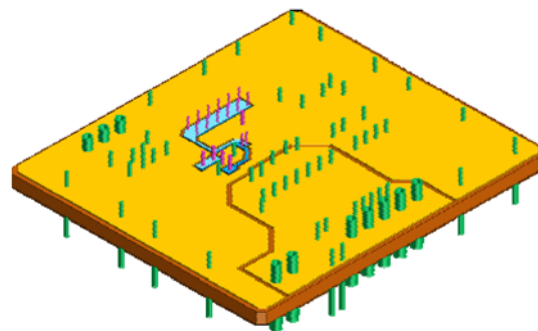


Figure 8. Ground Layer Guard Ring Drawing

11998-008

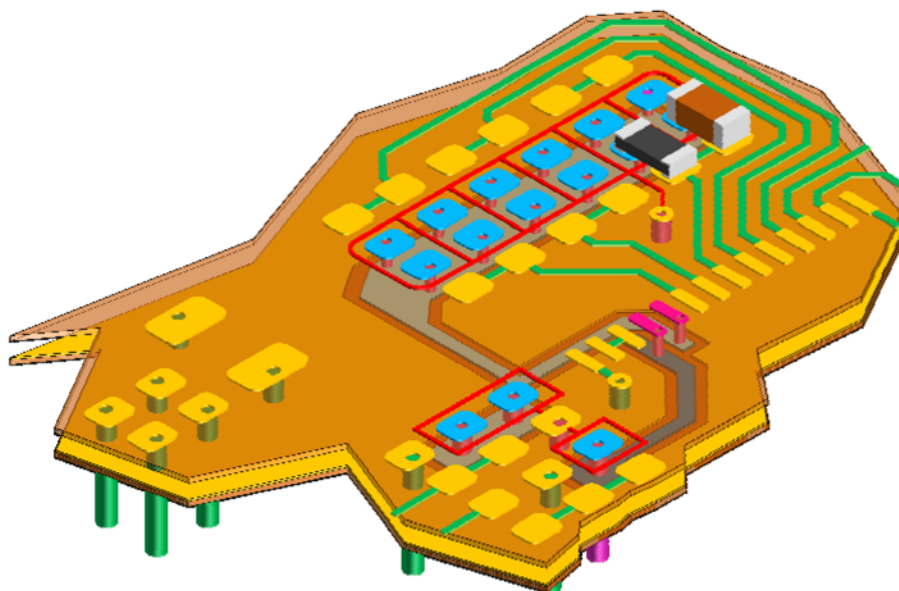


Figure 9. Guard Ring Details

11998-009

## EVALUATION BOARD SCHEMATIC AND ARTWORK

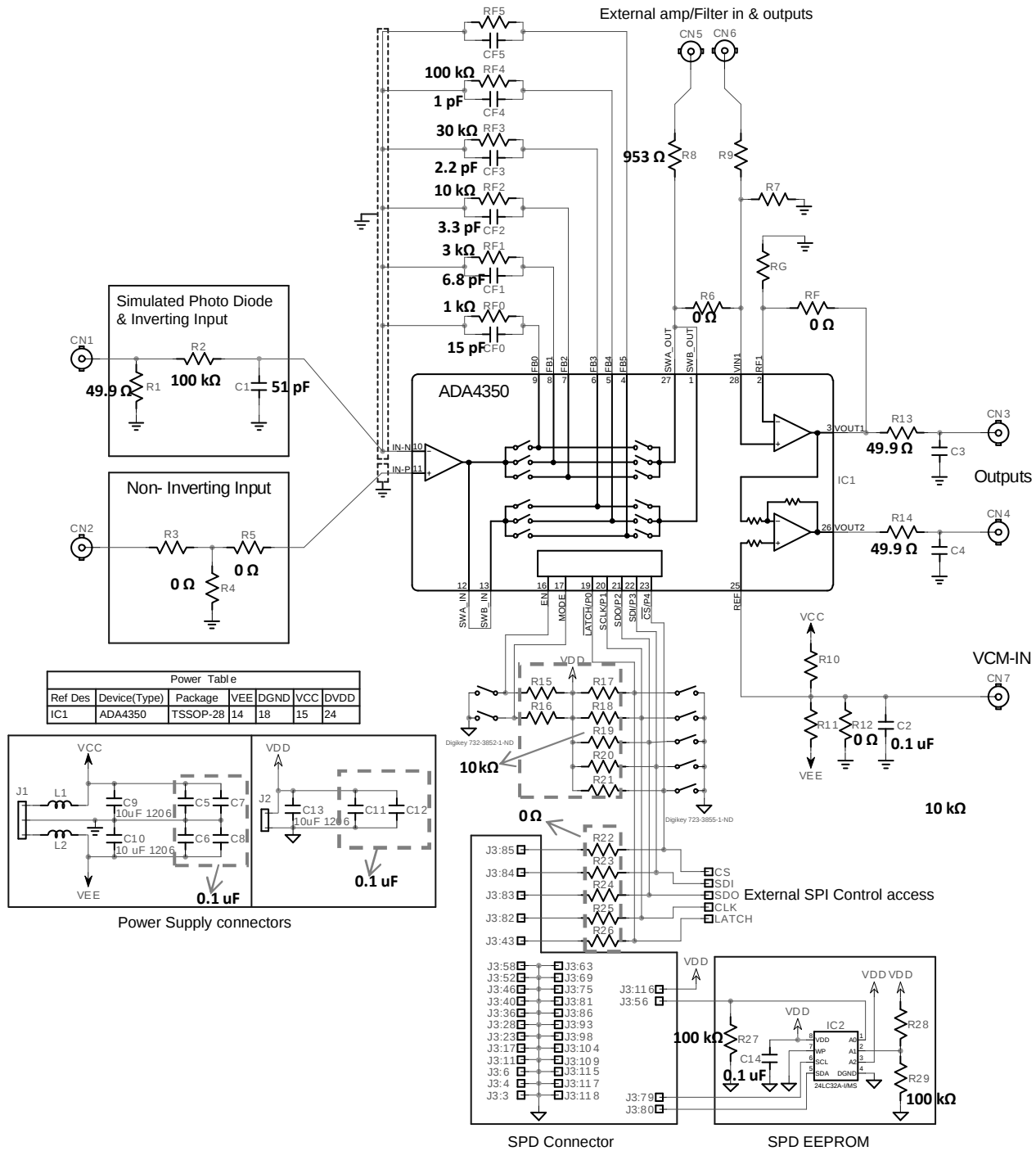


Figure 10. Schematic

11998-010

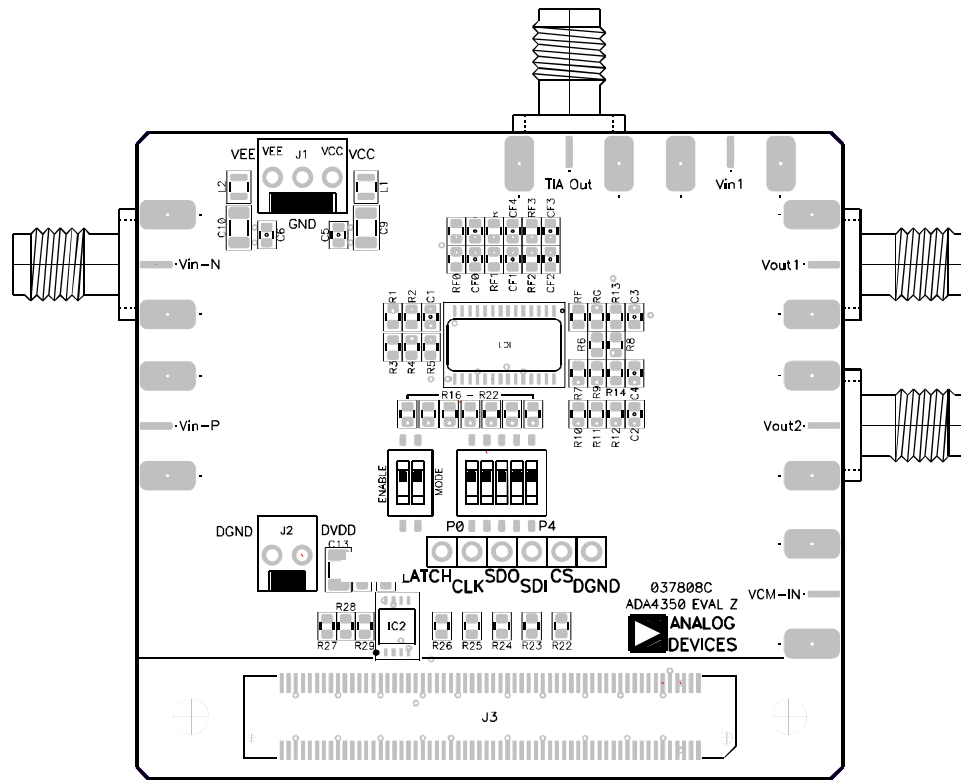


Figure 11. Component Side Assembly Drawing

# 6 LAYER STACKUP

|                                                            |  |                              |                     |
|------------------------------------------------------------|--|------------------------------|---------------------|
| NOMINAL FINISHED<br>BOARD THICKNESS<br>0.063" $\pm$ 0.007" |  | PRIMARY SILK SCREEN (.TSK)   |                     |
|                                                            |  | PRIMARY SOLDER MASK (.TMK)   |                     |
|                                                            |  | 50 ohms PRIMARY SIDE (.TOP)  | (LAYER 1)           |
|                                                            |  | GND PLANE (.GND)             | (LAYER 2)           |
|                                                            |  | SPACER                       | Adjust as necessary |
|                                                            |  | 1080 VCC PLANE (.VCC)        | (LAYER 3)           |
|                                                            |  | 1080 GND PLANE (.GND1)       | (LAYER 4)           |
|                                                            |  | 1080 VEE PLANE (.VEE)        | (LAYER 5)           |
|                                                            |  | SECONDARY SIDE (.BOT)        | (LAYER 6)           |
|                                                            |  | SECONDARY SOLDER MASK (.BMK) |                     |
|                                                            |  | SECONDARY SILK SCREEN (.BSK) |                     |

CHARACTERISTIC IMPEDANCE = 50 ohms  
 ARTWORK LINE WIDTH FOR  
 IMPEDANCE CONTROLLED LINES = 15 mils  
 Adjust impedance controlled lines down for best results.

Figure 12. Layer Stackup

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 2.

| Qty | Reference Designator                              | Description                                                      | Package              |
|-----|---------------------------------------------------|------------------------------------------------------------------|----------------------|
| 1   | None                                              | Analog supply connector                                          | 3-pin 100 mil header |
| 1   | None                                              | Digital supply connector                                         | 2-pin 100 mil header |
| 1   | None                                              | 2-pin mode selector                                              | 2-pin dip switch     |
| 1   | None                                              | 5-pin gain selector                                              | 5-pin dip switch     |
| 3   | C9, C10, C13                                      | 10 $\mu$ F capacitor                                             | 1206                 |
| 6   | C5 to C8, C11, C12                                | 0.1 $\mu$ F capacitor                                            | 0603                 |
| 10  | CF0 to CF5, C1 to C4                              | Capacitor, user defined                                          | 0603                 |
| 1   | <a href="#">ADA4350</a>                           | See the <a href="#">ADA4350</a> data sheet packaging information | 28-lead TSSOP        |
| 7   | Vin_P, Vin_N, VCM-IN, Vin1, Vout1, Vout2, TIA Out | SMA/SMT                                                          | SMA/SMT              |
| 29  | R1 to R21, RF0 to RF5, RF, RG                     | Resistor, user defined                                           | R0603                |
| 1   | SDP connector                                     | Standard 120-pin SDP connector                                   |                      |
| 1   | Small SDP connector                               | 5-pin SPI header                                                 |                      |
| 1   | 24LC32AF                                          | SDP EEPROM                                                       | MSOP                 |



#### ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

#### Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.