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Evaluating the ADA4350, a FET Input Analog Front End With ADC Driver Offered in a 28-Lead 9.8 mm × 6.4 mm TSSOP

FEATURES

Enables quick breadboarding/prototyping
User defined circuit configuration
Edge mounted SMA connector provisions
Easy connection to test equipment and other circuits
Guard ring to minimize leakage currents

GENERAL DESCRIPTION

The EVAL-ADA4350RUZ-P evaluation board is designed to help users evaluate the ADA4350 offered in a 28-lead, 9.8 mm × 6.4 mm thin shrink small outline package (TSSOP). The evaluation board is a populated board that enables users to quickly prototype the best configuration of the analog front end for their systems. Figure 1 shows the component side of the bare evaluation board, and Figure 2 shows the solder side of the bare evaluation board.

The evaluation board is a 6-layer printed circuit board (PCB) designed to minimize leakage currents with its guard ring features. It accepts SMA edge mounted connectors on the inputs and outputs for efficient connection to test equipment or other circuitry.

The evaluation board components are primarily SMT 0603 case size, with the exception of the electrolytic bypass capacitors (C9, C10, and C13), which are 1206 case size.

Figure 10 shows the ADA4350 configured as a transimpedance amplifier with multiple gains when a dual supply is used.

Figure 3 and Figure 4 show the signal gain/noise gain of the board when configured as Figure 10. Figure 7 to Figure 9 show the guard ring details. Figure 11 shows the assembly drawing and Figure 12 shows the 6-layer stackup along with the dimensions for each layer. The bill of materials is listed in Table 2.

DIGITAL PICTURES OF THE EVALUATION BOARD

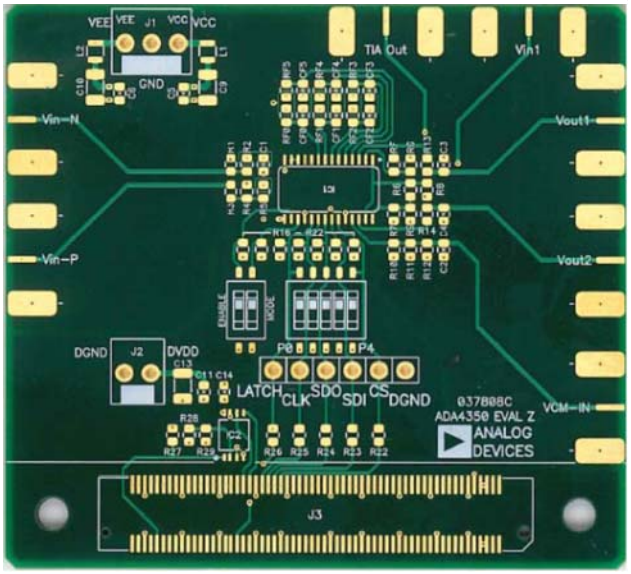

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Figure 1. ADA4350 Evaluation Board Component Side

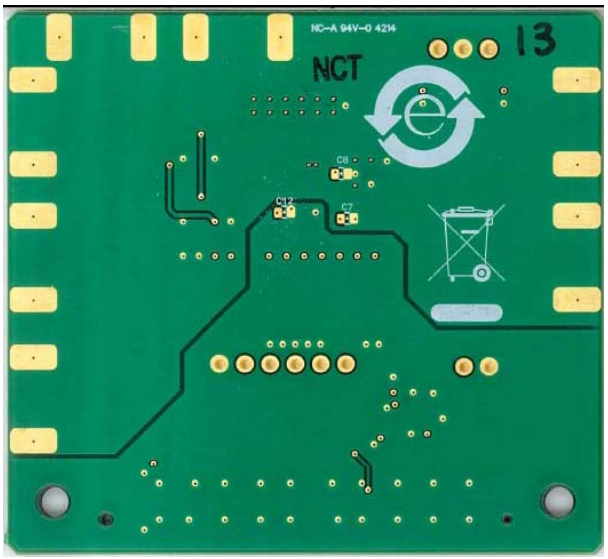

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Figure 2. ADA4350 Evaluation Board Solder Side

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REVISION HISTORY

5/15—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The ADA4350 has two supplies. The analog supply is used to power up all the analog circuitries while the digital supply is used to power up all the digital controls. The two supplies have separate grounds inside the chip. Table 1 shows the supply range of the analog and digital supply, the voltages to be applied to the supply pins in different configurations, and their limitations.

GUARD RING FEATURES

The ADA4350 evaluation board employs a two layer electrostatic guarding to minimize leakage currents from entering the TIA node.

Five mil wide guard rings encircle the inverting and noninverting input components on the top copper layer (see Figure 7 and Figure 9). The guard rings connect to the internal GND copper layer with 5 mil dia vias. Each component pad that connects to the TIA inverting and noninverting inputs is connected to an internal copper trace with 5 mil dia vias (see Figure 8 and Figure 9).

This electrostatic guarding scheme provides isolation from leakage currents but adds a 35 pF parasitic capacitance to the TIA inverting node.

FREQUENCY RESPONSE

The ADA4350 evaluation board is configured for a simulated photodiode input. The photodiode capacitance is represented by C1, a 51 pF capacitor. The photodiode current is simulated by the input voltage Vin-N and R2, a 100 kΩ resistor. $I_{PHOTODIODE}$ = (Vin-N)/100 kΩ.

The total capacitance (91 pF) seen by the TIA is the sum of the ADA4350 input capacitances (2 pF + 3 pF), the photodiode capacitance (51 pF), and the parasitic capacitance of the electrostatic guarding (35 pF).

The five feedback resistor values are approximately ½ decade apart. The five compensation capacitors are selected for maximum bandwidth and maximum gain flatness.

The normalized transimpedance and noise gain are shown in Figure 3 and Figure 4 with compensation capacitors installed and not installed.

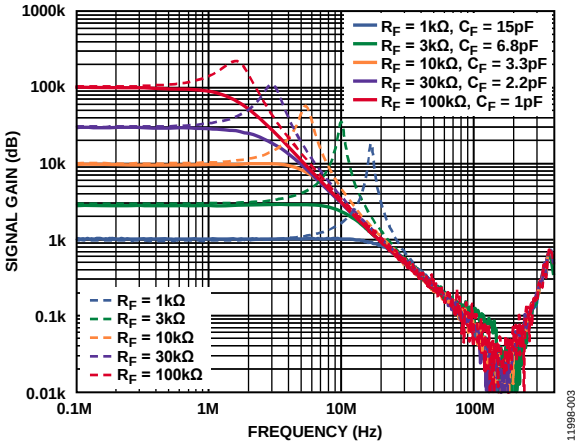

Figure 3. ADA4350 Signal Gain and Noise Gain Frequency Response

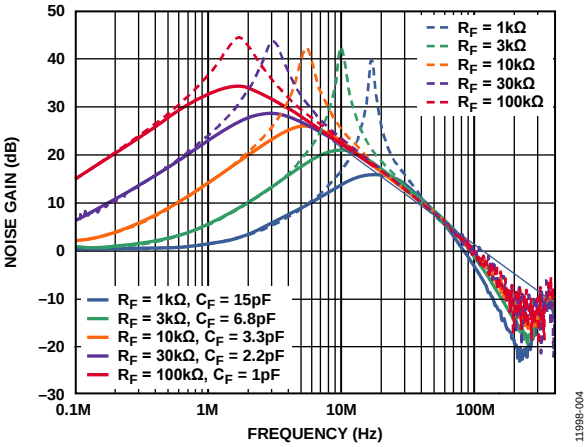

Figure 4. ADA4350 Signal Gain and Noise Gain Frequency Response

Table 1. Powering Up the Analog and Digital Supplies

Supply	Supply Range (V)	Dual Supplies (±V_S)			Single Supplies (+V_S)		
Analog	3.3 to 12	VCC	GND	VEE	VCC	GND	VEE
		+V_S	0	−V_S	+V_S	0	0
Digital	3.3 to 5.5	VCC to DGND			VCC to DGND		
		≥3 V			≥3 V		

EVALUATION BOARD CONTROL

This user guide focuses on setting up the evaluation board. For logic tables of the different control modes and for an in depth analysis of the circuit, refer to the ADA4350 data sheet.

Manual Mode

The evaluation board is configured for manual gain selection using the DIP switches. The DIP switch on position represents Logic 0. To operate manually, set the enable switch to Logic 1 (off position), and set the MODE switch to Logic 1 (off position).

To select one gain, set all gain select switches, P0 to P4, to Logic 0 (on position) and select a gain by setting the corresponding gain select switch to Logic 1 (off position).

Note that only five feedback paths (FB0 to FB4) can be accessed in the manual mode and that selecting more than one gain connects all the selected feedback resistors in parallel.

SPI Control (Parallel Mode)

The parallel mode works very similar to the manual mode except that five digital control lines (P0 to P4) are used instead of the manual switches. Set the enable switch to Logic 1 (off position), and set the MODE switch to Logic 1 (off position). Set the DIP switches (P0 to P4) to Logic 1 (off position), and connect the logic output of an external microcontroller or FPGA to the plated holes next to the P0 to P4 switches. A Logic 1 on each digital line selects the corresponding gain. Applying a Logic 1 to more than one line at a time connects all the selected gains in parallel.

SPI Control (Serial Mode)

Set the MODE switch and $\overline{\text{LATCH}}$ switch to Logic 0 (on position), and the ENABLE switch to Logic 1 (off position). Set all other gain select switches (P1 to P4) to Logic 1 (off position), and perform the following steps:

1. Plug the Analog Devices, Inc., SDP-S controller board onto the 120-pin connector on the ADA4350 evaluation board. The SDP-S control board can be purchased from Analog Devices.
   The user can also use an individual SPI interface through the 5-pin SPI connector on the evaluation board.
2. Download the LabVIEW® control panel from http://www.analog.com/ada4350-demoinstaller. Unzip the file, click **setup.exe**, and follow the installation prompts. If the installation is successful, the **ADA4350 Evaluation** icon appears under **Start** > **Programs** > **Analog Devices** (see Figure 5).

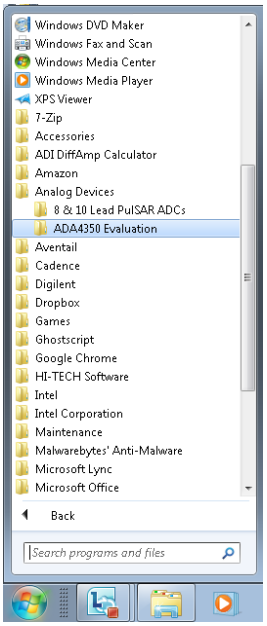

Figure 5. Location of the LabVIEW Control Panel Program

3. Open the LabVIEW control panel (see Figure 6). The control panel allows the user to open and close individual switches in the switch matrix of the ADA4350. For example, to select the FB0 feedback path, click the S0 and S6 switches, then click the **Write New Configuration** button.

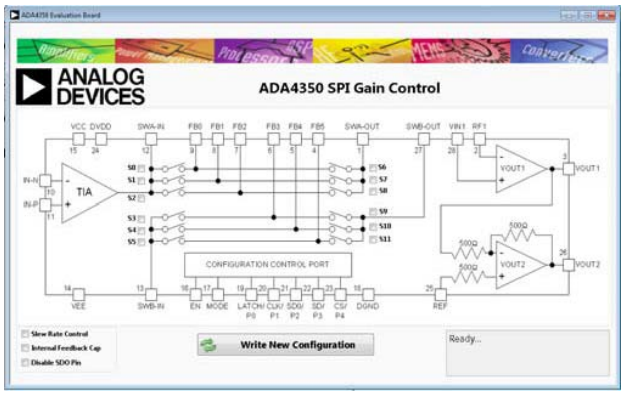

Figure 6. Labview Control Panel

Switches

The gain select switches (S0 to S5) have around 350 Ω series internal resistance that appears as a resistance in series with the TIA output, while S6 to S11 has around 150 Ω switch resistances.

EVALUATION BOARD ELECTROSTATIC GUARDING

The guard ring is represented by the red enclosed area around the inputs. The evaluation board uses the guard ring to minimize leakage currents entering the inputs causing offsets.

Note that the guard ring is employed all the way from the top copper layer through the inner layers and into the ground layer.

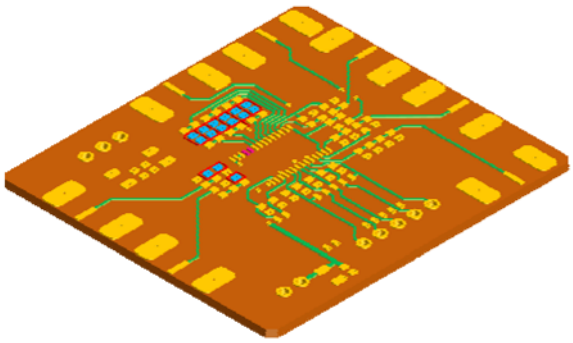

Figure 7. Top Layer Guard Ring Drawing

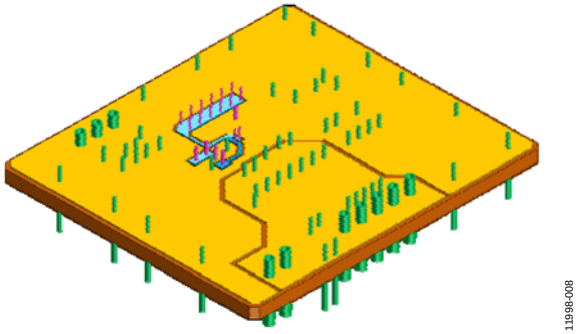

Figure 8. Ground Layer Guard Ring Drawing

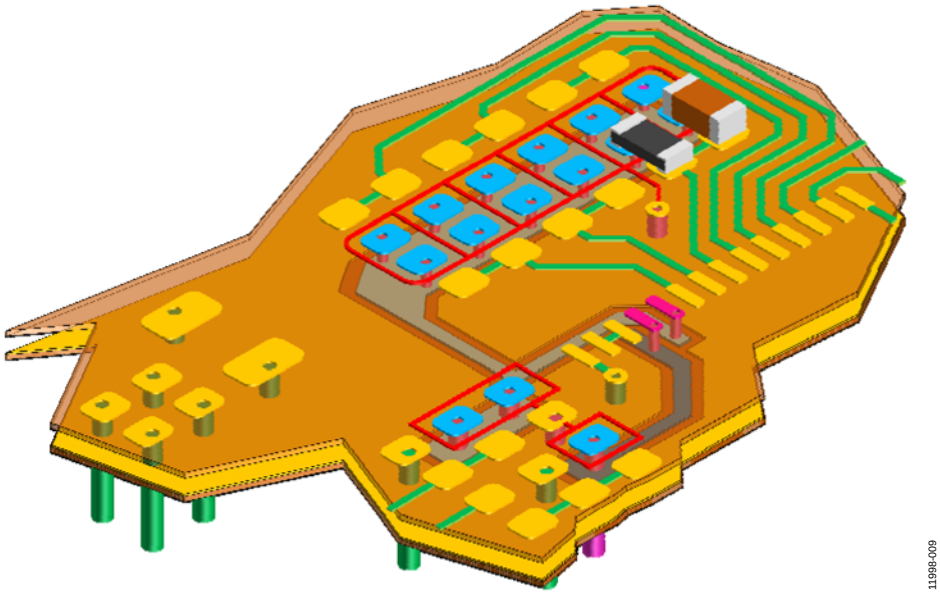

Figure 9. Guard Ring Details

EVALUATION BOARD SCHEMATIC AND ARTWORK

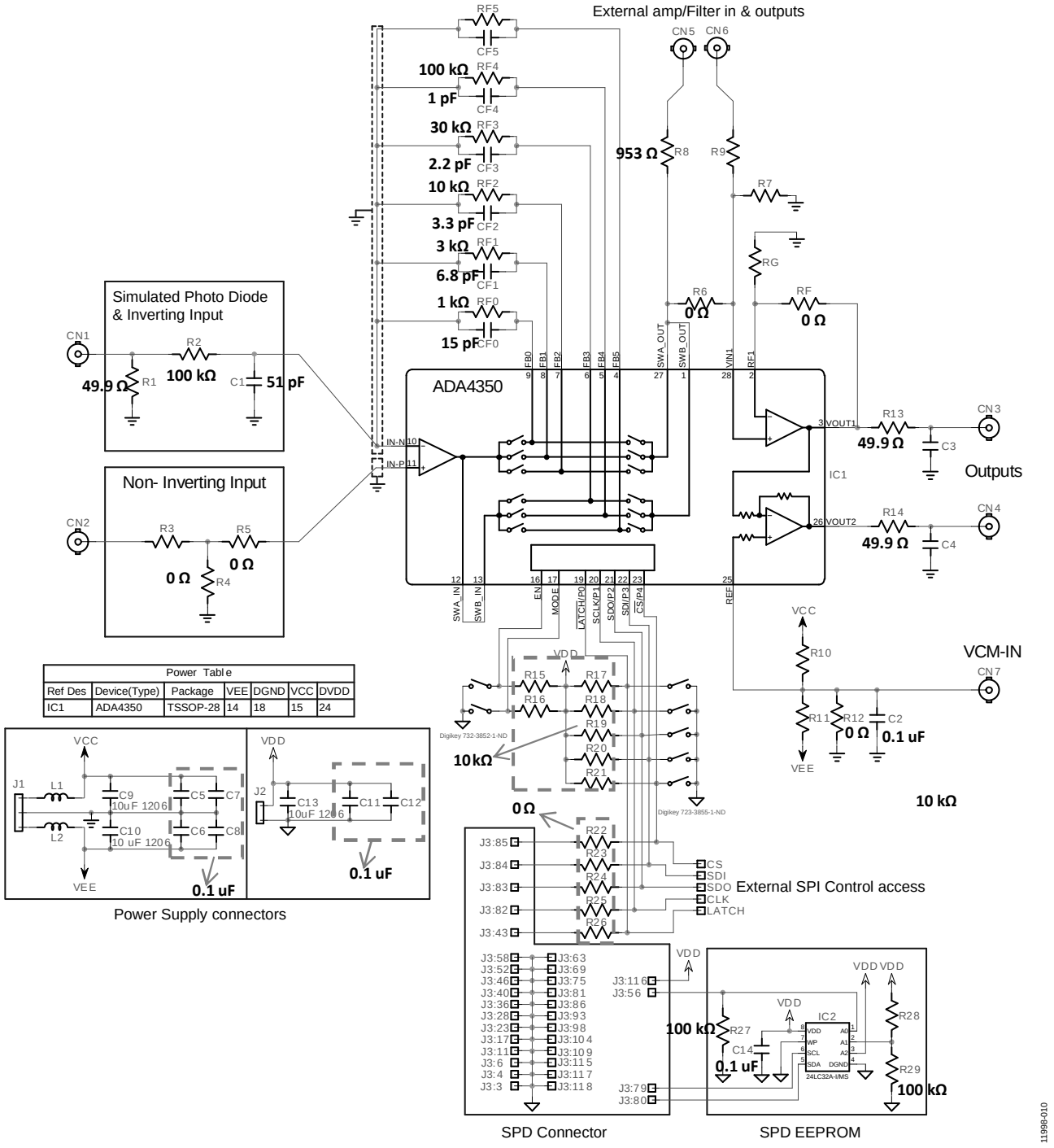

Figure 10. Schematic

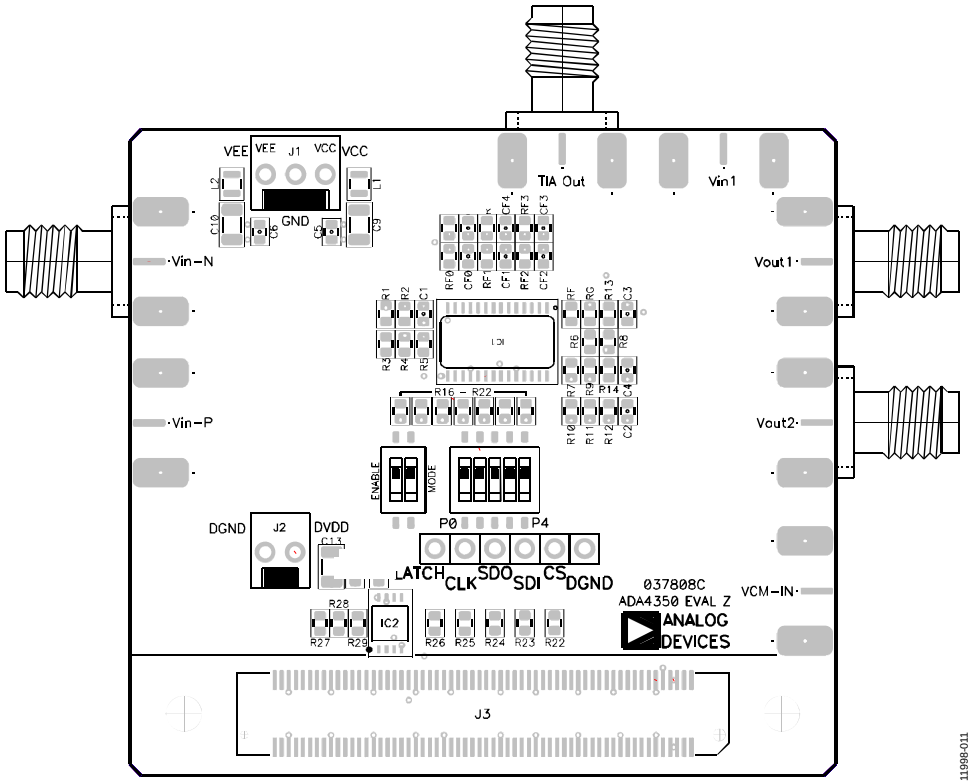

Figure 11. Component Side Assembly Drawing

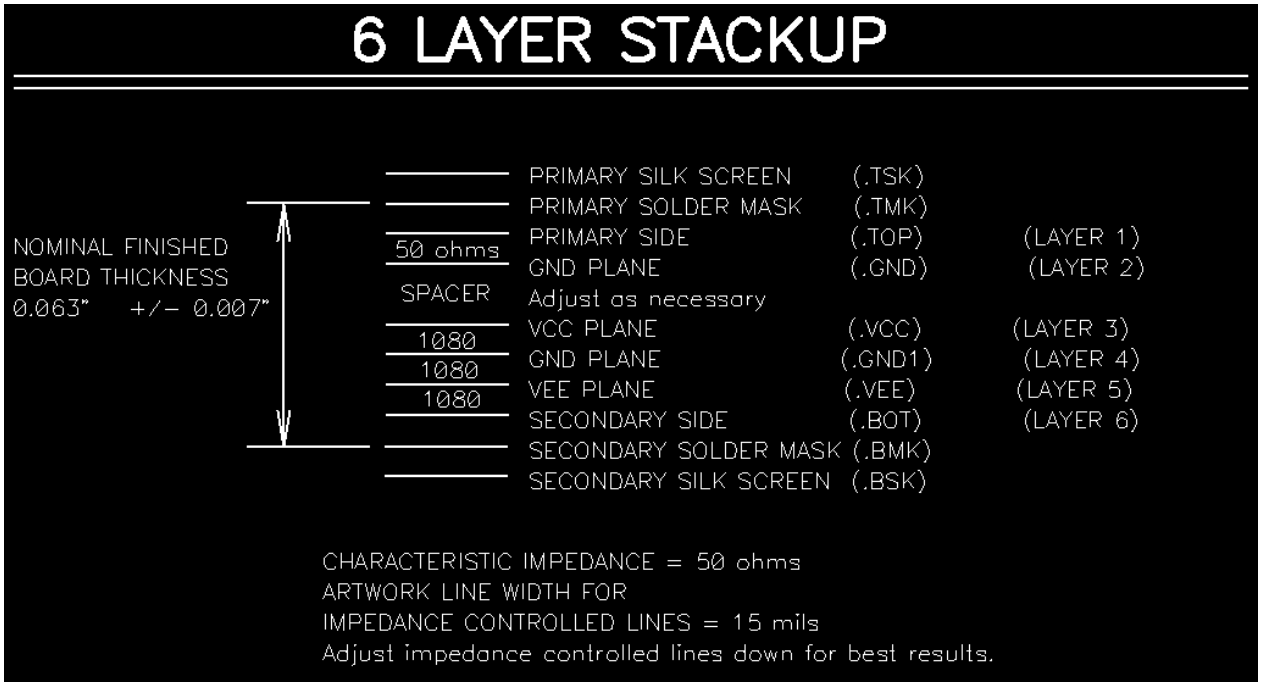

Figure 12. Layer Stackup

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Qty	Reference Designator	Description	Package
1	None	Analog supply connector	3-pin 100 mil header
1	None	Digital supply connector	2-pin 100 mil header
1	None	2-pin mode selector	2-pin dip switch
1	None	5-pin gain selector	5-pin dip switch
3	C9, C10, C13	10 µF capacitor	1206
6	C5 to C8, C11, C12	0.1 µF capacitor	0603
10	CF0 to CF5, C1 to C4	Capacitor, user defined	0603
1	ADA4350	See the ADA4350 data sheet packaging information	28-lead TSSOP
7	Vin_P, Vin_N, VCM-IN, Vin1, Vout1, Vout2, TIA Out	SMA/SMT	SMA/SMT
29	R1 to R21, RF0 to RF5, RF, RG	Resistor, user defined	R0603
1	SDP connector	Standard 120-pin SDP connector	
1	Small SDP connector	5-pin SPI header	
1	24LC32AF	SDP EEPROM	MSOP