Ordering number : ENA2223

LC79451KB

CMOS IC

Controller and Driver for Electronic Paper

ON Semiconductor®

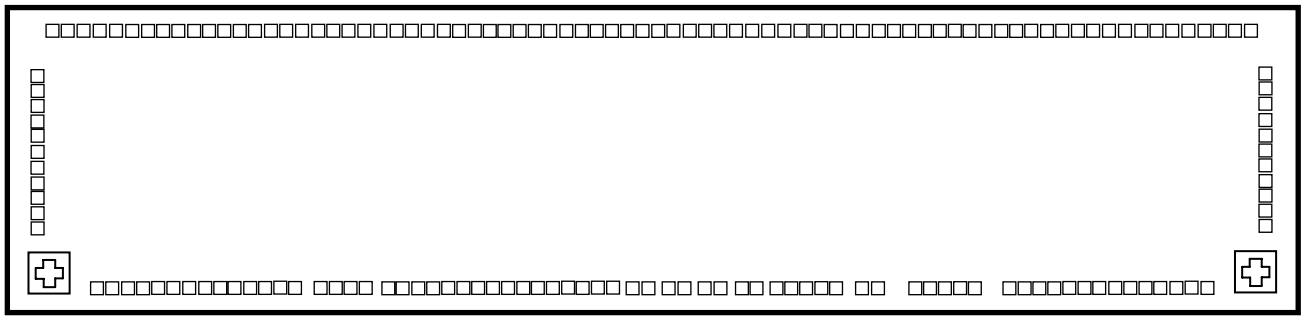
http://onsemi.com

1. Overview

LC79451KB is controller and driver IC for the electronic paper display (EPD). It can realize low supply voltage and low power consumption. It supports SPI and I^2C interface. It is equipped with waveform generator, oscillator, charge-pump and 128 segment drivers.

2. Features

- Logic power supply voltage (VDD) : +1.6V to +3.6V
- Analog power supply voltage (VDD2) : +1.8V to +3.6V
- Interface : SPI or I^2C
- Operating frequency : 400kHz max (I^2C) /10MHz max (SPI)
- Standby current : 1μA [max]
- Operating current : 30μA [typ] (no load, charge-pump frequency 1kHz)
- Number of segment drive output : 128
- Level of segment drive output : 3 level (-15V/0V/+15V)
- Waveform output : Internal waveform generator
- Internal charge-pump : +15V/-15V
- Frequency of CR oscillator : 32kHz +/-3%
- Automatic low power function : Automatic start and stop of internal circuit with the waveform output
  : Automatic shift to the lower charge-pump frequency with finish of the waveform output
- Gold bump chip : X = 6.55mm, Y = 1.43mm



* I^2C Bus is a trademark of Philips Corporation.

ORDERING INFORMATION

See detailed ordering and shipping information on page 38 of this data sheet.

Semiconductor Components Industries, LLC, 2013

3. Block Diagram

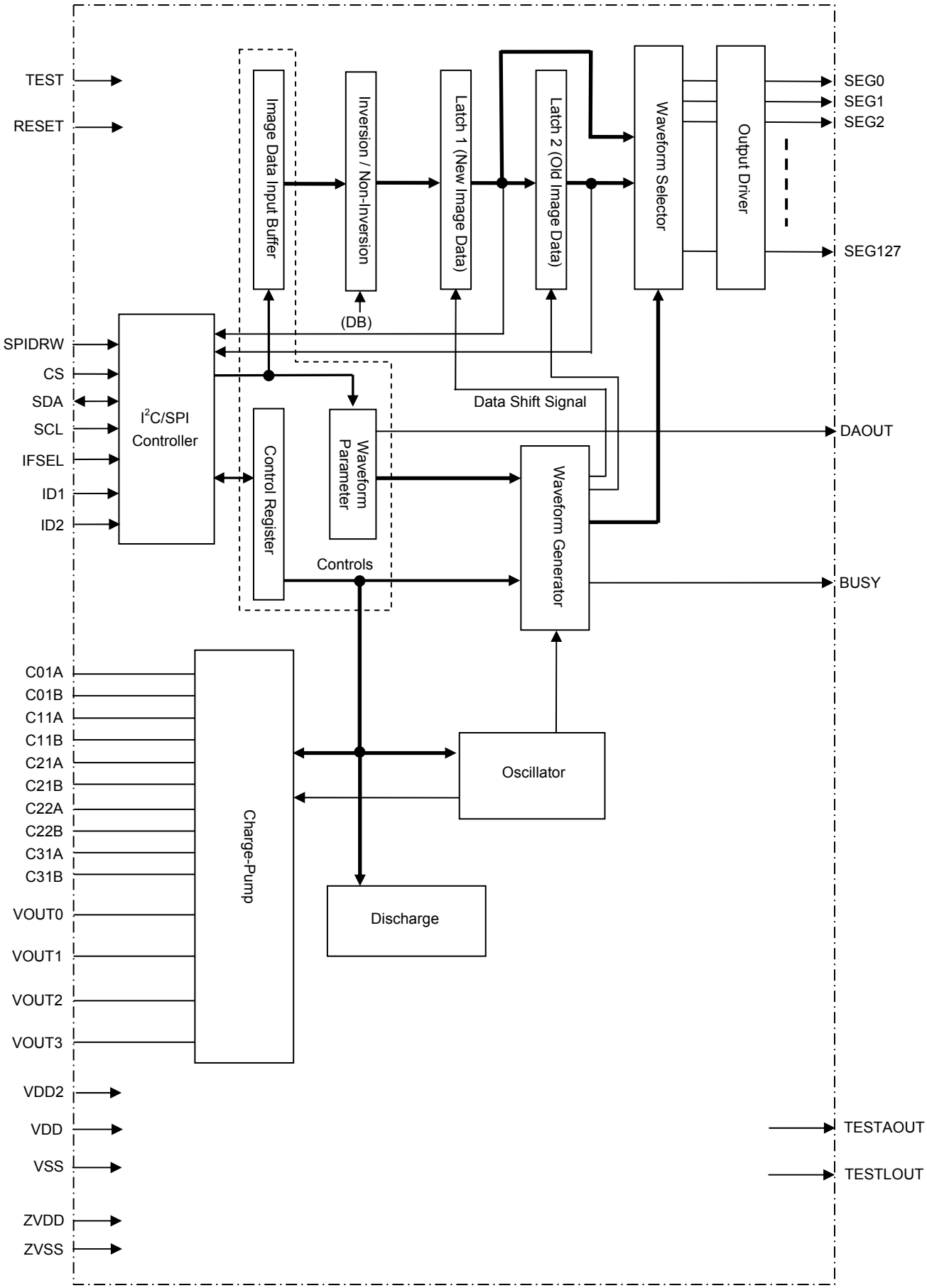


Fig.1. Block Diagram

4. Pin Functions

4-1. Pin List

Power Supply Pin

Symbol	Connection	I/O	Range	Function
VDD	Power supply	-	+1.6V to +3.6V	Logic power supply
VDD2	Power supply	-	+1.8V to +3.6V	Analog power supply
VSS	Power supply	-	0V	Ground

Interface Setting Pin

Symbol	Connection	I/O	Function
IFSEL	VDD/VSS	I	Interface selection IFSEL = L : 2-wire serial interface (I^2C) IFSEL = H : 3-wire serial interface (SPI)

I^2C Interface ID Setting Pin

Symbol	Connection	I/O	Function
ID1 ID2	VDD/VSS	I	I^2C interface ID Connected to VDD : ID = 1 Connected to VSS : ID = 0

External Interface Pin

Symbol	Connection	I/O	Function
RESET	External circuit	I	Reset signal RESET = L : Initialization RESET = H : Normal operation
CS	External circuit /VSS	I	LSI selection signal of 3-wire serial interface CS = L : LSI operates CS = H : LSI does not operate (When you select 2-wire serial interface, please connect VSS.)
SCL	External circuit	I	Serial clock of 2-wire serial interface Pull-up to VDD. Connect other device of open-drain output to Wired-OR. Serial clock of 3-wire serial interface
SDA	External circuit	I/O	Input and output data signal of 2-wire serial interface Input : Pull-up to VDD. Connect other device of open-drain output to Wired-OR. Output : Nch open-drain. Input data of 3-wire serial interface
SPIDRW	External circuit /VSS	I	Read / Write mode selection signal of 3-wire serial interface SPIDRW = L : Write Mode SPIDRW = H : Read Mode (When you select 2-wire serial interface, please connect VSS.)
DAOUT	External circuit /Open	O	RESET detection signal of 2-wire serial interface RESET detection signal or internal data of 3-wire serial interface SPIDRW = L : RESET detection signal SPIDRW = H : Internal data (With selecting 2-wire serial interface, DAOUT outputs STERR of control register 4. It shows RESET detection signal.)
BUSY	External circuit /Open	O	The signal which shows prohibition of the update of “waveform parameter” and “control register” (With selecting 2-wire serial interface, BUSY output START of control register 4. It shows prohibition of the update signal.)

Output Driver Pin

Symbol	Connection	I/O	Range	Function
SEG0 to 127	E-paper	O	+15V, 0V, -15V	Output for panel drive

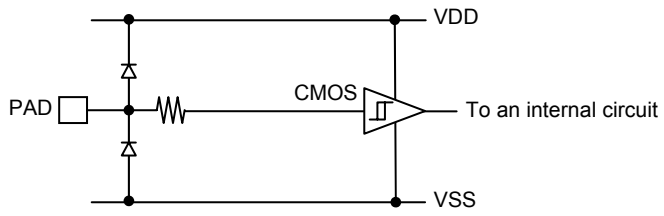
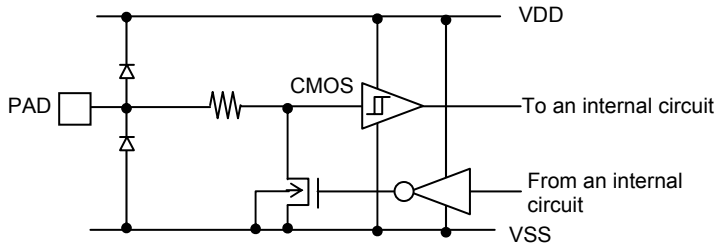
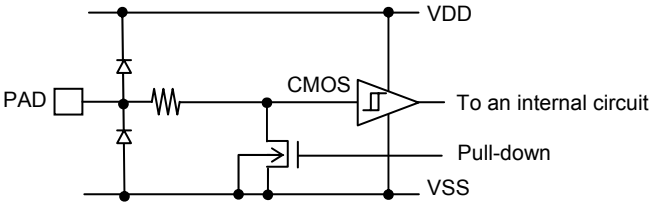
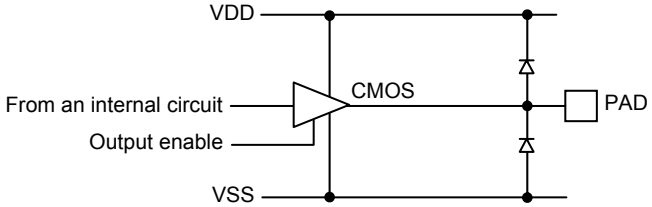
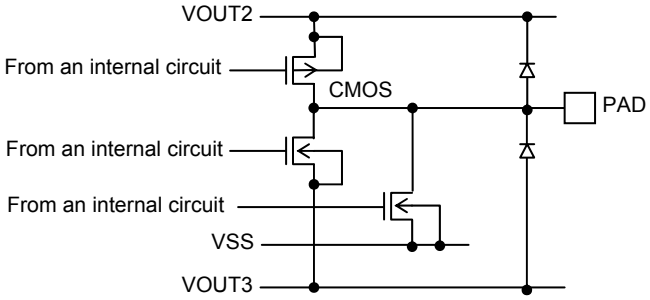
Charge-Pump Pin

Symbol	Connection	I/O	Range	Function
VOUT0	Capacitor	O	+2.5V	Charge-pump voltage or charge-pump reference voltage. Power supply voltage for oscillator. Please connect capacitor between VOUT0 and VSS.
VOUT1	Capacitor	O	+5.0V	Charge-pump voltage. VOUT1 = VOUT0 × 2 Please connect capacitor between VOUT1 and VSS.
VOUT2	Capacitor	O	+15.0V	Charge-pump voltage. VOUT2 = VOUT1 × 3 Please connect capacitor between VOUT2 and VSS.
VOUT3	Capacitor	O	-15.0V	Charge-pump voltage. VOUT3 = VOUT2 × -1 Please connect capacitor between VOUT3 and VSS.
C01A, C01B C11A, C11B C21A, C21B C22A, C22B C31A, C31B	Capacitor	-		Capacitor connection pin for Charge-pump. Please connect capacitor between corresponding CxyA and CxyB. CxyA is positive connection pin for the flying capacitor. CxyB is negative connection pin for the flying capacitor. (With setting of 2.5V for the reference voltage, the capacitance between terminals is not necessary between C01A and C01B.)

Test Pin

Symbol	Connection	I/O	Function
TEST	Open / VSS	I	Test mode setting signal. Please connect to VSS or Open during the normal operation.
TESTAOUT	Open	O	Output for the test. Please Open.
TESTLOUT	Open	O	Output for the test. Please Open.
ZVDD	Open	-	Power supply for the test. Please Open.
ZVSS	Open	-	Power supply for the test. Please Open.

4-2. Pin Equivalent Circuit

Symbol	Internal Equivalent Circuit	Connection when not in use
RESET CS SCL IFSEL ID1 ID2 SPIDRW	The CMOS schmidt trigger input buffer 	VSS
SDA	The CMOS schmidt trigger input-output buffer with Nch open-drain output 	VSS
TEST	The CMOS schmidt trigger input buffer with pull-down 	Open /VSS
DAOUT BUSY	The CMOS output buffer 	Open
SEG0 to 127	The CMOS output and Nch open-drain output buffer 	Open

5. Specifications

5-1. Absolute Maximum Ratings at VSS = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VDD		-0.3 to +4.0	V
	VDD2		-0.3 to +4.0	V
Input voltage	VIN		-0.3 to VDD+0.3	V
Operating temperature	Topr		-30 to +80	°C
Storage temperature	Tstg		-40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5-2. Allowable Operating Ranges at Ta = -30 to +80°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	VDD	VDD ≤ VDD2	+1.6	+2.5	+3.6	V
	VDD2	VDD ≤ VDD2	+1.8	+2.5	+3.6	V
	VSS			0		V
Input High-level voltage	VIH		0.8 × VDD		VDD	V
Input Low-level voltage	VIL		VSS		0.2 × VDD	V

5-3. Electrical Characteristics

DC Characteristics (Case without the special mention VDD = +2.5V, VDD2 = +2.7V, VSS = 0V, Ta=+25°C)

Parameter	Symbol	Condition	min	typ	max	Unit	Note
Input leak current	IIL	VIN = 0V to VDD	-1	-	1	μA	*1
Standby current VDD	IDDS	All Circuit Stops	0	-	1	μA	*2
Standby current VDD2	IDD2S	(RESET = L)	0	-	1	μA	*2
Operating current VDD	IDD	SPI (10MHz)	-	400	480	μA	
Operating current VDD2	IDD2		-	30	36	μA	*3
Output voltage	VOH	IOUT = -0.5mA	VDD - 0.36	VDD - 0.2	VDD	V	*4
	VOL1	IOUT = +0.5mA	0	0.1	0.18	V	*4
	VOL2	IOUT = +3mA	0	-	0.4	V	*5
<Output Driver Characteristics>							
SEG output resistance VOUT2	RON1	VOUT = VOUT2 -0.5V	8	10	12	kΩ	
SEG output resistance VSS	RON2	VOUT = +0.5V	7.5	10	12.5	kΩ	
SEG output resistance VOUT3	RON3	VOUT = VOUT3 +0.5V	8	10	12	kΩ	
<Charge-pump Characteristics>							
Output voltage VOUT2	VOUT2NL1	No Load	14.25	15.00	15.75	V	*6, *7
	VOUT2NL2					V	*6, *8
Output voltage VOUT3	VOUT3NL1	No Load	-15.75	-15.00	-14.25	V	*6, *7
	VOUT3NL2					V	*6, *8
Load output voltage VOUT2	VOUT2L1	Load Current = -100μA	0.90 × VOUT2	-	VOUT2	V	*6, *7
	VOUT2L2		0.95 × VOUT2	-	VOUT2	V	*6, *8
Load output voltage VOUT3	VOUT3L1	Load Current = +100μA	VOUT3	-	0.90 × VOUT3	V	*6, *7
	VOUT3L2		VOUT3	-	0.95 × VOUT3	V	*6, *8
Load voltage ratio regulation	VRATIO		0.97	1	1.03	-	*6, *9
<Oscillator Characteristics>							
Oscillator frequency	Fclk	VDD = 1.6V to 3.6V VDD2 = 1.8V to 3.6V	31.04	32.00	32.96	kHz	*10
<Discharge Characteristics>							
Discharge resistance VOUT2	RDON1	VOUT2 = +15V	8	10	12	kΩ	*11a
Discharge resistance VOUT3	RDON2	VOUT3 = -15V	8	10	12	kΩ	*11b

Note: *1. For RESET, SCL, SDA, CS, ID1, ID2, IFSEL, SPIDRW pin.

*2. The maximum current is prescribed with the limit value of the measuring instrument.

*3. The state of the circuit as follows.
Oscillator operates, charge-pump operates, output driver stops (No load), charge-pump voltage is in a stable state.
Charge-pump frequency 1kHz (control register 1 : CP_F10 = 0, CP_F11 = 0, CP_F12 = 0)
Charge-pump reference voltage 2.5V (control register 2 : VREGSEL=1)

*4. For BUSY, DAOUT pin.

*5. For SDA pin.

*6. Use external capacitors of the recommended capacitance value.

*7. Charge-pump frequency 32kHz (control register 1 : CP_F10 = 1, CP_F11 = 1, CP_F12 = 1)
Charge-pump reference voltage 1.25V (control register 2 : VREGSEL = 0)

*8. Charge-pump frequency 32kHz (control register 1 : CP_F10 = 1, CP_F11 = 1, CP_F12 = 1)
Charge-pump reference voltage 2.5V (control register 2 : VREGSEL = 1)

*9. The change ratio of the charge-pump voltage by the load.
(Output voltage VOUT2/Output voltage VOUT3) / (Load output voltage VOUT2/Load output voltage VOUT3)

*10. Charge-pump operates.

*11. Charge-pump stops.
(*11a) Between VOUT2 and VSS.
(*11b) Between VOUT3 and VSS.

5-4. AC Timing Characteristics (I^2C/SPI)

(Case without the special mention VDD = +2.5V, VSS = 0V, Ta = +25°C)

Parameter	Symbol	Condition	min	typ	max	Unit	Note
VDD - VDD2 setup time	tSU(1)		0	-	-	µs	
VDD2 - RESET setup time	tSU(2)		10	-	-	ms	
RESET pulse width	tPW(1)		5	-	-	µs	
RESET - START condition RESET - CS setup time	tSU(3)		1	-	-	µs	
RESET - VHON setup time RESET - START setup time	tSU(4)		10	-	-	ms	
HVON Flag hold time	tHD(1)	Automatic charge-pump mode	Typ × 0.97	(*1)	(Typ × 1.03)+1	ms	*2
		Manual charge-pump mode	Option				
LE Flag hold time	tHD(2)		-	-	1	µs	*2

Note: *1. It is same as rising period of the charge-pump. (Period be set by control register 1)
*2. The Flag is canceled automatically.

1) Timing of main signals from power-up to the initialize operation

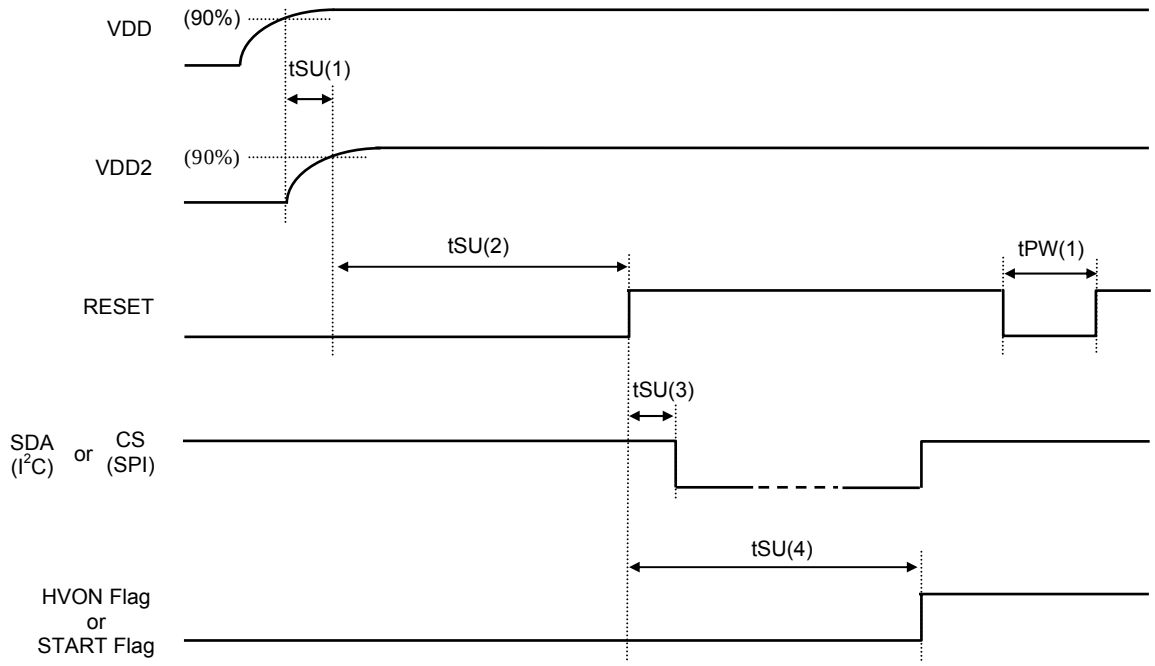


Fig.2. VDD, VDD2, RESET, SDA(I^2C) /CS(SPI), HVON Flag/START Flag timing

2) HVON Flag hold time

Charge-pump starts with HVON Flag = 1.

In automatic charge-pump mode, charge-pump stops automatically after charge-pump rising period (set to control register 1), and HVON Flag is automatically canceled (HVON Flag = 0.). HVON Flag is used for keeping the charge-pump voltage.

In manual charge-pump mode, charge-pump is active until canceled of HVON Flag.

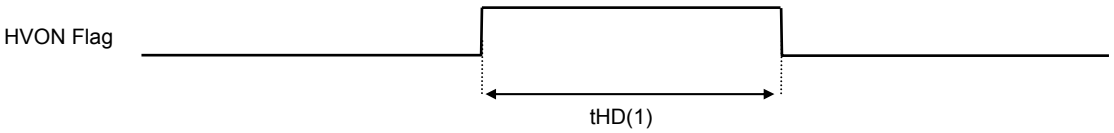


Fig.3. HVON Flag hold time

3) LE Flag hold time

The image data shift with LE Flag = 1.

When the data finish shifting, LE Flag is automatically canceled.

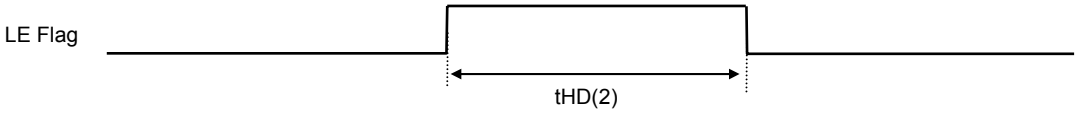


Fig.4. LE Flag hold time

5-5. I²C (2-wire serial interface) Timing Characteristics

(Case without the special mention VDD = +2.5V, VSS = 0V, Ta = +25°C)

Parameter	Symbol	Conditions	min	typ	max	Unit
SCL frequency	fSCL(1)		-	-	400	kHz
Start condition setup time	tSU(5)		600	-	-	ns
Start condition hold time	tHD(3)		600	-	-	ns
SDA rise time	trDA(1)		-	-	300	ns
SDA fall time	tfDA(1)		-	-	300	ns
SCL rise time	trCL(1)		-	-	300	ns
SCL fall time	tfCL(1)		-	-	300	ns
SCL low pulse width	tPW(3)		1300	-	-	ns
SCL high pulse width	tPW(2)		600	-	-	ns
Data setup time	tSU(6)		100	-	-	ns
Data hold time	tHD(4)		0	-	900	ns
Stop condition setup time	tSU(7)		600	-	-	ns
STOP - START bus open time	tBUF		1300	-	-	ns

1) I²C interface bus timing

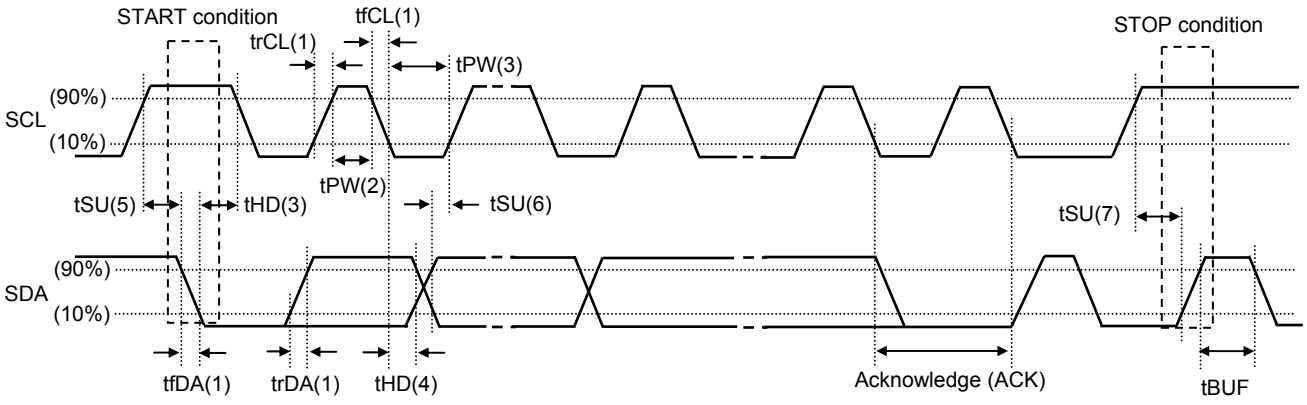
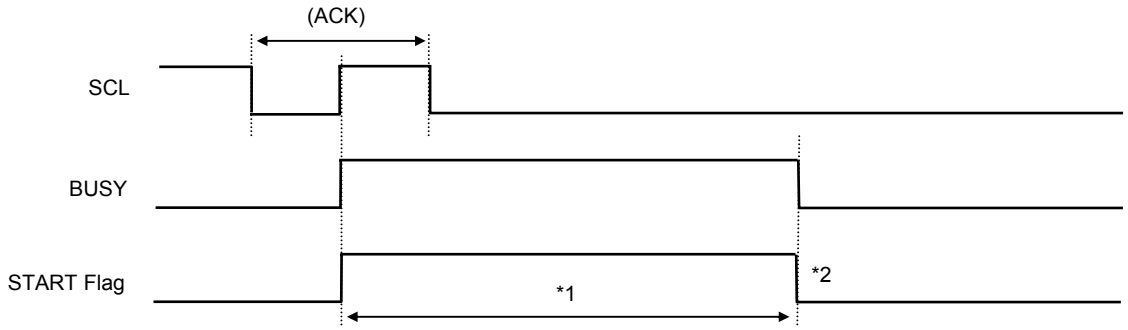


Fig.5. I²C bus timing

2) Timing of BUSY and START Flag after setting START command in I²C interface

Output of BUSY means START Flag. During in BUSY = 1, "WAVEFORM PARAMETER" and "CONTROL REGISTER" are write inhibit state. An internal state is charge-pump rising period before the waveform output or during the waveform output. After outputs waveform from segment, BUSY and START Flag are automatically canceled. (Cf. 6-3)



*1 Automatic charge-pump mode : charge-pump rising period (set to control register 1) + waveform output period (set to waveform parameter)

Manual charge-pump mode : waveform output period (set to waveform parameter)

*2 BUSY and START Flag are automatically canceled.

Fig.6. I²C BUSY output, and START Flag timing

5-6. SPI (3-wire serial interface) Timing Characteristics

(Case without the special mention VDD = +2.5V, VSS = 0V, Ta = +25°C)

Parameter	Symbol	Conditions	min	typ	max	Unit
SCL frequency	fSCL(2)	VDD = 1.6V to 2.0V	-	-	6	MHz
		VDD = 2.0V to 3.6V	-	-	10	MHz
CS - SCL setup time	tSU(8)		300	-	-	ns
SCL - CS hold time	tHD(5)		300	-	-	ns
SDA - SCL setup time	tSU(9)		50	-	-	ns
SCL - SDA hold time	tHD(6)		50	-	-	ns
SCL low pulse width	tPW(4)		50	-	-	ns
SCL high pulse width	tPW(5)		50	-	-	ns
CS interval time	tINT(1)		1000	-	-	ns

1) SPI interface bus timing

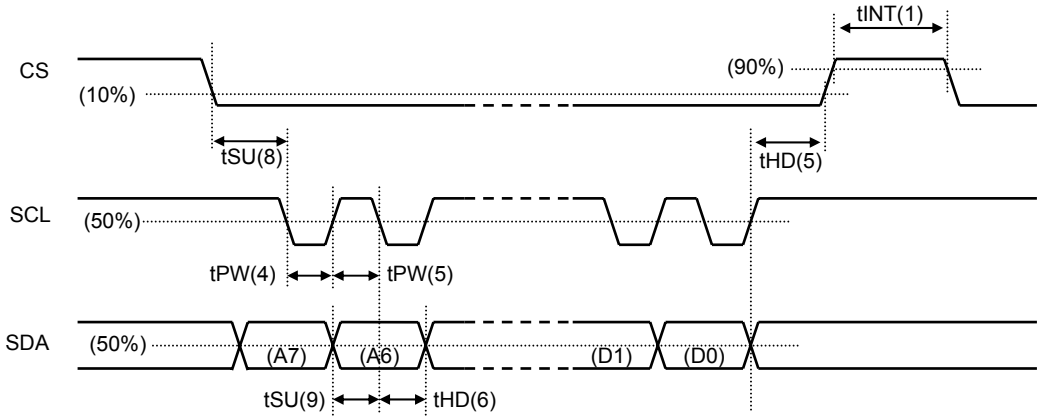
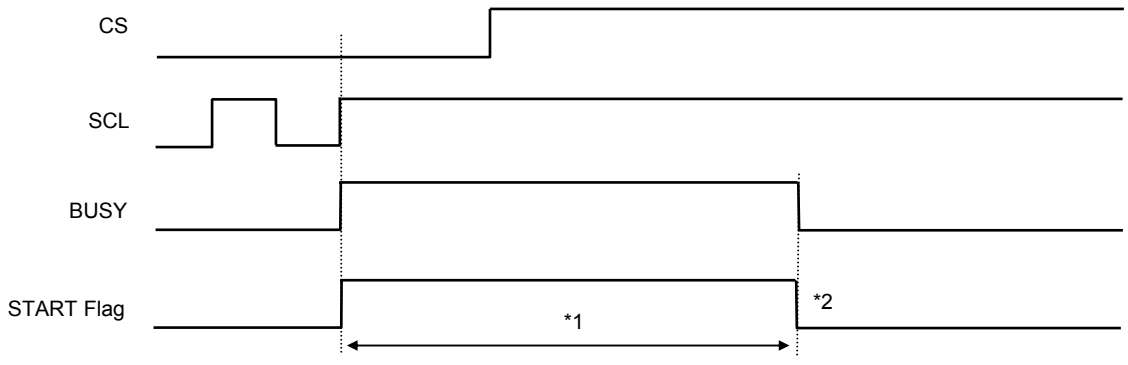


Fig.7. SPI bus timing

2) Timing of BUSY and START Flag after setting START command in SPI interface
Output of BUSY means START Flag. During in BUSY=1, "WAVEFORM PARAMETER" and "CONTROL REGISTER" are write inhibit state. An internal state is charge-pump rising period before the waveform output or during the waveform output. After outputs waveform from segment, BUSY and START FLAG are automatically canceled. (Cf. 6-3)



*1 Automatic charge-pump mode : charge-pump rising period (set to control register 1) + waveform output period (set to waveform parameter)
Manual charge-pump mode : waveform output period (set to waveform parameter)
*2 BUSY and START FLAG are automatically canceled.

Fig.8. SPI BUSY output, and START Flag timing

6. Function Explanation

6-1. I^2C/SPI Interface Selection Function

The interface supports 2-wire serial interface (I^2C) and 3-wire serial interface (SPI).
The interface is selected by connecting IFSEL pin to VDD or VSS.

I^2C $\Rightarrow$ Connect IFSEL to VSS
SPI $\Rightarrow$ Connect IFSEL to VDD

(1) I^2C Interface Signal

1) RESET	(In)	----	Reset signal.
2) SCL	(In)	----	Serial clock.
3) SDA	(In/Out)	----	Serial data.
4) IFSEL	(In)	----	Serial interface selection.
5) ID1	(In)	----	I^2C interface ID.
6) ID2	(In)	----	I^2C interface ID.
7) BUSY	(Out)	----	Prohibition signal of the update of specific register.
8) DAOUT	(Out)	----	Reset detection signal.

(2) SPI Interface Signal

1) RESET	(In)	----	Reset signal.
2) CS	(In)	----	Device selection.
3) SCL	(In)	----	Serial clock.
4) SDA	(In)	----	Serial data.
5) IFSEL	(In)	----	Serial interface selection.
6) BUSY	(Out)	----	Prohibition signal of the update of specific register.
7) SPIDRW	(In)	----	Read/Write mode selection signal.
8) DAOUT	(Out)	----	Reset detection signal. Internal data.

6-1-1. I²C Write Format

After entry of the register address in I²C interface write mode, 8 bits serial data of each address are written in registers in sequence. The address without the register allocation is skipped.

START condition	ID + $\overline{W}$	ACK	Register address (N)	ACK	Register data (N)	ACK	Register data (N+1)	•••

$\overline{W}$ shows R/$\overline{W}$ = 0

6-1-2. I²C Read Format

After entry of the register address in I²C interface write mode, input I²C interface read mode. And 8 bits serial data of each address are read from registers in sequence. The address without the register allocation is skipped.
When the register data of each address are less than 8 bits, the data of the remaining bit are read in "0."
In read image data, last bit is old (past) image data, and one high rank bit is new (current) image data.

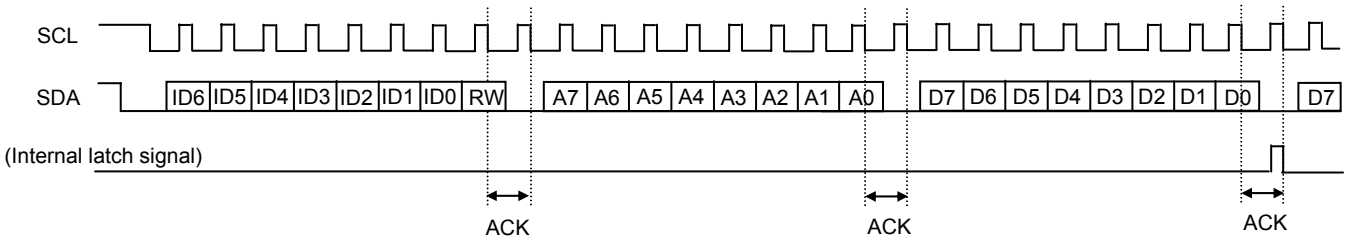
START condition	ID + $\overline{W}$	ACK	Register address (N)	ACK

START condition	ID + R	ACK	Register data (N)	ACK	Register data (N+1)	ACK	Register data (N+2)	•••

R shows R/$\overline{W}$ = 1

6-1-3. I²C Data Transmission

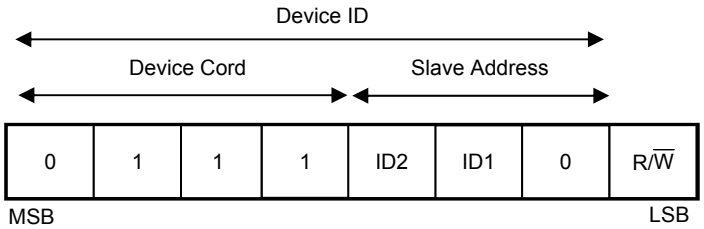
During the period when SCL line is "H", the change of SDA line from "H" to "L" is recognized to be START condition, and the change of SDA line from "L" to "H" is recognized to be STOP condition. The master device on the system can communicate with a particular slave device by sending the device ID of 7 bits long and instruction codes of 1 bit long as read "1"/write "0" on SDA line following START condition.
When the device ID of the master device accords with the device ID of the slave device, the slave device replies to SDA line with the acknowledge (ACK), and Read or Write operates according to Read/Write command code. The device is set to standby mode when device ID does not accord.
SDA line is changeable while SCL line is "L".
SDA line transfers the consecutive 8 bits from the master device. And SDA line is opened in the ninth clock cycle period. The slave device which receives data on the system bus sends low to SDA line. Sending low is the acknowledge signal indicating that data has been received.
The command data is comprised of address 8 bits and data 8 bits. The command data is stored by the rising of SCL line in the acknowledge period after having received the data 8 bits.



6-1-4. I²C ID Setting

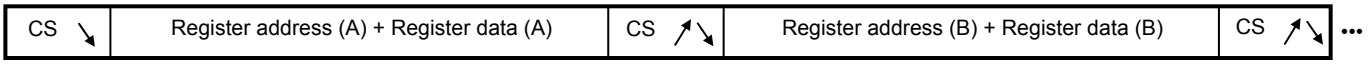
The device ID of 7 bits long is assigned to a slave device in I²C. The device ID is comprised of the device cord of 4 bits and the slave address of 3 bits. Upper 2 bits of the slave address is settable with ID1 pin, and ID2 pin. Please connect ID1 pin and ID2 pin to VDD or VSS.

Write "0" ⇒ connect to VSS
Read "1" ⇒ connect to VDD



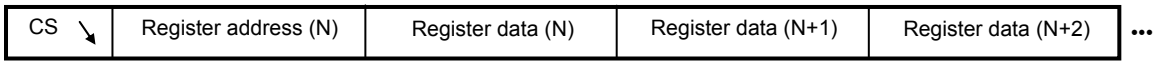
6-1-5. SPI Write Format

In SPI interface write mode, each register data is written with the register address.
Set SPIDRW to “L” in write mode.



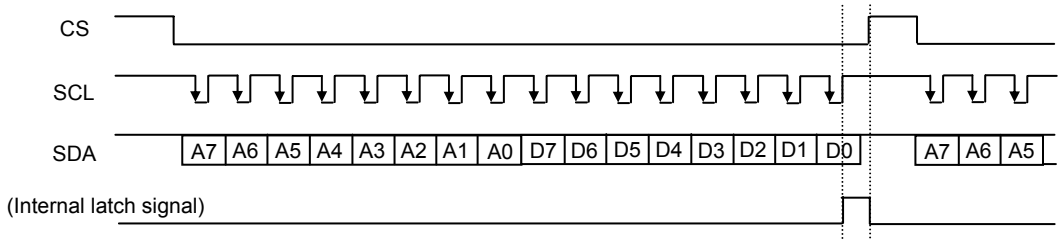
6-1-6. SPI Read Format

In SPI interface read mode, the register data are able to be read serially.
Set SPIDRW to “H” in read mode.
After entry of the register address, the register data can be read from DAOUT pin sync with SCL clock.
The address without the register allocation is skipped.
When the register data of each address are less than 8 bits, the data of the remaining bit are read in “0.”
In read image data, last bit is old (past) image data, and one high rank bit is new (current) image data.



6-1-7. SPI Data Transmission

SDA data is written in the latch by the falling of SCL, these data are stored in the registers by 16th rising of SCL.

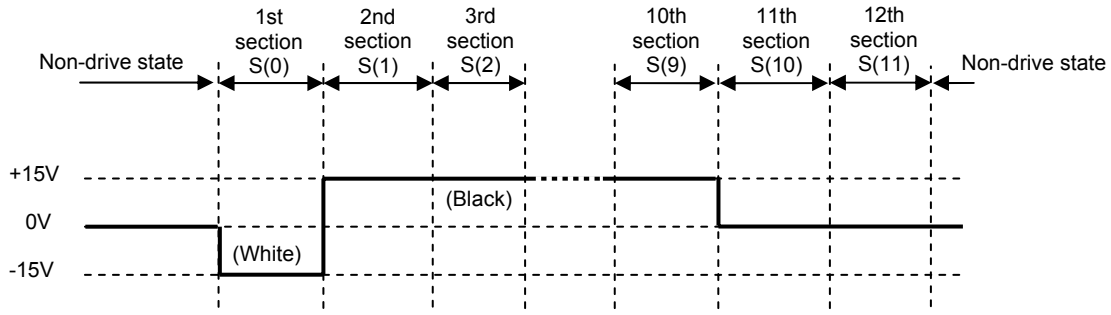


6-2. Waveform Generation Function

This device is equipped with a function to generate four kinds of the normal drive waveform, and one kind of the refresh waveform.
Each waveform can set the output level and the output time.

6-2-1. Normal Drive Waveform

The normal drive waveform is divided into 12 sections and can set the output level and the output time of each section by the registers.
The output level of one section selects among 3 levels of +15V, 0V, -15V.
The output time of one section selects from the range of 1ms to 256ms.



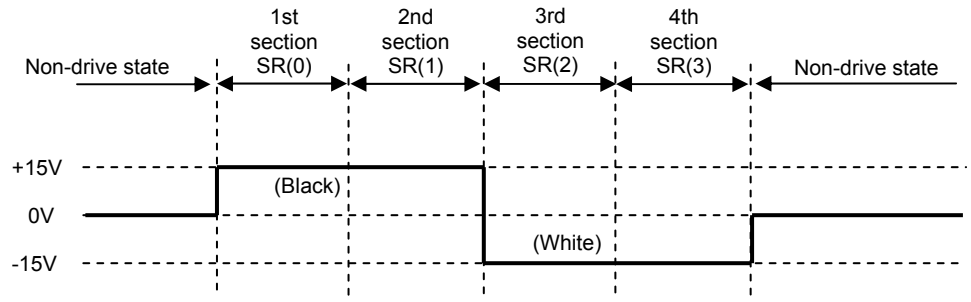
Transition of the following image state can set the normal drive waveform each.

White image ⇒ White image
White image ⇒ Black image
Black image ⇒ White image
Black image ⇒ Black image

Output driver outputs one waveform by setting START Flag.
White and black can turn over by setting DB Flag.

6-2-2. Refresh Drive Waveform

The image is changed to full screen white or full screen black by the refresh drive waveform.
The refresh drive waveform is divided into 4 sections and can set the output level and the output time of each section by the registers.
The output level of one section selects among 3 levels of +15V, 0V, -15V.
The output time of one section selects from the range of 8ms to 2048ms.



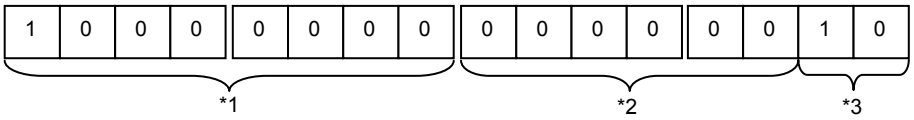
Output driver outputs one waveform by setting START Flag.

6-2-3. Waveform Parameter

<Parameter Definition>

(1) Output Level

e.g. (8002h) : Output level parameter setting of the normal drive waveform W0 – S(0)



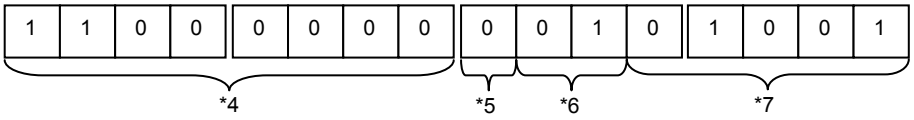
*1) Address (8bits)
*2) Invalid data (6bits)
*3) Output level (2bits) e.g. VNEG (-15V, White)

Output level	D1	D0
VSS (0V)	0	0
VPOS (+15V, Black)	0	1
VNEG (-15V, White)	1	0
(No inputs)	1	1

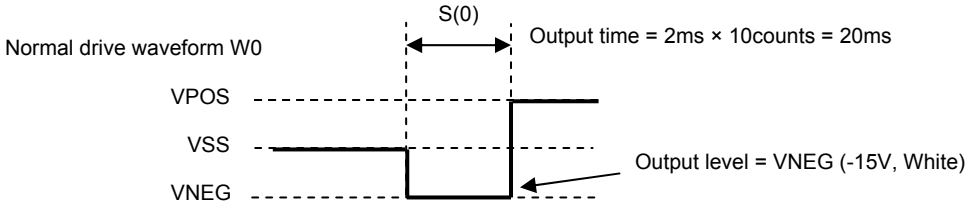
Note : When the output level inputs D1 to "1" and D0 to "1", VPOS or VNEG is selected.

(2) Output Time

e.g. (C029h) : Output time parameter setting of the normal drive waveform W0 – S(0)



*4) Address (8bits)
*5) Invalid data (1bit)
*6) Clock period for output time (2bits) e.g. 2ms
*7) Clock Count for output time (5bits) e.g. 10counts
} Pulse width



Clock period		D6	D5
Normal drive waveform	Refresh drive waveform		
1ms	8ms	0	0
2ms	16ms	0	1
4ms	32ms	1	0
8ms	64ms	1	1

Clock count	D4	D3	D2	D1	D0
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	0	1	1	0	1
15	0	1	1	1	0
16	0	1	1	1	1
17	1	0	0	0	0
18	1	0	0	0	1
19	1	0	0	1	0
20	1	0	0	1	1
21	1	0	1	0	0
22	1	0	1	0	1
23	1	0	1	1	0
24	1	0	1	1	1
25	1	1	0	0	0
26	1	1	0	0	1
27	1	1	0	1	0
28	1	1	0	1	1
29	1	1	1	0	0
30	1	1	1	0	1
31	1	1	1	1	0
32	1	1	1	1	1

Output time of 1 section is calculated in the following expression.

[Output time of 1 section] = [Clock period] × [Clock count]

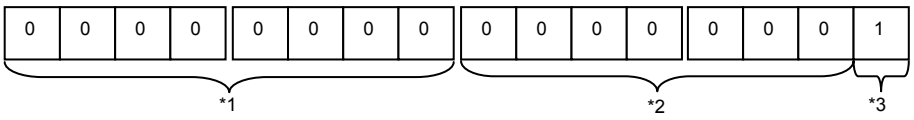
Output time of 1 section	Symbol	Min	Max
Normal drive waveform	T(*)	1ms	256ms
Refresh drive waveform	TR(*)	8ms	2048ms

The normal drive waveform consists of 12 sections.

The refresh drive waveform consists of 4 sections.

6-2-4. Image Data

e.g. (0001h) : Image data setting of the segment output SEG0



*1) Address (8bits)
*2) Invalid data (7bits)
*3) Image data (1bit)

e.g. Black

Image data	D0
White	0
Black	1

6-2-5. Waveform Parameter List

A. Normal Drive Waveform Parameter List

Waveform Name		Waveform Parameter	S(0)	S(1)	S(2)	S(3)	S(4)	S(5)	S(6)	S(7)	S(8)	S(9)	S(10)	S(11)
W0	(White→ White)	Output Level	L00	L01	L02	L03	L04	L05	L06	L07	L08	L09	L0A	L0B
W1	(White→ Black)	Output Level	L10	L11	L12	L13	L14	L15	L16	L17	L18	L19	L1A	L1B
W2	(Black→ White)	Output Level	L20	L21	L22	L23	L24	L25	L26	L27	L28	L29	L2A	L2B
W3	(Black→ Black)	Output Level	L30	L31	L32	L33	L34	L35	L36	L37	L38	L39	L3A	L3B
Common		Output Time	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	TA	TB

(Parameter default setting value)

Waveform Name		Waveform Parameter	S(0)	S(1)	S(2)	S(3)	S(4)	S(5)	S(6)	S(7)	S(8)	S(9)	S(10)	S(11)
W0	(White→ White)	Output Level	+15V	-15V	-15V	0V	0V	0V	0V	0V	0V	0V	0V	0V
W1	(White→ Black)	Output Level	-15V	+15V	+15V	+15V	+15V	+15V	+15V	+15V	0V	0V	0V	0V
W2	(Black→ White)	Output Level	+15V	-15V	-15V	-15V	-15V	-15V	-15V	-15V	0V	0V	0V	0V
W3	(Black→ Black)	Output Level	-15V	+15V	+15V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Common		Clock Period	1ms	1ms	1ms	1ms	1ms	1ms	1ms	1ms	1ms	1ms	1ms	1ms
		Clock Count	6	15	15	30	30	30	30	30	2	2	2	2

B. Refresh Drive Waveform Parameter List

Waveform Name	Waveform Parameter	SR(0)	SR(1)	SR(2)	SR(3)
WR	Output Level	LR0	LR1	LR2	LR3
	Output Time	TR0	TR1	TR2	TR3

(Parameter default setting value)

Waveform Name	Waveform Parameter	SR(0)	SR(1)	SR(2)	SR(3)
WR	Output Level	+15V	+15V	-15V	-15V
	Clock Period	8ms	8ms	8ms	8ms
	Clock Count	8	8	8	8

Note: Parameter Name
XYZ / XZ
X · · · L: Output level
T: Output time
Y · · · 0 to 3: Normal drive
R: Refresh drive
Z · · · Section number

6-3. Mode selection for control of charge-pump and oscillator

Control mode of charge-pump and oscillator is selected by the following.

- Automatic charge-pump mode
- Manual charge-pump mode

6-3-1. Automatic Charge-pump Mode

Automatic charge-pump mode automatically controls stopping from operating charge-pump and oscillator.
Charge-pump and oscillator stop while waveform output standby period. Automatic charge-pump mode is low power than manual charge-pump mode, though charge-pump takes time to start.

<Flow of operation>
Charge-pump and oscillator start operating with START Flag =1. Waveform is output automatically with finishing of charge-pump rising period. Charge-pump and oscillator stop automatically after finishing of waveform output period, and START Flag is automatically canceled.
Charge-pump and oscillator start operating with HVON Flag =1. Charge-pump and oscillator stop automatically after charge-pump rising period, and HVON Flag is automatically canceled.

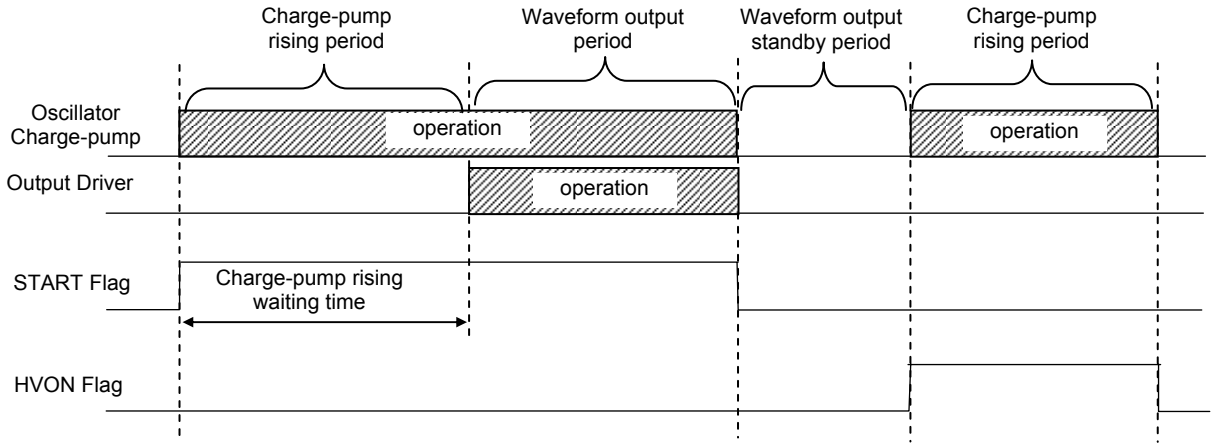


Fig.9. Flow of automatic charge-pump mode

6-3-2. Manual Charge-pump Mode

Manual charge-pump mode automatically controls stopping from operating charge-pump and oscillator.
Charge-pump and oscillator are active while waveform output standby period. Manual charge-pump mode is high power than automatic charge-pump mode, though charge-pump takes no time to start.

<Flow of operation>
Charge-pump and oscillator start operating with HVON Flag =1. The state shifts to waveform output standby period with finishing of charge-pump rising period. While waveform output standby period, waveform output is started with START Flag =1, and START Flag is automatically canceled after finishing of waveform output period. Charge-pump and oscillator stop when HVON Flag is canceled.

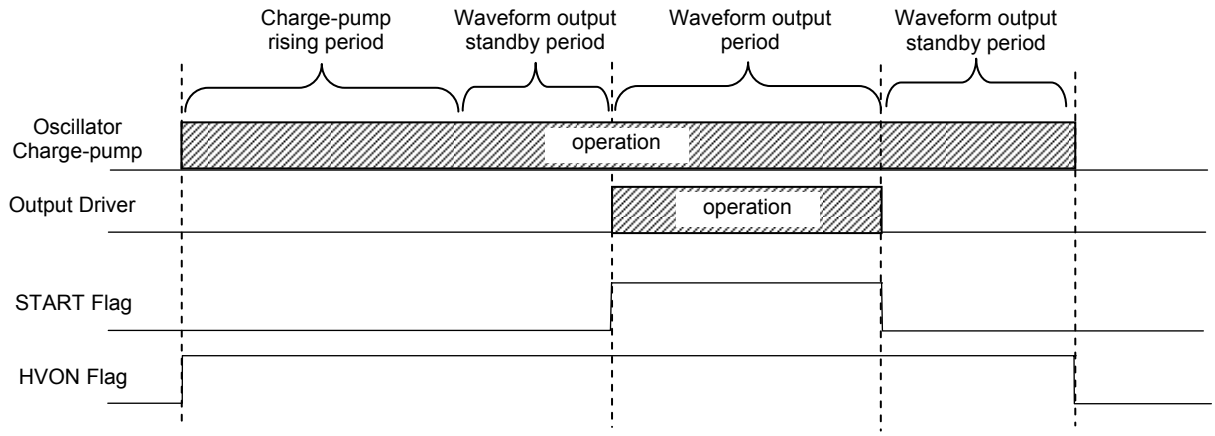


Fig.10. Flow of manual charge-pump mode

6-4. Automatic Switching Function of Charge-pump Frequency

This device can set charge-pump frequency of each state to reduce consumption. When a state changes, charge-pump frequency is changed automatically. Please set charge-pump frequency by each load.

Charge-pump rising period	⇒ 32kHz
Waveform output standby period	⇒ Select from 1kHz, 2kHz, 4kHz, 8kHz, 16kHz, 32kHz
Waveform output period	⇒ Select from 4kHz, 8kHz, 16kHz, 32kHz

6-5. Setting Function of Charge-pump References Voltage

This device can set charge-pump reference voltage to reduce consumption by the use range of the power supply voltage.
When VDD2 is more over 2.7V, we recommend setting 2.5V to reference voltage.

Charge-pump reference voltage 1.25V

VDD2 active range : 1.8V to 3.6V
+/-15V are generated from 1.25V multiplied by 12.

Charge-pump reference voltage 2.50V

VDD2 active range : 2.7V to 3.6V
+/-15V are generated from 2.5V multiplied by 6.

6-6. Automatic Discharge Function and the Change of Image Function after Power Off

After VDD power off, when stored electric charge is left to the external capacitor, the image may be changed. Therefore this device is equipped with a function (cf. 10-3) to discharge stored electric charge. When stored electric charge is not discharged, discharge is performed automatically if the following condition is met.

Condition for automatic discharge

- VOUT0 ≥ 2.0V, VOUT1 ≥ 4.0V, VOUT2 ≥ 10V, VOUT3 ≤ -10V
- Charge-pump stop
- VDD voltage falls to 0.3V within one second

In addition, you can display full screen black by automatic discharge in the following setting and condition.

Setting and condition of full screen black image

- Full screen black image setting of automatic discharge (control register 2: OFFBLK = 1)
- The voltage level of RESET keeps VDD
- VOUT0 ≥ 2.0V, VOUT1 ≥ 4.0V, VOUT2 ≥ 10V, VOUT3 ≤ -10V
- Charge-pump stop
- VDD voltage falls to 0.3V within one second

Notice : During setting full screen black image function, all segment pin output VOUT2.
VOUT2 output continues until to VDD and VOUT1 raise to some extent, or VOUT2 voltage is discharged naturally. When the panel shows abnormality by applying it for the long time, please do not use it.

7. Register

7-1. Interface Register List

Address	Data								
HEX	D7	D6	D5	D4	D3	D2	D1	D0	Contents
00h	-	-	-	-	-	-	-	SEG0 (0)	Image Data SEG0
(to)	-	-	-	-	-	-	-	SEG* (0)	Image Data SEG1 to 126
7Fh	-	-	-	-	-	-	-	SEG127 (0)	Image Data SEG127
80h	-	-	-	-	-	-	L00 (0)	 (1)	Output Level W0 - S(0)
81h	-	-	-	-	-	-	L01 (1)	 (0)	Output Level W0 - S(1)
82h	-	-	-	-	-	-	L02 (1)	 (0)	Output Level W0 - S(2)
83h	-	-	-	-	-	-	L03 (0)	 (0)	Output Level W0 - S(3)
84h	-	-	-	-	-	-	L04 (0)	 (0)	Output Level W0 - S(4)
85h	-	-	-	-	-	-	L05 (0)	 (0)	Output Level W0 - S(5)
86h	-	-	-	-	-	-	L06 (0)	 (0)	Output Level W0 - S(6)
87h	-	-	-	-	-	-	L07 (0)	 (0)	Output Level W0 - S(7)
88h	-	-	-	-	-	-	L08 (0)	 (0)	Output Level W0 - S(8)
89h	-	-	-	-	-	-	L09 (0)	 (0)	Output Level W0 - S(9)
8Ah	-	-	-	-	-	-	L0A (0)	 (0)	Output Level W0 - S(A)
8Bh	-	-	-	-	-	-	L0B (0)	 (0)	Output Level W0 - S(B)
90h	-	-	-	-	-	-	L10 (1)	 (0)	Output Level W1 - S(0)
91h	-	-	-	-	-	-	L11 (0)	 (1)	Output Level W1 - S(1)
92h	-	-	-	-	-	-	L12 (0)	 (1)	Output Level W1 - S(2)
93h	-	-	-	-	-	-	L13 (0)	 (1)	Output Level W1 - S(3)
94h	-	-	-	-	-	-	L14 (0)	 (1)	Output Level W1 - S(4)
95h	-	-	-	-	-	-	L15 (0)	 (1)	Output Level W1 - S(5)
96h	-	-	-	-	-	-	L16 (0)	 (1)	Output Level W1 - S(6)
97h	-	-	-	-	-	-	L17 (0)	 (1)	Output Level W1 - S(7)
98h	-	-	-	-	-	-	L18 (0)	 (0)	Output Level W1 - S(8)

Address	Data								
HEX	D7	D6	D5	D4	D3	D2	D1	D0	Contents
99h	-	-	-	-	-	-	L19		Output Level
							(0)	(0)	W1 - S(9)
9Ah	-	-	-	-	-	-	L1A		Output Level
							(0)	(0)	W1 - S(A)
9Bh	-	-	-	-	-	-	L1B		Output Level
							(0)	(0)	W1 - S(B)
A0h	-	-	-	-	-	-	L20		Output Level
							(0)	(1)	W2 - S(0)
A1h	-	-	-	-	-	-	L21		Output Level
							(1)	(0)	W2 - S(1)
A2h	-	-	-	-	-	-	L22		Output Level
							(1)	(0)	W2 - S(2)
A3h	-	-	-	-	-	-	L23		Output Level
							(1)	(0)	W2 - S(3)
A4h	-	-	-	-	-	-	L24		Output Level
							(1)	(0)	W2 - S(4)
A5h	-	-	-	-	-	-	L25		Output Level
							(1)	(0)	W2 - S(5)
A6h	-	-	-	-	-	-	L26		Output Level
							(1)	(0)	W2 - S(6)
A7h	-	-	-	-	-	-	L27		Output Level
							(1)	(0)	W2 - S(7)
A8h	-	-	-	-	-	-	L28		Output Level
							(0)	(0)	W2 - S(8)
A9h	-	-	-	-	-	-	L29		Output Level
							(0)	(0)	W2 - S(9)
AAh	-	-	-	-	-	-	L3A		Output Level
							(0)	(0)	W2 - S(A)
ABh	-	-	-	-	-	-	L2B		Output Level
							(0)	(0)	W2 - S(B)
B0h	-	-	-	-	-	-	L30		Output Level
							(1)	(0)	W3 - S(0)
B1h	-	-	-	-	-	-	L31		Output Level
							(0)	(1)	W3 - S(1)
B2h	-	-	-	-	-	-	L32		Output Level
							(0)	(1)	W3 - S(2)
B3h	-	-	-	-	-	-	L33		Output Level
							(0)	(0)	W3 - S(3)
B4h	-	-	-	-	-	-	L34		Output Level
							(0)	(0)	W3 - S(4)
B5h	-	-	-	-	-	-	L35		Output Level
							(0)	(0)	W3 - S(5)
B6h	-	-	-	-	-	-	L36		Output Level
							(0)	(0)	W3 - S(6)
B7h	-	-	-	-	-	-	L37		Output Level
							(0)	(0)	W3 - S(7)
B8h	-	-	-	-	-	-	L38		Output Level
							(0)	(0)	W3 - S(8)
B9h	-	-	-	-	-	-	L39		Output Level
							(0)	(0)	W3 - S(9)

Address	Data								
HEX	D7	D6	D5	D4	D3	D2	D1	D0	Contents
BAh	-	-	-	-	-	-	L3A		Output Level
							(0)	(0)	W3 - S(A)
BBh	-	-	-	-	-	-	L3B		Output Level
							(0)	(0)	W3 - S(B)
C0h	-	T0							Output Time
		(0)	(0)	(0)	(0)	(1)	(0)	(1)	W0 to W3 - S(0)
C1h	-	T1							Output Time
		(0)	(0)	(0)	(1)	(1)	(1)	(0)	W0 to W3 - S(1)
C2h	-	T2							Output Time
		(0)	(0)	(0)	(1)	(1)	(1)	(0)	W0 to W3 - S(2)
C3h	-	T3							Output Time
		(0)	(0)	(1)	(1)	(1)	(0)	(1)	W0 to W3 - S(3)
C4h	-	T4							Output Time
		(0)	(0)	(1)	(1)	(1)	(0)	(1)	W0 to W3 - S(4)
C5h	-	T5							Output Time
		(0)	(0)	(1)	(1)	(1)	(0)	(1)	W0 to W3 - S(5)
C6h	-	T6							Output Time
		(0)	(0)	(1)	(1)	(1)	(0)	(1)	W0 to W3 - S(6)
C7h	-	T7							Output Time
		(0)	(0)	(1)	(1)	(1)	(0)	(1)	W0 to W3 - S(7)
C8h	-	T8							Output Time
		(0)	(0)	(0)	(0)	(0)	(0)	(1)	W0 to W3 - S(8)
C9h	-	T9							Output Time
		(0)	(0)	(0)	(0)	(0)	(0)	(1)	W0 to W3 - S(9)
CAh	-	TA							Output Time
		(0)	(0)	(0)	(0)	(0)	(0)	(1)	W0 to W3 - S(A)
CBh	-	TB							Output Time
		(0)	(0)	(0)	(0)	(0)	(0)	(1)	W0 to W3 - S(B)
D0h	-	-	-	-	-	-	LR0		Output Level
							(0)	(1)	WR - S(0)
D1h	-	-	-	-	-	-	LR1		Output Level
							(0)	(1)	WR - S(1)
D2h	-	-	-	-	-	-	LR2		Output Level
							(1)	(0)	WR - S(2)
D3h	-	-	-	-	-	-	LR3		Output Level
							(1)	(0)	WR - S(3)
E0h	-	TR0							Output Time
		(0)	(0)	(0)	(0)	(1)	(1)	(1)	WR - S(0)
E1h	-	TR1							Output Time
		(0)	(0)	(0)	(0)	(1)	(1)	(1)	WR - S(1)
E2h	-	TR2							Output Time
		(0)	(0)	(0)	(0)	(1)	(1)	(1)	WR - S(2)
E3h	-	TR3							Output Time
		(0)	(0)	(0)	(0)	(1)	(1)	(1)	WR - S(3)

Address	Data								
HEX	D7	D6	D5	D4	D3	D2	D1	D0	Contents
F0h	CP_F21	CP_F20	CP_F12	CP_F11	CP_F10	CP_T2	CP_T1	CP_T0	Control Register 1
	(1)	(1)	(0)	(0)	(0)	(1)	(1)	(0)	
F1h	-	-	-	OFFBLK	DISCON	VREGSEL	HVON	MODSEL	Control Register 2
				(0)	(0)	(0)	(0)	(0)	
F2h	-	-	-	-	-	DB	LE	RFSH	Control Register 3
						(0)	(0)	(0)	
F3h	-	-	-	-	-	-	STERR	START	Control Register 4
							(1)	(0)	

7-2. Control Register

(1) Control Register 1 (Charge-pump Control)

Address : F0

D7	D6	D5	D4	D3	D2	D1	D0
CP_F21	CP_F20	CP_F12	CP_F11	CP_F10	CP_T2	CP_T1	CP_T0
(1)	(1)	(0)	(0)	(0)	(1)	(1)	(0)

( ) default

1) CP_T0 to T2 ··· Charge-pump rising period

CP_T2	CP_T1	CP_T0	Charge-pump rising period	Charge-pump voltage generation order	Use condition	
0	0	0	2ms	VOUT0 to VOUT3 all at once	VOUT2 ≥ +12V VOUT3 ≤ -12V	
0	0	1	4ms			
0	1	0	8ms			
0	1	1	16ms			
1	0	0	16ms	VOUT0 to VOUT3 in turn	-	
1	0	1	32ms		-	
1	1	0	64ms		-	(default)
1	1	1	128ms		-	

Notice : Charge-pump rising period can shorten by capacity value connected outside, electric charge stored to capacitor, VDD2 power supply voltage, and charge-pump reference voltage. But, please evaluate the module when you change a default value of charge-pump rising period or recommended capacity value. In addition, please confirm that charge-pump rising period is enough.
When conditions of use are not met, and select “all at once” of charge-pump voltage generation, this device may be destroyed.

2) CP_F10 to F12 ··· Charge-pump frequency of waveform output standby period

CP_F12	CP_F11	CP_F10	Frequency	
0	0	0	1kHz	(default)
0	0	1	2kHz	
0	1	0	Stop *1	*1) Cf. 10 - 2
0	1	1	Stop *1	
1	0	0	4kHz	
1	0	1	8kHz	
1	1	0	16kHz	
1	1	1	32kHz	

3) CP_F20 to F21 ··· Charge-pump frequency of waveform output period

CP_F21	CP_F20	Frequency	
0	0	4kHz	
0	1	8kHz	
1	0	16kHz	
1	1	32kHz	(default)

(2) Control Register 2 (Operating Control)

Address : F1

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	OFFBLK	DISCON	VREGSEL	HVON	MODSEL
*	*	*	(0)	(0)	(0)	(0)	(0)

*: Non use ( ) default

1) MODSEL ··· Control mode selection of charge-pump and oscillator
   0 : Automatic charge-pump mode.
   This device sets START Flag or HVON Flag, and automatically controls stopping from operating.
   1 : Manual charge-pump mode.
   This device sets HVON Flag, and manually controls stopping from operating.

2) HVON ··· Operation of charge-pump and oscillator
   In automatic charge-pump mode, HVON Flag is automatically canceled after charge-pump rising period, and charge-pump and oscillator stop.
   In manual charge-pump mode, charge-pump and oscillator is active until canceled of HVON Flag.
   0 : Stop
   1 : Operate

3) VREGSEL ··· Selection of charge-pump reference voltage
   0 : 1.25V Condition of use VDD2 ≥ 1.8V
   1 : 2.50V Condition of use VDD2 ≥ 2.7V

4) DISCON ··· Operation setting of discharge circuit
   0 : Stop
   1 : Operate

5) OFFBLK ··· Selection of image when operated automatic discharge function.
   0 : Panel maintains current image.
   1 : Panel displays black.
   Note: Turn off power supply as setting of RESET = 1 when want to be black.

(3) Control Register 3 (Image Control)

Address : F2

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	*	DB	LE	RFSH
*	*	*	*	*	(0)	(0)	(0)

*: Non use ( ) default

1) RFSH ··· Waveform mode selection
   0 : Normal drive
   1 : Refresh drive

2) LE ··· Data latch
   This signal is used when want to latch (shift) only image data without changing image.
   0 : Data do not shift.
   1 : Data shift.
   Latch 1 (New image data) ⇒ Latch 2 (Old image data)
   Image data input buffer ⇒ Latch 1 (New image data)
   LE Flag is automatically canceled with finish of latch.

3) DB ··· Image data inversion
   0 : Non-inversion
   1 : Inversion

(4) Control Register 4 (Waveform Generation and RESET Detection)

Address : F3

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	*	*	STERR	START
*	*	*	*	*	*	(1)	(0)

*: Non use ( ) default

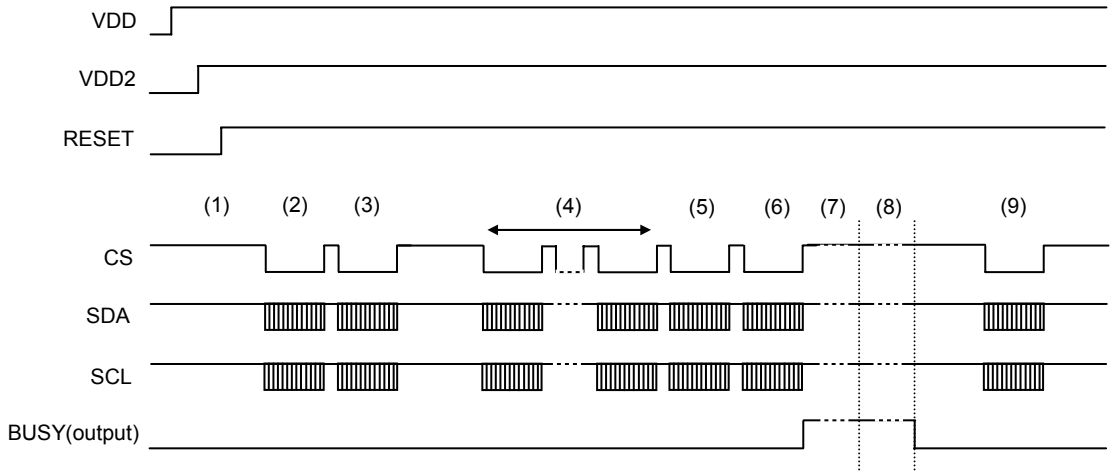
1) START ··· Waveform output signal
   0 : Waveform is not output. Data do not shift.
   1 : Waveform is output. Data shift.
   START Flag is automatically canceled with finish of waveform output.

2) STERR ··· RESET detection signal
   You can detect reset outbreak by set “0” after RESET = H, and reading a register or monitoring DAOUT.
   0 : No outbreak of reset.
   1 : Outbreak of reset.

8. Timing Chart (Recommended Sequence)

8-1. Automatic Charge-pump Mode

8-1-1. Initialization

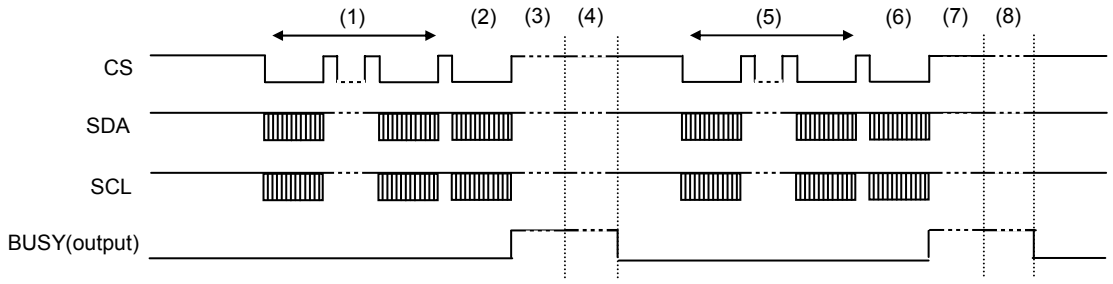


< sequence >

(1) Set RESET pin high
(2) Charge-pump frequency setting (Control register 1 = C6h)
(3) Operating control setting (Control register 2 = 00h)
(4) Waveform parameter setting
(5) RFSH Flag setting (Control register 3 = 01h)
(6) START Flag setting (Control register 4 = 01h)
(7) Waiting time (Charge-pump start ⇒ voltage be stable)
(8) Drive period (Waveform output) *Charge-pump and Oscillator stop with BUSY = Low.
(9) RFSH Flag cancel (Control register 3 = 00h)

You may set waveform parameter (4) and RFSH Flag (5) during waiting time (7).
Waiting time (7) is set at charge-pump frequency (2).

8-1-2. Sequential Image Change



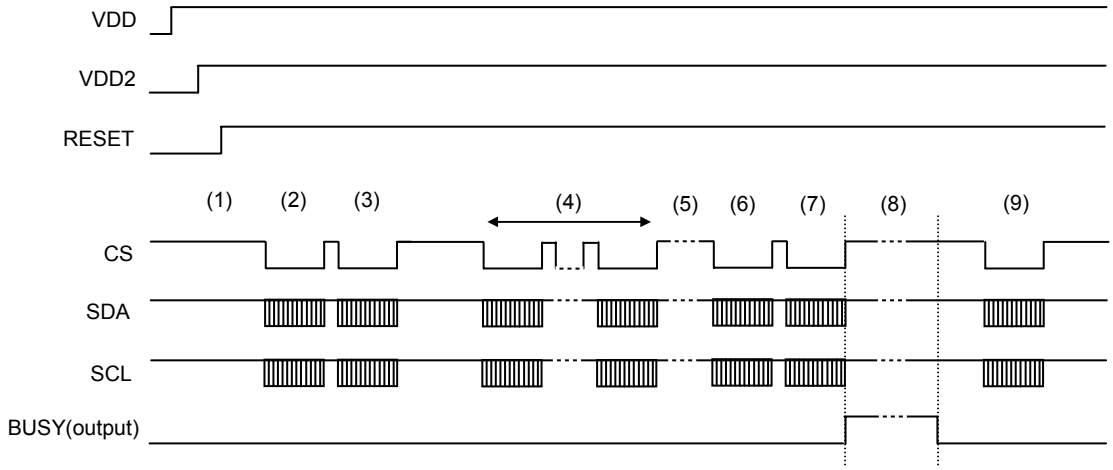
< sequence >

(1) The first image data transmission
(2) START Flag setting (Control register 4 = 01h)
(3) Waiting time (Charge-pump start ⇒ voltage be stable)
(4) Drive period (Waveform output) * Charge-pump and Oscillator stop with BUSY = Low.
(5) The second image data transmission
(6) START Flag setting (Control register 4 = 01h)
(7) Waiting time (Charge-pump start ⇒ voltage be stable)
(8) Drive period (Waveform output) *Oscillator and Charge-pump stop with BUSY = Low.

You may set the second image data transmission (5) during waiting (3) and drive period (4). But "control register" and "waveform parameter" must not update.
Please set the setting of STRAT Flag (6) at the time of BUSY = Low of first image or STRAT Flag = Low.

8-2. Manual Charge-pump Mode

8-2-1. Initialization

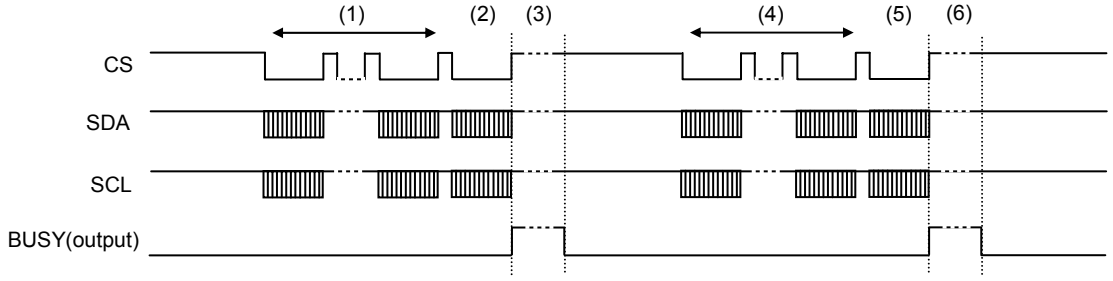


< sequence >

(1) Set RESET pin high
(2) Charge-pump frequency setting (Control register 1 = C6h)
(3) Operating control setting and Charge-pump start (Control register 2 = 03h)
(4) Waveform parameter setting
(5) Waiting time (Voltage be stable)
(6) RFSH Flag setting (Control register 3 = 01h)
(7) START Flag setting (Control register 4 = 01h)
(8) Drive period (Waveform output)
(9) RFSH Flag cancel (Control register 3 = 00h)

When START Flag (7) is set in waiting time (5), sequence waits for the end of waiting time (5) and shifts to drive period (8).

8-2-2. Sequential Image Change



< sequence >

(1) The first image data transmission
(2) START Flag setting (Control register 4 = 01h)
(3) Drive period (Waveform output)
(4) The second image data transmission
(5) START Flag setting (Control register 4 = 01h)
(6) Drive period (Waveform output)

You may set the second image data transmission (4) during drive period (3). But “control register” and “waveform parameter” must not update.

Please set the setting of STRAT Flag (5) at the time of BUSY = Low of first image or STRAT Flag = Low.

9. PAD Assignment

9-1. PAD Assignment

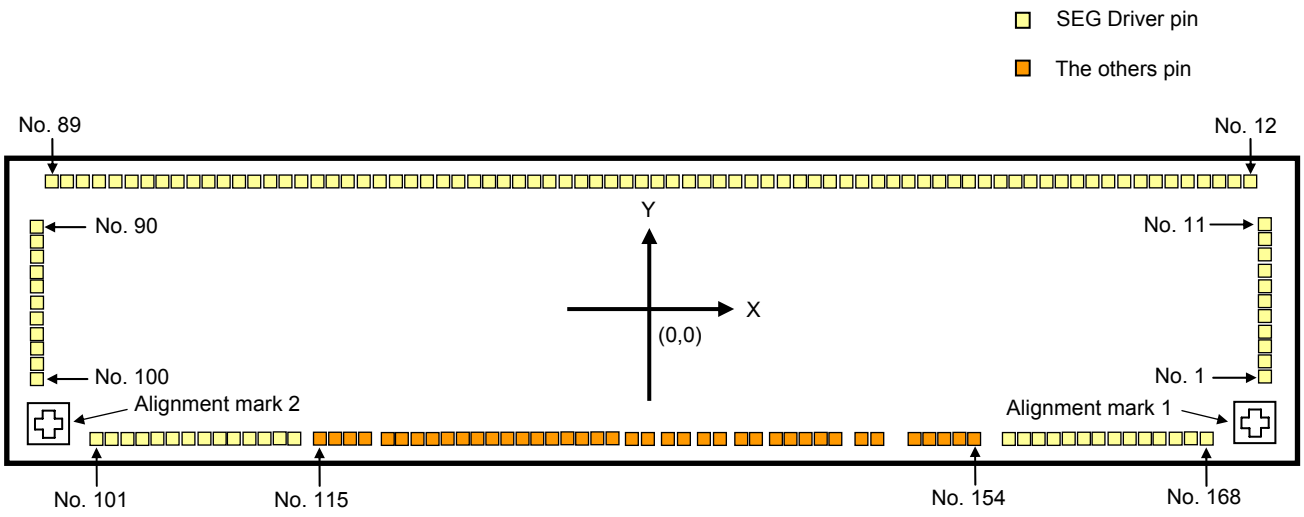


Fig.11. PAD Assignment

Note: 1. Chip size (before dicing) X = 6.55 [mm] Y = 1.43 [mm] S = 9.37 [mm^2]
2. Scribe line width 80 [µm]
3. Chip thickness 400±30 [µm]

Bump shape (Bump height = 17±3 [µm])

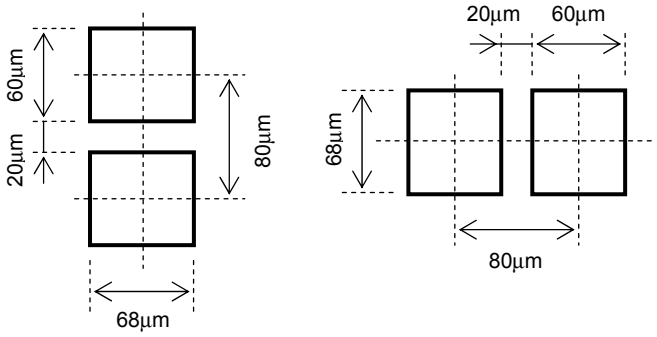


Fig.12. Gold bump shape

Alignment mark (No bump)

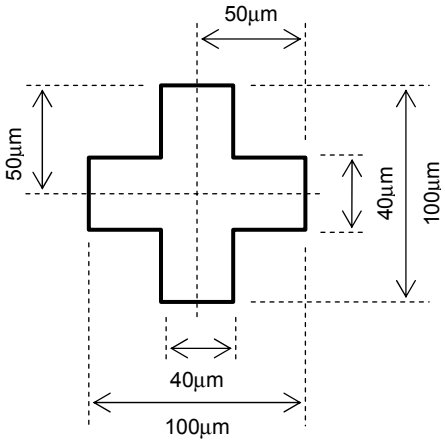


Fig.13. Alignment mark shape

9-2. PAD Coordinates

PAD No.	PAD Name	X coordinate [μm]	Y coordinate [μm]
1	SEG14	3167.00	-383.00
2	SEG15	3167.00	-303.00
3	SEG16	3167.00	-223.00
4	SEG17	3167.00	-143.00
5	SEG18	3167.00	-63.00
6	SEG19	3167.00	17.00
7	SEG20	3167.00	97.00
8	SEG21	3167.00	177.00
9	SEG22	3167.00	257.00
10	SEG23	3167.00	337.00
11	SEG24	3167.00	417.00
12	SEG25	3080.00	608.00
13	SEG26	3000.00	608.00
14	SEG27	2920.00	608.00
15	SEG28	2840.00	608.00
16	SEG29	2760.00	608.00
17	SEG30	2680.00	608.00
18	SEG31	2600.00	608.00
19	SEG32	2520.00	608.00
20	SEG33	2440.00	608.00
21	SEG34	2360.00	608.00
22	SEG35	2280.00	608.00
23	SEG36	2200.00	608.00
24	SEG37	2120.00	608.00
25	SEG38	2040.00	608.00
26	SEG39	1960.00	608.00
27	SEG40	1880.00	608.00
28	SEG41	1800.00	608.00
29	SEG42	1720.00	608.00
30	SEG43	1640.00	608.00
31	SEG44	1560.00	608.00
32	SEG45	1480.00	608.00
33	SEG46	1400.00	608.00
34	SEG47	1320.00	608.00
35	SEG48	1240.00	608.00
36	SEG49	1160.00	608.00
37	SEG50	1080.00	608.00
38	SEG51	1000.00	608.00
39	SEG52	920.00	608.00
40	SEG53	840.00	608.00
41	SEG54	760.00	608.00
42	SEG55	680.00	608.00
43	SEG56	600.00	608.00
44	SEG57	520.00	608.00
45	SEG58	440.00	608.00
46	SEG59	360.00	608.00
47	SEG60	280.00	608.00
48	SEG61	200.00	608.00
49	SEG62	120.00	608.00
50	SEG63	40.00	608.00

PAD No.	PAD Name	X coordinate [μm]	Y coordinate [μm]
51	SEG64	-40.00	608.00
52	SEG65	-120.00	608.00
53	SEG66	-200.00	608.00
54	SEG67	-280.00	608.00
55	SEG68	-360.00	608.00
56	SEG69	-440.00	608.00
57	SEG70	-520.00	608.00
58	SEG71	-600.00	608.00
59	SEG72	-680.00	608.00
60	SEG73	-760.00	608.00
61	SEG74	-840.00	608.00
62	SEG75	-920.00	608.00
63	SEG76	-1000.00	608.00
64	SEG77	-1080.00	608.00
65	SEG78	-1160.00	608.00
66	SEG79	-1240.00	608.00
67	SEG80	-1320.00	608.00
68	SEG81	-1400.00	608.00
69	SEG82	-1480.00	608.00
70	SEG83	-1560.00	608.00
71	SEG84	-1640.00	608.00
72	SEG85	-1720.00	608.00
73	SEG86	-1800.00	608.00
74	SEG87	-1880.00	608.00
75	SEG88	-1960.00	608.00
76	SEG89	-2040.00	608.00
77	SEG90	-2120.00	608.00
78	SEG91	-2200.00	608.00
79	SEG92	-2280.00	608.00
80	SEG93	-2360.00	608.00
81	SEG94	-2440.00	608.00
82	SEG95	-2520.00	608.00
83	SEG96	-2600.00	608.00
84	SEG97	-2680.00	608.00
85	SEG98	-2760.00	608.00
86	SEG99	-2840.00	608.00
87	SEG100	-2920.00	608.00
88	SEG101	-3000.00	608.00
89	SEG102	-3080.00	608.00
90	SEG103	-3167.00	417.00
91	SEG104	-3167.00	337.00
92	SEG105	-3167.00	257.00
93	SEG106	-3167.00	177.00
94	SEG107	-3167.00	97.00
95	SEG108	-3167.00	17.00
96	SEG109	-3167.00	-63.00
97	SEG110	-3167.00	-143.00
98	SEG111	-3167.00	-223.00
99	SEG112	-3167.00	-303.00
100	SEG113	-3167.00	-383.00

PAD No.	PAD Name	X coordinate [μm]	Y coordinate [μm]
101	SEG114	-2972.00	-607.00
102	SEG115	-2892.00	-607.00
103	SEG116	-2812.00	-607.00
104	SEG117	-2732.00	-607.00
105	SEG118	-2652.00	-607.00
106	SEG119	-2572.00	-607.00
107	SEG120	-2492.00	-607.00
108	SEG121	-2412.00	-607.00
109	SEG122	-2332.00	-607.00
110	SEG123	-2252.00	-607.00
111	SEG124	-2172.00	-607.00
112	SEG125	-2092.00	-607.00
113	SEG126	-2012.00	-607.00
114	SEG127	-1932.00	-607.00
115	ZVDD	-1818.00	-607.00
116	ZVDD	-1738.00	-607.00
117	ZVSS	-1658.00	-607.00
118	ZVSS	-1578.00	-607.00
119	TEST	-1472.00	-607.00
120	RESET	-1392.00	-607.00
121	VSS	-1312.00	-607.00
122	ID1	-1232.00	-607.00
123	ID2	-1152.00	-607.00
124	VDD	-1072.00	-607.00
125	IFSEL	-992.00	-607.00
126	VSS	-912.00	-607.00
127	SPIDRW	-832.00	-607.00
128	CS	-752.00	-607.00
129	SDA	-672.00	-607.00
130	SCL	-592.00	-607.00
131	TESTLOUT	-512.00	-607.00
132	TESTAOUT	-432.00	-607.00
133	BUSY	-352.00	-607.00
134	DAOUT	-272.00	-607.00

PAD No.	PAD Name	X coordinate [μm]	Y coordinate [μm]
135	VDD2	-173.25	-607.00
136	C01B	-93.25	-607.00
137	C01A	37.65	-607.00
138	VOUT0	117.65	-607.00
139	C11B	248.55	-607.00
140	C11A	328.55	-607.00
141	VOUT1	441.97	-607.00
142	C21B	521.88	-607.00
143	C22B	649.74	-607.00
144	C21A	735.63	-607.00
145	C21A	815.63	-607.00
146	C22A	902.49	-607.00
147	C22A	982.49	-607.00
148	VOUT2	1137.59	-607.00
149	VOUT2	1217.59	-607.00
150	C31A	1479.48	-607.00
151	C31A	1559.48	-607.00
152	C31B	1639.48	-607.00
153	C31B	1719.48	-607.00
154	VOUT3	1799.48	-607.00
155	SEG0	1932.00	-607.00
156	SEG1	2012.00	-607.00
157	SEG2	2092.00	-607.00
158	SEG3	2172.00	-607.00
159	SEG4	2252.00	-607.00
160	SEG5	2332.00	-607.00
161	SEG6	2412.00	-607.00
162	SEG7	2492.00	-607.00
163	SEG8	2572.00	-607.00
164	SEG9	2652.00	-607.00
165	SEG10	2732.00	-607.00
166	SEG11	2812.00	-607.00
167	SEG12	2892.00	-607.00
168	SEG13	2972.00	-607.00

9-3. Alignment Mark Coordinates

PAD No.	PAD Name	X coordinate [μm]	Y coordinate [μm]
—	MARK1	3126.00	-566.00

Central coordinate of the mark.

PAD No.	PAD Name	X coordinate [μm]	Y coordinate [μm]
—	MARK2	-3126.00	-566.00

Central coordinate of the mark.

10. Instructions

10-1. Recommended Specifications Example of the External Parts

The following shows a recommended specifications example of the external parts.
When charge-pump reference voltage is 2.5V, C01 is unnecessary.

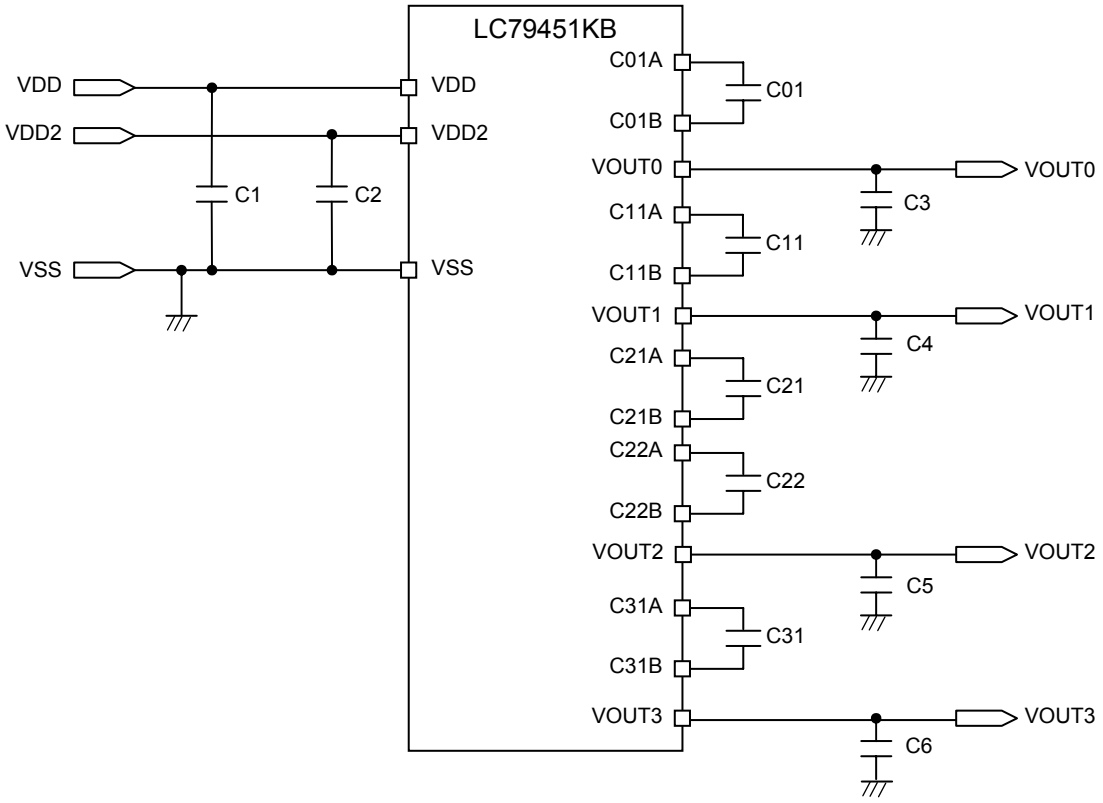


Fig.14. Recommended specifications example of the external part

Symbol	Pin	Voltage	Capacity value	Voltage rating of capacitor	Note
C1	VDD	VDD	1.0μF	6V	-
C2	VDD2	VDD2	1.0μF	6V	-
C3	VOUT0	2.5V	1.0μF	6V	B characteristic
C4	VOUT1	5.0V	1.0μF	6V	B characteristic
C5	VOUT2	15.0V	0.1μF	25V	B characteristic
C6	VOUT3	-15.0V	0.1μF	25V	B characteristic
C01	C01A/B	1.25V	1.0μF	6V	B characteristic
C11	C11A/B	2.5V	1.0μF	6V	B characteristic
C21	C21A/B	5.0V	0.1μF	6V	B characteristic
C22	C22A/B	10.0V	0.1μF	16V	B characteristic
C31	C31A/B	15.0V	0.1μF	25V	B characteristic

Notice : These value are recommendation. “Electrical characteristic” of Cf.5 is the value using the recommendation.
The capacity value, please decide the most suitable value after having evaluated the module.
The external parts are located near this device by wiring as short as possible, because may have an influence of the characteristic drop by parasitic resistance in the pattern wiring.

10-2. Interface Connection Example

The following shows a connection example of I^2C and SPI interface.
The figure omits the capacitor connection of the power supply.

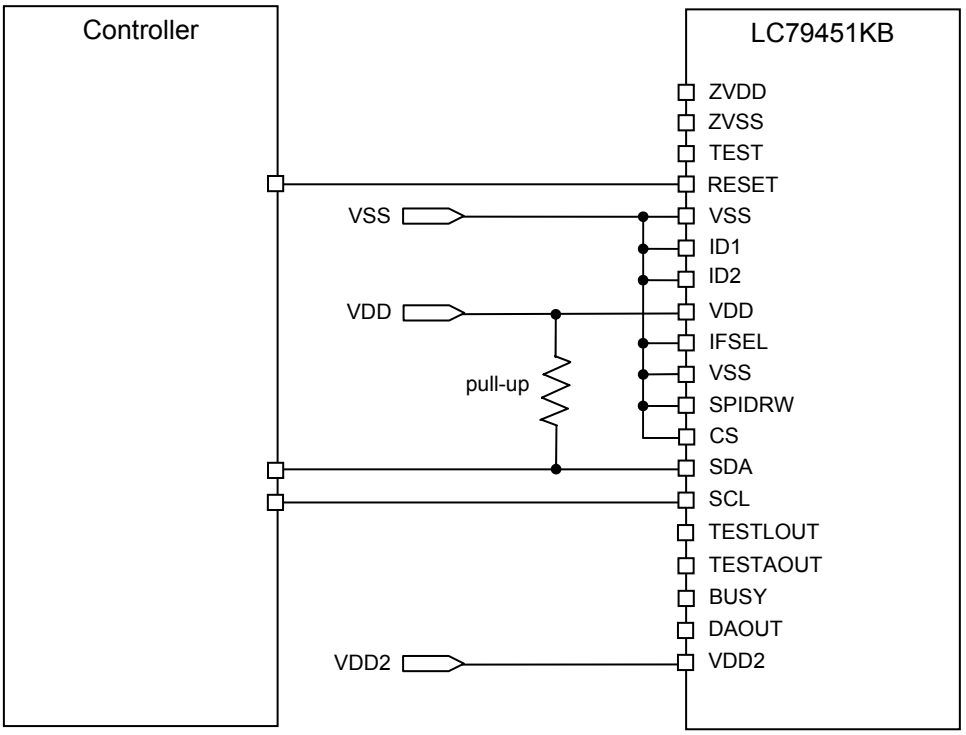


Fig.15. I^2C interface connection example

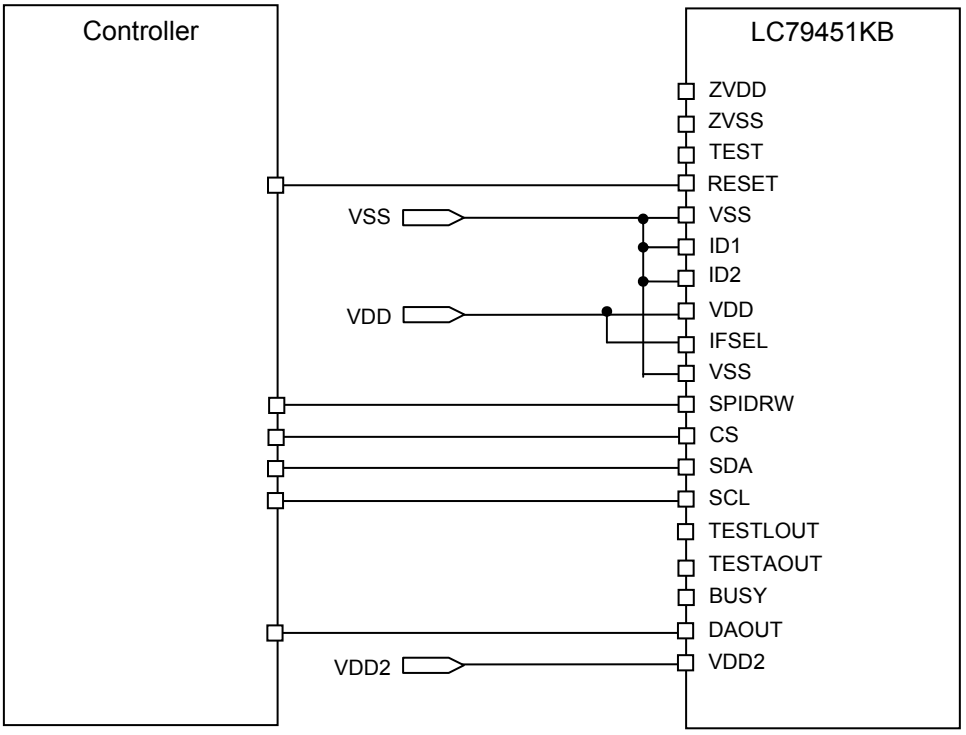


Fig.16. SPI interface connection example

The following shows a connection example of I^2C interface and charge-pump pin, when you use these two devices and share the charge-pump voltage.
The figure omits the capacitor connection of the power supply.
Please set CP_F12: 11 = (0, 1) (control register 1) to the slave side.
Please input START command of control register 4 to slave device just after input to master device.

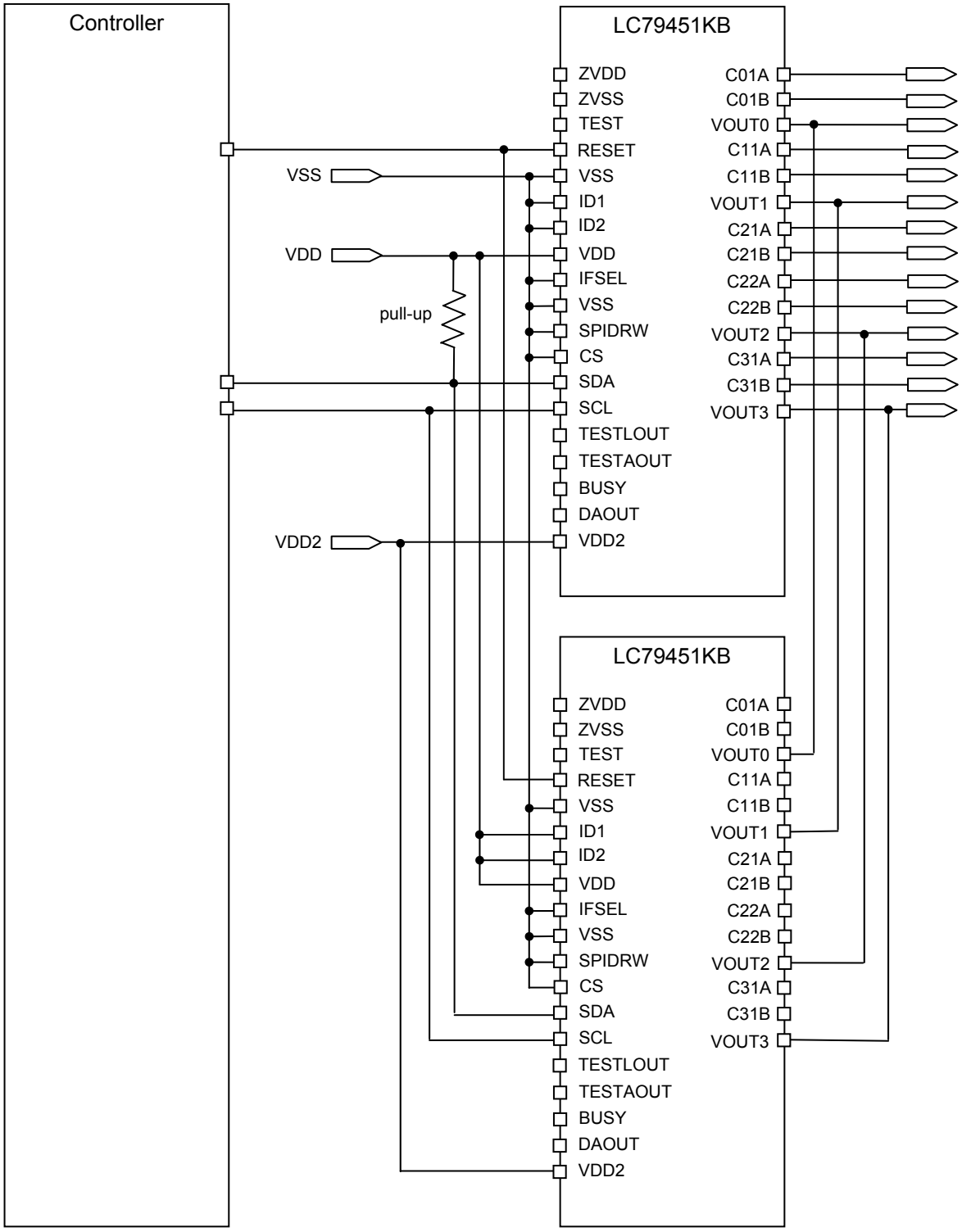


Fig.17. I^2C interface connection example (Joint charge-pump voltage)

Notice : The use example using the plural IC is out of a guarantee.

The following shows a connection example of SPI interface and charge-pump pin, when you use these two devices and share the charge-pump voltage.
The figure omits the capacitor connection of the power supply.
Please set CP_F12: 11 = (0, 1) (control register 1) to the slave side.
Please input START command of control register 4 to slave device at the same time input to master device.

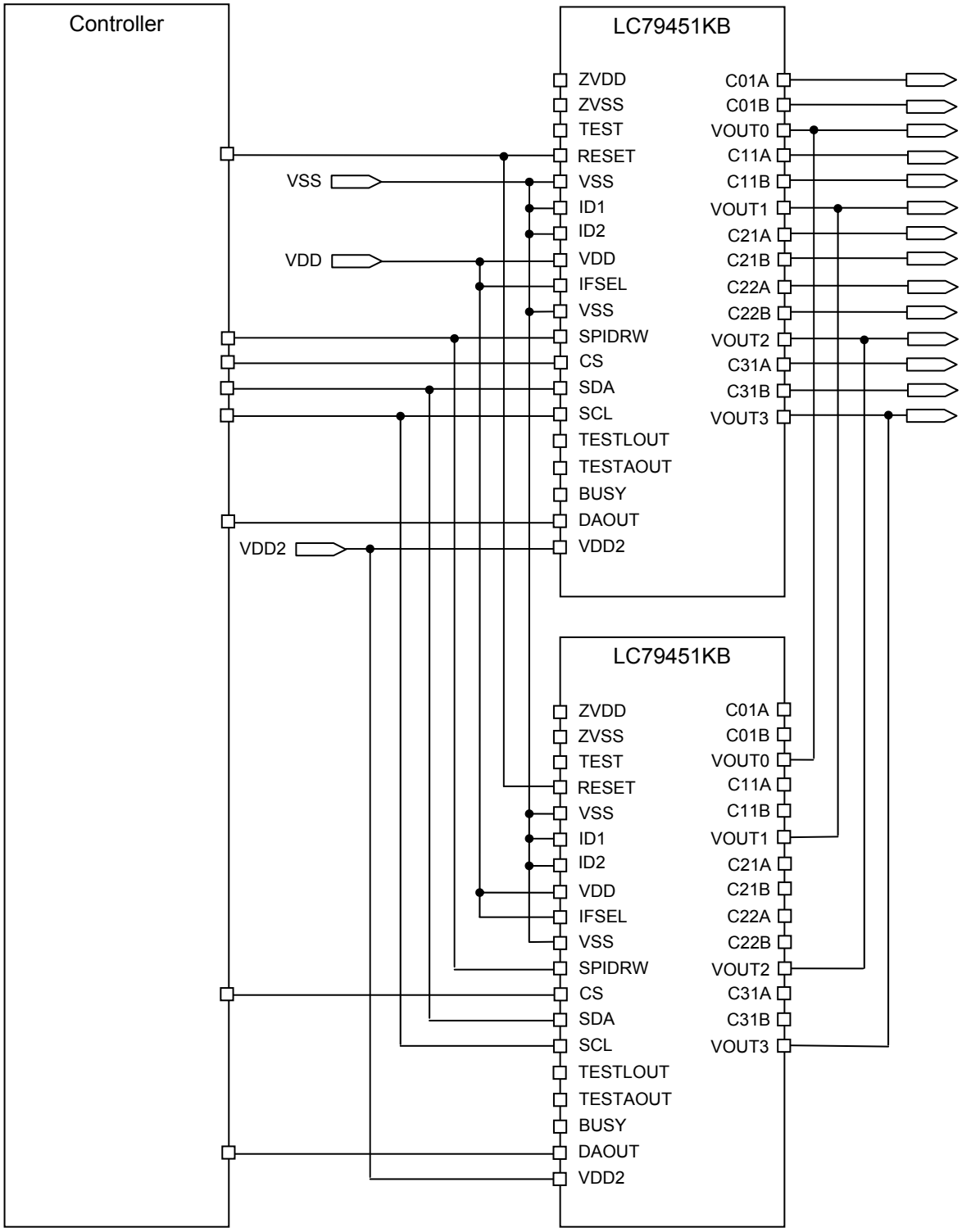


Fig.18. SPI interface connection example (Joint charge-pump voltage)

Notice : The use example using the plural IC is out of a guarantee.

10-3. Power Supply OFF Sequence

When you turn off VDD power supply, the discharge of a stored electric charge is recommended. This is because image may change when an electric charge is left in the external capacitor of VOUT2 and VOUT3.
You can discharge a stored electric charge in the following procedures when you cannot meet a condition of Cf.6-6.

(1) Operate charge-pump if VOUT0 < 2.0V or VOUT1 < 4.0V.
(2) Stop charge-pump.
(3) Operate discharge. (control register 2: DISCON = 1)
(4) Turn off VDD power supply.

You can maintain a discharge state when you turn off VDD power supply during discharge operation as RESET = VDD.

10-4. Parasitic Circuit between Charge-pump Pins and Power Supply Pins

Between charge-pump pins and power supply pins, parasitic diode is connected equivalently to constitute a circuit.

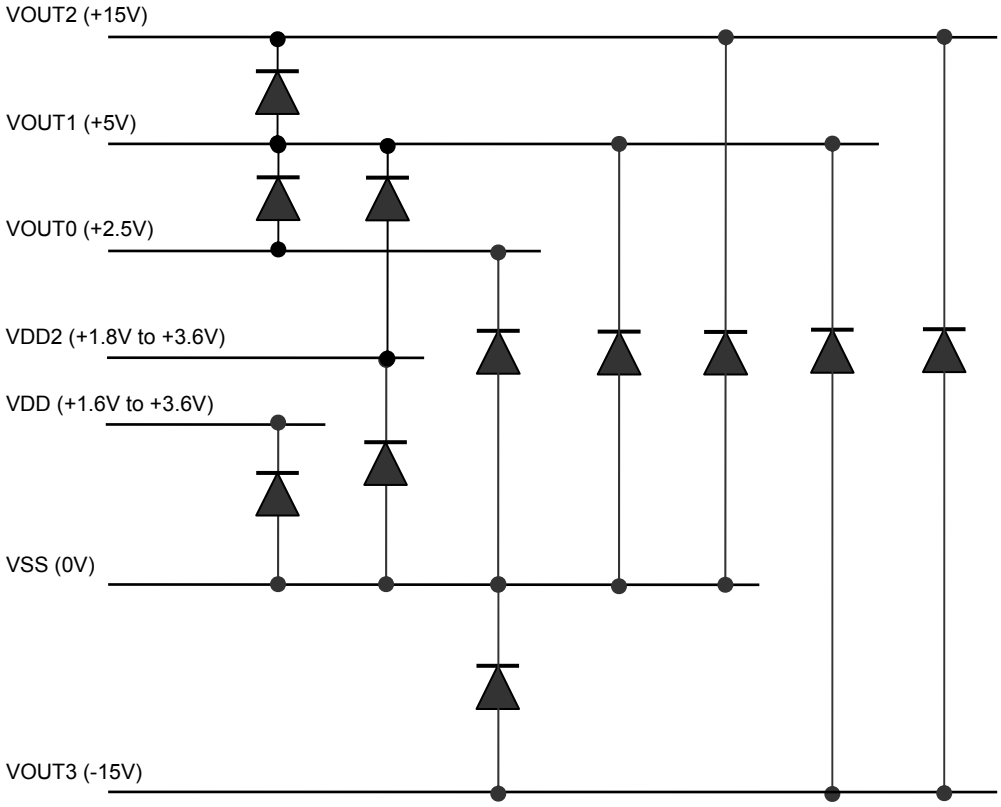


Fig.19. Parasitic circuit diagram between pin

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC79451KB-X2T	CHIP (Pb-Free)	850 / Tray Foam

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